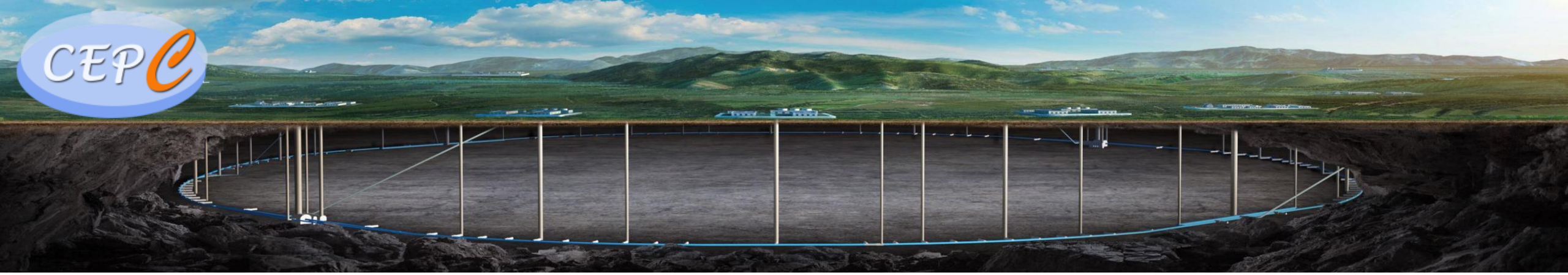

# TDAQ and Online of CEPC ref-Detector TDR

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# Content

- Introduction
- Requirements
- Overall design
- Trigger simulation
- Detailed design
- Cost
- IDRC feedback
- Research team and R&D plan
- Summary

# Introduction

- This talk is about the design and development of the TDAQ and online
- This talk relates to the Ref-TDR Ch 12.

# Physics Requirements

- Physical event rates
  - 87 Hz @ Higgs (240GeV)
  - 10.5 kHz @ Low lum. Z (91GeV)
  - 41.9 kHz @ High lum. Z
  - 56 Hz cosmic ray
  - Under study for low energy events from $\gamma\gamma$ collision
- Physical event rates are sufficiently low compared to the bunch crossing rate.
  - <1/10000 @Higgs, <1/1000 @Z
- Keep physical events as more as possible
  - By a rough selection of the relevant objects ( jet, e, muon, tau, $\gamma$, ...) and their combinations.
  - Required detailed signal feature extraction and simulation studies.

Table 12.1: CEPC baseline parameters

| | ZH | Z | | W | $t\bar{t}$ |
|---|---|---|---|---|---|
| SR power per beam (MW) | 50 | 10 | 50 | | |
| Bunch number | 446 | 3978 | 13104 | 2162 | 58 |
| Bunch spacing (ns) | 277 (x12) | 69.2 (x3) | 23.1 (x1) | 138.5 (x6) | 2700.0 (x117) |
| Train gap (%) | 63 | 17 | 9 | 10 | 53 |
| Bunch crossing rate(MHz) | 1.33 | 12 | 39.4 | 6.5 | 0.17 |
| Luminosity per IP ($10^{34}$cm$^{-2}$s$-1$) | 8.3 | 26 | 95.2 | 26.7 | 0.8 |
| Run time (years) | 10 | 1 | 2 | 1 | 5 |
| Event yields [2 IPs] | 4.3x$10^6$ | 2.9x$10^{11}$ | 2.0x$10^{12}$ | 2.1x$10^8$ | 6x$10^5$ |

Table 12.2: Expected event rate at the ZH mode for 50 MW

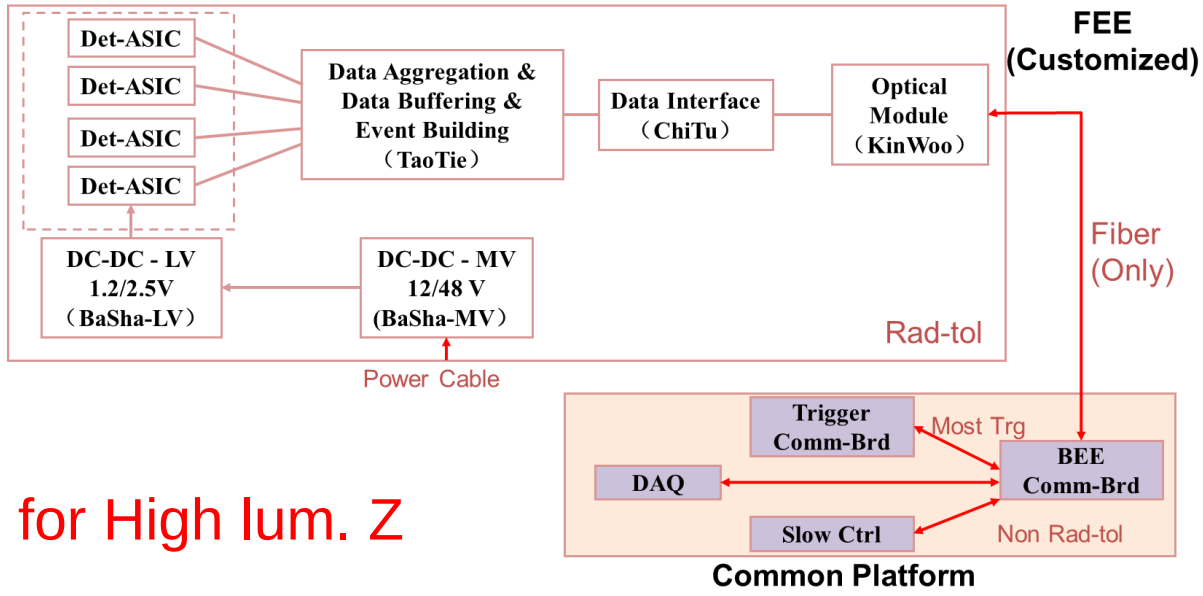
| Processes | Cross section (fb) | Event rate (Hz) |
|---|---|---|
| ZH | 203.66 | 0.017 |
| Two Fermions background (exclude Bhabha) | $6.4 \times 10^4$ | 5.3 |
| Four Fermions background | $1.9 \times 10^4$ | 1.6 |
| Bhabha | $1.0 \times 10^6$ | 80 |

Table 12.3: Expected event rate at the Z mode for 10 MW

| Processes | Cross section (fb) | Event rate (Hz) |
|---|---|---|
| qq | $31 \times 10^6$ | 7970 |
| $\mu\mu$ | $1.5 \times 10^6$ | 400 |
| $\tau\tau$ | $1.5 \times 10^6$ | 396 |
| Bhabha | $6.6 \times 10^6$ | 1714 |

# Detector and Electronics Requirements

- Detector trigger, read out and reconstruction window
  - TPC: max draft time 34 us
    - Pileup: 123 BX/event @Higgs, 492 BX/event @Low lum. Z, 1472 BX/event @High lum. Z
    - Too long, need special readout and trigger treatment for pileup tracks
  - ECAL & HCAL: trigger uncertainty <25 ns, readout window 100 ns
    - Pileup: 2 BX/event @Low lum. Z, 5 BX/event @High lum. Z
  - Silicon/Muon: trigger uncertainty <10 ns, readout window 10+25 = 35 ns
- Electronics framework schema
  - System clock: 43.3 MHz
  - Transmit full raw data from Front-End to Back-End Electronics
    - Through fiber asynchronous link
  - Trigger receive primitives from BEE
  - Trigger send L1A back to BEE
- Trigger latency
  - Millisecond data buffer @ BEE DDR
  - Possible need send fast trigger to FEE for High lum. Z
    - Few us latency



# Beam Background Rate Estimation

- BG data rate before trigger
  - 400 GB/s @ Higgs
  - 1.37 TB/s @ Low lum. Z
  - 4.11 TB/s @ High lum. Z
- Readout event size
  - 1 Mbytes
  - 2 Mbytes @High lum. Z
- Storage event size
  - 500 Kbytes(1 Mbytes @High lum. Z)
- Storage event rate of TDAQ
  - 1k Hz @ Higgs
  - 20 kHz @ Low lum. Z
  - 80 kHz @ High lum. Z
    - Assume 1:1 physics vs background

| | Vertex | Pix(ITKB) | Strip (ITKE) | OTK | TPC | ECAL | HCAL | Muon |
|---|---|---|---|---|---|---|---|---|
| Channels per chip | 512*1024 | 512*128 | 1024 | 128 | 128 | 8~16 | | |
| Data Width /hit | 32bit | 42bit | 32bit | 48bit | 48bit | 48bit | | |
| Avg Data Vol @Higgs | 474.2 Gbps | 400.5 Gbps | | 277 Gbps | 34.4 Gbps | 710 Gbps | 1348.8 Gbps | 24.1 Gbps |
| Sum | 3.2 Tbps = 400 GB/s, 300 Kbytes/BX @Higgs | | | | | | | |
| Avg Data Vol @Low lum. Z | 2440 Gbps | 3480 Gbps | | 420 Gbps | 55.8 Gbps | 910 Gbps | 3650 Gbps | 5 Gbps |
| Sum | 10.96 Tbps = 1.37 TB/s , 115 Kbytes/BX @ Low lum. Z | | | | | | | |
| Sum | 10.96x3 Tbps = 4.11 TB/s , 115 Kbytes/BX @ High lum. Z | | | | | | | |

Background event size with readout window:

300 + 34.4/1.33/8*122 = 695 Kbytes @ Higgs

115 + 55.8/12/8*491 + (910+3650)/12/8*1 = 448 Kbytes @ Low lum. Z

115 + 55.8*3/39.4/8*1471 + (910+3650)*3/39.4/8*4 = 1070 Kbytes @ High lum. Z

Need compress event size especially for TPC with track reconstruction.

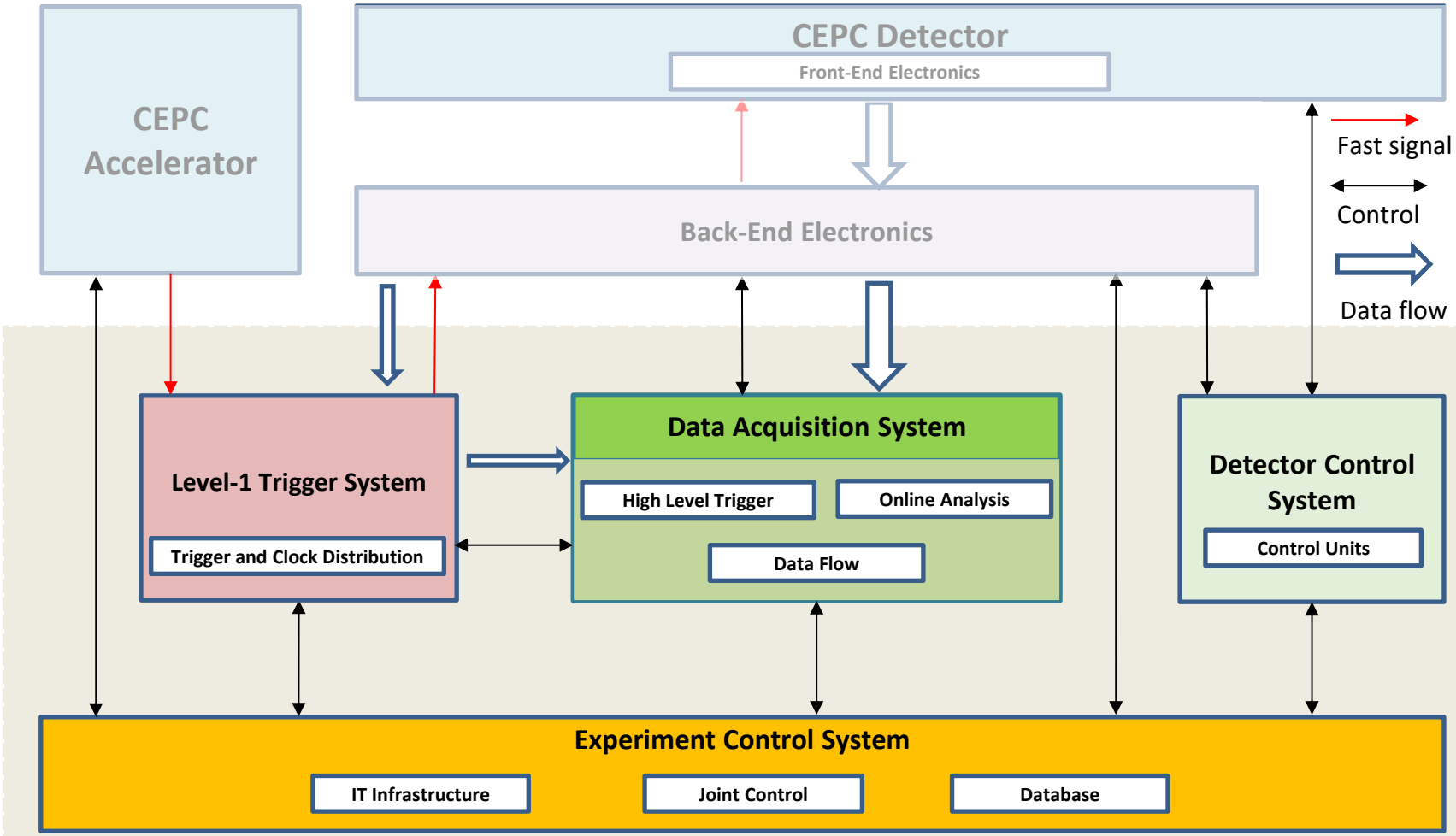
Preliminary rate estimation without safety factor

# Main Technical Challenges

- High efficiency algorithms in trigger and background compression
  - 1.33 MHz->O(1k)Hz @Higgs
  - 12 MHz->O(20k)Hz @Low lum. Z
  - 39.4 MHz->O(80k)Hz @High lum. Z
- Trigger solution for lower-energy events, e.g. from $\gamma\gamma$ collisions
- Trigger primitive synchronization control with asynchronous data readout from subdetector electronics
  - Manage data disorder due to data transfer queuing and delay
  - Align sub-detector data of each bunch crossing within limited time and resource

# TDAQ Overall Design

- TDAQ solutions
  - Level 1 hardware trigger(L1) + high level trigger(HLT)
  - Single type of common hardware trigger board
  - Provide both normal and fast trigger menu
  - Ethernet readout
  - Joint control and monitoring
  - Unified online service and IT infrastructure




Overall structure of CEPC Detector TDAQ and Online system

# Preliminary Trigger Simulation

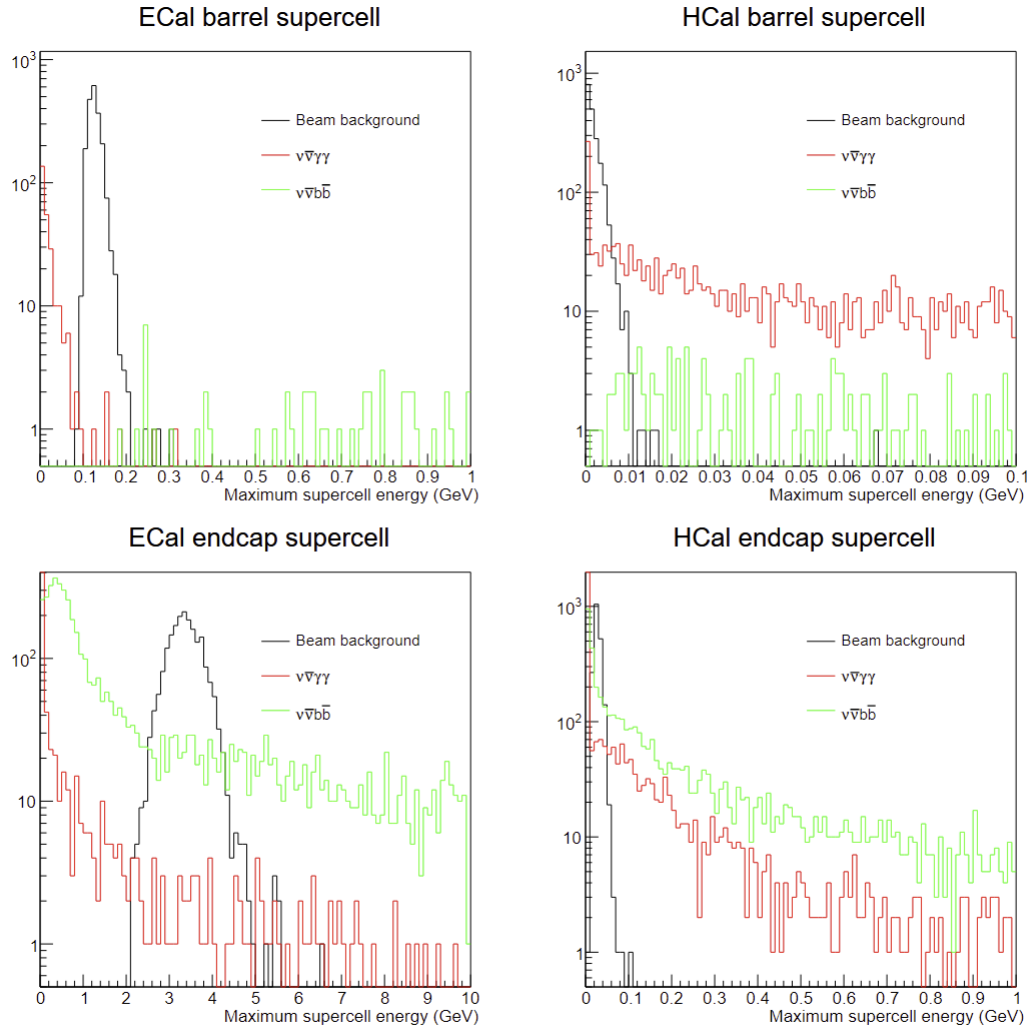



**Figure 12.14:** Maximum energy distribution of the supercell of beam background, $e^+e^- \to Z(\nu\bar{\nu})H(\gamma\gamma)$ and $e^+e^- \to Z(\nu\bar{\nu})H(b\bar{b})$. Up: Barrel; down: Endcap; left: ECAL; right: HCAL.

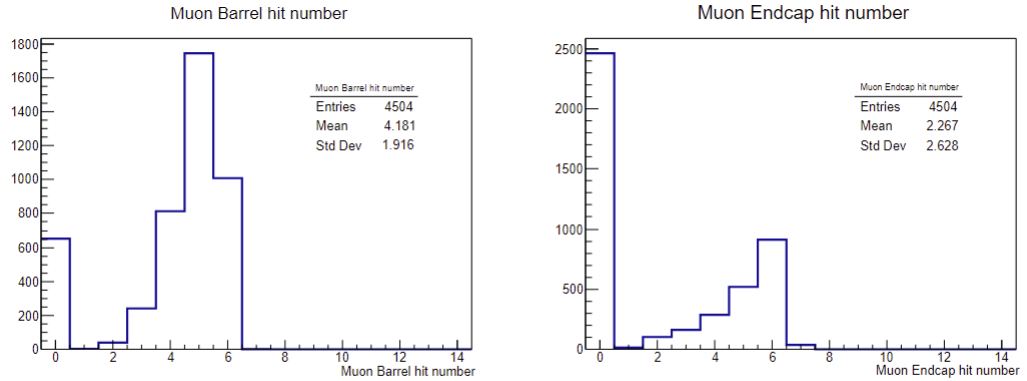



**Figure 12.15:** Number of hits for the $e^+e^- \to Z(\nu\bar{\nu})H(\mu^+\mu^-)$ process on the Muon Barrel(left) and Endcap(right) detector.

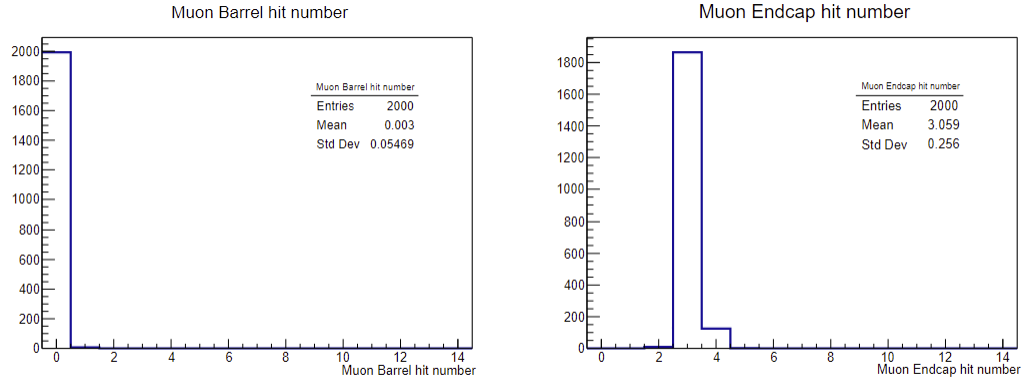



**Figure 12.16:** Number of hits for the beam background on the Muon Barrel(left) and Endcap(right) detector.

Trigger and background simulation with supercell energy and muon hits

# Preliminary L1 Trigger Algorithm

- Trigger efficiency > 99%
  - Separate and independent events of physics and background
  - L1 trigger condition @ZH
    - ECAL Barrel supercell > 0.5 GeV
    - HCAL Barrel supercell > 0.1 GeV
    - ECAL Endcap supercell > 4.8 GeV
    - HCAL Endcap supercell > 0.1 GeV
    - Track tag Number of Muon track > 0
  - L1 trigger condition @Low lum. Z
    - ECAL Barrel supercell >0.25 GeV
    - HCAL Barrel supercell >0.1 GeV
    - ECAL Endcap supercell >2.7 GeV
    - HCAL Endcap supercell >0.2 GeV
    - Track tag Number of Muon track > 0
- Good veto efficiency with current beam background simulation
  - Need more event samples and noise studies

**Table 12.8:** Calorimeter threshold efficiency at the ZH mode for 50 MW

| Process | Efficiency | Process | Efficiency | Background | Veto rate |
|---|---|---|---|---|---|
| $Z(\nu\bar{\nu})H(b\bar{b})$ | $> 99\%$ | $Z(\nu\bar{\nu})H(W^+W^-)$ | $> 99\%$ | Beam background | $> 99\%$ |
| $Z(\nu\bar{\nu})H(\tau^+\tau^-)$ | $> 99\%$ | $Z(\nu\bar{\nu})H(ZZ)$ | $> 99\%$ | | |
| $Z(\nu\bar{\nu})H(\gamma\gamma)$ | $> 99\%$ | $Z(\nu\bar{\nu})H(\gamma Z)$ | $> 99\%$ | | |
| $Z(\nu\bar{\nu})H(\mu^+\mu^-)$ | $\sim 99\%$ | Bhabha | $> 99\%$ | | |
| $\mu^+\mu^-$ | $\sim 98\%$ | | | | |

**Table 12.9:** Calorimeter threshold efficiency at the Z mode for 10 MW

| Process | Efficiency | Process | Efficiency | Background | Veto rate |
|---|---|---|---|---|---|
| $q\bar{q}$ | $> 99\%$ | $\mu^+\mu^-$ | 94% | Beam background | $> 99\%$ |
| Bhabha | $> 99\%$ | $\tau^+\tau^-$ | $\sim 99\%$ | | |

**Table 12.10:** Muon trigger efficiency at the ZH mode for 50 MW

| Process | Efficiency | Process | Efficiency | Background | Veto rate |
|---|---|---|---|---|---|
| $Z(\nu\bar{\nu})H(\mu^+\mu^-)$ | 96.4% | $\mu^+\mu^-$ | 86.8% | Beam background | $> 99\%$ |

**Table 12.11:** Muon trigger efficiency at the Z mode for 10 MW

| Process | Efficiency | Background | Veto rate |
|---|---|---|---|
| $\mu^+\mu^-$ | 95.3% | Beam background | $> 99\%$ |

**Table 12.13:** Expected L1 trigger rate at the ZH mode for 50 MW and at the Z mode for 10 MW. Samples are simulated with CEPCSW tdr24.12.0. Electronic noise is not added. Pile up event is not added. Beam background is using version 241227.

| ZH mode | Efficiency | Z mode | Efficiency |
|---|---|---|---|
| ZH | >99% | $q\bar{q}$ | >99% |
| Two Fermions processes (exclude Bhabha) | >99% | $\mu^+\mu^-$ | >99% |
| Four Fermions processes | >95% | $\tau^+\tau^-$ | >99% |
| Bhabha | >99% | Bhabha | >99% |
| **Background** | **Veto rate** | **Background** | **Veto rate** |
| Beam background | >99% | Beam background | >99% |

# Estimation of Trigger and data rate

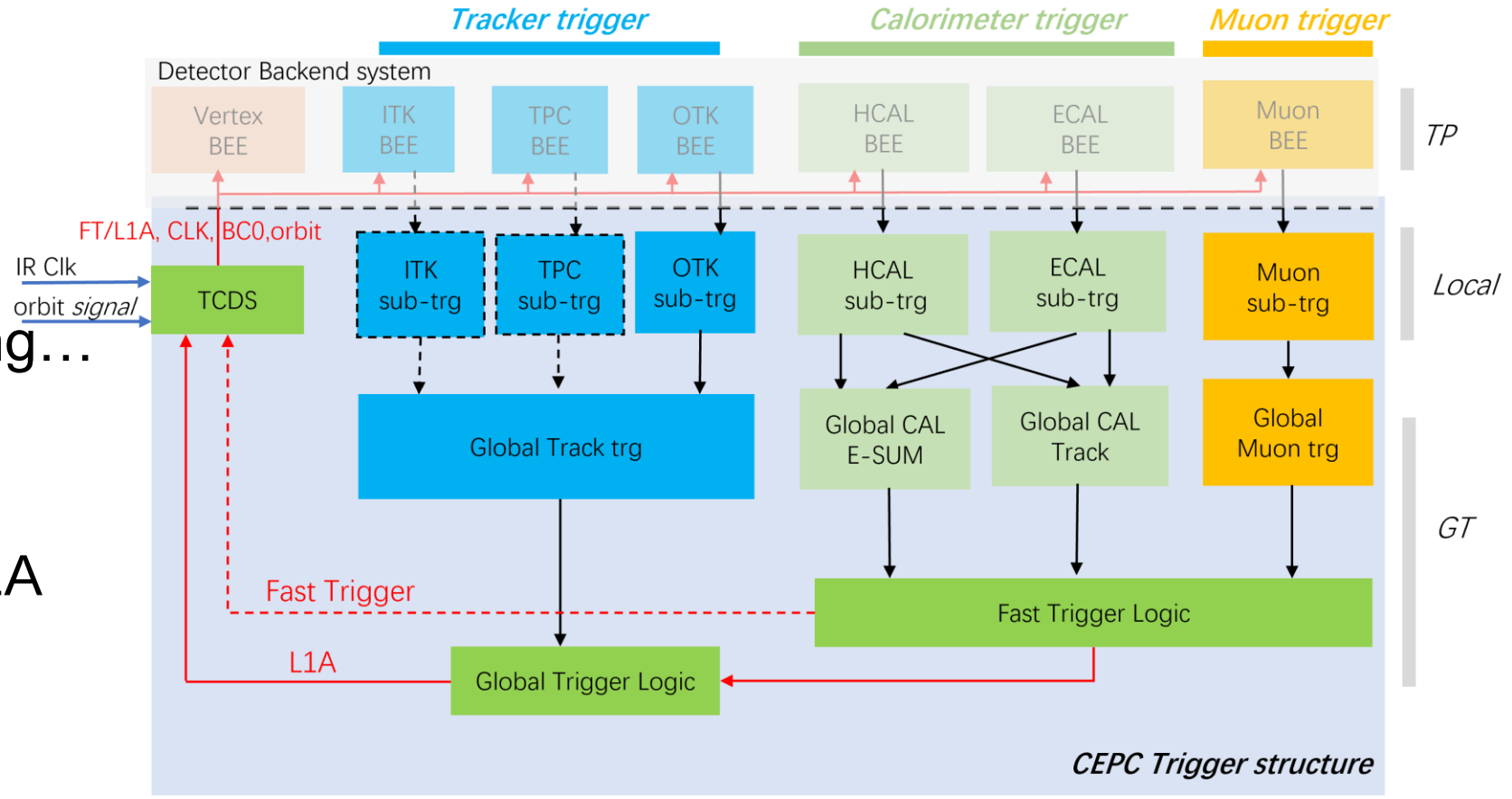
- L1 trigger rate
  - Expect reduce beam background to 1%
  - 120 kHz @ Low lum. Z
  - Simplify trigger design and implementation to do more @HLT
- HLT rate
  - Expect reduce beam background to 0.1%
  - 20 kHz @ Low lum. Z
- DAQ data rate
  - Read out:
    - 120 GB/s @ Low lum. Z
  - Storage:
    - 500 MB/s @ Higgs
    - 10 GB/s @Low lum. Z
  - 1 year(3600h):
    - 6.48 PB @ Higgs
    - 129.6 PB @ Low lum. Z

**Table 12.5:** Trigger rate estimation table for different run conditions.

| Condition | Higgs | Z(10MW) | Z(50MW) | W | $t\bar{t}$ |
|---|---|---|---|---|---|
| Luminosity $(10^{34}/cm^2/s)$ | 8.3 | 26 | 95.2 | 26.7 | 0.8 |
| Bunch space (ns) | 277 | 69.3 | 23.1 | 253.8 | 4523.1 |
| Bunch crossing rate (MHz) | 1.34 | 12 | 39.4 | 6.5 | 0.18 |
| Background data size/bunch crossing (kbyte) | 300 | 162 | 162 | 300 | 300 |
| Background data rate (Tbyte/s) | 0.4 | 1.94 | 7.7 | 1.95 | 0.048 |
| Physical event rate (kHz) | 0.087 | 10.5 | 41.9 | 0.1 | 0.002 |
| L1 triger rate (kHz) | 13 | 120 | 400 | 65 | 2 |
| Background event size (kbyte) | 695 | 448 | 1070 | - | - |
| Readout event size (kbyte) | 1000 | 1000 | 2000 | 1000 | 1000 |
| DAQ readout rate (Gbyte/s) | 13 | 120 | 800 | 65 | 2 |
| High level trigger rate (kHz) | 1 | 20 | 80 | 6 | 1 |
| Storage event size (kbyte) | 500 | 500 | 1000 | 500 | 500 |
| DAQ storage rate (Gbyte/s) | 0.5 | 10 | 80 | 3 | 0.5 |

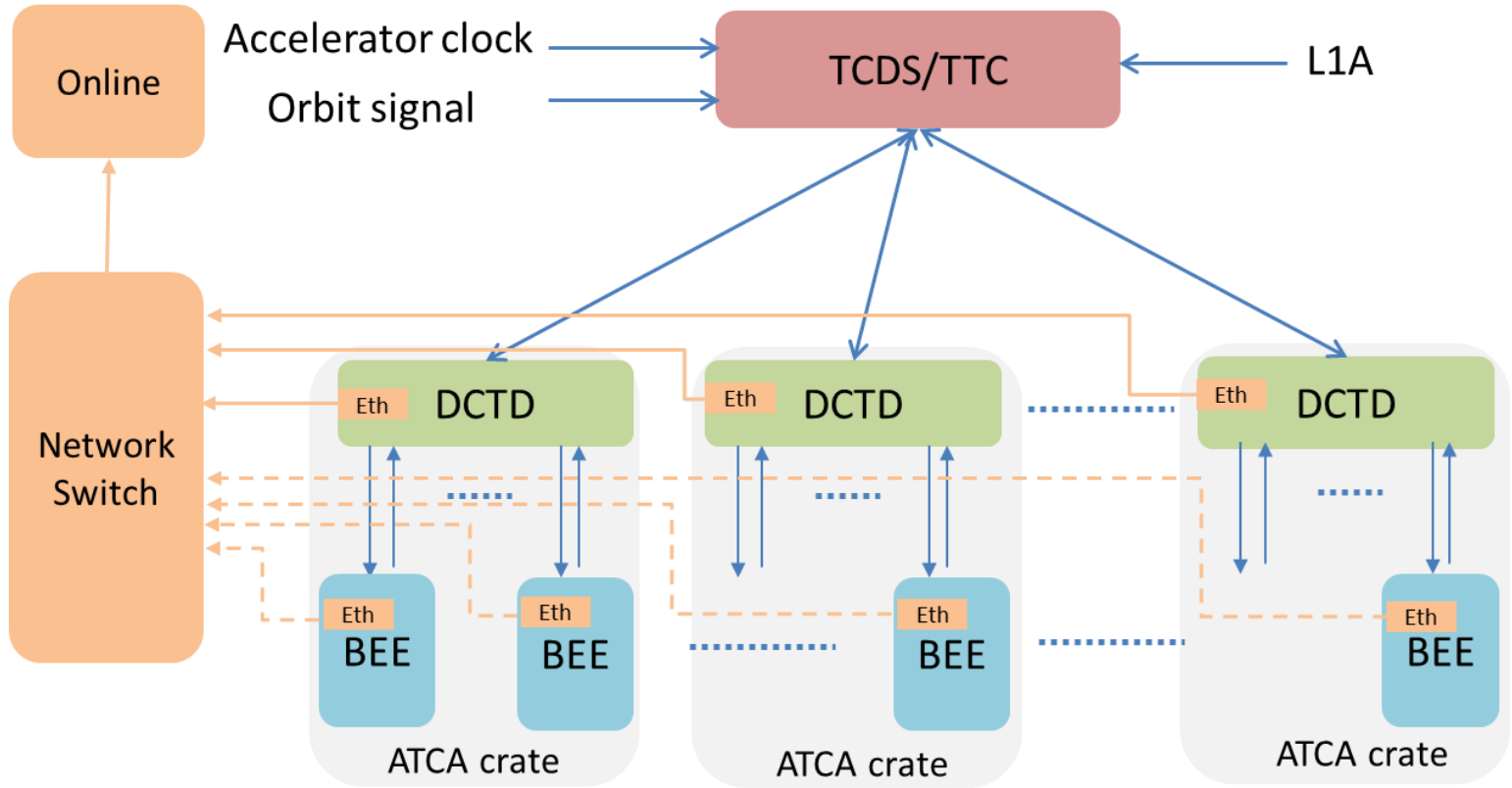
# Design of Hardware Trigger Structure

- Trigger primitive(TP)
  - Extracted @ BEE
- Local detector trigger
  - Sub energy and tracking…
- Global trigger
  - E-sum and tracking
  - Fast trigger(FT) and L1A generation on demand
- TCDS (Trigger Clock Distribution System)
  - Distribute clock and fast control signals to BEE
- Which detectors participate in trigger needs to be studied



# Design of TCDS and Readout Interface

- TCDS/TTC
  - Clock, BC0, Trigger, orbit start signal distribution
  - Full, ERR signal feed back to TCDS/TTC and mask or stop L1A
- Data readout from BEE
  - Read out directly or concentrated by DCTD board
  - Depending on the size of the data volume
  - Ethernet speed: 10 Gbps

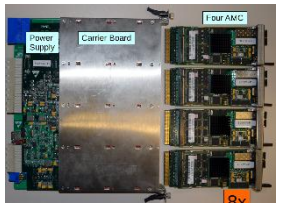


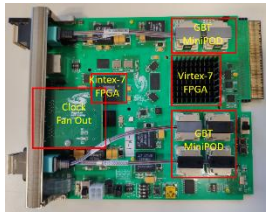

- TCDS-Trigger Clock Distribution System
- TTC- Trigger, Timing and Control
- DCTD-Data Concentrator and Timing Distribution
- BEE-Backend board Electronic

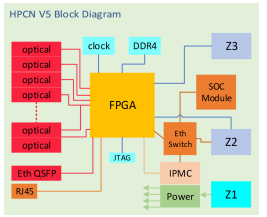
# R&D efforts and results

- xTCA for physics standard(ATCA/MTCA extension)
  - IHEP is a founding and development lab together with DESY, FNAL and SLAC
- Developed a series of xTCA boards
  - Started the design of an ATCA common trigger board for CEPC





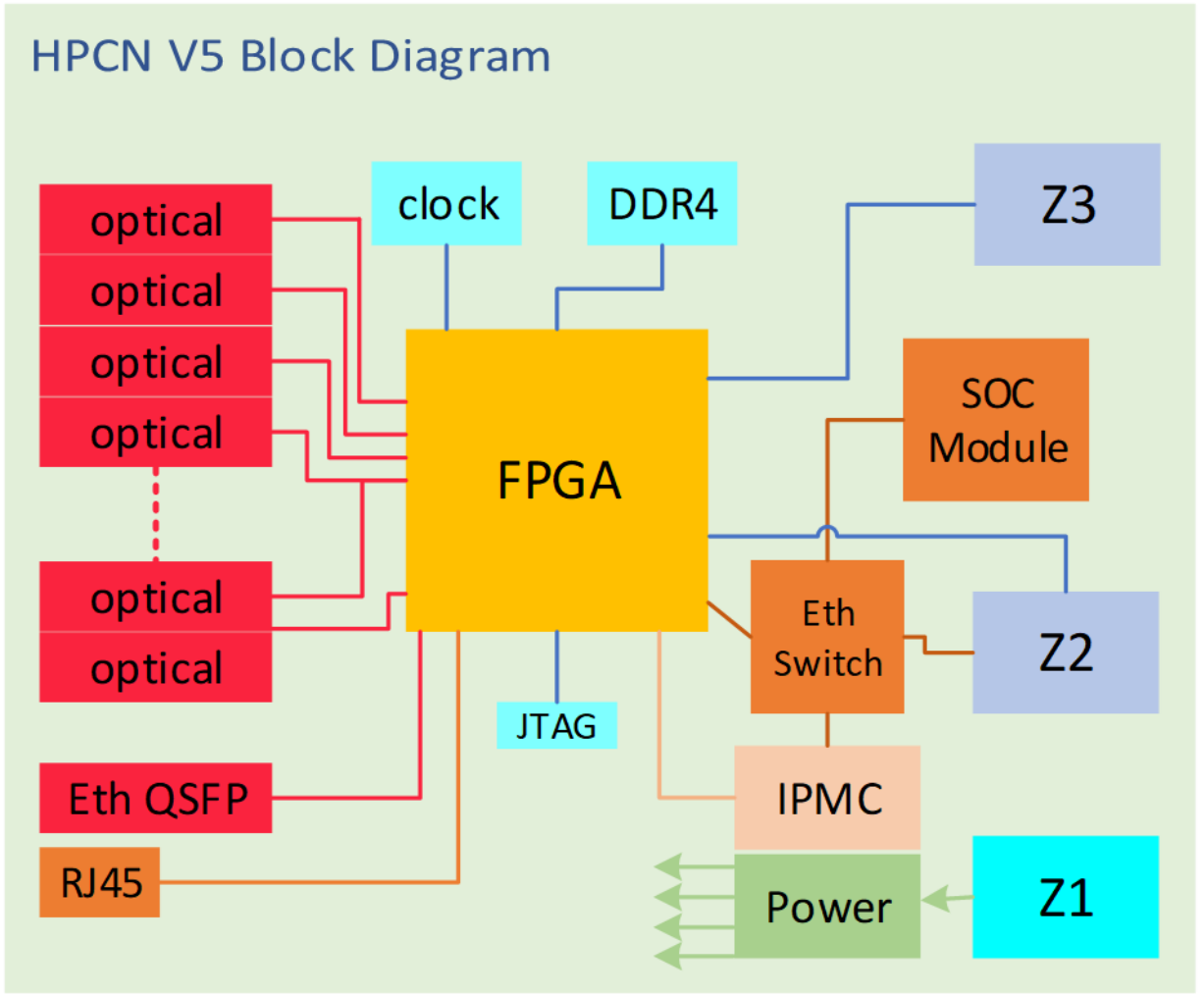



| Version | HPCN V1 | HPCN V2 | HPCN V3 | CPPF | HPCN V4 | Serenity | HPCN V5 |
|---|---|---|---|---|---|---|---|
| Line rate | 3Gbps | 3Gbps | 6Gbps | 10Gbps | 10Gbps | 25Gbps | >=16Gbps |
| Num. of ch | 8 ch | 8ch | 8-16ch | 36ch | 48ch | 124ch | 36-80 ch |
| Buffer | 2GB | 2GB | 4GB | — | 48GB | — | TBD |
| Ethernet | 1GbE | | | 1/10GbE | 10GbE | 100GbE | 40-100GbE |
| Aplication | PANDA | | Belle II/PXD | CMS Phase-I | CMS Phase-II | | CEPC R&D |
| Time | 2006- | | 2009- | 2013- | 2017- | | 2024- |

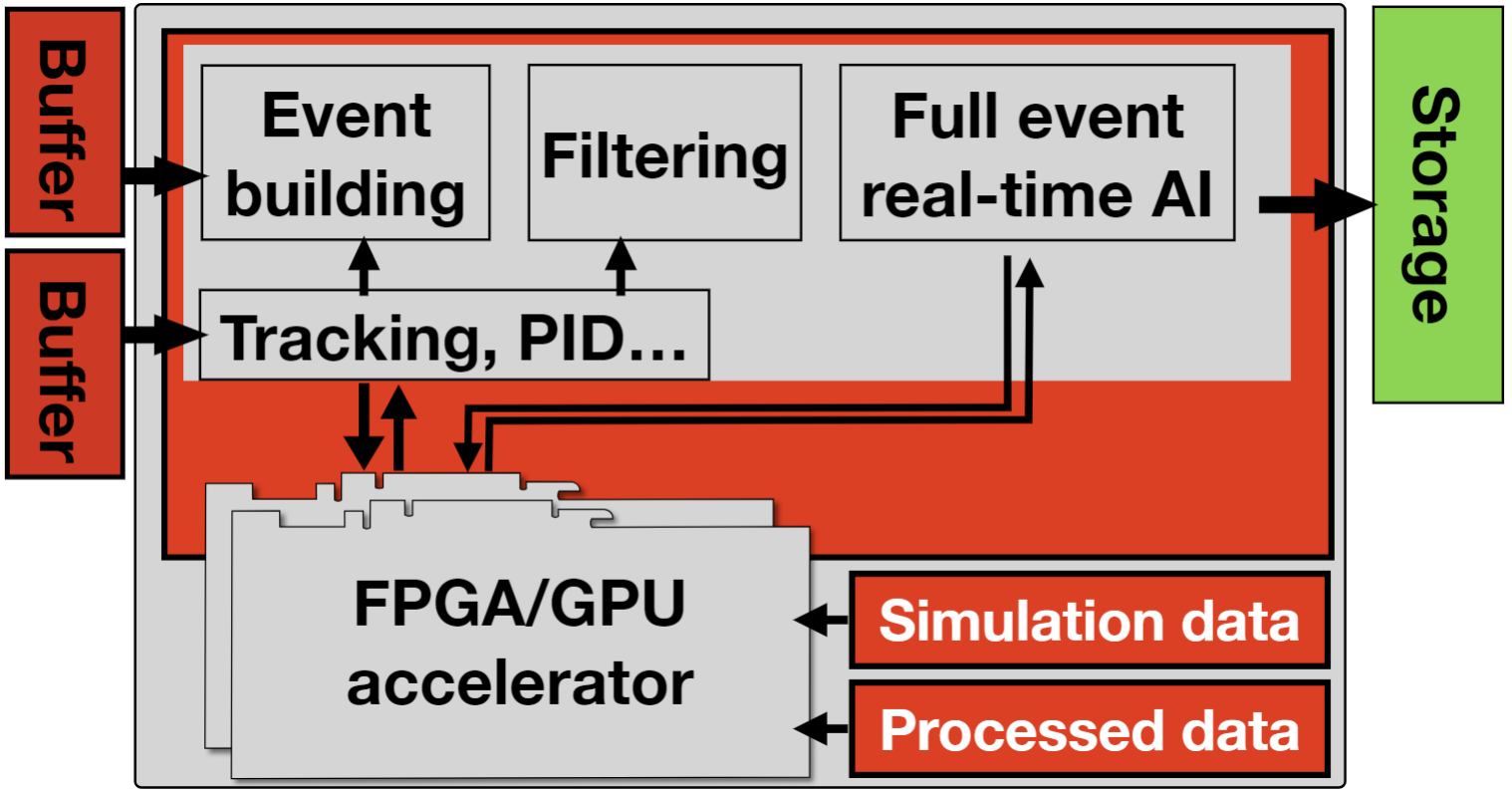
# Design of the Common Trigger Board

- Common Trigger board function list
  - ATCA standard
  - Virtex-7 FPGA
  - Optical channel: 10-25 Gbps/ch
  - Channel number:36-80 channels
  - Optical Ethernet port: 40-100GbE
  - DDR4 for mass data buffering
  - SoC module for board management
  - IPMC module for Power management



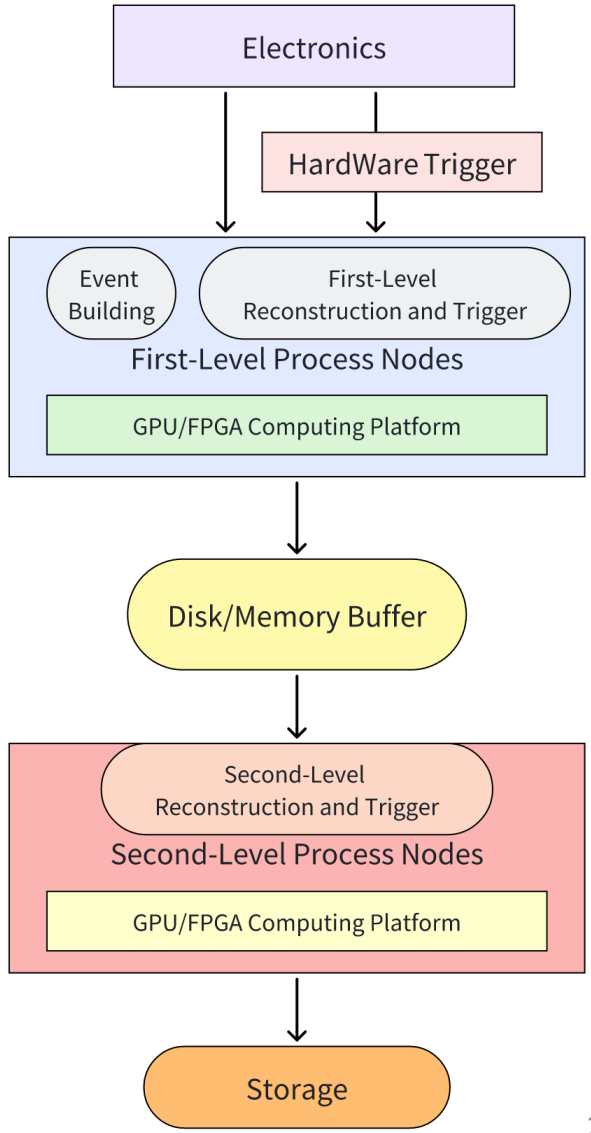
# High Level Trigger

- Event selection and data reduction
  - Distributed Computing
  - Advanced Software Tools
  - Real-Time Constraints
  - Detector Limitations
- Implement feature
  - Feature Extraction
  - Track Seed Finding
  - Lightweight PID
  - Calibration
  - Physics Skim
- Accelerated by GPUs and FPGA
- CPU cores estimation
  - 1 s@Higgs and 1.2 s@low Z for background event tracking reconstruction
    - < 20% background events >=1 track
  - ? s/Z event, max 6.5 s/ZH event
  - Fast reconstruction: 0.5 s/core/event, 13kHz*0.5s=6.5k cores, 120kHz*0.5s=60k cores



# Architecture Design of DAQ

- Compatible design with or without HW trigger
- Full COTS(commercial-off-the-shelf) hardware
- RADAR software framework
  - Heterogeneous computing
- GPU/FPGA acceleration for HLT
- Disk or memory buffer
  - Decouple computing environments
  - Complete offline algorithm can be run online



# DAQ Readout Interface and Protocol

- Readout data rate
  - 13 Gbytes/s@Higgs
  - 120 Gbytes/s@Low lum. Z
- Interface
  - Ethernet 10 Gbps fiber
  - 10 Gbps/BEE
  - 10 Gbps/crate
- Protocol
  - TCP
  - RDMA over FPGA
    - Under R&D
- Readout full TPC data
  - 34 us window
  - Overlap among many events
  - Assemble data by time fragment

Table 12.14: Requirements for Detector Readout

| Detector | Avg Background Data Vol after L1-Trigger (Gbps) @Higgs | Avg Background Data Vol after L1-Trigger (Gbps) @Low Lumi Z | BEE Number | Data rate per BEE (Gbps) @Low Lumi Z |
|---|---|---|---|---|
| Vertex | 4.7 | 24.4 | 6 | 4.07 |
| TPC | 34.4 | 55.8 | 32 | 1.74 |
| ITK | 4.0 | 34.8 | 245 | 0.142 |
| OTK_B | 2.5 | 3.8 | 34 | 0.084 |
| OTK_E | 0.3 | 0.4 | 45 | 0.009 |
| ECAL_B | 4.6 | 12.8 | 60 | 0.213 |
| ECAL_E | 1.9 | 5.4 | 34 | 0.159 |
| HCAL_B | 8.1 | 56.8 | 346 | 0.164 |
| HCAL_E | 5.4 | 16.2 | 192 | 0.084 |
| Muon | 0.2 | 0.05 | 24 | 0.002 |
| Trigger | - | - | 65 | - |
| Sum | 66.1 | 210.45 | 1083 | |

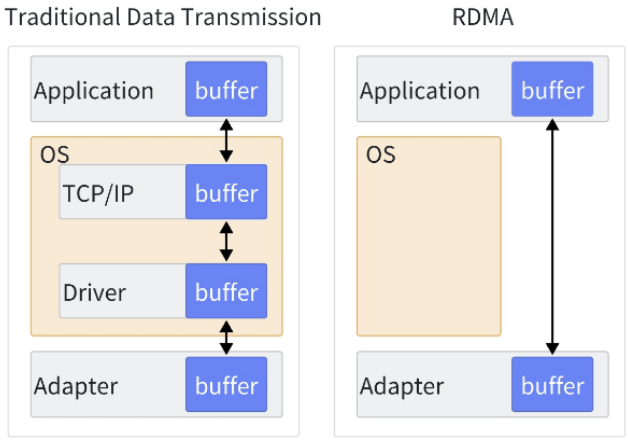



Figure 12.24: Traditional Data Transmission vs RDMA.

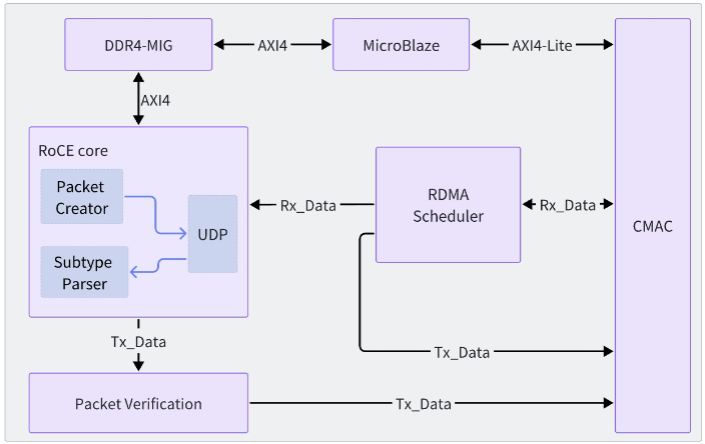
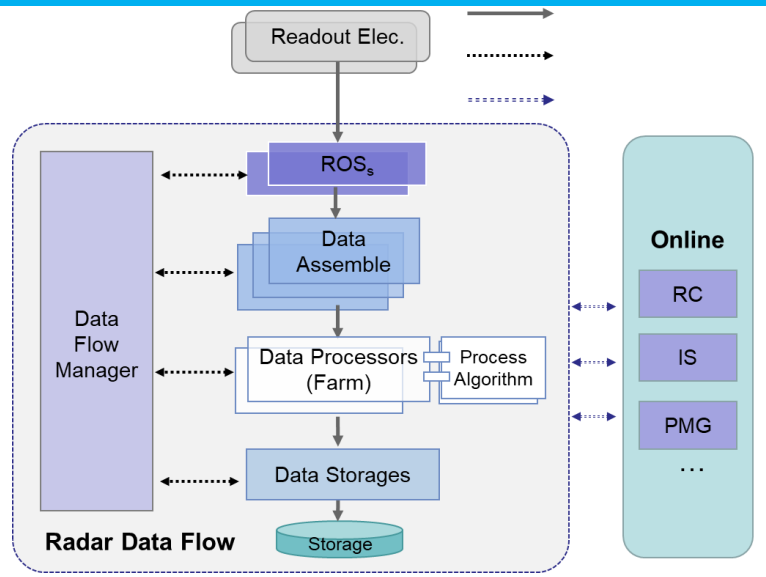



Figure 12.25: RDMA Firmware Design.

# Streaming Software Framework – RADAR

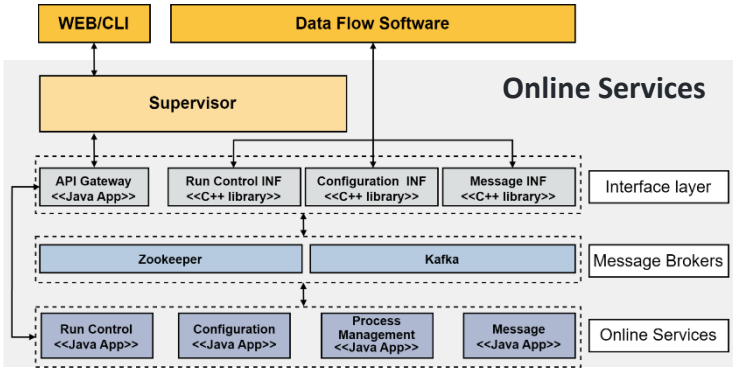
*heteRogeneous Architecture of Data Acquisition and pRocessing*

- **V1:** deployed in LHAASO (3.5 GB/s data rate), *software trigger mode*
- **V2:** upgraded for JUNO (40 GB/s data rate), *mixed trigger mode*
  - Containerized running
- **V3:** **CEPC-oriented** (~ TB/s data rate) , under development




- **Motivation:**
  - High-throughput data acquisition and processing
- **Current Status:**
  - Over a decade of work led to significant progress, validated through experiments
- **Recent Focus:**
  - **Heterogeneous online processing platforms with GPU**
  - **Real-time data processing acceleration solutions**
- **Expansion:**
  - **Application across various domains** (DAQ, triggering, control, etc.)
  - **Integration of AI technologies** (ML, NLP, expert systems, etc.)

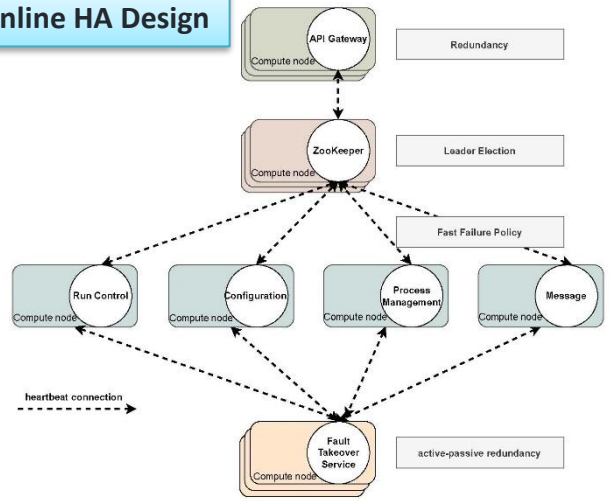
- **General-purpose distributed framework**
- **Lightweight structure**
- **Plug-in modules design**
- **Microservices architecture**



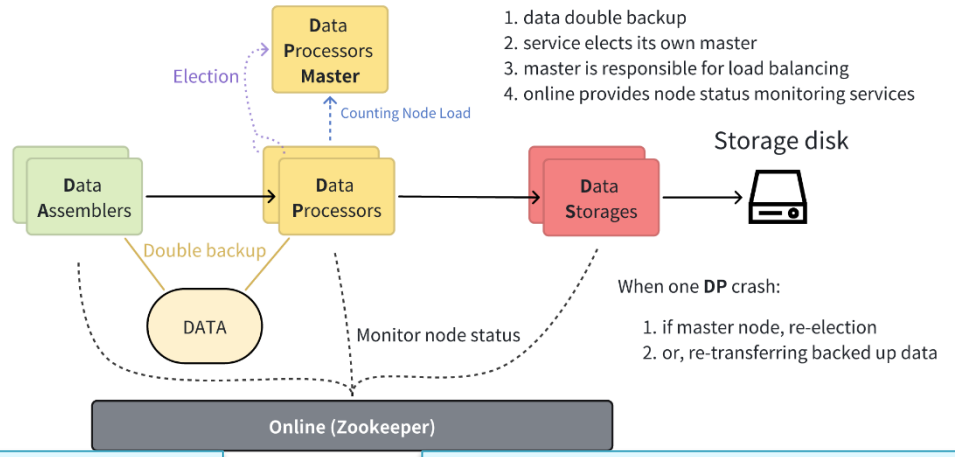

Start to develop new version with GPU acceleration.

# R&D efforts and results

## Online HA Design




## Dataflow HA Design



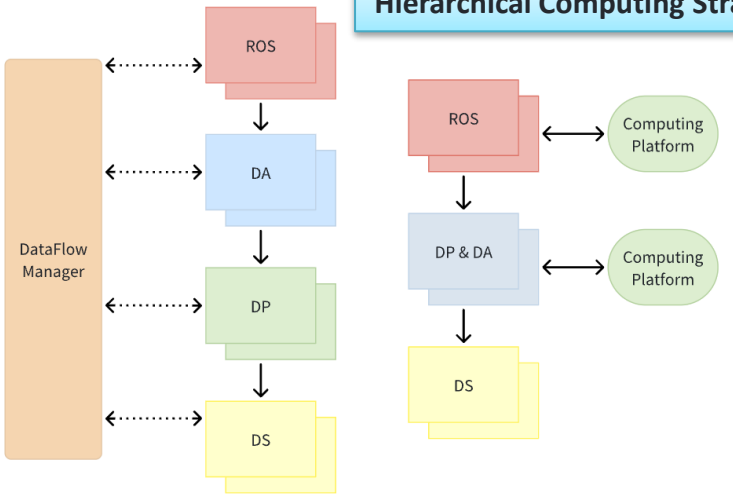

High Availability (HA):

1. data double backup
2. service elects its own master
3. master is responsible for load balancing
4. online provides node status monitoring services

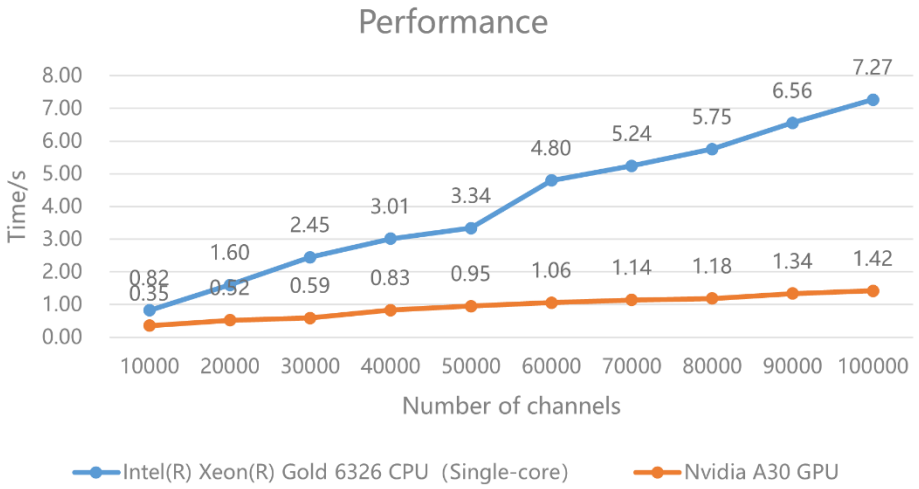
When one **DP** crash:

1. if master node, re-election
2. or, re-transferring backed up data

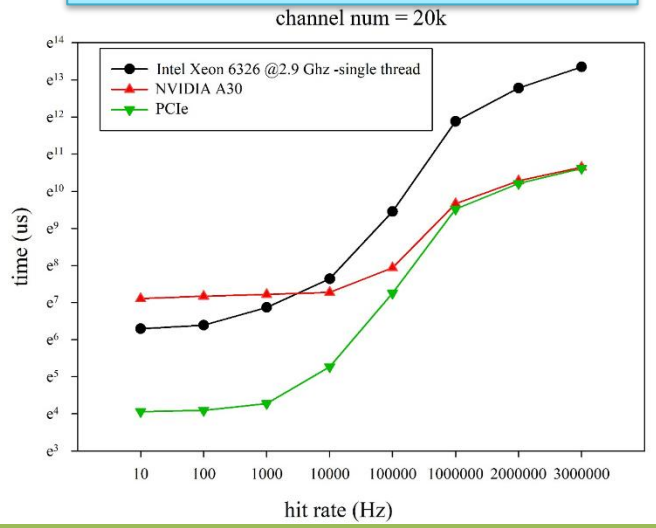
## Hierarchical Computing Strategy



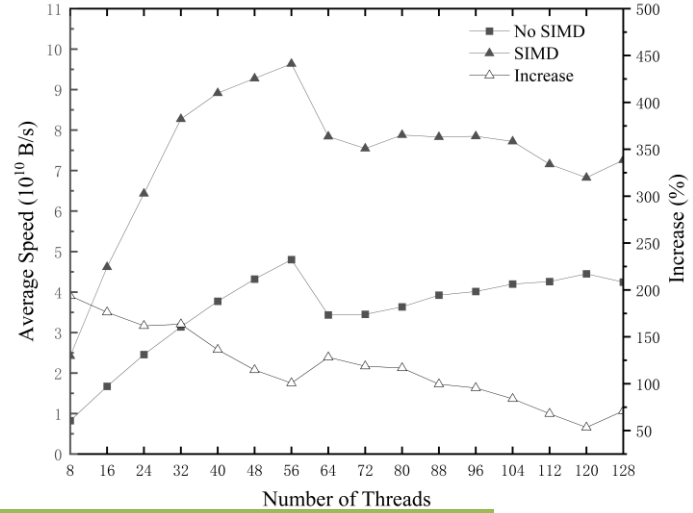

## GPU based online waveform reconstruction in JUNO




## GPU based nHit trigger algorithm study

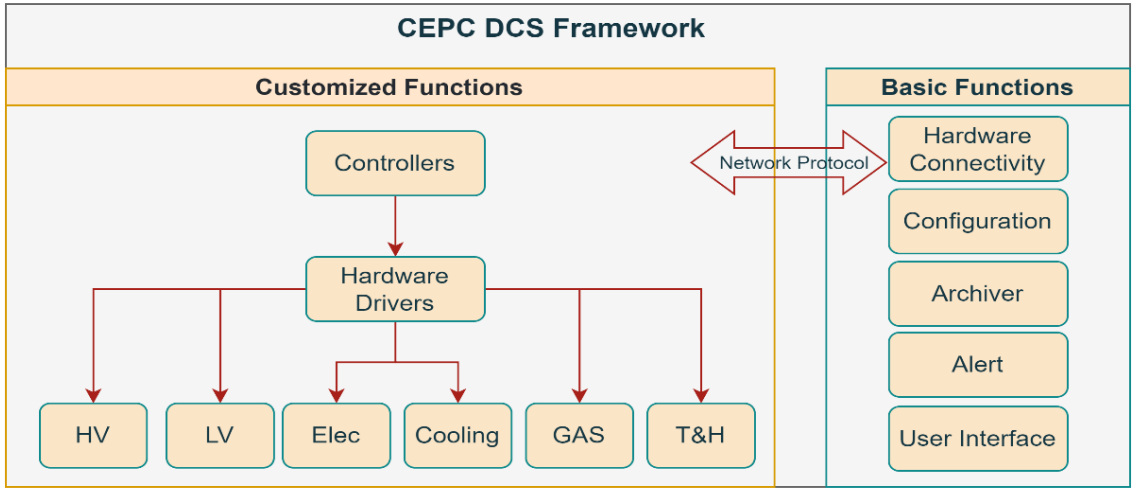



## SIMD based CPU processing acceleration




Acceleration progress for waveform reconstruction and software trigger algorithm.

# Design of Detector Control System



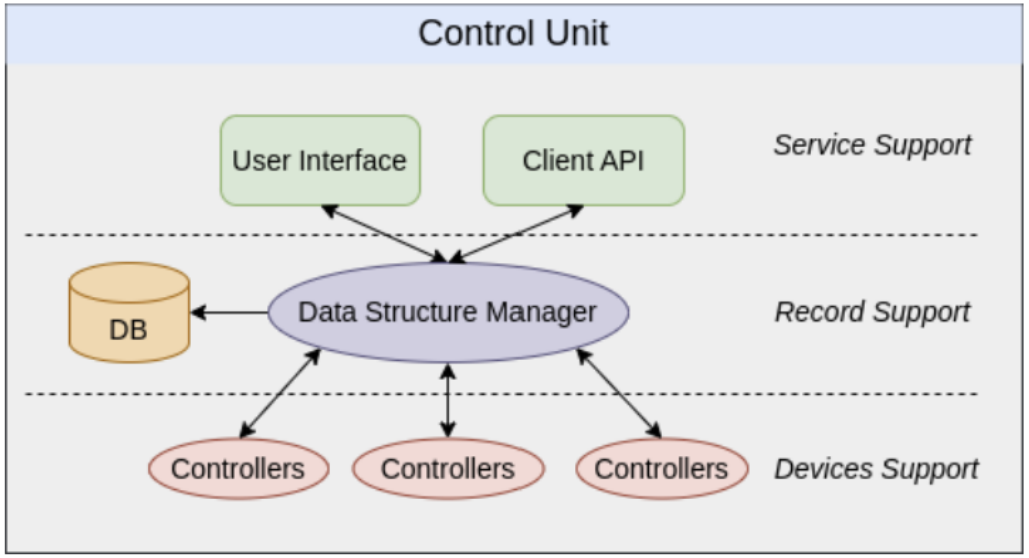




**Figure 12.29:** Software architecture of the control unit.

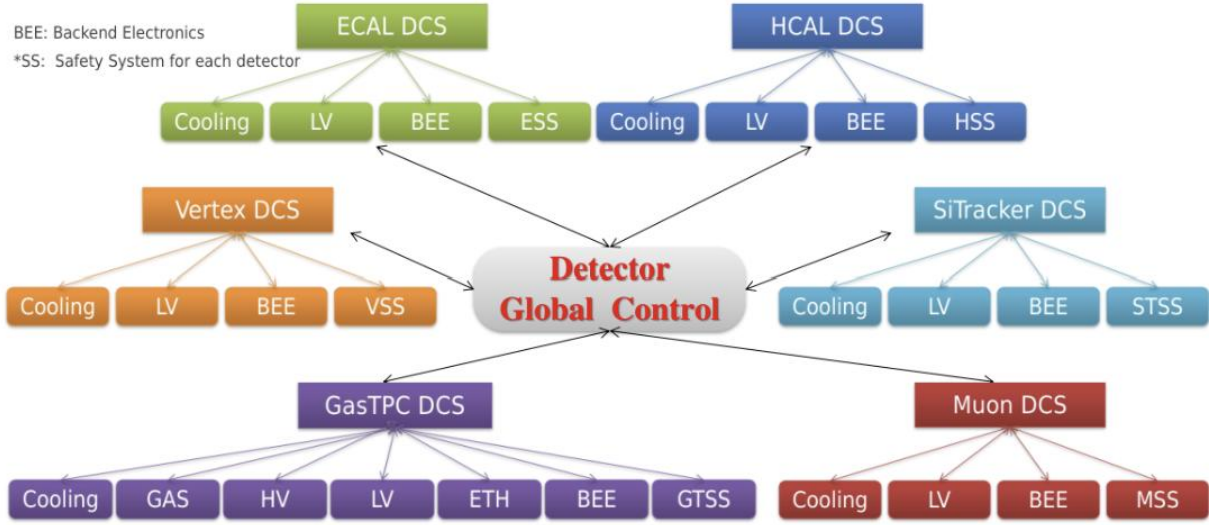



**Figure 12.28:** CEPC DCS requirments overview.

**Table 12.16:** Summary of detector control and monitoring quantities

| Equipment | Channel Number | Control and Monitoring Items | Total Count |
|---|---|---|---|
| AC-DC Crate | 55 | Switch, voltage, current, etc., about 6 items | 330 |
| AD-DC Channel | 550 | Switch, voltage, current, etc., about 6 items | 3300 |
| FEE Power Crate | 390 | Switch, voltage, current, etc., about 6 items | 2340 |
| FEE Power Channel | 17946 | Switch, voltage, current, etc., about 6 items | ~110,000 |
| FEE Board | 27984 | Voltage, current, temperature, etc., about 10 items | ~280,000 |
| BEE Crate | 180 | Switch, fan, status, etc., about 10 items | 1800 |
| BEE Board | 1749 | Switch, voltage, current, etc., about 6 items | ~10,000 |
| Trigger Crate | 21 | Switch, fan, status, etc., about 10 items | 210 |
| Trigger Board | 161 | Switch, fan, status, etc., about 10 items | 1610 |
| HV Crate | 77 | Switch, fan, status, etc., about 10 items | 770 |
| HV Channel | 8896 | Voltage, current, status, etc., about 6 items | ~55,000 |
| Cooling, Gas | 12 cooling + 1 gas | Flow control, humidity, etc., about 30 items | 390 |
| Environmental | ~30 | Temperature, humidity | 60 |
| Total | | | ~470,000 |

Designed framework based on existed solutions

# Design of Experiment Control System

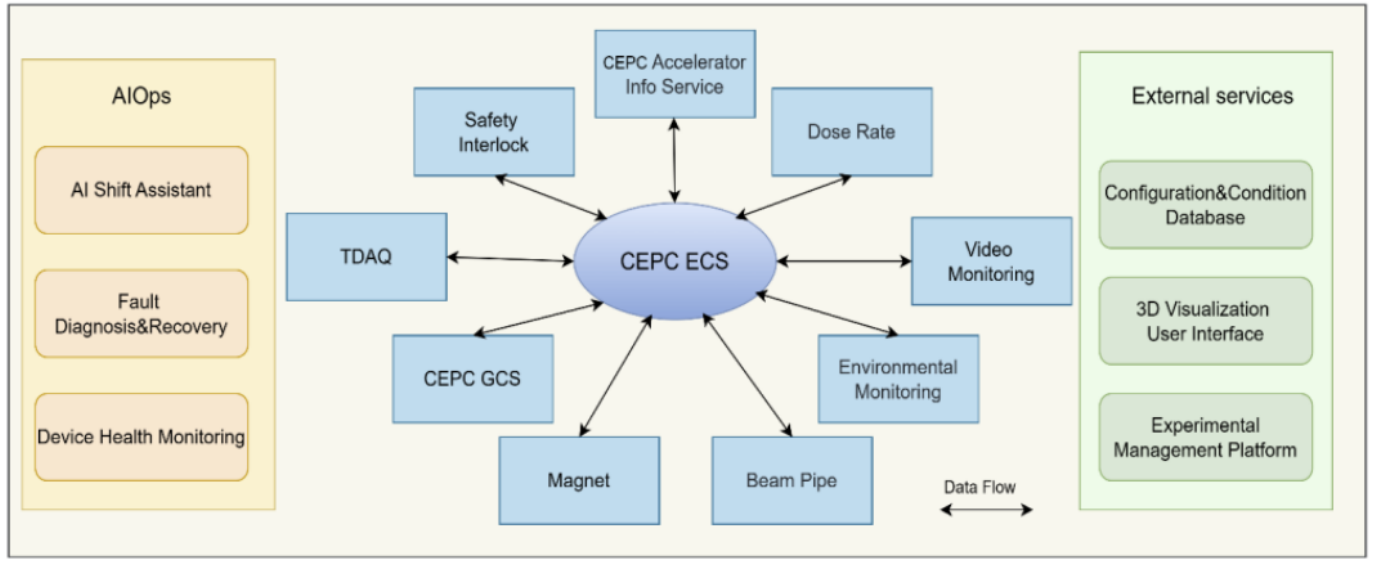



Figure 12.30: CEPC ECS structural overview.

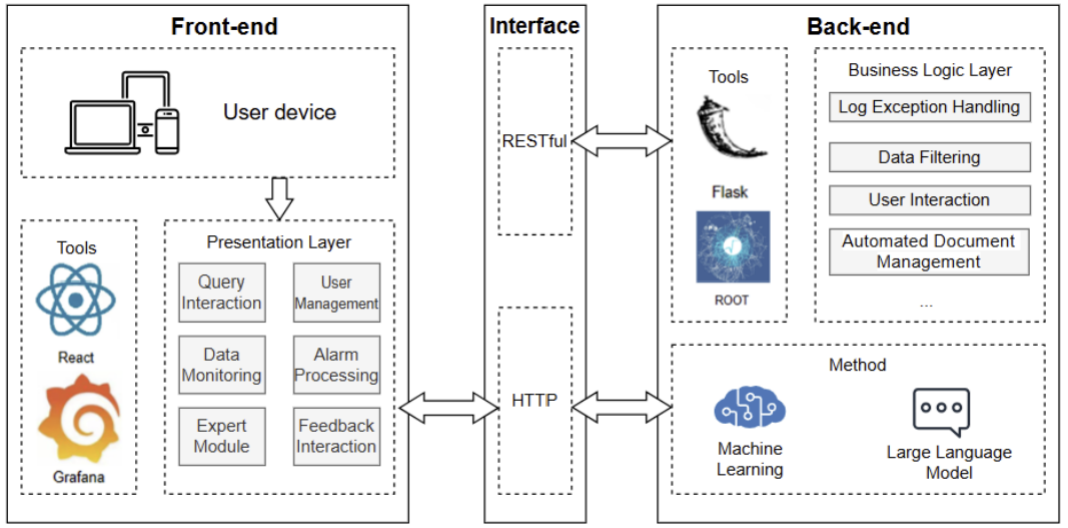



Figure 12.31: ECS software architecture.

- R&D progress from JUNO and BESIII
  - 3D Visualization Monitoring
  - AI shift assistant based on LLM+RAG (TAOChat)
  - ROOT-based Online Visualization System
- Unified control and monitoring for all system
  - TDAQ, DCS, electronics, accelerator and others

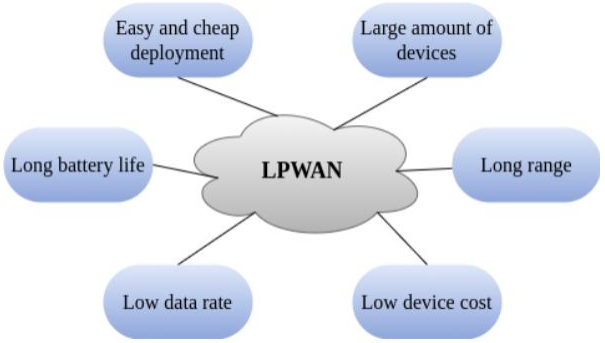



Figure 12.33: LPWAN technical advantages.

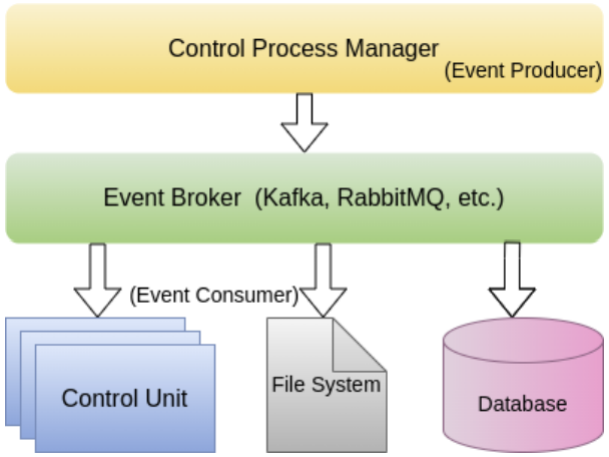



Figure 12.32: Central control software architecture.

# Primary Cost Estimation

- TDAQ total: 52M RMB @Higgs, + 77M RMB @Low lum.Z
- L1 Trigger： 15M RMB
  - ATCA boards (130k RMB/boards): 72+12 (10.92M RMB)
  - ATCA crate(150k RMB/crate) : 10 (1.5M RMB)
  - Firmware (20k RMB/person-months): 120 (2.4M RMB)
- HLT： 12M RMB @Higgs, + 65M @Low lum.Z
  - CPU cores(1k RMB/core): 6.5k @Higgs(6.5M), 60k @Low lum. Z
  - Network: 200*25Gbps*2 Gbps(1M), 1875*25Gbps*2(5M)
  - Algorithm software(20k RMB/person-months): 192 (3.84M RMB)
- DAQ： 10.1M RMB @Higgs, + 12M RMB@Low lum. Z
  - CPU cores(1.5k RMB/core): 1k @Higgs(1.5M RMB), 4k @Low lum. Z(6M RMB)
  - Storage: 1PB @ Higgs(1M RMB), 10 PB @ Low lum. Z(5M RMB)
  - Network: 1083*10Gbps for BEE + 47*25Gbps*2 (2.5M RMB), 125*25Gbps*2@Z(1M RMB)
  - Software (20k RMB/person-months): 240 (4.8M RMB)
- DCS/ECS: 15 M RMB
  - Computing/control room: 5M RMB
  - Hardware: 5M RMB
  - Software (20k RMB/person-months): 144 (2.88M RMB)
- FW and SW development costs are estimated based on the engineering development needs of students, post-docs and engineers hired for the project in addition to regular staff

# Findings



- The requirements for the TDAQ system are dictated by the need to collect all ZH, WW and Z pole events and provide the bandwidth needed to store these data. The data rates, before trigger, range from <1 TB/s for ZH running up to several TB/s at the Z peak with an expected event size below 2MB. The storage rate after the trigger ranges from 0.1 for ZH to 100 kHz at the Z pole. Contributions from beam-related backgrounds (for both single-beam and sources that scale with luminosity) are based on dedicated simulations and are included in rate estimates and preliminary trigger design.
- The baseline plan is to transmit the full raw data to the front-end electronics and connect the trigger to the back-end electronics. This strategy is sound. Similar strategies have been successfully implemented in CMS and LHCb, where data rates are much higher. A hierarchical trigger scheme is foreseen to bring event data rates down from ~3MHz to ~1kHz in HZ running and ~40 MHz to ~100 kHz at the Z pole.
- Early trigger studies are based on primitives from the calorimeter and muon detector which show promise for selecting desired physics at high efficiency while rejecting beam backgrounds. These studies do not yet include any high-level trigger information, which should be very effective at further refining the selection.
- The system design foresees a common hardware trigger board to collect trigger primitives from the BEE common boards and send trigger accept signals to the BEEs. High-throughput DAQ and processing building on the RADAR framework used in previous projects will be extended to meet the requirements at CEPC. Initial designs for the Timing, Clock, and Control Distribution System (TCDS/TTC), as well as the Detector Control System (DCS) and Experiment Control System (ECS), are currently under development. The hardware trigger scheme is also in progress, with a preliminary design already presented. As more detailed information about data volumes from individual detectors becomes available, several key design decisions will need to be made to ensure optimal system performance
- The RDT has extensive experience in TDAQ and has designed and built hardware boards, firmware and software for several leading projects: BESIII, PANDA at GSI, Belle2 and CMS as well as several neutrino experiments, and have implemented machine learning (a NN for tau reconstruction) in the ATLAS global trigger upgrade. Their expertise is consistent with providing the TDAQ for the CEPC reference detector, and they are planning to increase capacity by adding additional members.

# Comments



- The detailed (bottom-up) design of the TDAQ must await further details on the subdetector design.
- Work on the trigger primitives is needed to bring the rate down to an acceptable input for the second-level trigger, and to inform further planning for the processing farms in the DAQ design. Should it be needed, a track trigger could provide a powerful additional primitive.
- High-level triggering will also need to weigh the physics-versus-bandwidth tradeoff for lower-energy events, e.g. from gamma-gamma collisions.

- Agree. Especially background study and data rate estimation from each sub detectors.
- Beam background could be compressed 99% with basic trigger primitives from Ecal/Hcal and Muon. Track trigger is under simulation both for L1 and HLT
- Need more simulation and study

# Recommendations



1. Prioritizing a straightforward simulation of subdetector-based trigger inputs using robust algorithms is essential. The simulation should include an appropriate safety factor for beam-related backgrounds. This approach will enable a more detailed specification of the requirements for TDAQ hardware and help identify areas that require further attention.
2. Further work should include an evaluation of benefits of implementing a track trigger as a complement to the calorimeter and muon primitives, and to clarify the bandwidth foreseen for gamma-gamma events.

- According to primary simulation with all detectors, calorimeter energy and muon hit trigger condition are good efficiency. A 10-fold safety factor for beam related backgrounds has been investigated. 100-fold safety factor is planed.
- Under study, advanced algorithm like ML could be useful.

# Research Team

- 15 staff of IHEP TDAQ group
- DAQ (4/6)
  - Fei Li (DAQ, team leader)
  - Hongyu Zhang (readout)
  - Xiaolu Ji (online processing)
  - Minhao Gu (software architecture)
- Trigger (4/5)
  - Zhenan Liu (trigger schema)
  - Jingzhou Zhao (hardware trigger)
  - Boping Chen (simulation/algorithm)
  - Sheng Dong (firmware/DCS)
- DCS/ECS (1/4)
  - Si Ma

- IHEP Students(20 totally)
  - 2 PhD and 3 master
- New member planned
  - 1 staff
  - 2 postdoc
- Collaborators
  - Qidong Zhou (HLT, SDU)
  - Yi Liu (HLT, ZZU)
  - Junhao Yin(HLT, NKU)
  - 3 students planned
- We're looking for more collaborators

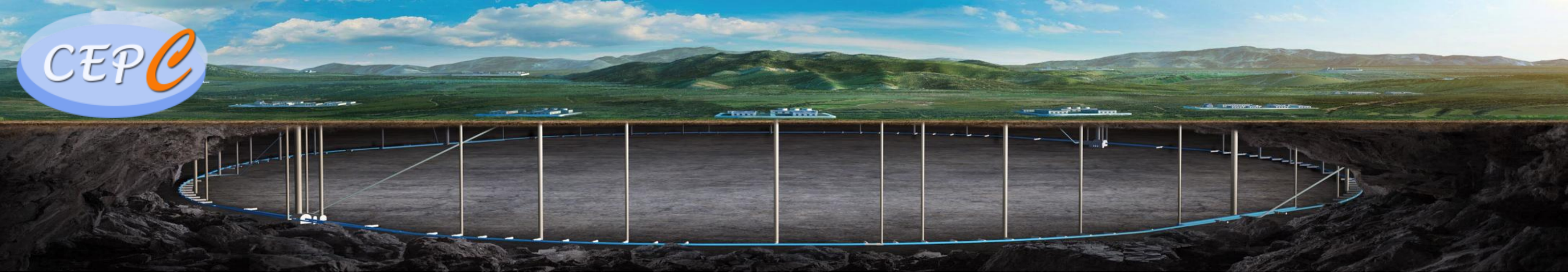
Gathering manpower for R&D, 9 staff and 5 students was involved from IHEP

# Working plan

- TDR related
  - Further simulation and algorithm include low energy event from $\gamma\gamma$ collisions
  - Detailed hardware trigger and interface design
  - Finalize TDAQ and online design scheme
- R&D directions
  - Trigger hardware, fast control and clock distribution
  - High throughput software framework(RADAR)
    - FPGA/GPU acceleration and heterogeneous computing
    - Memory-based distributed buffer
  - Detailed trigger simulation and algorithm
  - ML/AI algorithm application
    - Trigger/data compression/ AI operation and maintenance
  - ROCE/RDMA readout protocol and smart NIC

# Summary

- Following update of sub detectors design and simulation
- Many progress for technical design of TDAQ and online
- No critical technology risk found for TDAQ and online scheme
  - Challenges: efficient trigger algorithm and handling data at manageable hardware scale
- More detailed R&D efforts needed to move forward

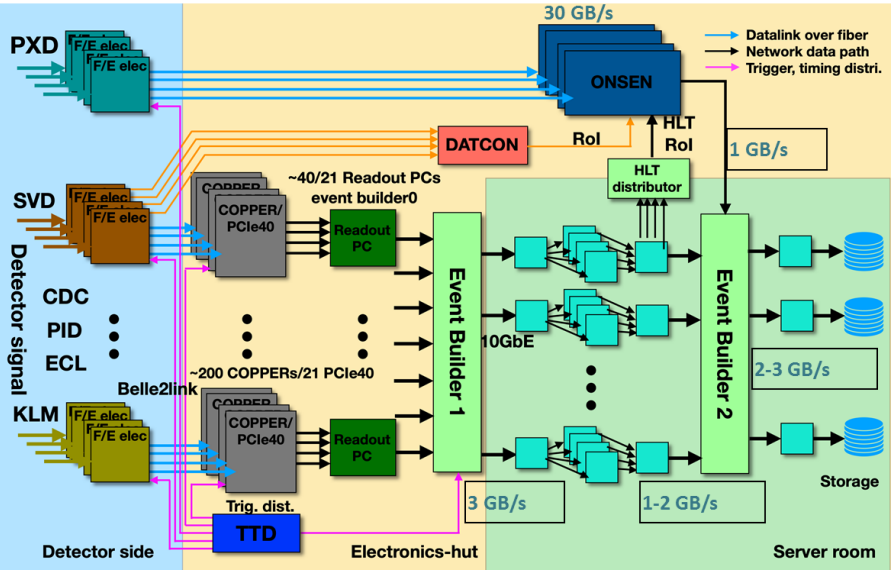


# Thanks for your attention!

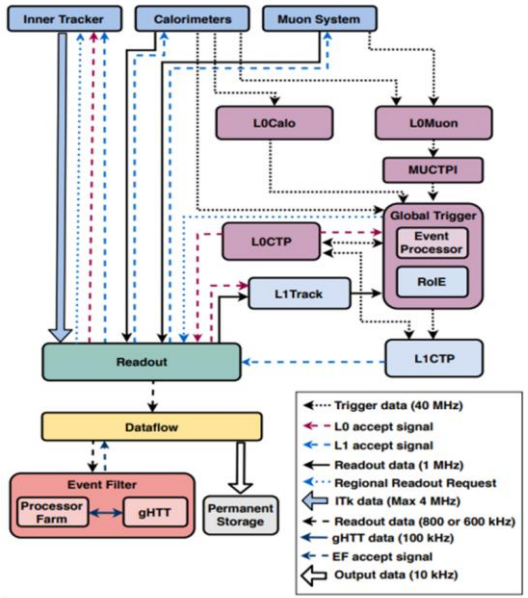
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# Technology survey

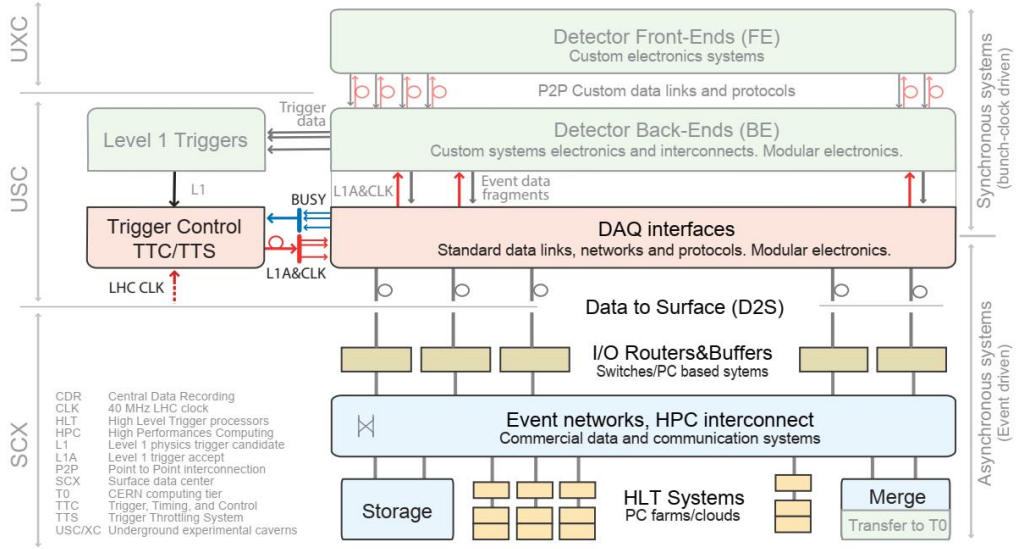
BELLE II



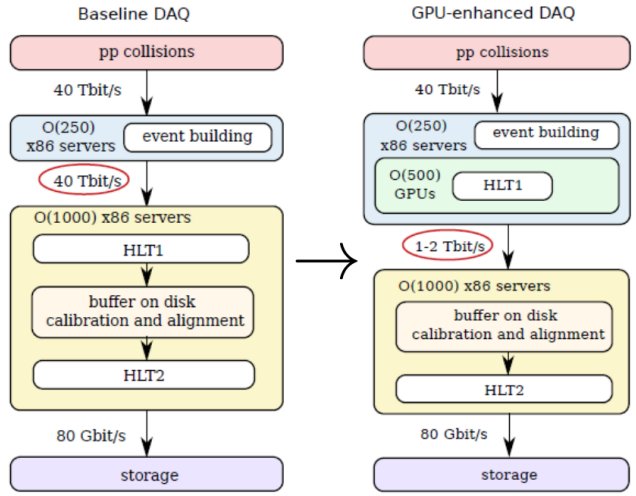

ATLAS Phase II




CMS Phase II




LHCb Phase II




- A few common backend boards (ATCA)
- Network or PCIe bus readout
- GPU/FPGA acceleration at HLT, ML in trigger
  - GPU power has increased 1,000 times in the last decade
- Full software trigger @LHCb
  - Deal with higher occupancy and more accurate tracking.

# Previous experience with TDAQ Hardware

- Designed and constructed BESIII trigger system
  - Comprehensive trigger simulation/hardware design/core trigger firmware development
- GSI PANDA TDAQ R&D
  - High performance computing node (HPCN) board
- Designed and constructed for Belle II DAQ
  - Belle2Link and HPCN V3 as ONSEN
- Constructed CPPF system for CMS Phase-I trigger
  - MTCA board, Cluster finding for Muon/RPC
- Designing for CMS Phase-II backend and trigger
  - ATCA common board for iRPC/RPC



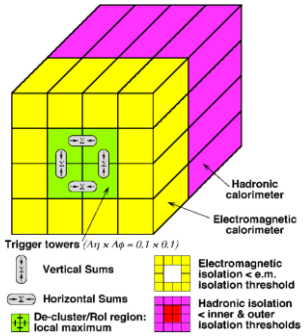


Extensive experience in TDAQ system design, algorithm and hardware development

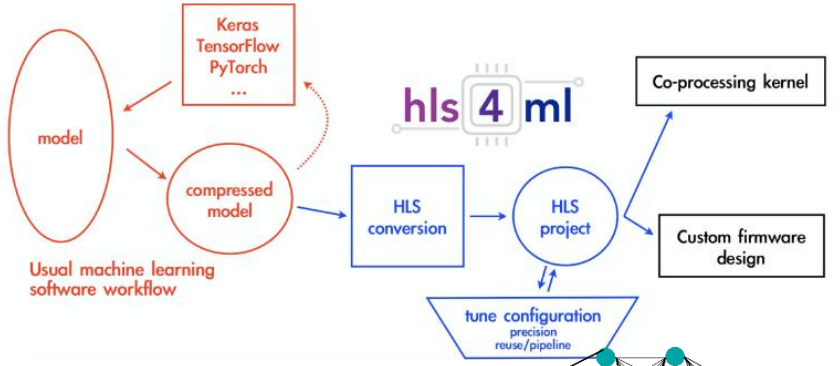
# Previous experience with ML algorithm

## Neural network used in ATLAS global trigger

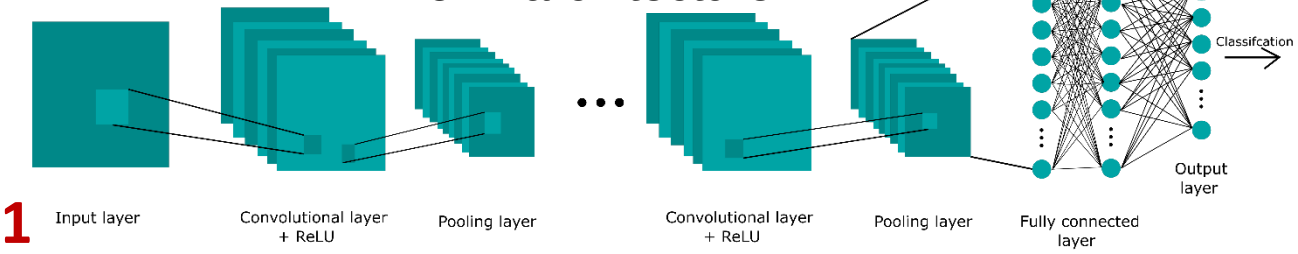
- Example: tau reconstruction at the hardware trigger level
- Train the neural network (NN) with ROI
- Use hls4ml to convert NN model to hls project



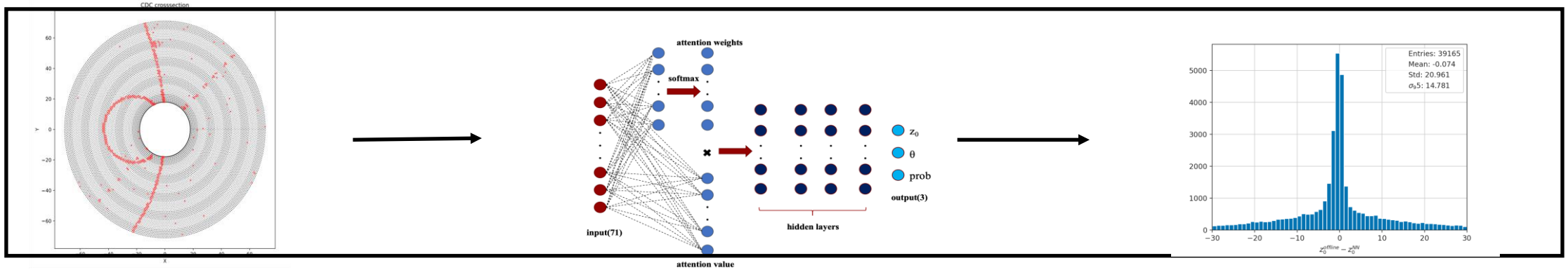

Seed and cluster




CNN architecture



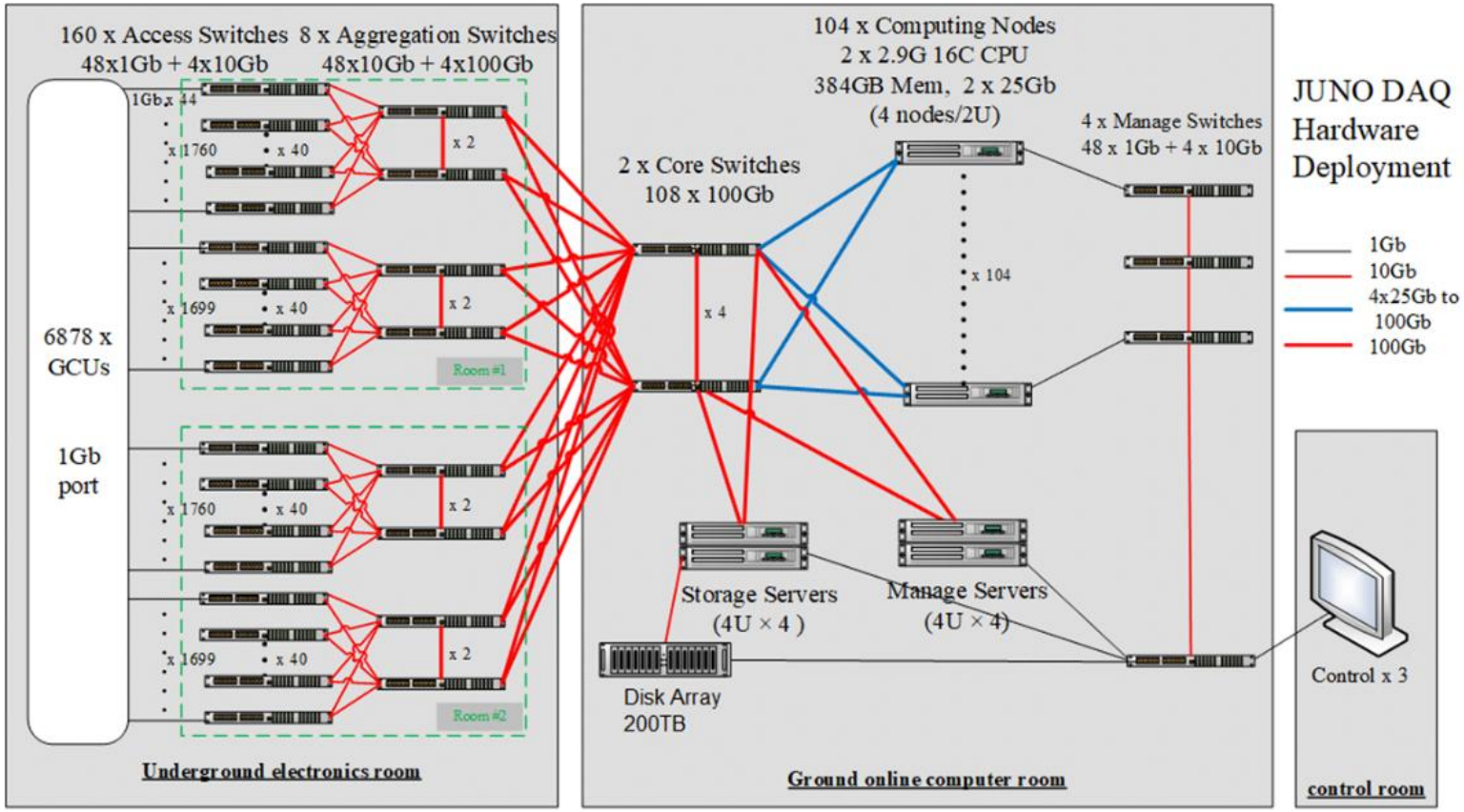

## DNN based tracking algorithm for Belle II L1




Some experience in ML algorithm development at L1 trigger

# Previous experience with DAQ&DCS

- BESIII DAQ & DCS
  - Running since 2008
- Dayabay experiment DAQ&DCS
  - Operated from 2011 to 2020
- LHAASO DAQ
  - Operated since 2019
  - Full software trigger
- JUNO DAQ&DCS
  - Two types of data stream
    - HW trigger for waveform
    - Software trigger for TQ hits
  - Online event classification




Extensive experience in DAQ&DCS development and operation, including software trigger