Wafer Probing @IHEP Status and Plan

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IHEP

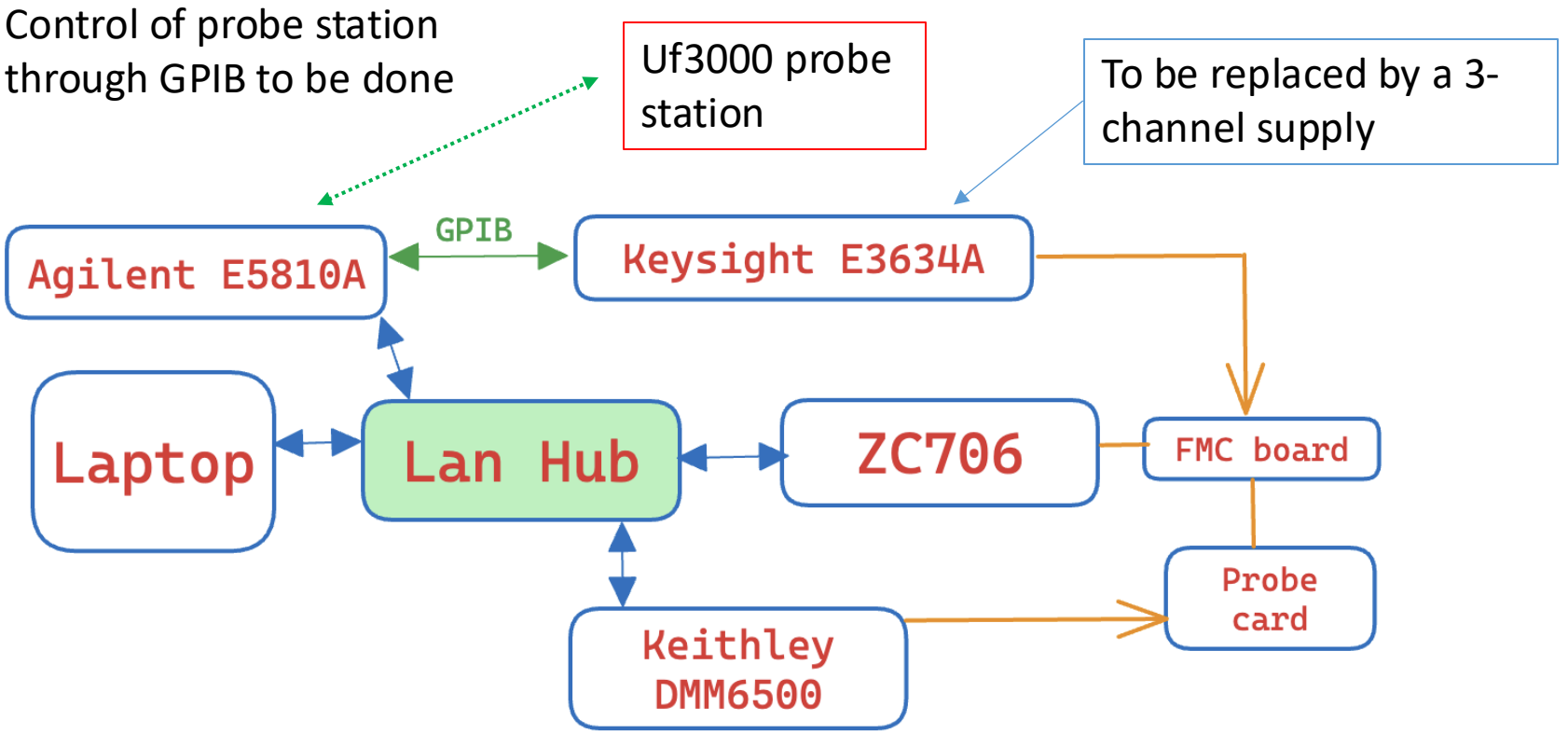
Current status and plan

- Tested about half of the wafer
  - Most scans are tested, results are reasonable
  - Some tests still not validated yet: efuse, lumi, sram, speed
- Probe card has been repaired
  - Lack of experience about cleaning of probe tips
  - Need to be more careful when tuning the contact to the WB pads
- Plan: finish probing on first wafer before next mini-week
  - Maybe go to the lab later this week or next week, to be confirmed with the lab about the schedule
  - Probe card modifications need to be done in Shanghai
  - Modifications on FMC board to use external vdd can be done at IHEP, but need to be further confirmed by IJCLab (Miaoran)
  - Expect 2 days for validate setup and 2 days of probing

List of tests and criteria

- Luminosity scan
  - passing at least one shifted window contains all the hits
- SRAM scan
  - Not defined yet
- Monitoring scan
- Vthc scan @ Vth=380 -> determine per pixel threshold correction
  - Dac_vthc within 10 ~ 240
- Charge scan @ Vth=400
  - Eff<0.1 when Qdac=0, Eff>0.95 when Q=10 fC, threshold within 1 fC ~ 8 fC, noise < 0.4 fC, jitter < 50 ps when Q=10 fC, TOTRMS <150 when Q=10 fC
- Speed test (charge scan at different speed)
  - Eff > 0.99
- Width scan -> TOT LSB
  - TOT LSB within 100 ps ~ 200 ps
- Delay scan -> TOA LSB
  - TOA LSB within 5 ps ~ 40 ps

Setup schematic

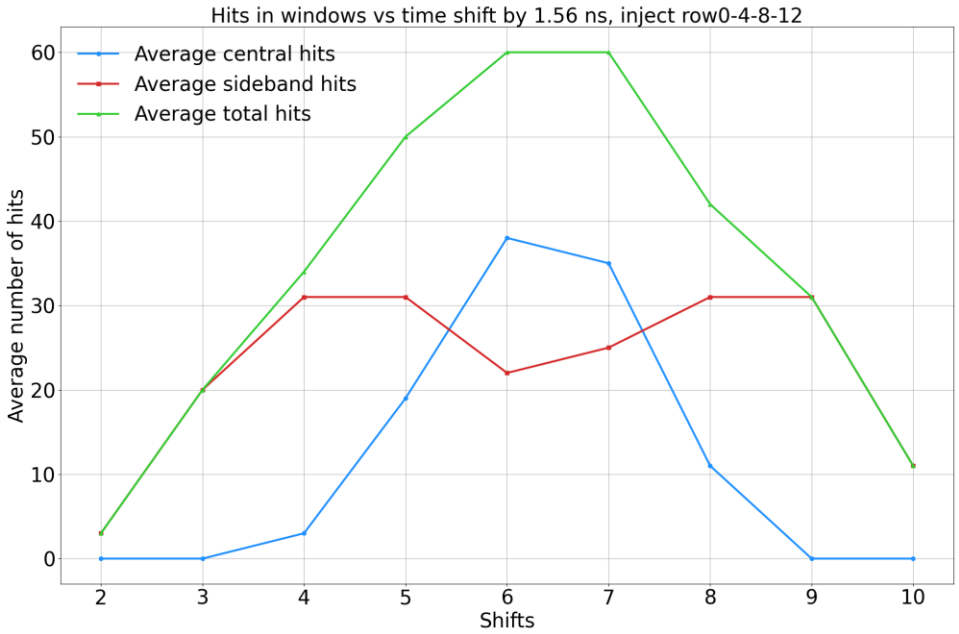


Most equipment are connected by LAN through a Lan hub.
LV power supply connected by GPIB

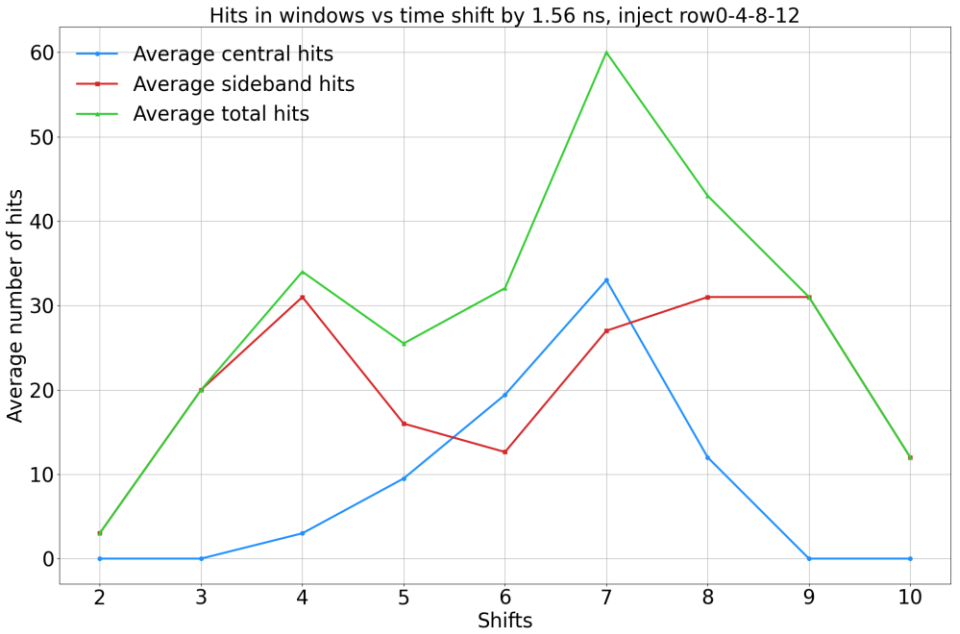
Review of past results

Luminosity

Chip37 (05,08)



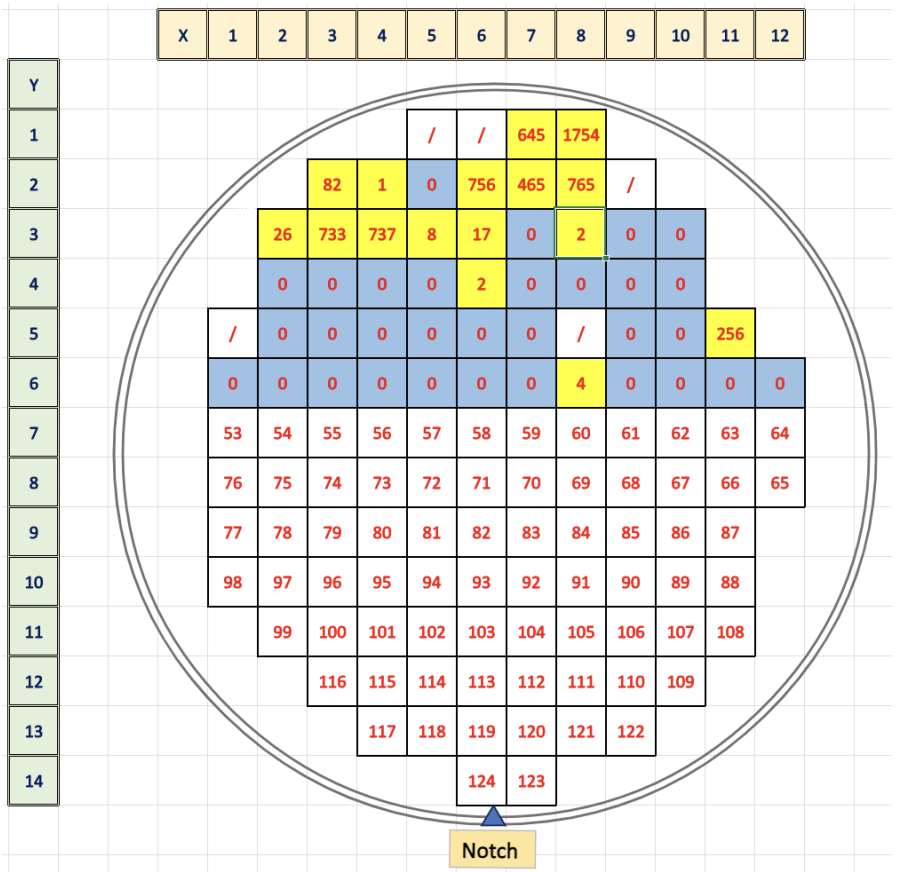
Chip79 (09,03)

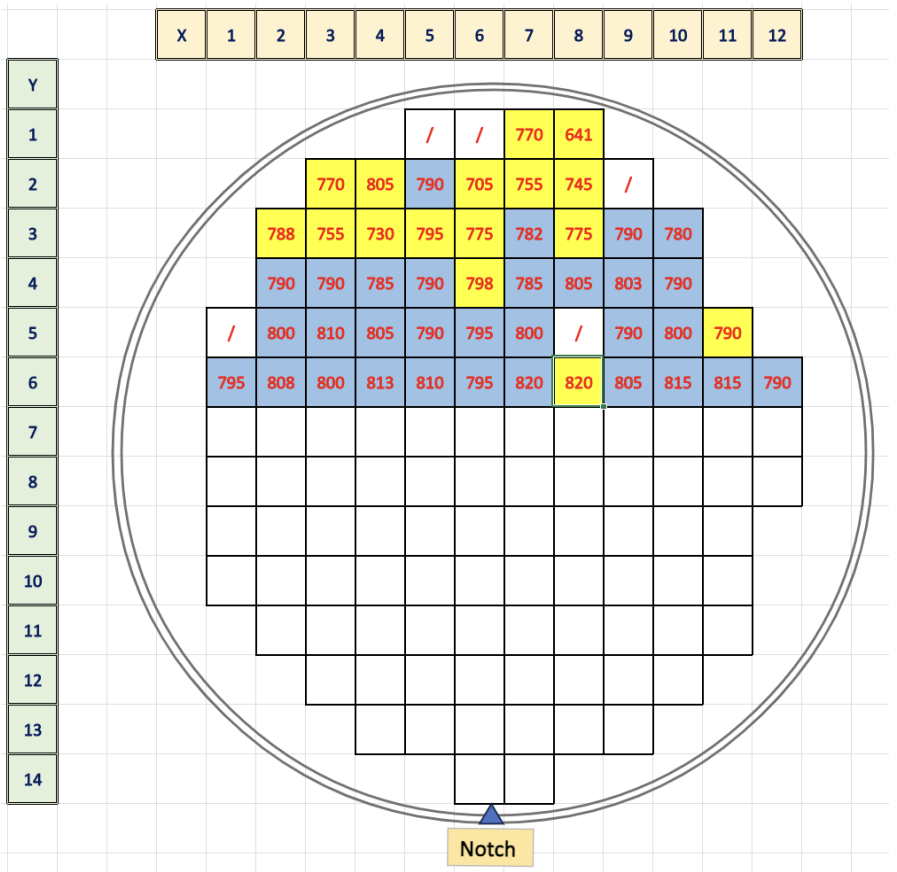


We only have luminosity tested with updated scripts for few chips, the results seem not good. Total hits vary a lot, is this due to the windows setting?

Need more tests to understand

SRAM test analysis



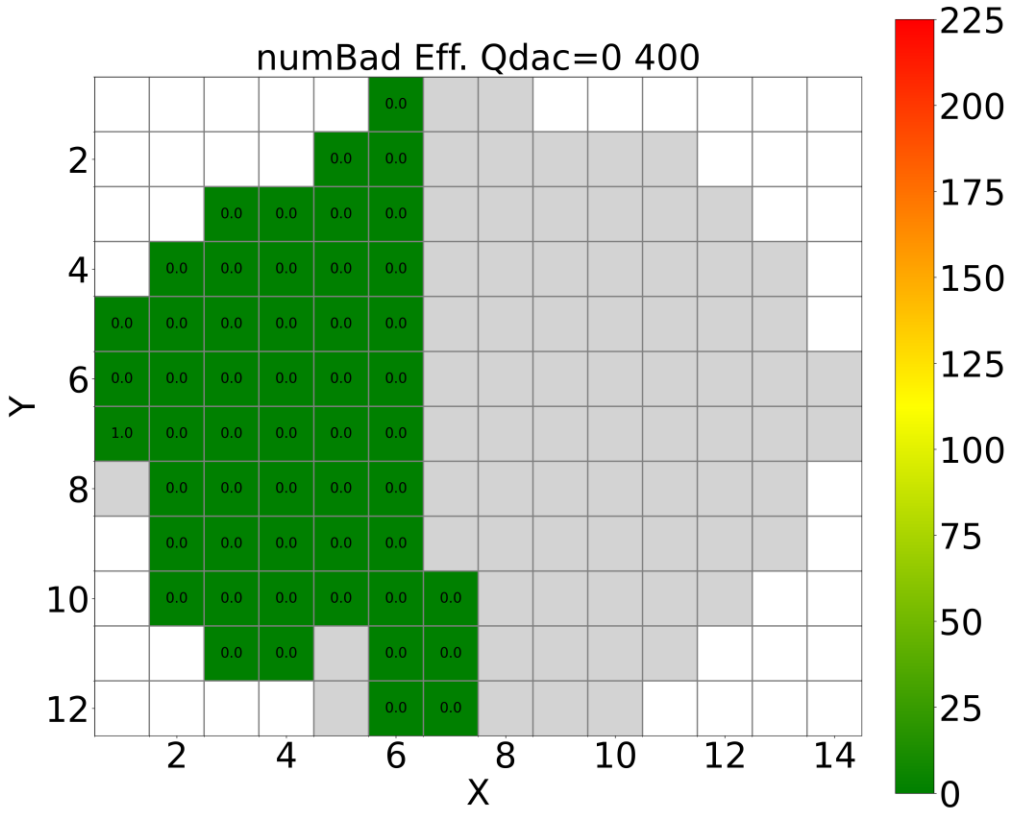


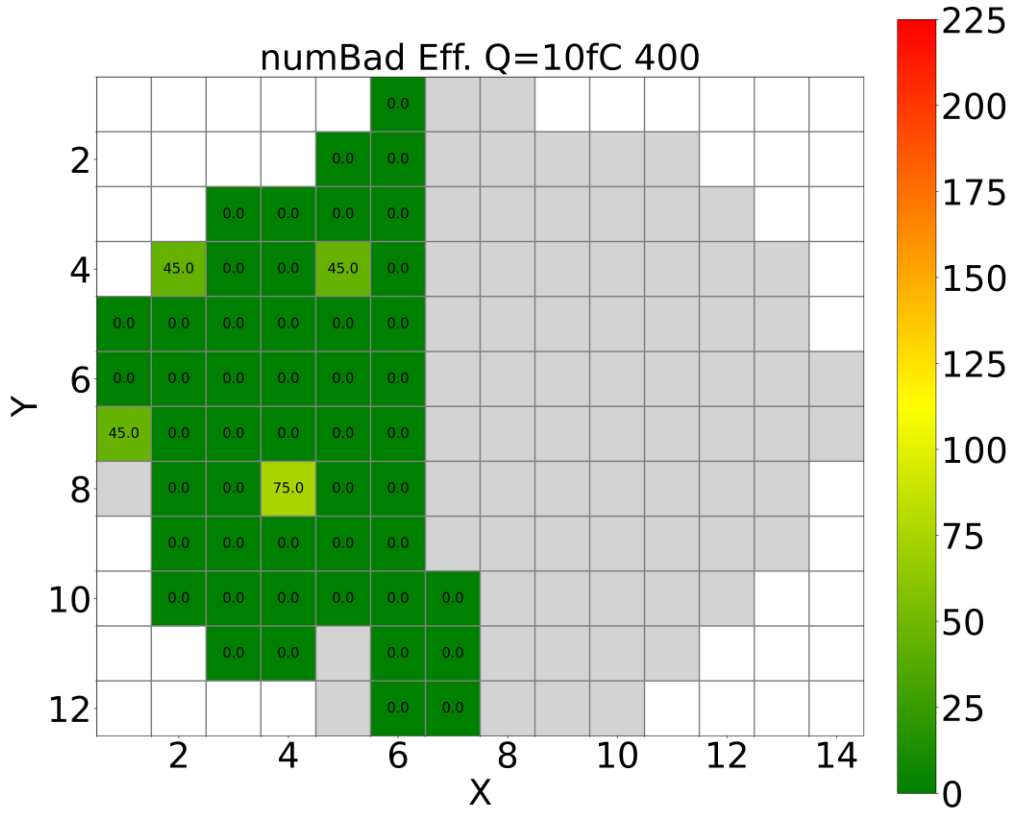
Number of error reported by SRAM test

Monit_Vddd

Need more tests to confirm the impact of vddd

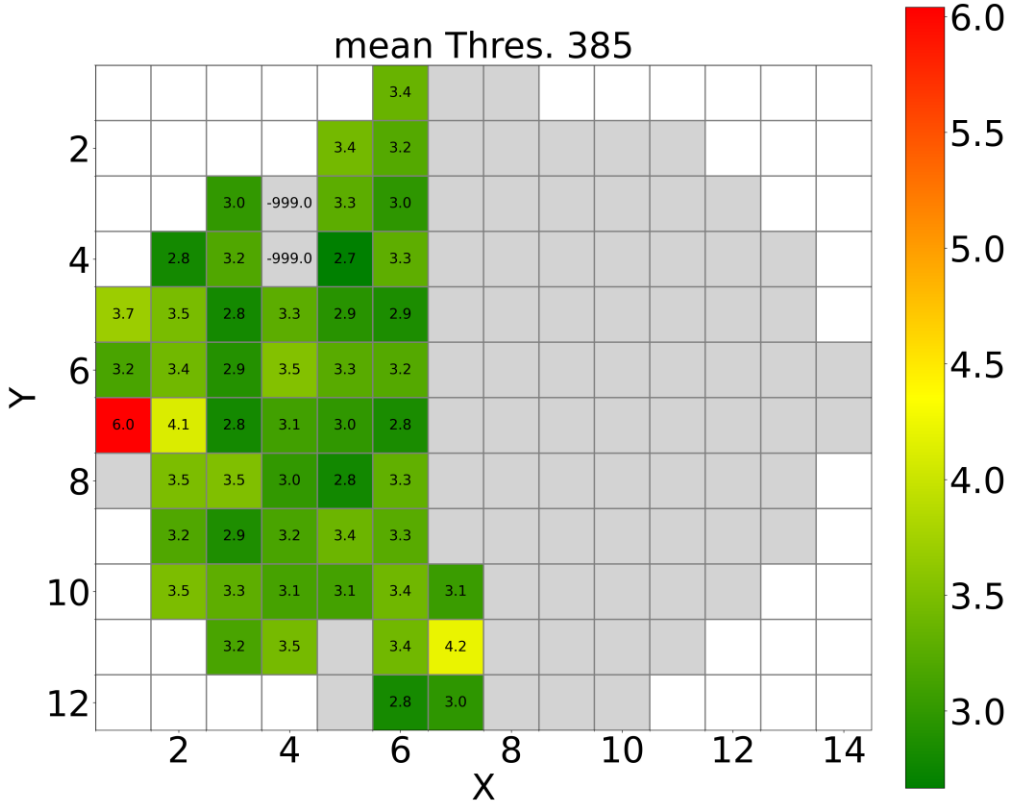
Charge scan efficiency curve

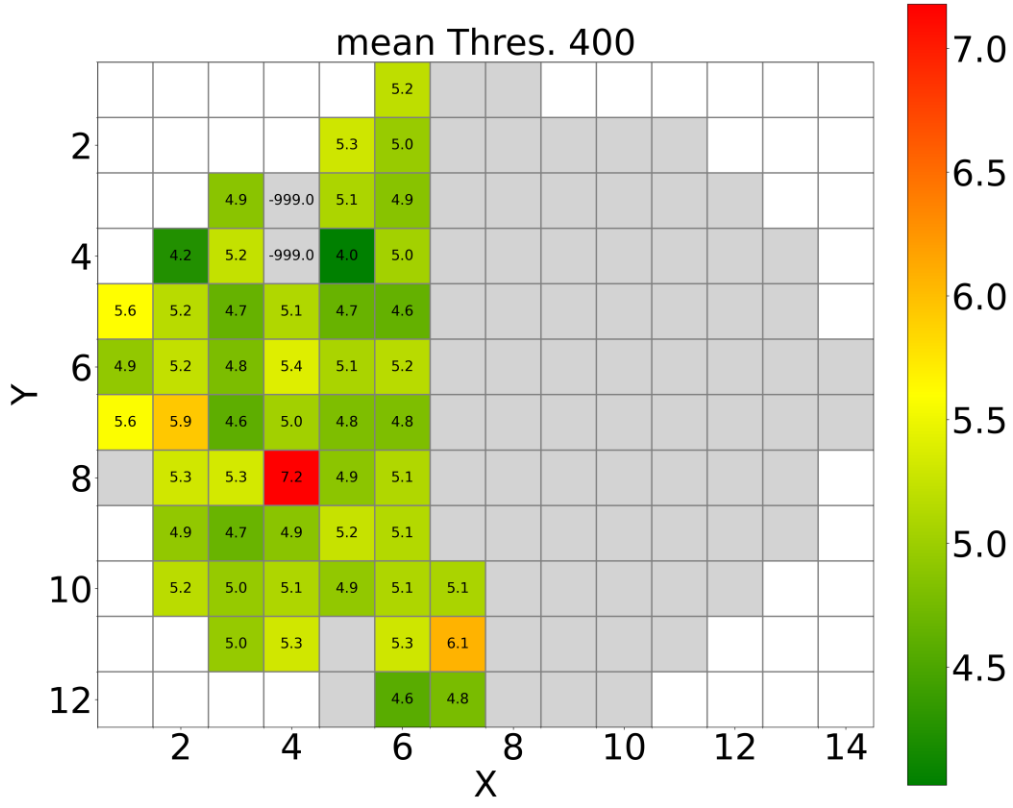




Charge scan @ Vth=400, efficiency is much better (except some chips known to be bad)

Charge scan threshold

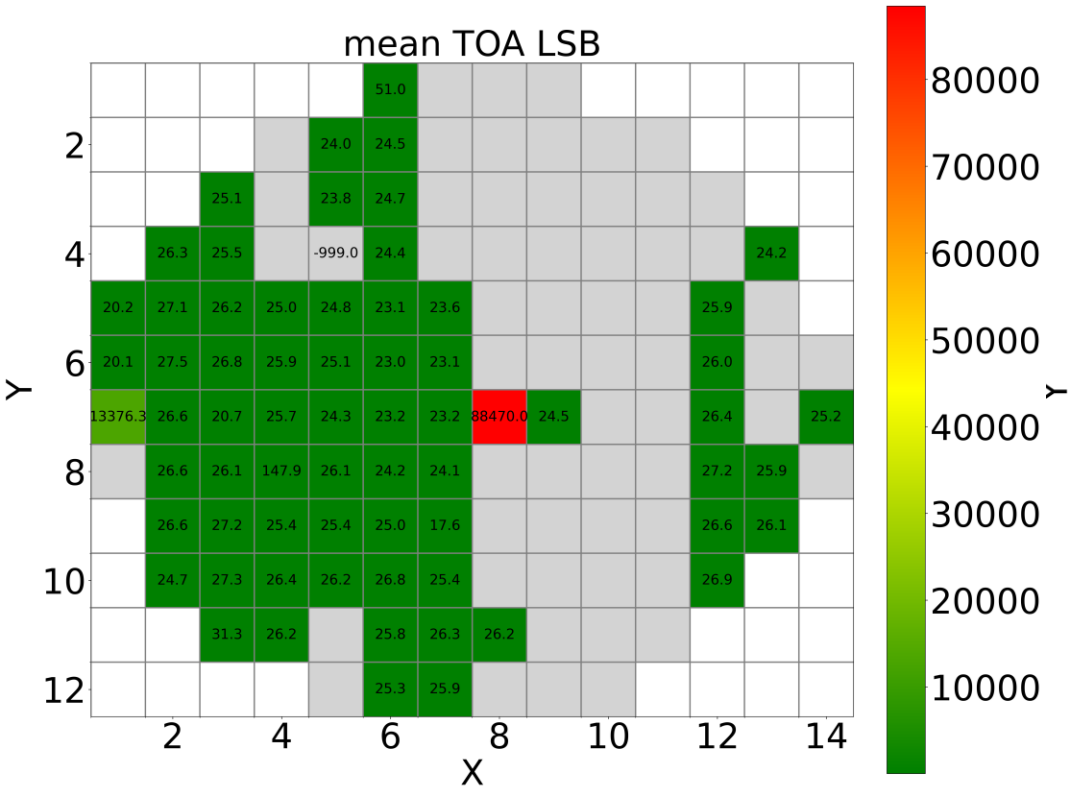


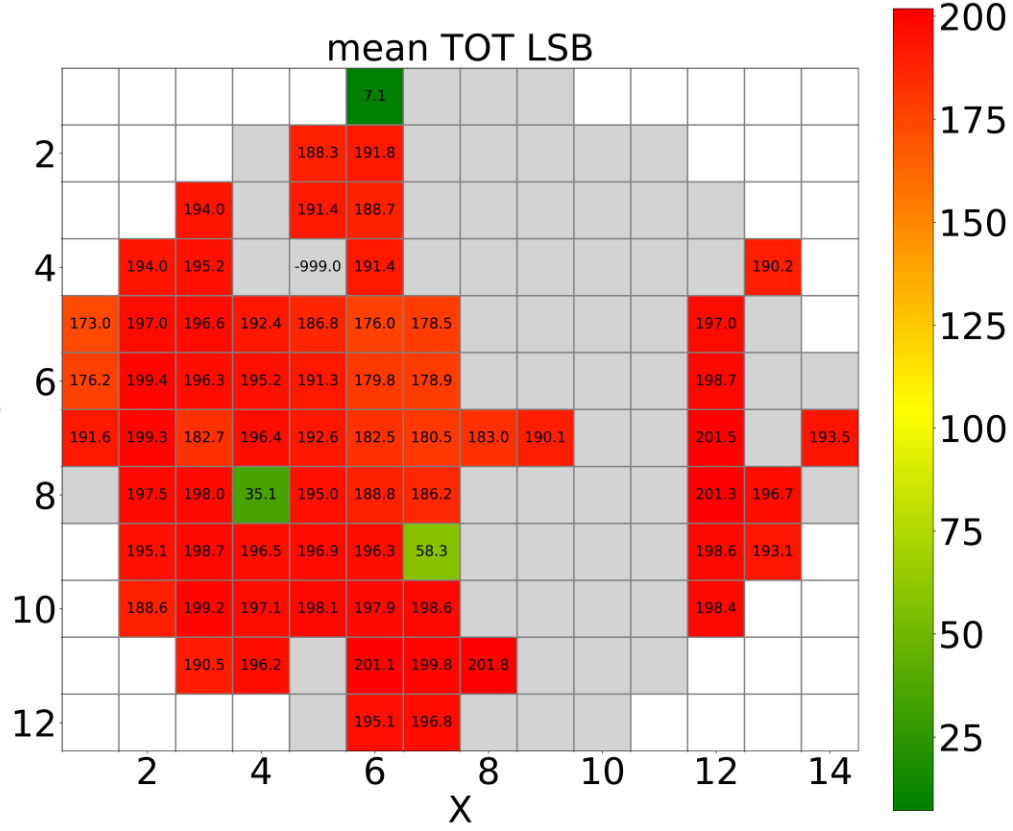


Threshold @ Vth=385 ~ 3 fC but with quite large variation

Threshold @ Vth=390 ~ 5 fC, much better uniformity

TOA and TOT LSB





TOA and TOT LSB are basically OK

TOT LSB can be further reduced by tuning Vctrl voltage

Things to be done

EFUSE

- Need another 2.5V power supply on probe card for burning and reading
- Modification to be done on probe card:
  - Remove Relay_2RT, R94, D3 and Q3
  - R100 with 0 Ohm
  - Confirmed by Jimmy, all components found on probe card
- From Miaoran, the modification and scripts work at IJCLab
  - Will be tested with highest priority when we resume probing
- EFUSE string definition:
  - 1 bit of test site
  - 7 bits of chip id
  - 8 bits of wafer id
  - 2 bits of production batch

2.3 ASIC

A serial number of the ASIC component looks like : 20 W AS V P DDDDCCC .

Digit	Represent	Comment
1,2	20	ATLAS experiment
3	W	HGTD sub-detector project
4,5	AS	AS=ASIC
6	V	Test site: V=H (IHEP), V=J (IJCLab)
7	P	Production: P=M (main production), P=P (Pre-production) P=D (demonstrator), P=T (test), P=O (other)
8..,12,13,14	DDDDCCC	Wafer_ID: Wafer_ID=Wafer_Nr*1000 + Chip_ID Chip_ID: is given by geometrical position in wafer Wafer_ID=DDDDCCC, DDDD=Wafer_Nr, CCC=Chip_ID

Table 4: ASIC serial number definition.