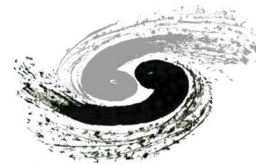


中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

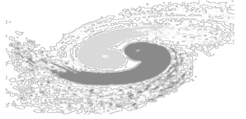
# Status of the Elec-TDAQ system for the CEPC Det. Ref-TDR

**Wei Wei**

**On behalf of the Elec-TDAQ system of the CEPC Ref-TDR**

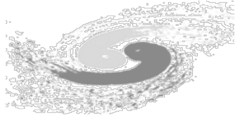
**2025-01-24**
**CEPC Day**

# Outline



- **Summary of the connection, crate & power**
  - **Update of the electronics room arrangement**
- **Status of the key ASICs R&D**

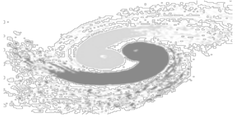
# Summary table for FEE related information @Higgs



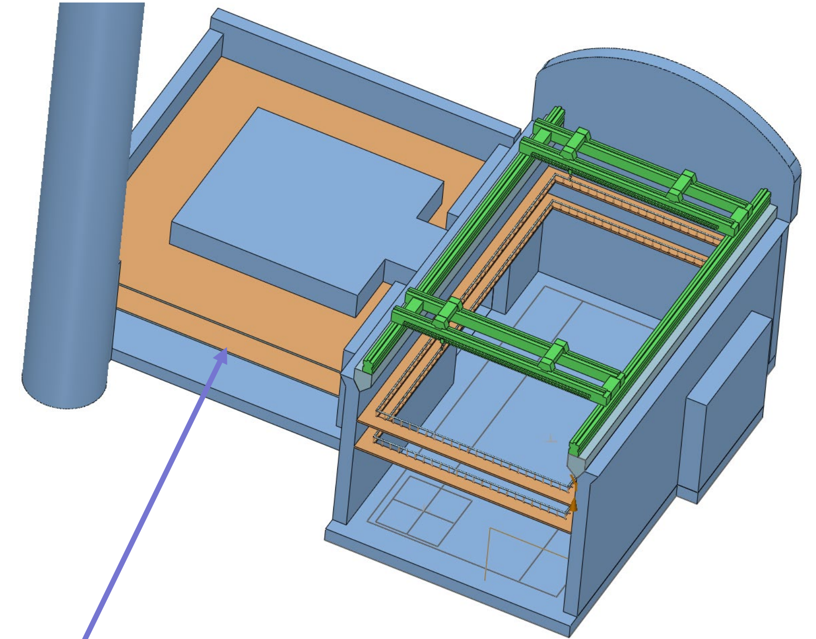
| Detector | Max data rate per fiber (Gbps) | Fibers per module | Fiber sum | BEE sum | Data crate sum | Module Max Power (W) | Total Power (kW) | Power channels | Power crate sum | HV requirements | HV channels sum | HV crates sum | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VTX | 8 | 1~2 | 88 | 6 | 1 | 25 | 0.45 | 66 | 2 | ~-10V | 66 | 1 | |
| TPC | 0.1 | 1 | 496 | 32 | 4 | 32.2 | 16 | 496 | 6 | -500V | 496 | 4 | |
| ITK-Barrel | 0.96 | 1 | 2204 | 139 | 14 | 11.2 | 31.59 | 2204 | 29 | 50~200V | 2204 | 10 | |
| ITK-EndCap | 2.2 | 1 | 1696 | 106 | 12 | 7.4 | 11.1 | 192 | 2 | 50~200V | 1696 | 8 | |
| OTK-Barrel | 1.4 | 1 | 540 | 34 | 4 | 56.3 | 251.1 | 3780 | 79 | 150~200V | 3780 | 17 | Det needs opt |
| OTK-EndCap | 0.7 | 1 | 720 | 45 | 6 | 58.9 | 35.6 | 720 | 16 | 150~200V | 720 | 4 | Det needs opt |
| ECAL-Barrel | 4.8 | 2 | 960 | 60 | 6 | 31 | 17.5 | 480 | 5 | 40~60V | 480 | 2 | |
| ECAL-EndCap | 4.8 | 2 | 520 | 34 | 4 | 31 | 9.5 | 260 | 4 | 40~60V | 260 | 2 | |
| HCAL-Barrel | 0.14 | 1 | 5536 | 346 | 36 | 9 | 66.1 | 5536 | 58 | 40~60V | 5536 | 26 | |
| HCAL-EndCap | 1.75 | 1 | 3072 | 192 | 20 | 11 | 41.3 | 3072 | 32 | 40~60V | 3072 | 14 | |
| Muon-Barrel | 0.004 | 1 | 288 | 18 | 2 | 2.6 | 0.76 | 288 | 3 | 40~60V | 288 | 2 | |
| Muon-EndCap | 0.01 | 1 | 96 | 6 | 1 | 4.7 | 0.45 | 96 | 1 | 40~60V | 96 | 1 | |
| Sum | | | 16216 | 1018 | 110 | | 481.45 | 17190 | 237 | | 18694 | 91 | |

Only FEE Power summarized in the table. Extra power for BEE & crate efficiency hard to be calc. at the moment

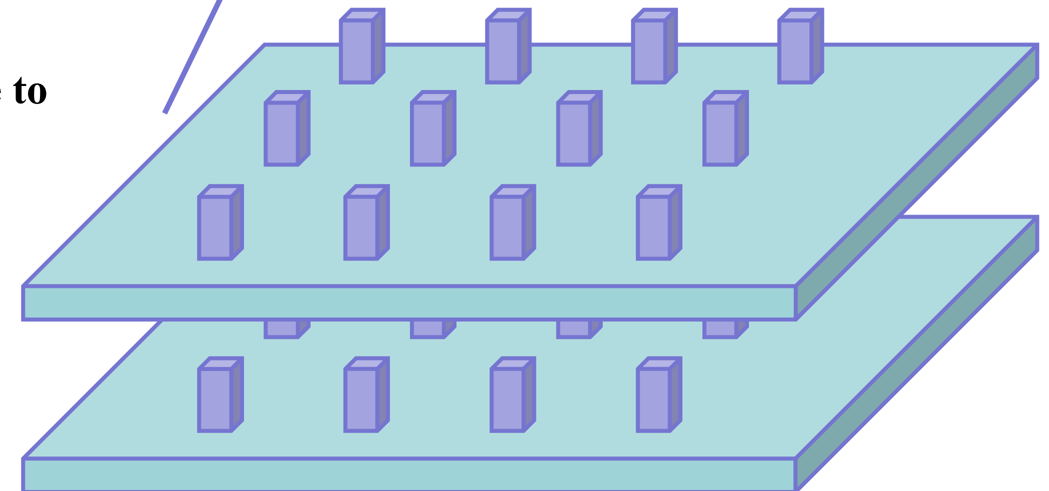
# Electronics room



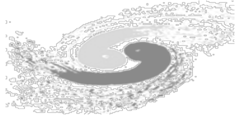
- Minimum crates from current MDI
  - 110 data crates, 237 power crates, 91 Det-HV crates, 20 Trigger crates
- Minimum racks from current MDI
  - 37 data racks, 24 power racks, 23 Det-HV racks, 10 trigger racks (94 in total)
  - More 2 racks for AC-DC power for all the above racks
  - 96 racks in total
- Racks Size: 0.5m × 0.5m
- Side clearance 1.5m for heat, face clearance 2m for cabling & heat
  - Very rough estimation: 20% more power will be consumed due to the crate efficiency
- Total room: $500m^2 \times 2$floor = 25m × 20m × 2floor
  - 10 × 10 × 2=200 racks capacity
  - Necessary redundancy for future upgrade



See Quan Ji's talk on Mechanics

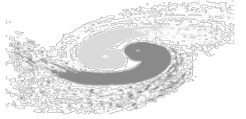


# Comment on (some of) the ASIC/chip power



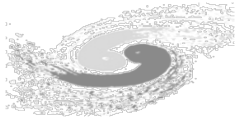
- Taichu-Stitching @ Vertex
  - 40mW/cm$^2$ (@TJ65nm)
  - Same level as ALICE-ITS3 (world leading), but with higher (bkgrd) rate (higher challenge)
  - Currently have difficulties of using TJ65 (political issues), if only TJ180nm can be used, the power will be 60mW/cm$^2$
- Juloong @ OTK
  - 20mW/ch @ 7pF Cd for 30ps
  - Strongly depend on sensor design & capacitance & timing requirement
  - Current value is a self-consistent calculation based on current AC-LGAD, only for Ref-TDR
  - Co-optimization is a must for sensor, electronics & cooling (urgent sensor prototyping on going)
- ChoMin @ SiPM for ECAL/HCAL/Muon
  - 15mW/ch
  - Same level as HGCROC (state-of-the-art), a reasonable value and seems not a heavy load for cooling by simulation
  - Concerning on the high bkgrd-rate, lower power is not reasonable at current stage
  - However, many spec not well-understood related to the SiPM-device, crystal & bkgrd, ASIC scheme may have to change with a higher power

# Comment on other chip power



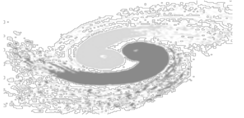
- COFFEE @ ITK
  - 200mW/cm$^2$, a typically value of a pixel chip
- “TEPIX” @ TPC
  - 100mW/cm$^2$
  - Total power of 8kW/endcap, limited directly by detector design
- Common ASICs
  - ChiTu @ Data Link
    - 0.75W, same value as lpGBT (world-leading in HEP)
  - KinWoo @ Opto-elec interface
    - 0.25W, same value as VTRx (word-leading in HEP)
  - TaoTie @ Data Aggregation
    - Currently power & spec is not strongly constraint
    - Will be focusing on ChiTu implementation, and to be understood in the next stage
  - Basha series@ power
    - Power conversion efficiency 80%~90%
    - Same level as bPol (world-class in HEP)

# Summary table for data



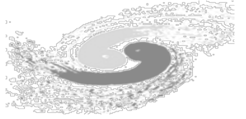
| | Vertex | Pix(ITKB) | Strip (ITKE) | OTKB | OTKE | TPC | ECAL-B | ECAL-E | HCAL-B | HCAL-E | Muon |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Channels per chip | 512*1024 Pixelized | 512*128 | 1024 | 128 | | 128 | 8~16 @common SiPM ASIC | | | | |
| Ref. Signal processing | XY addr + BX ID | XY addr + timing | Hit + TOT + timing | ADC+TDC/TOT+TOA | | ADC + BX ID | TOT + TOA/ ADC + TDC | | | | |
| Data Width /hit | 32bit | 42bit | 32bit | 40~48bit | | 48bit | 48bit | | | | |
| Max Data rate / chip | 2Gbps/chip@Triggerless@Low LumiZ Innermost | Avg. 3.53Mbps/chip<br>Max. 68.9Mbps/chip | Avg. 21.5Mbps/chip<br>Max. 100.8MHz/chip | Avg：2.9Mbps/chip<br>Max：3.85Mbps/chip | Avg：38.8Mbps/chip<br>Max：452.7Mbps/chip | ~70Mbps/module Inmost | Avg. 0.96Gbps/module<br>Max:9.6Gbps/module | | Max. 144Mbps/module-layer | Max. 350Mbps/module-layer | Max： 10 Mbps/board |
| Data aggregation | 10~20:1, @2Gbps | 14:1@O(100Mbps) | 22:1 @O(100Mbps) | i. 22:1 @O(5Mbps)<br>ii. 7:1 @O(100Mbps) | i. 22:1 @O(50Mbps)<br>ii. 10:1 @O(500Mbps) | 1. 279:1 FEE-0<br>2. 4:1 Module | i. 4~5:1 side<br>ii. 7*4 / 14*4 back brd @ O(100Mbps) | | < 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC) | < 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC) | <=24:1 @ O (400 Mbps) |
| Detector Channel/module | 1882 chips @Stch &Ladder | 30,856 chips 2204 modules | 23008 chips 1696 modules | 83160 chips 3780 modules | 11520 chips 720 modules | 492 Module | 0.96M chn ~60000 chips 480 modules | 0.52M chn ~32500 chips 260 modules | 3.38M chn 5536 aggregation board | 2.24M chn 1536 Aggregation board | 43.2k ch 72 Aggregation board |
| Avg Data Vol before trigger | 474.2Gbps | 101.7Gbps | 298.8Gbps | 249.1Gbps | 27.9Gbps | 34.4Gbps | 460Gbps | 250Gbps | 811.2Gbps | 537.6Gbps | ~ 2.07 Gbps |

# A summary of FEE power



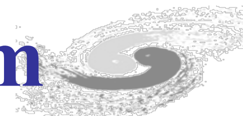
| | Vertex | Pix(ITKB) | Strip (ITKE) | OTKB | OTKE | TPC | ECAL-B | ECAL-E | HCAL-B | HCAL-E | Muon |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Channels per chip | 512*1024 Pixelized | 512*128 | 1024 | 128 | | 128 | 8~16 @common SiPM ASIC | | | | |
| Technology | 65nm CIS | 55nm HVCMOS | 55nm HVCMOS | 55nm CMOS | | 65 CMOS | 55nm CMOS (or 180 CMOS?) | | | | |
| Power Supply Voltage (for DC-DC) (V) | 1.2 | 1.2 | 1.2 | 1.2 | | 1.2 | 1.2 (or 1.8?) | | | | |
| Power@chip | 40mW/cm$^2$ 200mW/chip | 200mW/cm$^2$ 800mW/chip | 200mW/cm$^2$ 336mW/chip | 20mW/chn 2.56W/chip | | 280μW/chn 35mW/chip 100mW/cm$^2$ | 15mW/chn 240mW/chip | | | | |
| Max chips@module | 29 | 14 | 22 | 22 | 3 | 1115 | 64 | 120 | 8 | 92 | 167 |
| Power@module (W) | 5.8 | 11.2 | 7.39 | 56.3 | 58.9 | 32.2 | 30 | 30 | 9 | 11 | 4.7 |

# Status of the new ASICs R&D



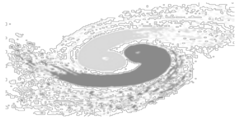
- (Major) concern/comment from IDRC on Electronics system:
  - By far the highest risk in the electronics is designing and delivering the 6 FEE-ASICs needed. For the 6 FEE-ASICs needed to readout the detector subsystems, there is significant effort needed.
  - There are design teams already working on 2 of the chips (for VTX and TPC detectors) and another has been identified for the ITK.
- New ASICs (common & FEE) R&D Plan & team
  - HVCMOS@ITK, TEPIX@TPC not focused
    - Chip prototypes & fixed design team already exists for several years
- Current status

# Timeline for all the FE ASICs – common ASIC – long term

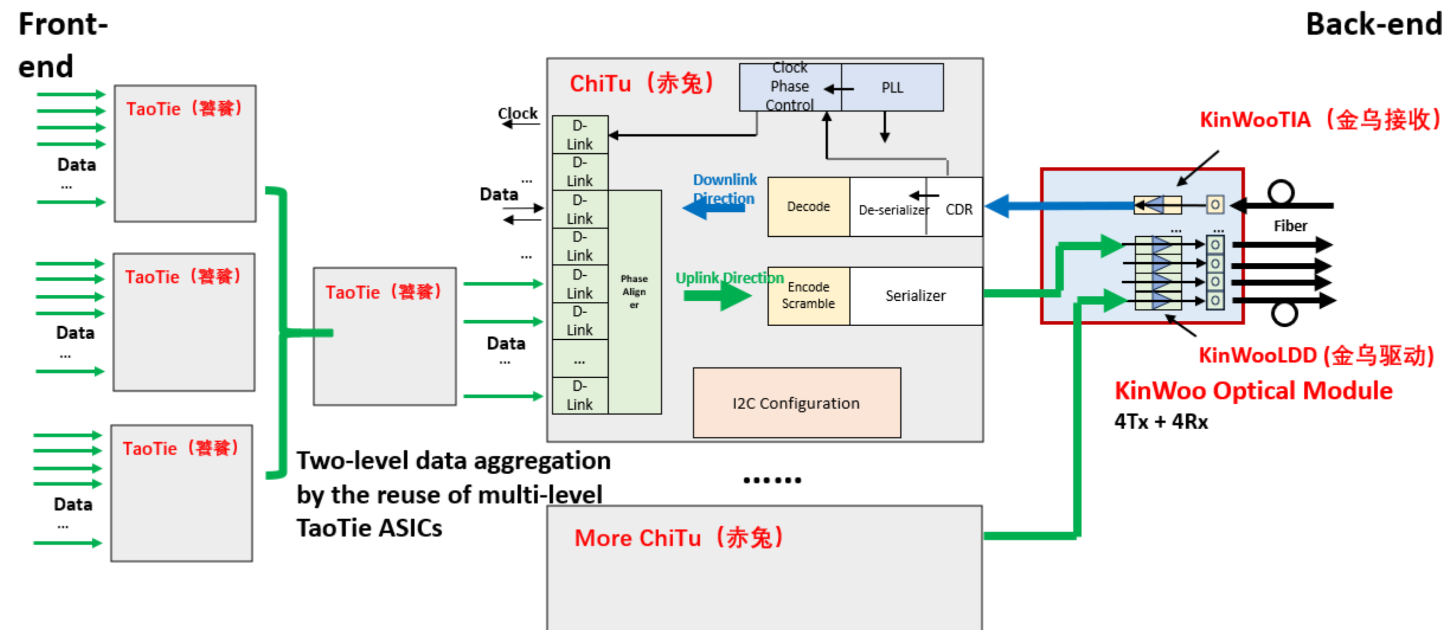


| Overall Electronics system | Elec TDR Draft1 2024.12 | | Ref-TDR release 2025.6 | | 1st Milestone 2027.12 | Towards final CEPC detectors | 2nd Milestone 2029.12 |
|---|---|---|---|---|---|---|---|
| Power & DC-DC (BaSha霸下) | 2024.11 GaN Selection | 2025.1 DC-DC Controller schematic design | 2025.4 1st tapeout | 2026.12 BaSha func module prototype | 2027.12 Module on detector test | 2028.12 Rad enhancement & Inductor design | 2029.12 Rad-tol & Mag proof BaSha prototype |
| Data Link (TaoTie饕餮、ChiTu赤兔 & KinWoo金乌) | 2024.10 Protocol define | 2025.1 Scheme define | 2025.4 1st tapeout Chip set | 2026.12 ChiTu & KinWoo func prototype | 2027.12 ChiTu & KinWoo on detector test | 2028.12 Rad enhancement & Taotie development | 2029.12 Rad-tol ChiTu DataLink prototype |
| VTX STCH (Taichu-Stitching 太初-补天) | 2024.12 Preliminary scheme for Stitching | 2025.1 Taichu-stitching-180 development → | 2025.12 1st design of wafer-level stitch onTJ180 → ; TJ65 design kit finalization → | 2026.12 TJ65 single chip design → | 2027.12 wafer-level stitching mechanical prototype → ; TJ65 single chip prototype → | | 2029.12 TJ65 wafer-level Stitching detector prototype |
| PIX TPC | | | 2025.6 Prototype beamtest | 2026.12 Chip optim for optimized TPC | 2027.12 Optimized Prototype beamtest | | 2029.12 Chip Finalization |
| OTK AC-LGAD (JuLoong烛龙) | 2024.12 FPMROC chip test (for FASTPMT) → ; Preliminary scheme → | 2025.4 1st tapeout → | 2025.12 FPMROC prototype test (for FASTPMT) → ; OTK detector optimization → | 2026.6 ASIC-128chn tapeout → | 2027.10 AC-LGAD detector co-test → | | 2029.12 Chip Finalization & detector co-test |
| ECAL/HCAL/Muon SiPM ASIC (ChoMin重明) | | 2025.1 Spec finalization & device selection | 2025.4 1st tapeout ; 2025.12 1st SiPM ASIC test (N / Y) | 2026.12 N: Existing chip based modification → ; Y: SiPM ASIC optimization → | 2027.12 HCAL module prototype | | 2027.12 Chip Finalization |

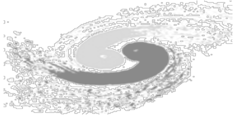
# Current status of the Data Link chip set

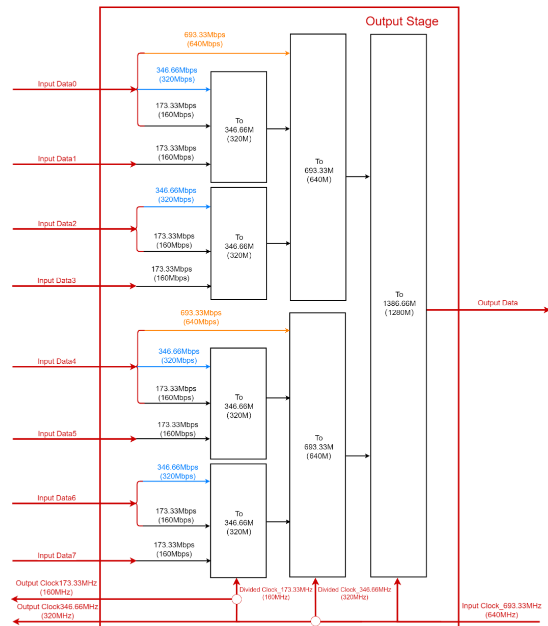


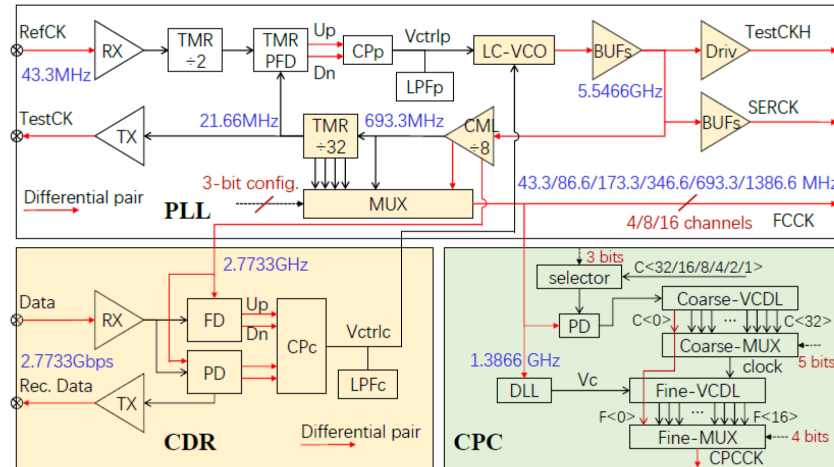
- Aiming to have the 1st tapeout in April, a full chip set
  - Main target: a full functional ChiTu chip, the kernel chip of the data link system
  - Secondary target: a full (but minimum) chip set that can form a data transmission system
  - May delay to July due to the complexity
- The major three parts: TaoTie@Aggregation, ChiTu@Data Link, KinWoo@optical module, all have detailed schemes, interface, block division, and task allocation



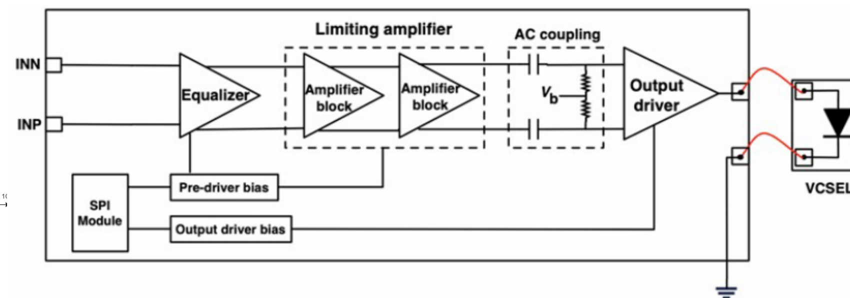
# Current status of the Data Link chip set



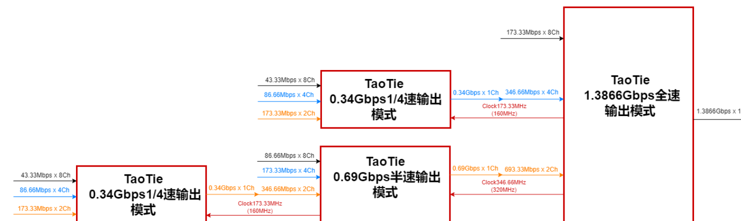



ChiTu clock system



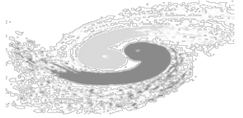

KinWoo VCSEL Driver

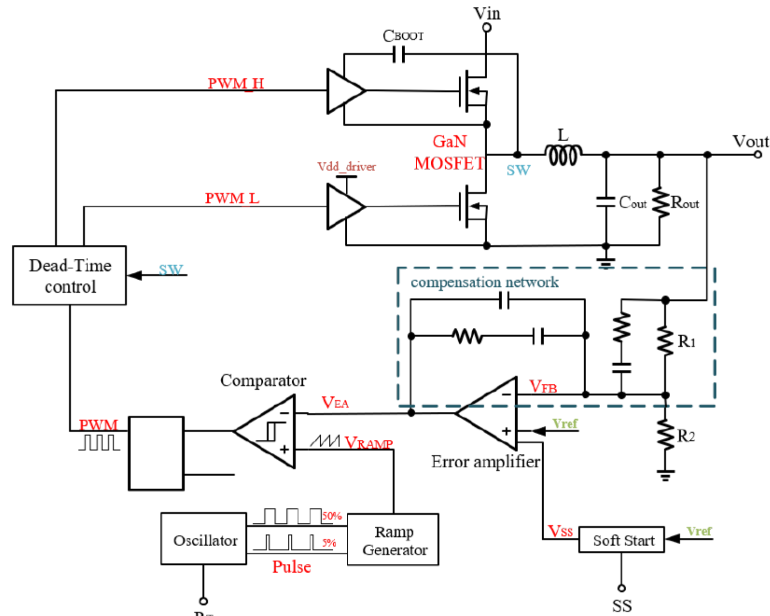



TaoTie

- **Main schemes established (details skipped)**
- **Most new design proceeded to the code level with block simulation**
  - **To do co-simulation**
- **Design Team (not FTE)**
  - **IHEP:3 staffs +3 students**
  - **CCNU:2+8**
  - **NWPU:2+2**
  - **USTC:1+2**
  - **WTU:2+2**
  - **IPAS:1+1**
  - **HPU:1+2**

# Current status of the Basha Power module






DC-DC controller scheme (ready)

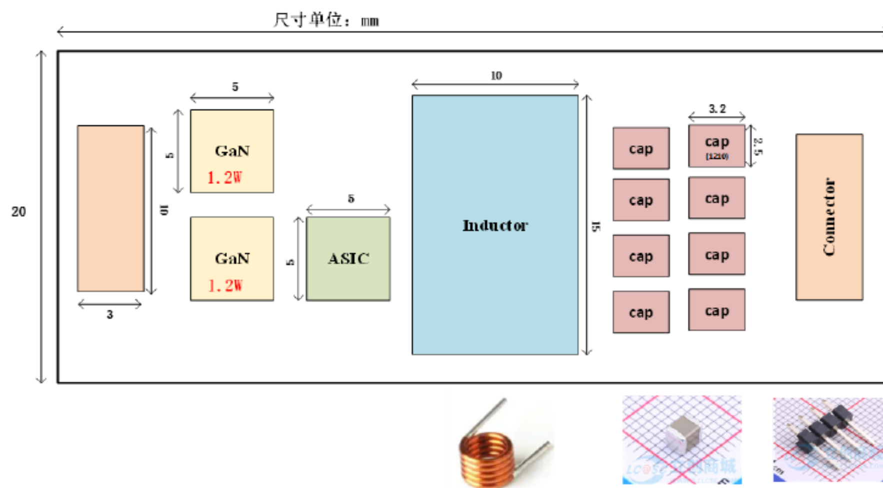
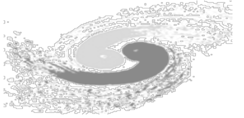
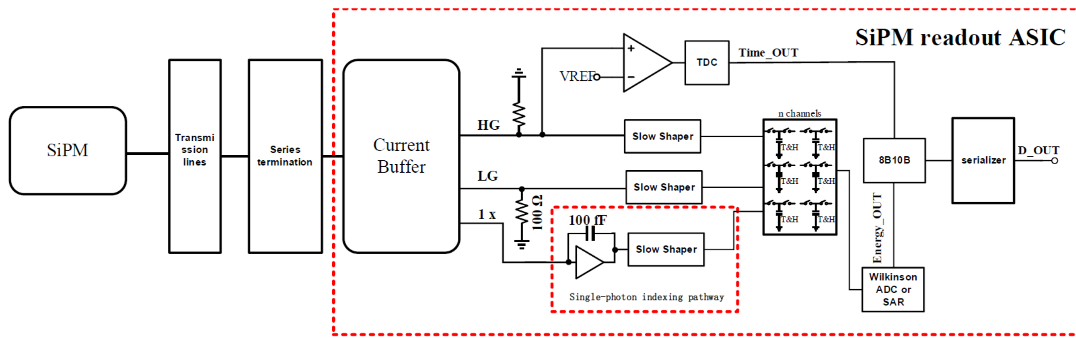


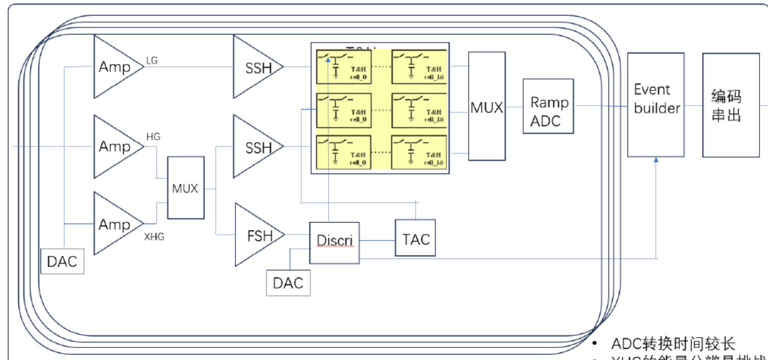

Figure 11.61: Floor plan of Basha DC-DC module

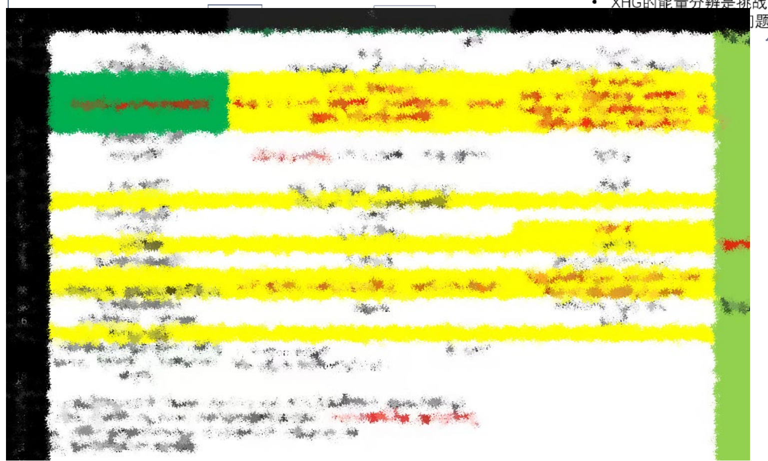
- **Chip design:**
  - The kernel GaN transistor selected by rad-test
  - DC-DC controller 1st tapeout in April
  - Schematic design accomplished, to be co-sim and layout
- **Module design**
  - Scheme defined to be 48V→12V， 12V→LV
  - Experienced design team from Univ. & Industry contacted and will be involved very soon
- **Air Core Inductor study**
  - Main constraint for the module size
  - Try to investigate with industrial help
- **Commercial DC-DC & LDO**
  - By TID test, some COTS power device found that can even survive at CEPC level
  - Can be backup devices at early stage for prototypes
- **Design team**
  - IHEP: 3
  - NWPU: 1+2
  - USTC: 1+1
  - TECHORILUX: 2

# Current status of the ChoMin ASIC for SiPM





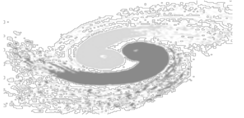



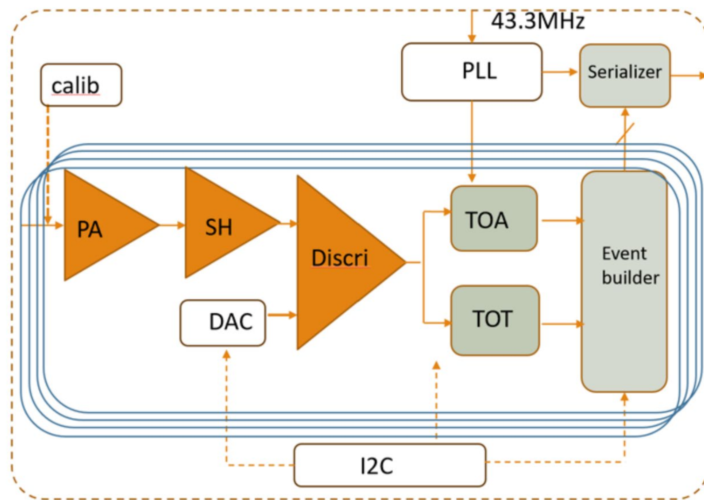



(pre-defined) spec list of ChoMin

- The recent discussion focus in electronics system
- Several possible schemes prepared for major cases (normal rate, high bkgrd, dispersion signals)
  - Many characteristics still unclear up to now
- Will try to summarize a spec list with co-agreement with CAL/MUON very soon
  - Parameters with reasonable prospective optimization, e.g. Cd@pF
- 1st single chn MPW in April
  - Very tight schedule left
- Design team
  - IHEP: 3+3
  - CCNU: 1+3
  - NWPU: 1+1

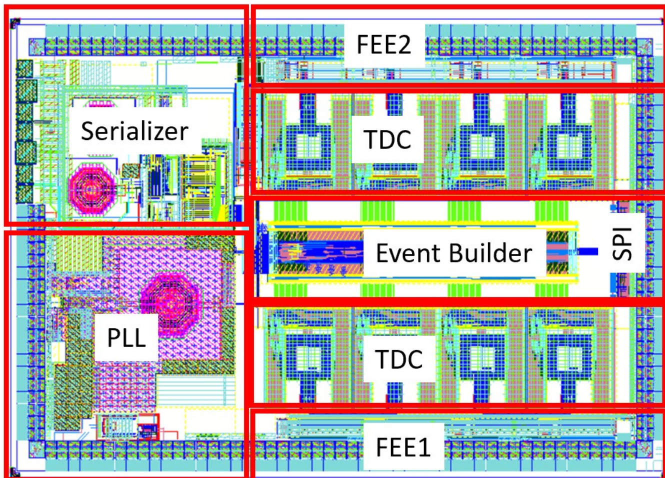
# Current status of the JuLoong ASIC for OTK

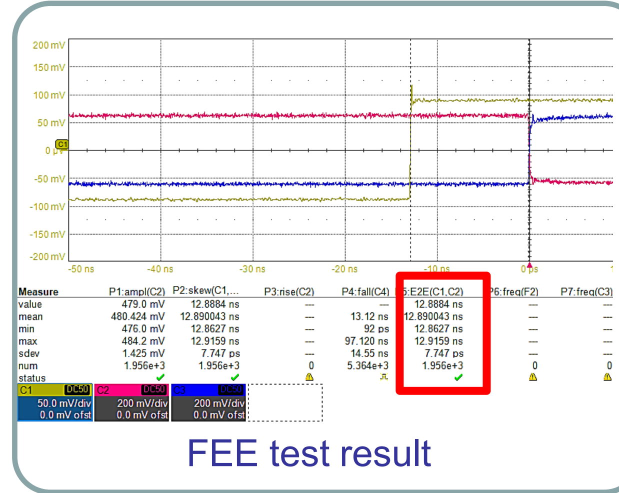




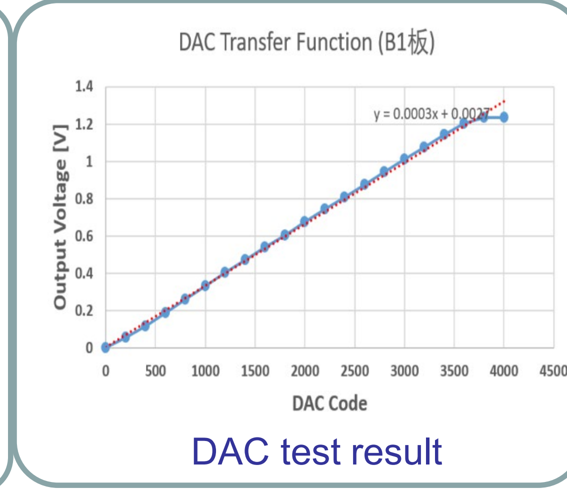

JuLoong diagram

- **JuLoong scheme proposed according to current OTK design (for Ref-TDR)**
  - **Waiting for the new LGAD prototype for further optim.**
  - **1st tapeout expected in April**
- **For the co-test at early stage, FPMROC (for TOF-PET) has been tapeout and tested with 10ps spec**
  - **Key analog blocks with similar scheme as JuLoong, power will be optimized for 30ps spec**
  - **TDC scheme will be replaced by a low-power version**



FEE test result

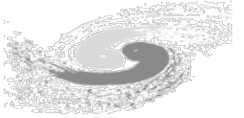


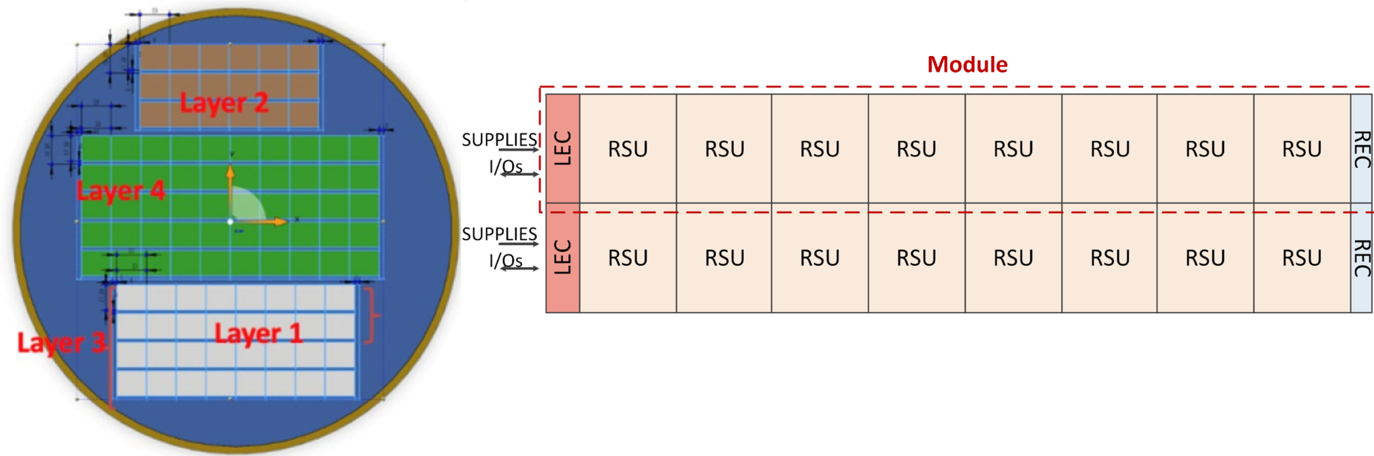

DAC test result

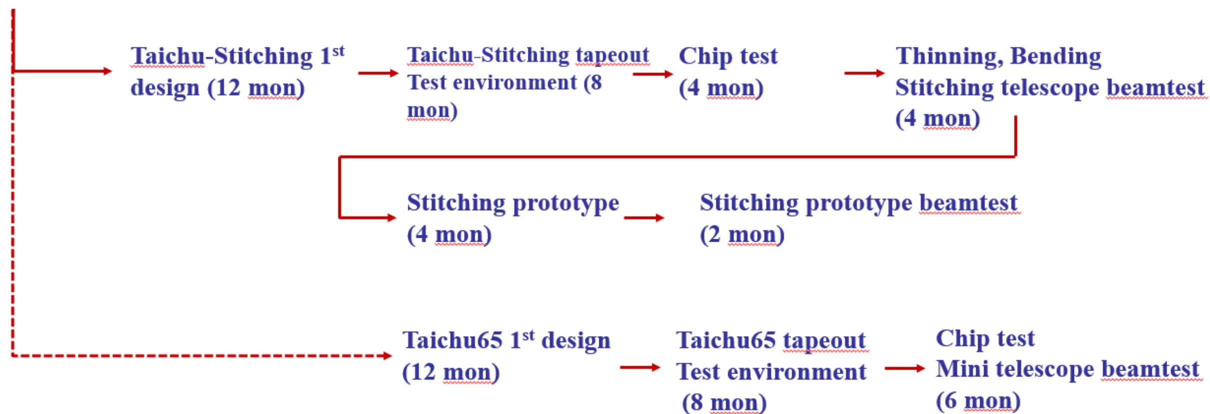
FPMROC 1st tapeout

- **Design team**
  - **IHEP: 3+2**
  - **CCNU: 2+3**
  - **WTU: 1+1**
  - **HPU: 1**

# Current status of the Taichu-Stitching Design for VTX

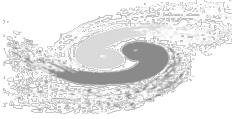





- Although Taichu exists, very high challenges remain for a stitching VTX, almost a new ASIC
- Final scheme will be separately verified due to high cost, risk and political issues
- Main target:
  - A stitching prototype, fully functional, most spec of CEPC achieved, to verify the main scheme of CEPC VTX
  - Will based on TJ180-STH & Taichu matrix
- Secondary target
  - Verify most other specs of CEPC, only without stitching
  - Will based on TJ65, waiting for the availability of technology
- Design team
  - IHEP: 5+4
  - NWPU: 2+3
  - SDU: 1+1
  - CCNU: 1
  - NCU: 1

# Naming of the common ASICs



ChiTu & the God of War Guan Yu

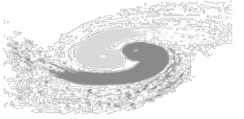
KinWoo in the sun

TaoTie

BaSha carrying a monument

- **ChiTu (赤兔) @ Data Link:**
  - the most famous horse in Chinese tales, ridden by the Chinese God of War Guan Yu. It is in charge of transportation with ultra fast speed, just as Data Link chip is doing.
- **KinWoo (金乌) @ Optical module:**
  - the bird who lives in the sun in Chinese tales, an avatar of the sun and in charge of the light, just as the optical module does, to convert electronic signal to/from optical.
- **TaoTie (饕餮) @ Data aggregation:**
  - a mythical animal in Chinese tales, who can swallow anything, just as the chip does, to collect all the input data streams.
- **BaSha (霸下) @ Power module :**
  - one of the nine sons of the Chinese Loong, who is famous for its strongness and always to bear a monument. Just like the powering system which is the basement and support of all electronics.

# Naming of the new FEE ASICs



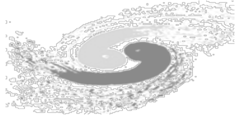
Nuwa Mends the Sky (Taichu-Stitching)

JuLoong in Classic of Mountains and Seas

A statue of the bird of ChoMin

- **Taichu-Stitching(太初-补天) @ VTX:**
  - One of the most events happened in the very beginning of the ancient world (Taichu's Period 太初时期) is "Nuwa Mends the Sky（女娲补天）", well known in Chinese story. The action mending equals to stitching, both make a surface seamless.
- **JuLoong(烛龙) @ OTK:**
  - A divine beast in Chinese mythology that governs time. As the front-end ASIC of the OTK detector, its primary design goal is to achieve the highest time resolution performance of the entire detector, corresponding to the function governed by JuLoong
- **ChoMin (重明) @ SiPM for ECAL/HCAL/Muon:**
  - An ancient Chinese legend tells of a mythical bird called "Double Vision" with two eyeballs in each eye. This bird will serve as a versatile ASIC in ECAL, HCAL, and Muon detectors, symbolizing the concept of ChoMin, which is to detect signals from multiple detectors. The main design challenge is to accommodate the wide dynamic range of ECAL, so the chip will feature dual-range amplification in the front-end, aligning with the idea of multiple visions.

# Summary for the new chip status



- Schemes almost defined
- 1st tapeout in April for most of chips, 4 MPWs
  - Depend on complexity (and paper work), some may postponed to July
- A wide collaboration established with major affiliations in the field
- ~20 FTE involved (not precise)
  - Still far from enough (compared with CERN experience), real work can be started at least
  - Many common blocks design in multiple chips, with shared manpower
    - A similar “Matrix management” is running
    - Redundant head counting in the former chip design team, which is the real case
- Targeting milestones in a word (from now on)
  - 3 years with functional prototypes and co-test, ready for the acceptance review
  - 5 years with (almost) design finalization of chips, ready for pre-production

Thank you!