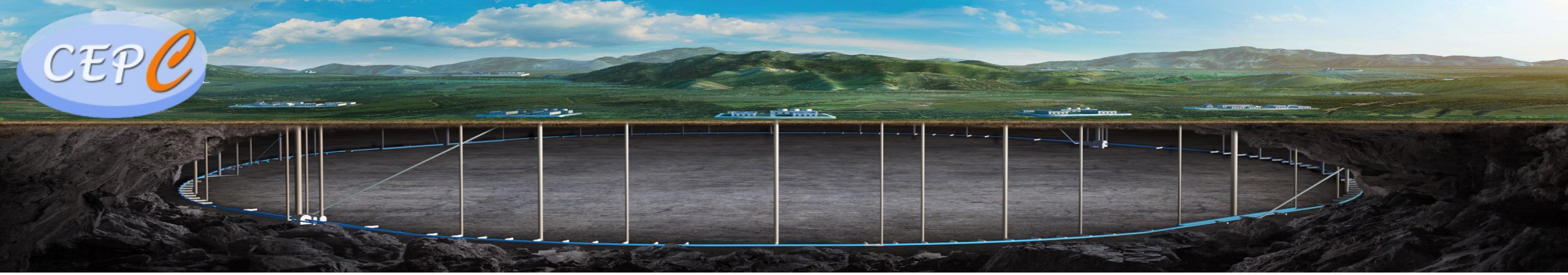

CEPC vertex Detector

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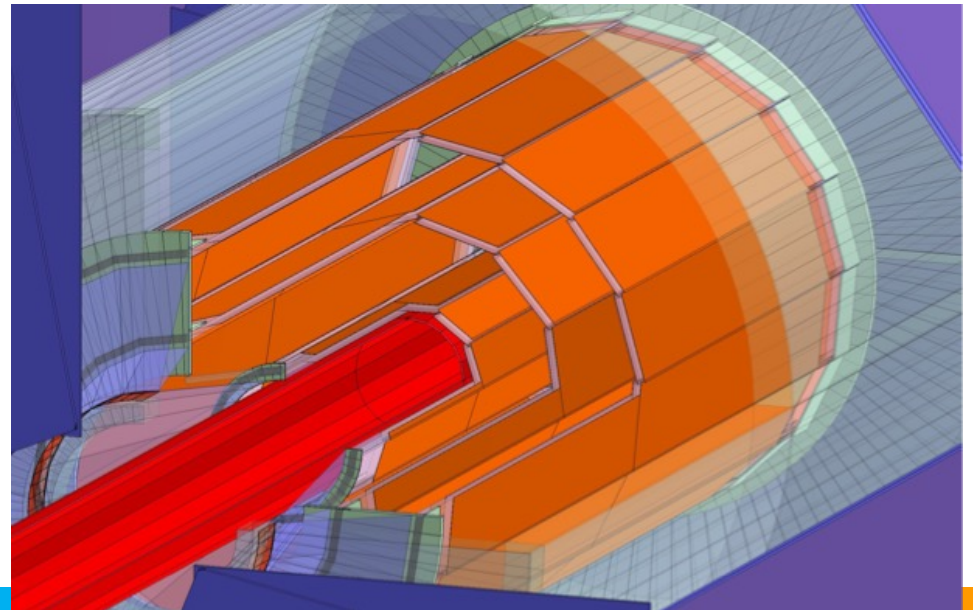
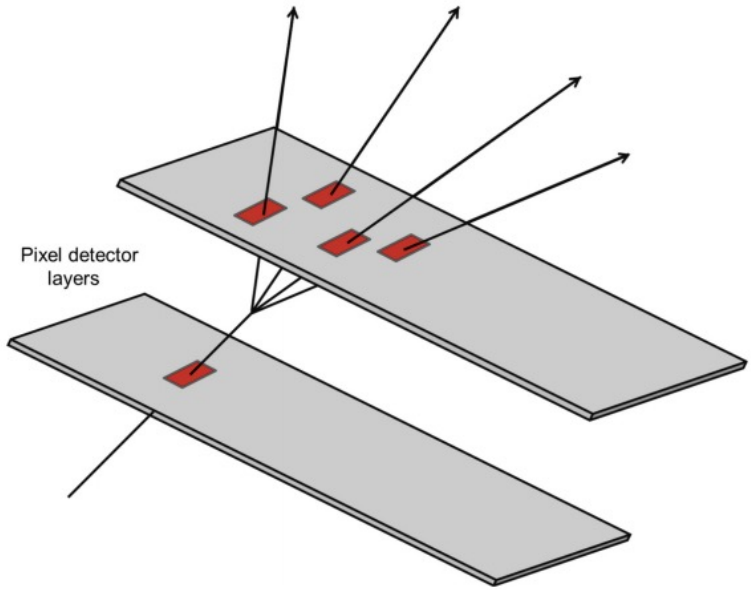
Content

- Introduction
- Requirements
- Technology survey and our choices
- Technical challenges
- R&D efforts and results
- Detailed design including electronics, cooling and mechanics
- Readout electronics & BEC
- Performance from simulation
- Research team and working plan
- Summary

Introduction: vertex detector

- Vertex detector optimized for first 10 year of operation (ZH, low lumi-Z)
- This talk relates to the Ref-TDR Ch04.
- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for H → cc and H → gg physics, which is an important goal for CEPC





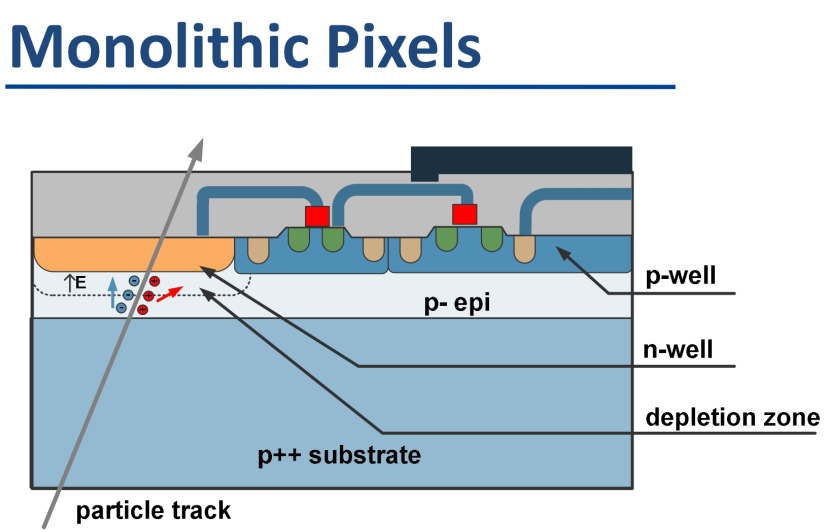
Vertex Requirement

- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)
- High data rate: (especially at Z pole , ~43MHz, 1Gbps per chip)
  - **Challenges**: 1Gbps per chip high data rate especially at Z pole
- Low material budget (less than 0.15%X0 per layer)
- Detector Cooling with air cooling (power consumption<=40 mW/cm^2)
- Spatial Resolution (3-5 um)
- Radiation level (~1Mrad per year in average)

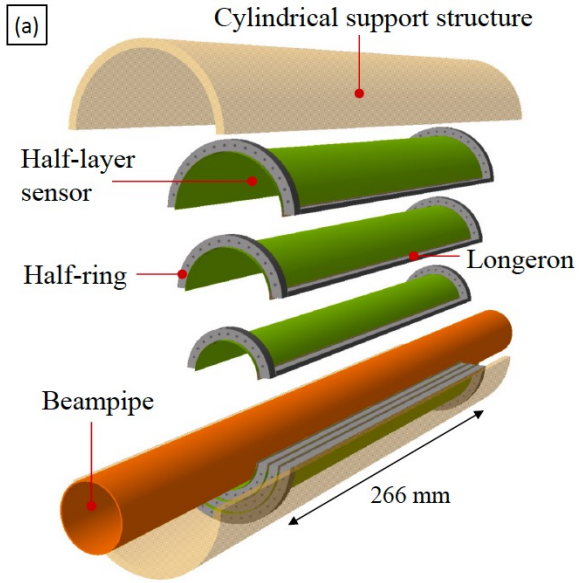
Technology survey and our choices

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

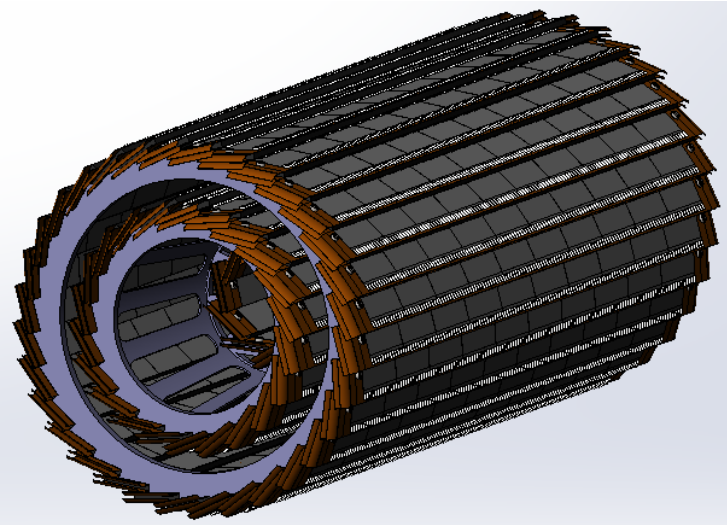
Monolithic active Pixel CMOS (MAPS)



Baseline: curved MAPS



Alternative: ladder based MAPS



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Progress after 2024 IDRC Review: background

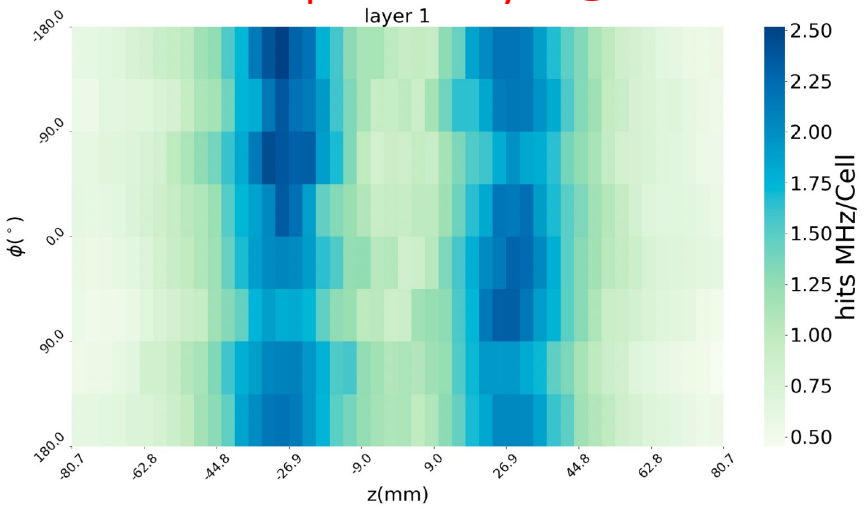
- Background rate are simulated and digitated with updated digitation model
  - Pair production and SR photons are dominated backgrounds

Background rate for Higgs and low-lumi Z runs

Table 4.7: Summary of background estimation. Current detector scheme cannot completely handle high-lumi Z mode, so the result of high-lumi Z will not be shown here. For the results of high-lumi Z, based on accelerator parameters, a rough estimation can be made by simply multiplying the existing low-lumi Z results by a factor of 3. Synchrotron radiation is included.

Layer	Ave. Hit Rate MHz/cm^2	Max. Hit Rate MHz/cm^2	Ave. Hit Rate×C MHz/cm^2	Max. Hit Rate×C MHz/cm^2	Ave. Data Rate Mbps/cm^2	Max. Data Rate Mbps/cm^2
Higgs: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 346ns, 53 %Gap, 25× 25 μm^2/ pixel)						
1	2.234	2.509	8.053	10.737	257.710	343.599
2	0.653	1.082	2.318	3.922	74.161	125.511
3	0.175	0.363	0.673	1.382	21.532	44.217
4	0.084	0.163	0.349	0.951	11.163	30.428
5	0.021	0.095	0.117	0.788	3.737	25.212
6	0.016	0.064	0.082	0.434	2.631	13.882
Z mode: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 69ns, 9 %Gap, 25× 25 μm^2/ pixel)						
1	8.817	17.101	44.052	100.165	1409.672	3205.273
2	0.871	1.392	3.870	8.765	123.845	280.475
3	0.328	0.841	1.568	4.755	50.185	152.163
4	0.199	0.480	0.966	3.657	30.923	117.024
5	0.030	0.063	0.207	0.552	6.630	17.662
6	0.024	0.049	0.151	0.344	4.833	10.993

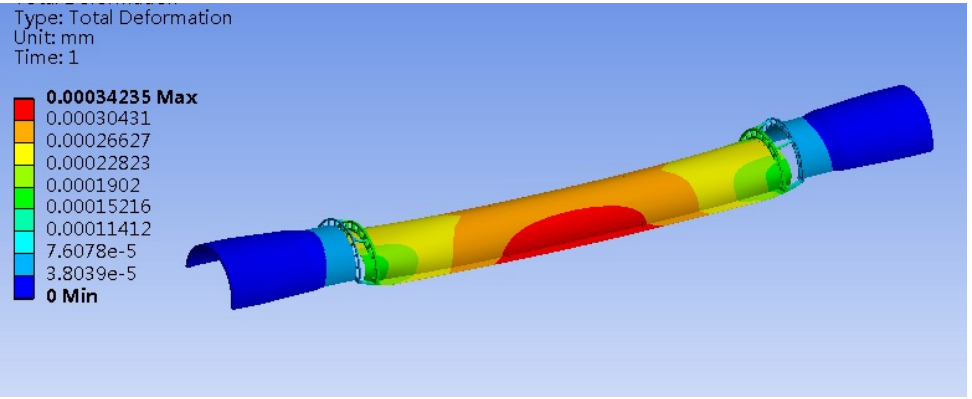
Hit rate map for 1st layer @ low-lumi Z run

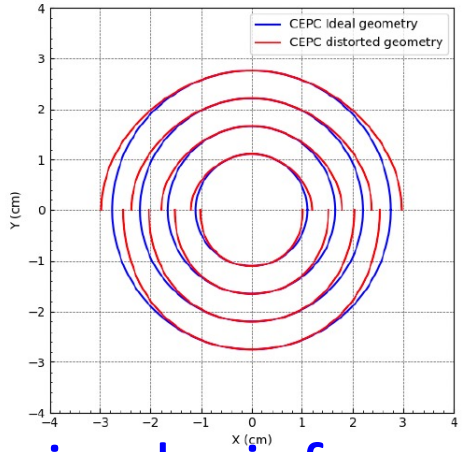


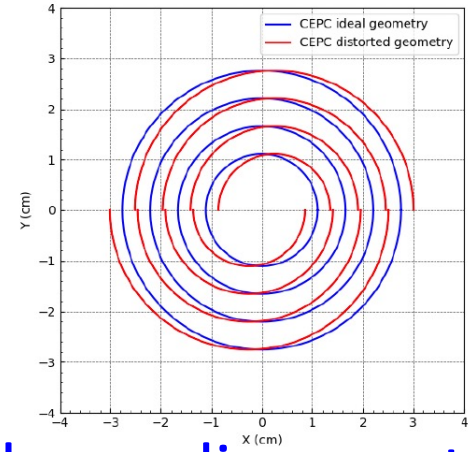
- This study is to address the IDRC comment:
  - Thorough analysis and simulation of the background are essential, as they directly influence key aspects of detector design and operation, such as data rates and power consumption.

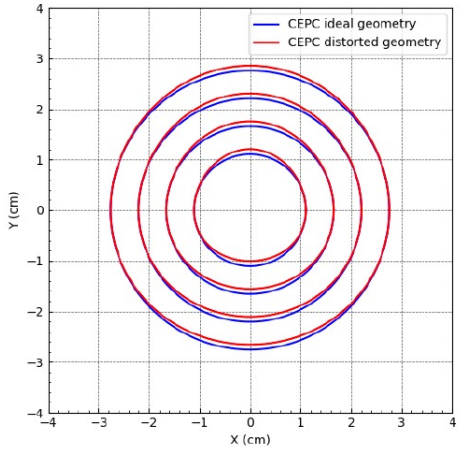
Progress after 2024 IDRC Review: Alignment for vertex detector

- Deformation mode study simulated by FEA.
- Analytic function for deformation are studied



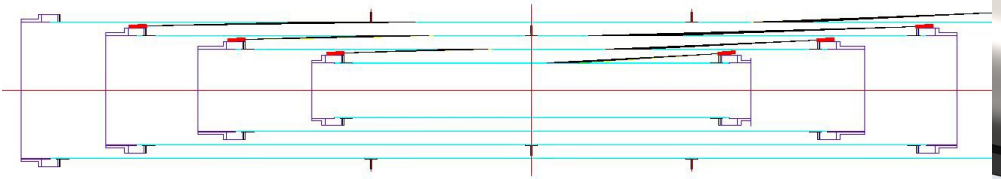


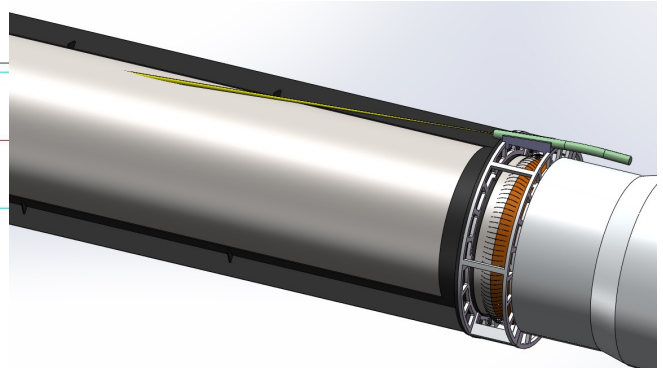




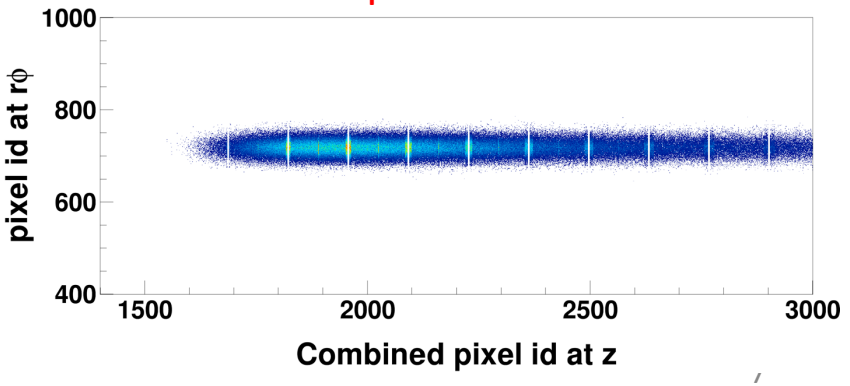
- Real time Deformation monitoring by infra-red laser alignment system

2D and 3D model on laser alignment system on vertex detector





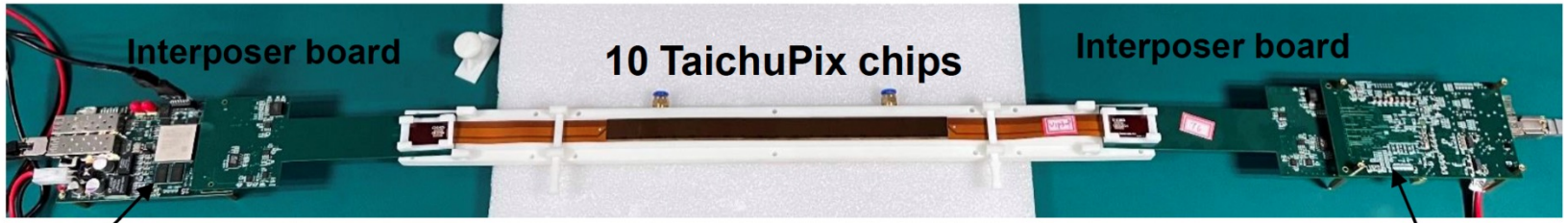
laser beamspot on bent-MAPS



R&D status and final goal

Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 μm	3-5 μm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm
Stitching	11×11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

R&D effort: vertex detector prototype

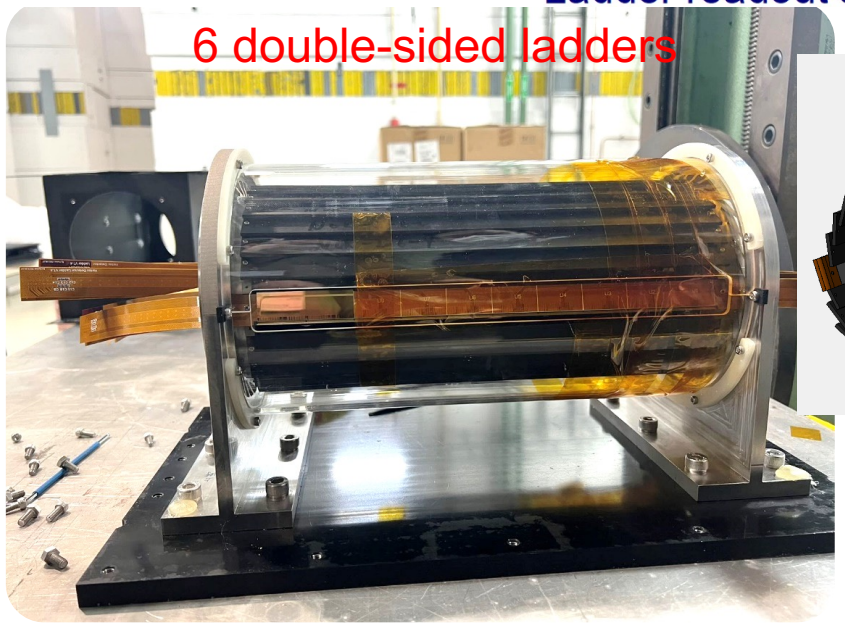


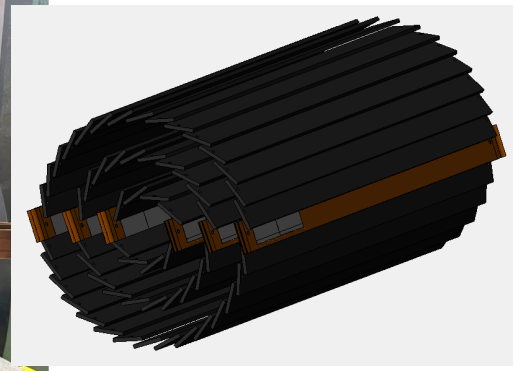
TaichuPix-based prototype detector tested at DESY in April 2023

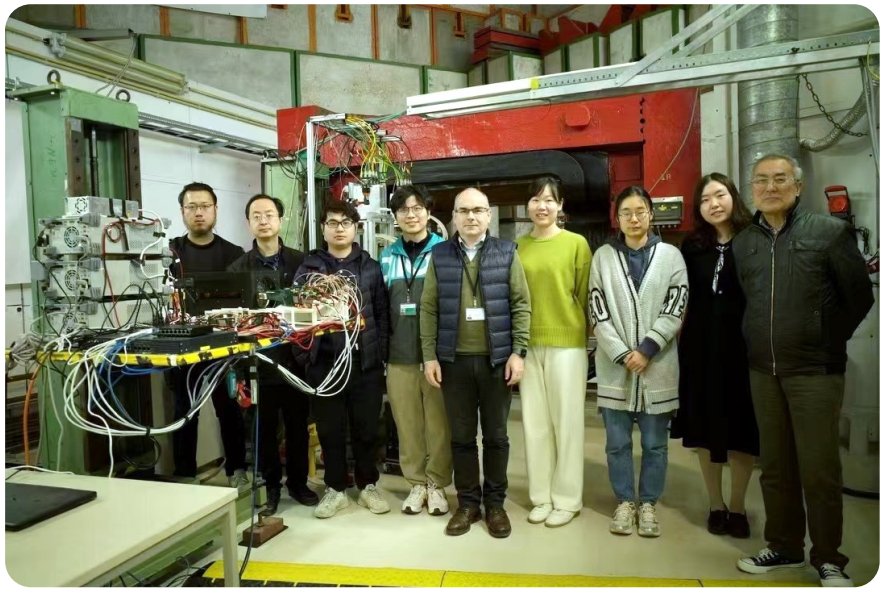
Spatial resolution ~ **4.9 μm**

Ladder readout system

6 double-sided ladders



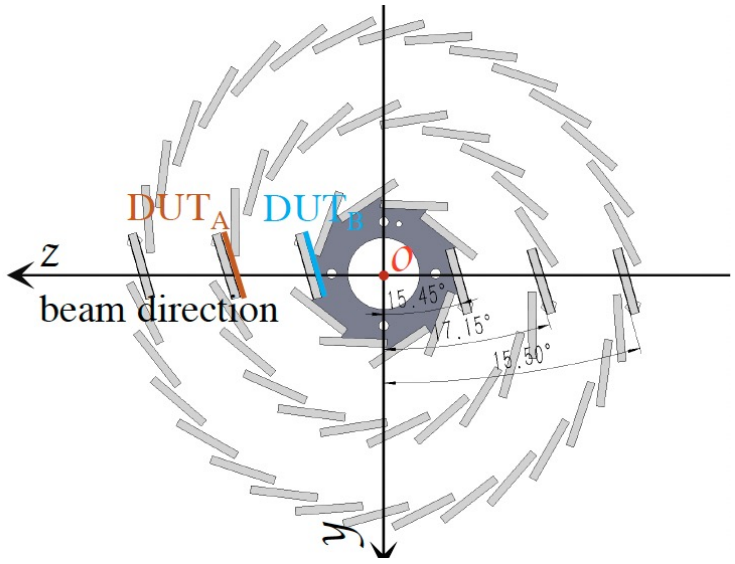


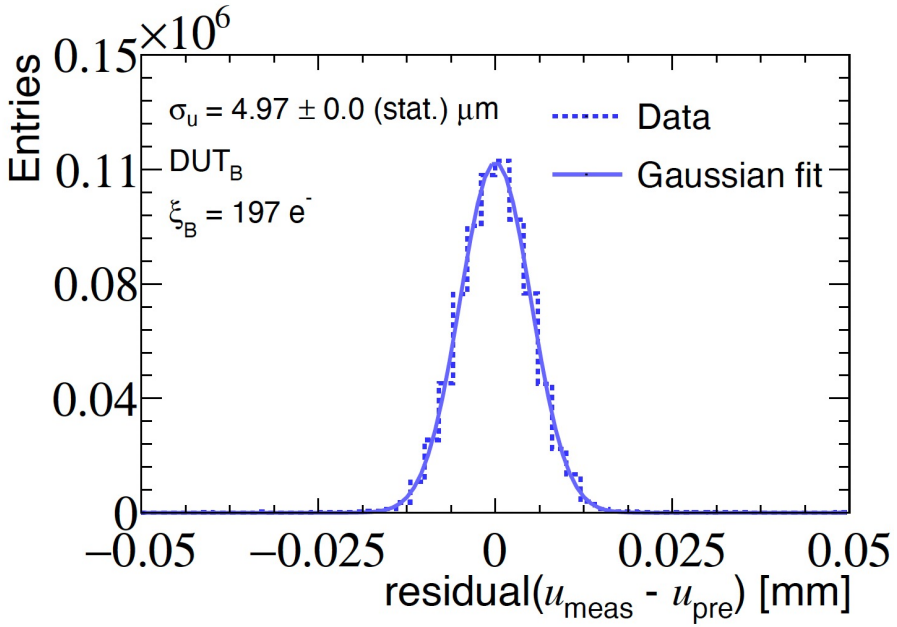


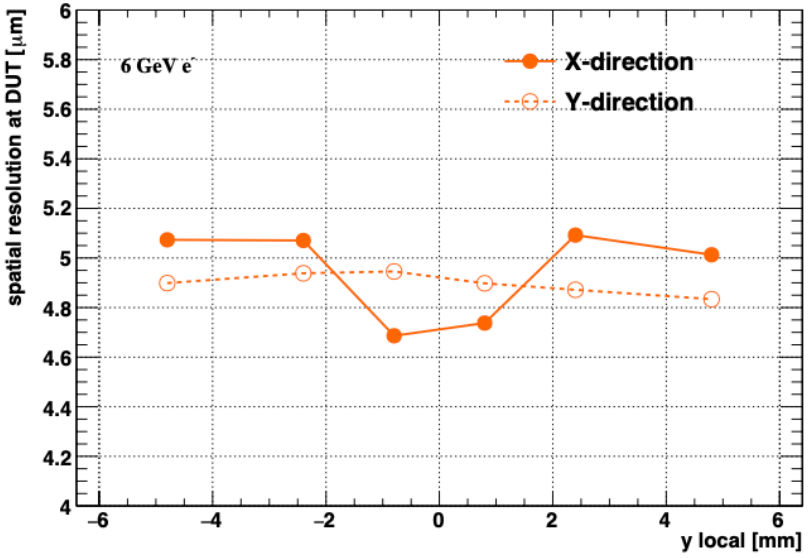
	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts and results: vertex detector prototype beam test

Spatial resolution ~ **5 μm**



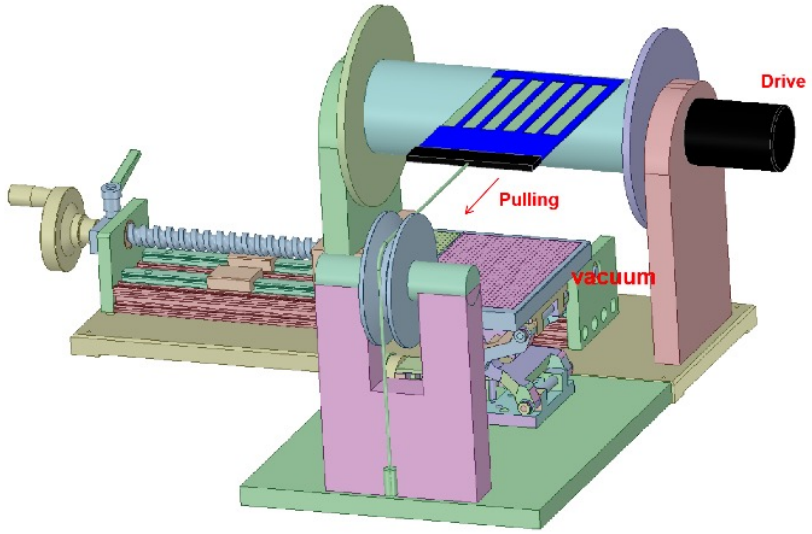


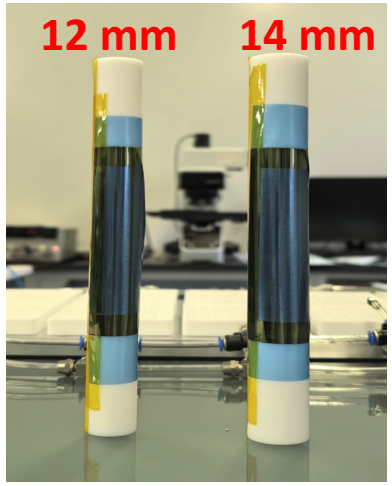


	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm
  - The dummy wafer has been thinned to 40μm





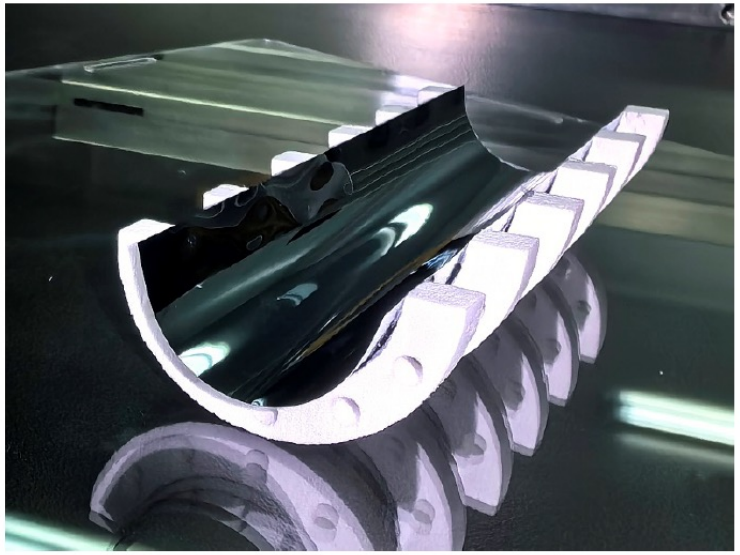
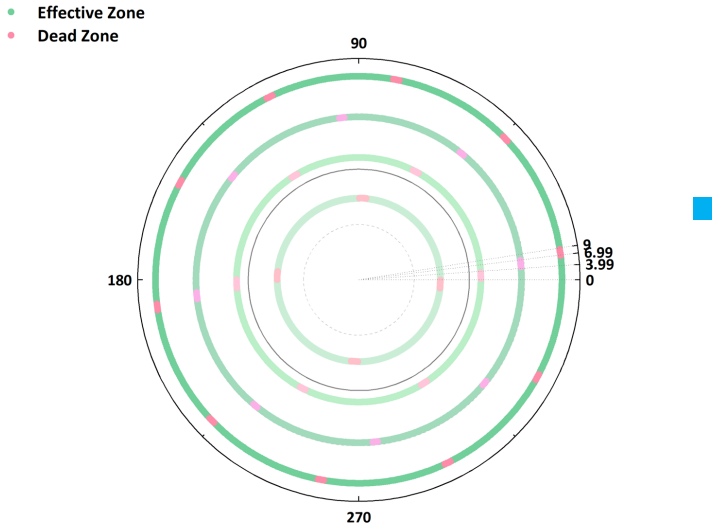


Figure 4.25: 12 mm bending radius.

	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

baseline: bent MAPS

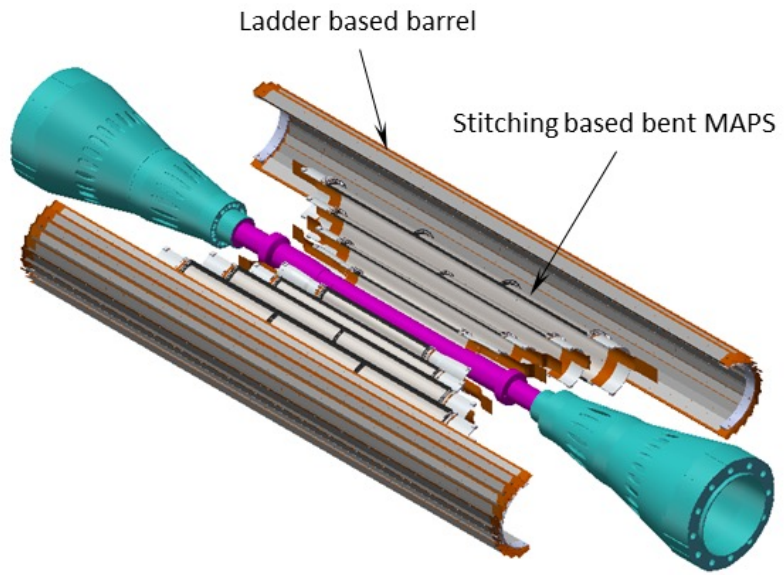
- 4 single layer of bent MAPS + 1 double layer ladder
  - Material budget is much lower than alternative option
- Use single bent MAPS for Inner layer (~0.15m^2)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area

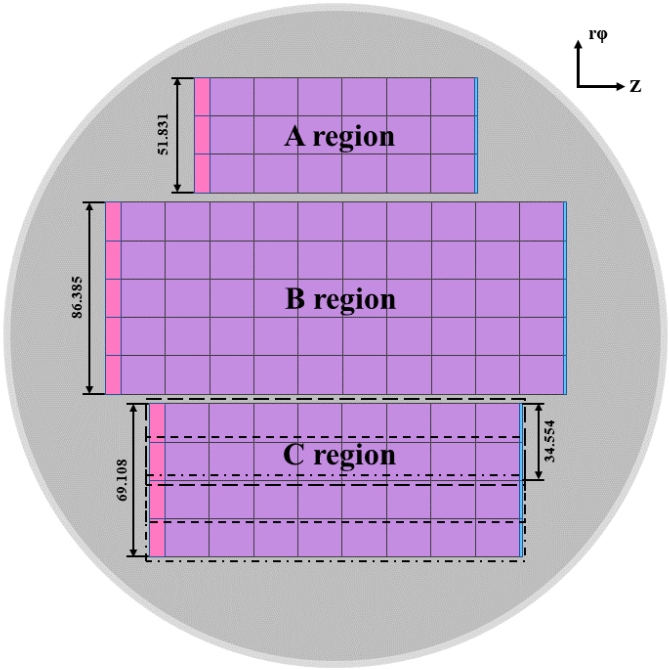


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

Long barrel layout (no endcap disk)
to cover cos θ<=0.991

layer	Radius	Material
Layer 1	11mm	0.06% X0
Layer 2	16.5mm	0.06% X0
Layer 3	22mm	0.06% X0
Layer 4	27.5mm	0.06% X0
Layer 5/6 (Ladders)	35-40 mm	0.33% X0
Total		0.57% X0





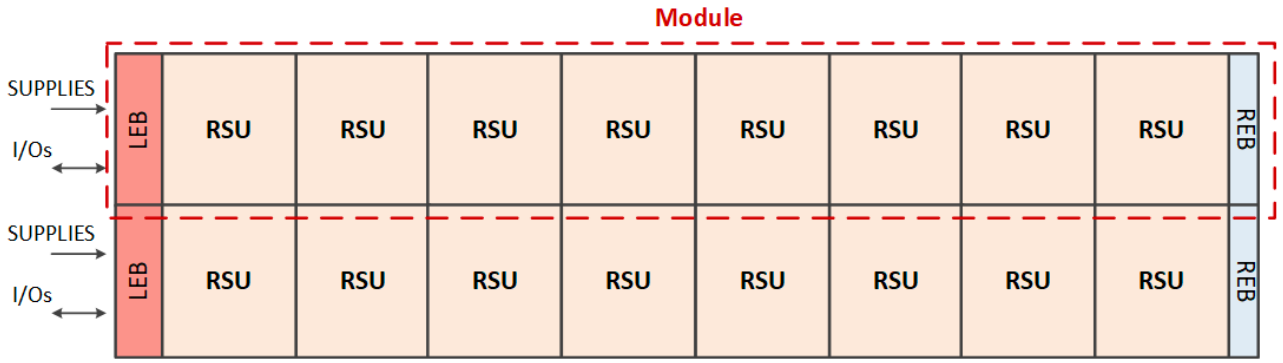
Ladder Electronics

– Baseline: stitching on wafer to replace PCB

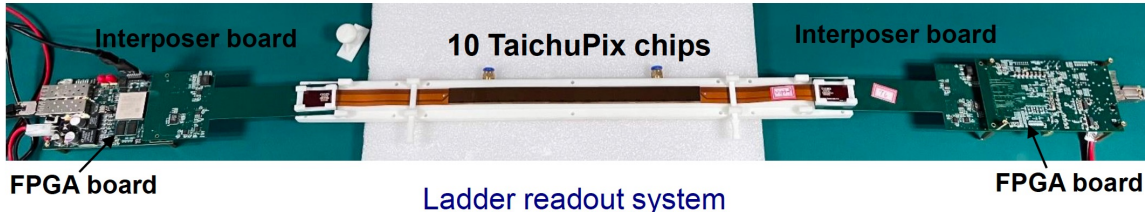
– Alternative: flexible PCB

- Signal, clock, control, power, ground will be handled by control board through flexible PCB

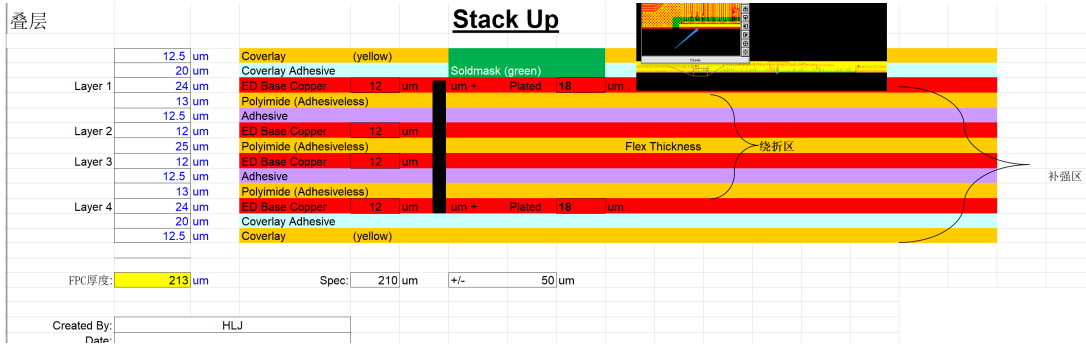
Baseline: ALICE ITS3 like stitching



Alternative: flexible PCB



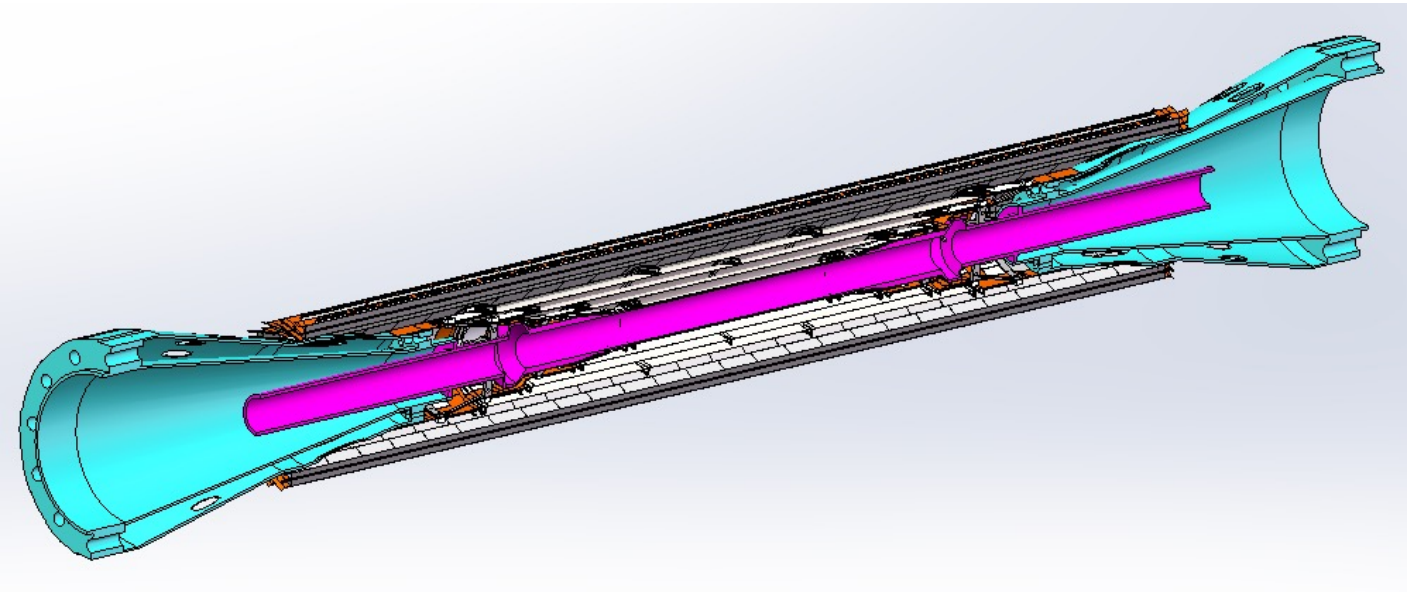
Ladder readout system

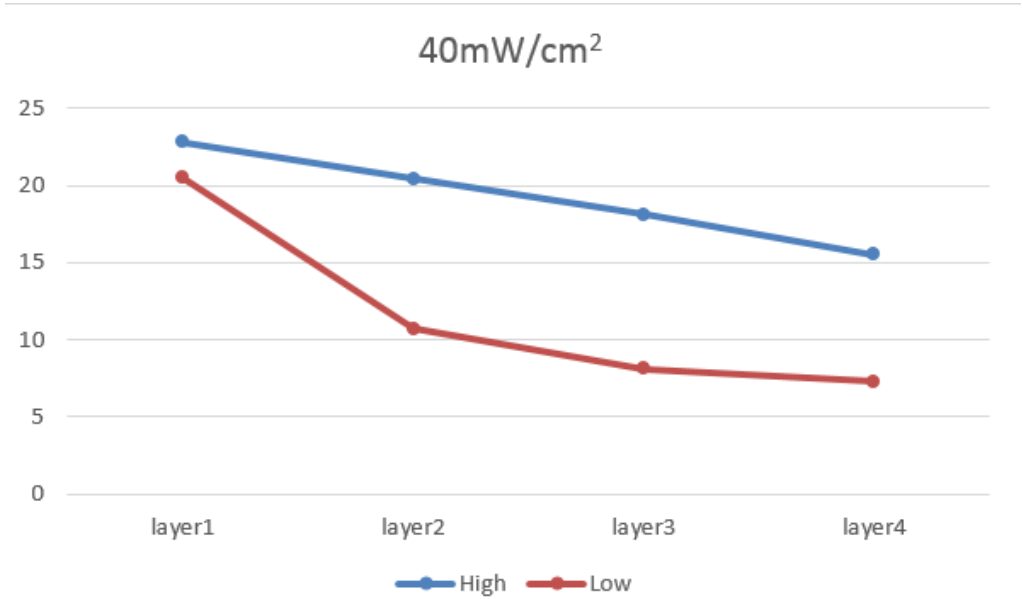


[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Mechanics and cooling

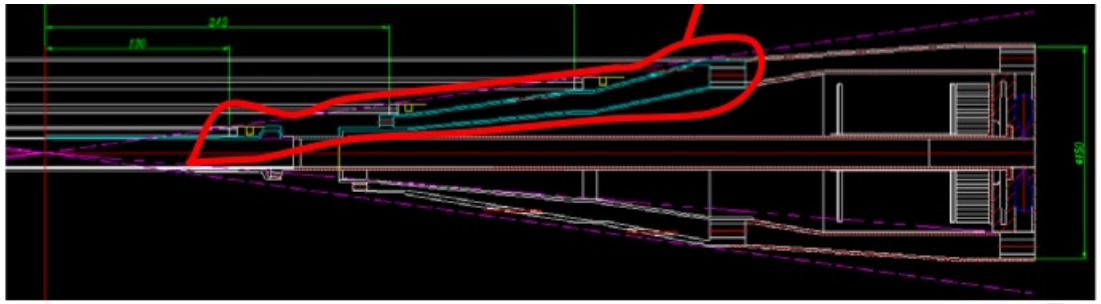
- Power consumption
  - 65nm technology， Power consumption at low lumi Z can reduced to ~40mW/cm^2
- Air cooling feasibility study
  - Baseline layout can be cooled down below ~25 ℃
    - Based on 2.5 m/s air speed, estimated by thermal simulation





Vertex technologies: Cables and services

- Limited space in the MDI region for cables and services
  - Utilizes DC-DC powering; MAPS silicon substrate requires a common negative bias
  - Signal are transmitted through a flexible PCB and then converted to optical fiber.

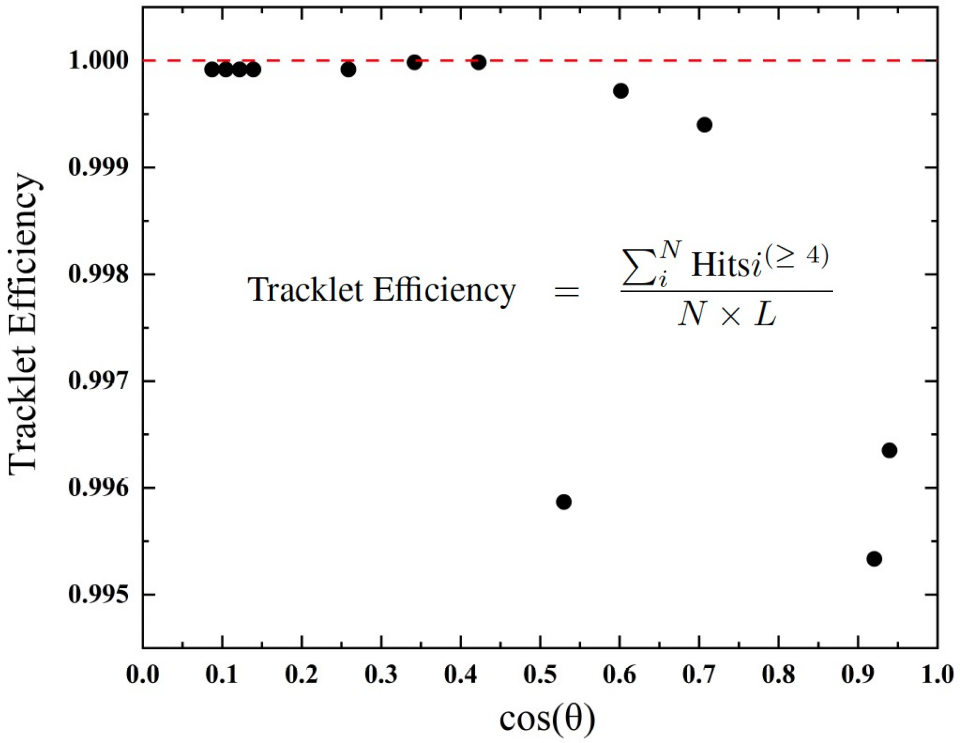


Cables routing using 3D printed model

Performance from simulation: Impact parameter resolution

- Baseline (Stitching) Compared to alternative (ladder) option
  - baseline (stitching) has significant improvement (25-40%) in low momentum case

Tracklet efficiency >99.5%



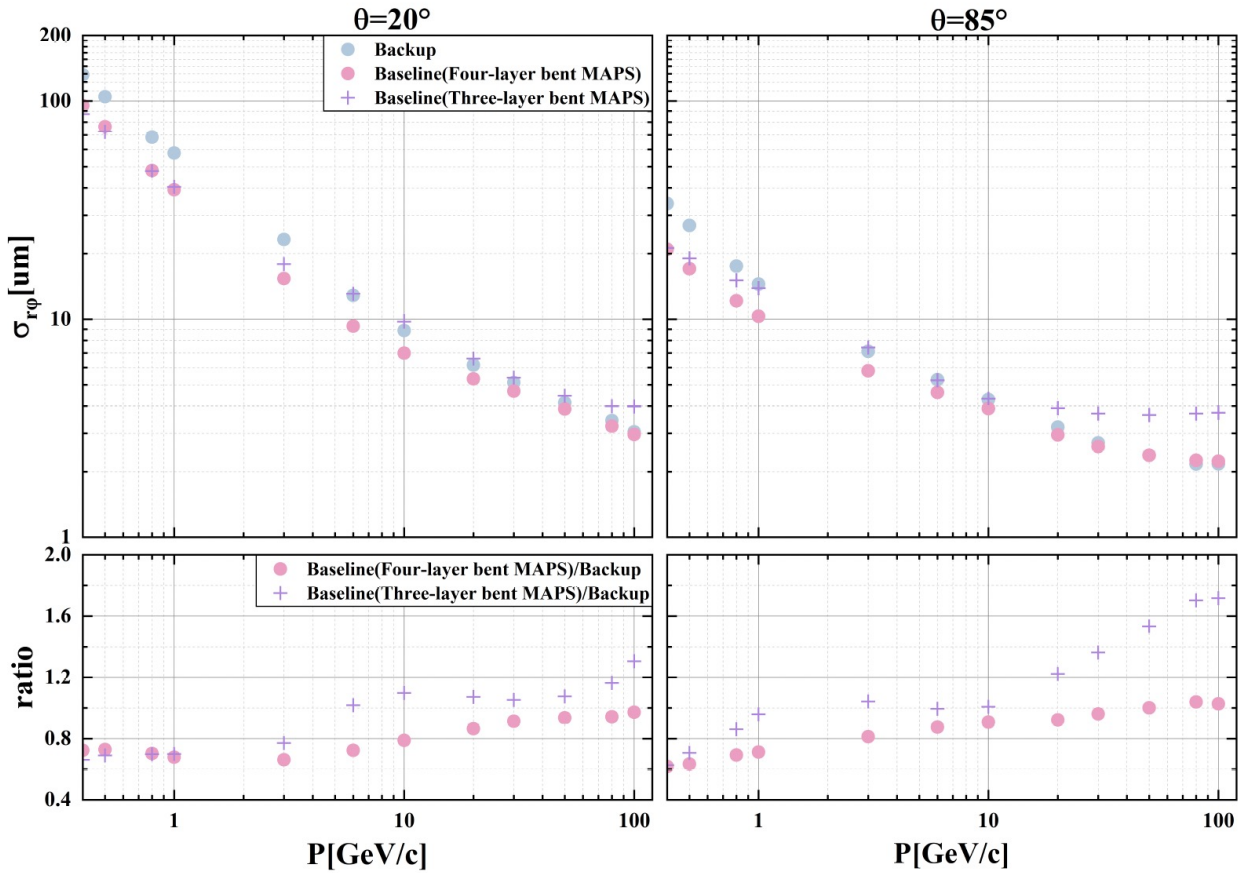


Figure 4.45: The resolution of the impact parameter d_0 in the three schemes varies with the change in the momentum of the outgoing particles.

Research team

- IHEP: Joao Costa, et al, 15 faculty, 5 postdoc, 6 students
  - CEPC vertex prototype, X-ray camera, ATLAS ITK strip and HGTD upgrade
- IPHC/CNRS: Christine Hu et al (3 faculty)
  - CEPC Jadepix design, ALICE ITS3 upgrade (especially on MAPS design, stitching)
- IFAE: Chip design , Sebastian Grinstein et al (2 faculty)
  - CEPC Taichupix chip design, ATLAS ITK pixel and HGTD upgrade
- ShanDong U.: Stitching chip design (3 faculty, 1 postdoc, 3 students)
- CCNU: chip design, ladder assembly (3 faculty, 1 postdoc, 5 students)
- Northwestern Polytechnical U. : Chip design (5 faculty, 2 postdoc, 5 students)
- Nanchang U. : chip design, (1 faculty, 1 students)
- Nanjing: irradiation study, chip design : (2 faculty, 4 students)
- Total : 36 faculty, 9 postdoc, 26 students

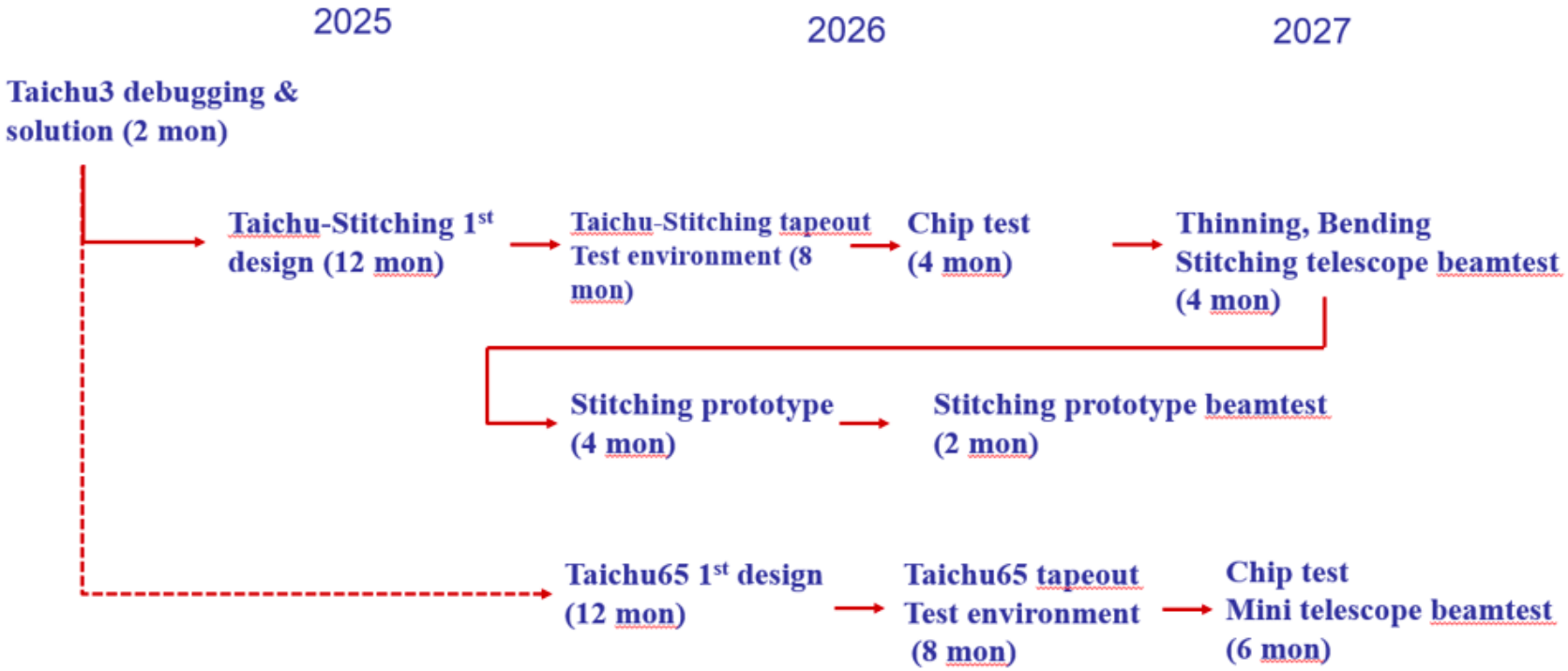
Summary: working plan

- CEPC vertex detector timeline is about 3-4 years after AlICE ITS3 upgrade
  - It will benefit from experience from AlICE ITS3 upgrade

	CEPC Final goal	CEPC Expected date	AlICE ITS3 schedule
CMOS chip technology	65nm CIS	2028 Full-size 65nm chip	2025
Spatial resolution	3-5 μm with final chip	2028	2025
Stitching	65nm CIS stitched sensor	2029	2026 wafer production
Bent silicon with small radius	Bent final wafer with radius ~11mm	2030	2027
Detector cooling	Air cooling with full power	2027： thermal mockup	2027
Detector integration	Detector with bent silicon design	2032	2028

Summary of Answer to Review comments

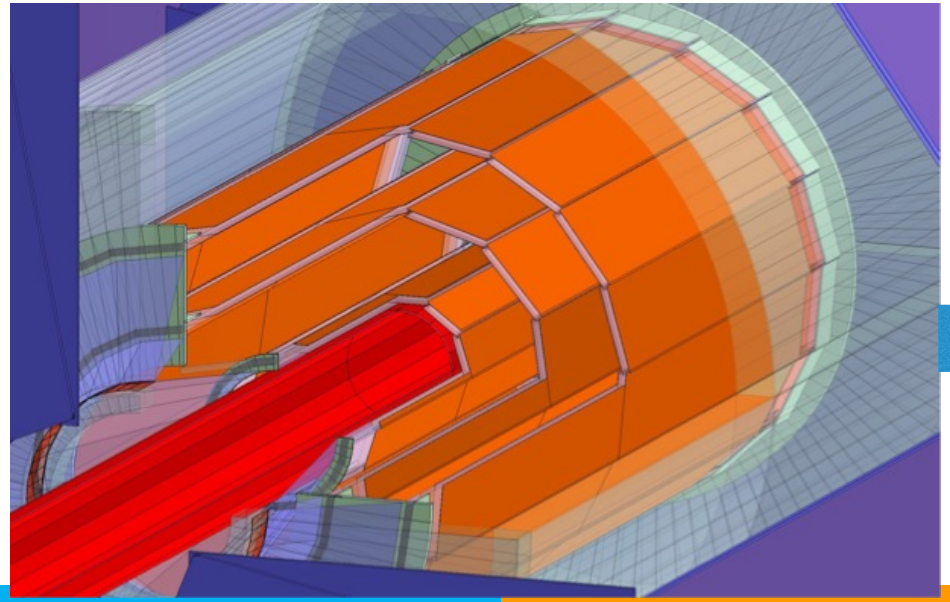
- The timeline of the CEPC project raises concerns that the process with the required features, such as modified doping profiles, may not be available when needed. Therefore, early communication with the vendor is essential, along with exploring potential developments with a secondary supplier. This proactive approach could also prove to be cost-effective in the long term.
  - Answer: Plan to work with TJ180 and TPSCO65nm in next few years to develop stitched MAPS
  - Exploring HLMC 55nm foundry as secondary supplier (meeting in April 1st in Shanghai)



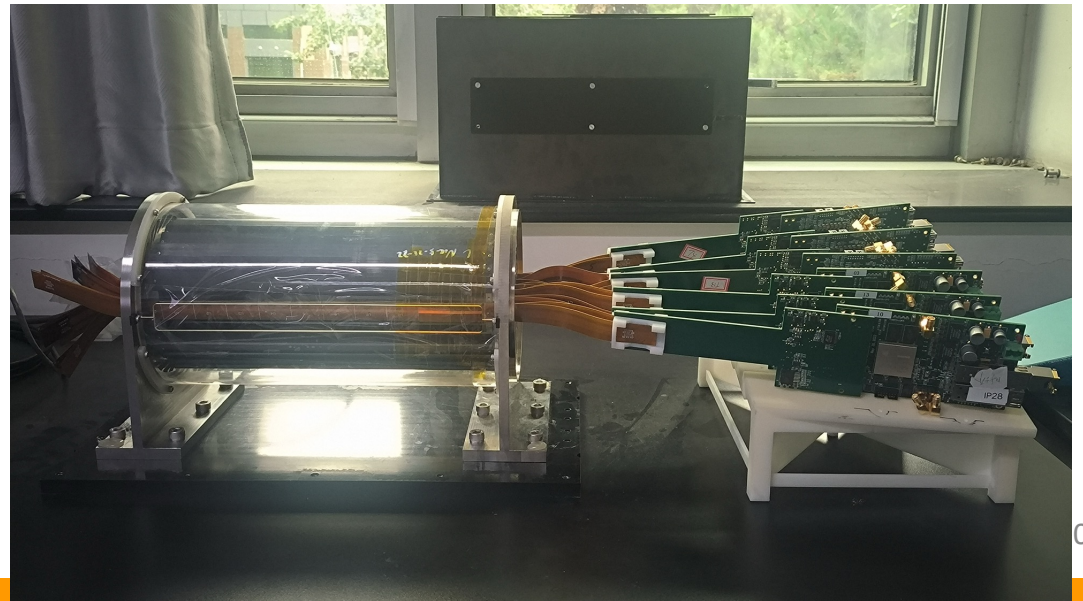
Summary

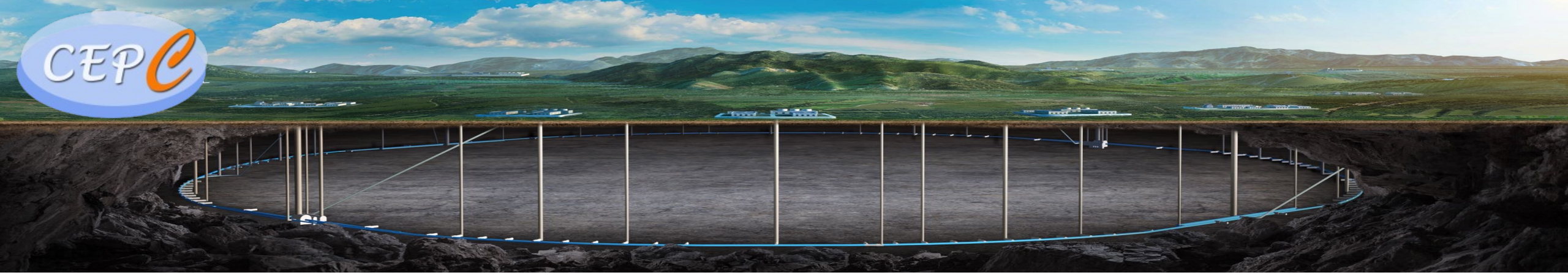
- 1st full-size Prototype based the ladder design for CEPC vertex detector has been developed
- The Curved MAPS option has been chosen as baseline for the reference detector TDR.
- We active expanding international collaboration and explore synergies with other projects
  - We are members of ECFA DRD3 collaboration (solid state detectors)

CEPC vertex conceptional design (2016)



CEPC vertex prototype (2023)



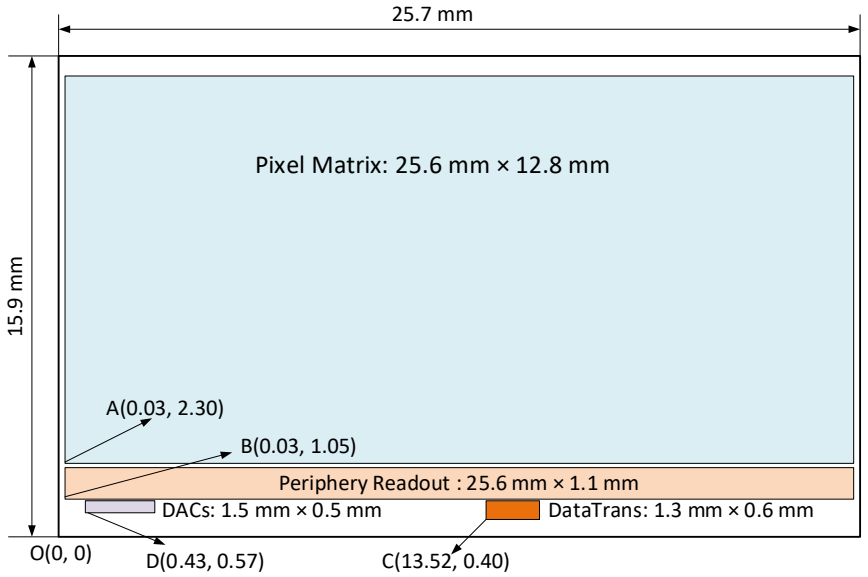


Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Chip design for ref- TDR and power consumption

- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm^2
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation



	Matrix	Periphery	DataTrans.	DACs	Total Power	Power density
TaiChu3 180nm chip @ triggerless	304 mW	135 mW	206 mW	10 mW	655 mW	160 mW/cm^2
65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z)	60 mW	80 mW	36 mW	10 mW	186 mW	~40 mW/cm^2