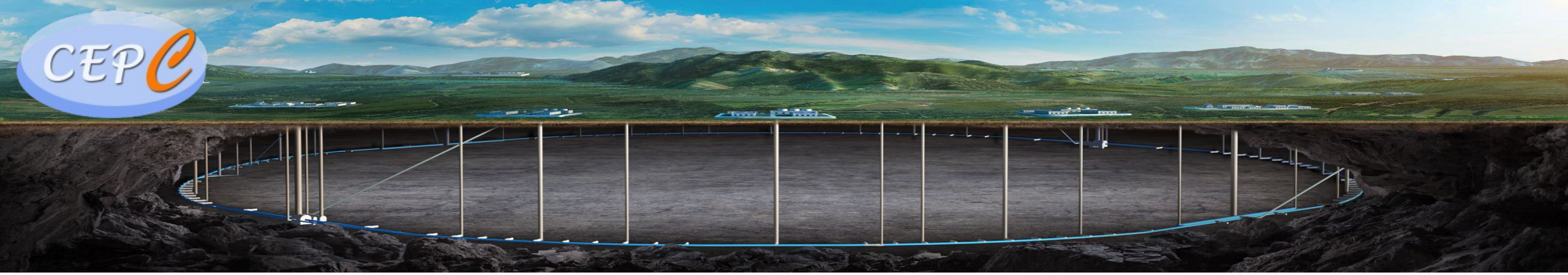

CEPC Silicon Tracker Detector

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Introduction

Chapter 5 Silicon Trackers

5.1 Requirements
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5.1.2 Specific requirements on Silicon Tracker
5.2 Overview of ITK and OTK
5.2.1 Technology options and boundary conditions
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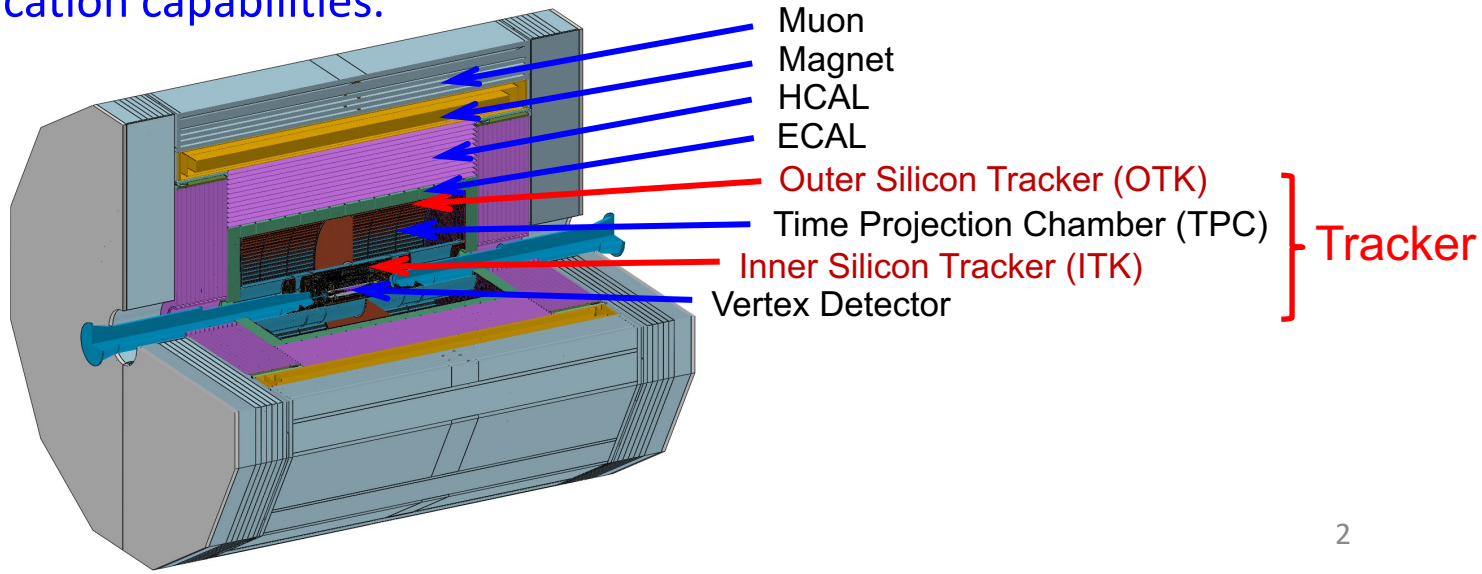
5.9 Summary

- The CEPC tracker system includes several detectors: the Vertex Detector, Inner Silicon Tracker, Time Projection Chamber (TPC), and Outer Silicon Tracker. This presentation, corresponding to Chapter 5 of Ref-TDR on Silicon Trackers, will focus on the Inner Silicon Tracker (ITK) and Outer Silicon Tracker (OTK).

- The ITK employs advanced CMOS sensor technology to achieve precise position measurements for accurate particle trajectory determination.

- In addition to position measurement, the OTK integrates the AC-LGAD semiconductor detector for precision time measurement of charged particles, significantly enhancing particle identification capabilities.

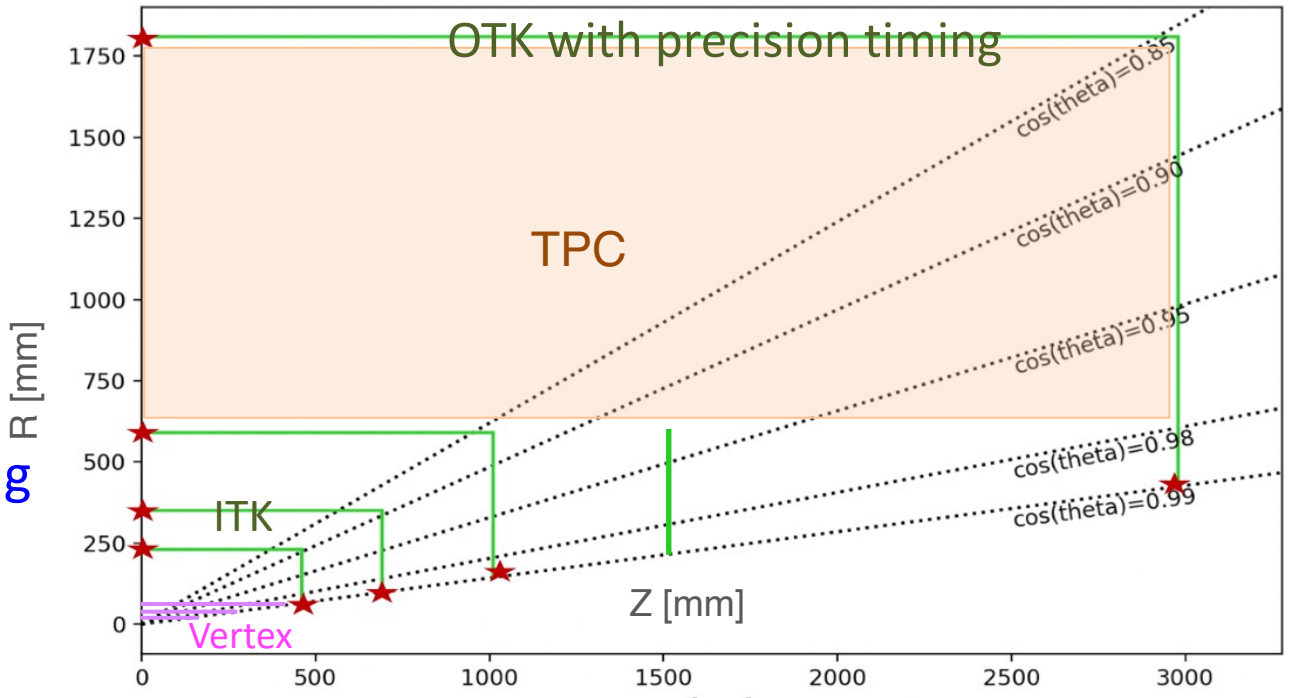


Requirements

- Inner silicon tracker (ITK)
  - Spatial resolution:
    Barrel: σ_ϕ< 10 μm (bending), σ_z< 50 μm
    Endcap: σ_ϕ< 10 μm (bending), σ_r< 100 μm
  - Material budget:
    <1% X_0 per layer
  - Operate at high luminosity Z-pole mode:
    A few ns timing resolution to tag 23 ns bunches
  - Cost effectiveness:
    ~20 m^2 area
- Outer silicon tracker (OTK) with precision timing
  - Spatial resolution:
    σ_ϕ< 10 μm (bending)
  - Material budget:
    1-2% X_0
  - Timing resolution:
    σ_t<50 ps
  - Cost effectiveness:
    ~85 m^2 area

5.1 Requirements

Figure 5.2



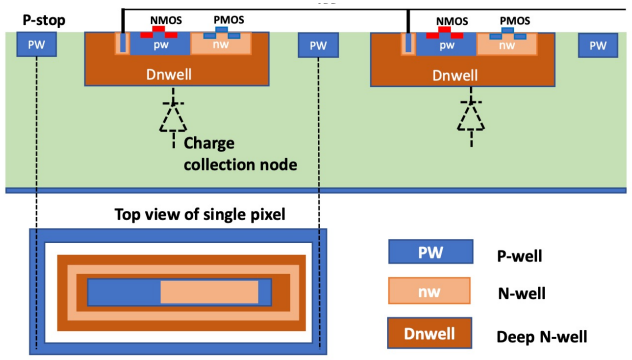
The overall track momentum resolution requirement: ~0.1% for momenta below 100 GeV/c.

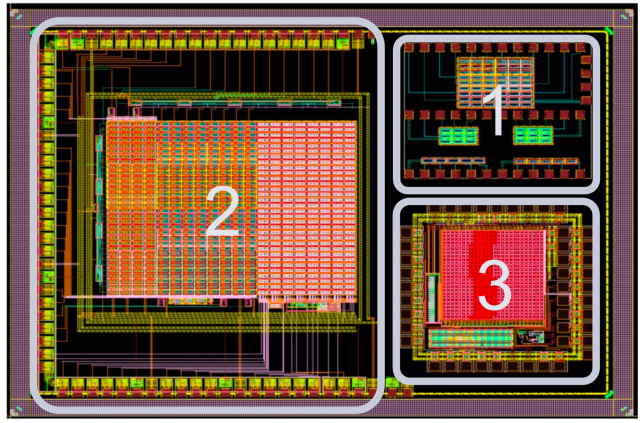
Technology Survey and Our Choice for ITK

- CMOS sensor technology:
  - Cost-effective: CMOS technology is widely used in the semiconductor industry, offering a unique opportunity for development of advanced semiconductor detectors for HEP.
  - Simplified: The active detection layer and readout electronics are integrated into a single chip.
- HV-CMOS pixels:
  - Large depletion depth (full depletion), large signal, and good time resolution.
  - Radiation hard.
  - Low materials.
- Key parameters of HV-CMOS pixel sensor (COFFEE) for CEPC:
  - Process node: 55 nm
  - Chip size: 2 cm × 2 cm
  - Array size: 512 rows × 128 columns
  - Pixel size: 34 μm × 150 μm
  - Spatial resolution: 8 μm × 40 μm
  - Time resolution: 3-5 ns
  - Power consumption: 200 mW/cm^2

5.3.1 CMOS chip R&D

Figure 5.9





HV-CMOS COFFEE2 chip

R&D: CMOS Chip Development

5.3.1.1 HV-CMOS pixel R&D

- CMOS pixels (COFFEE2): 55 nm CMOS process

Submitted in Aug 2023, received in Dec 2023

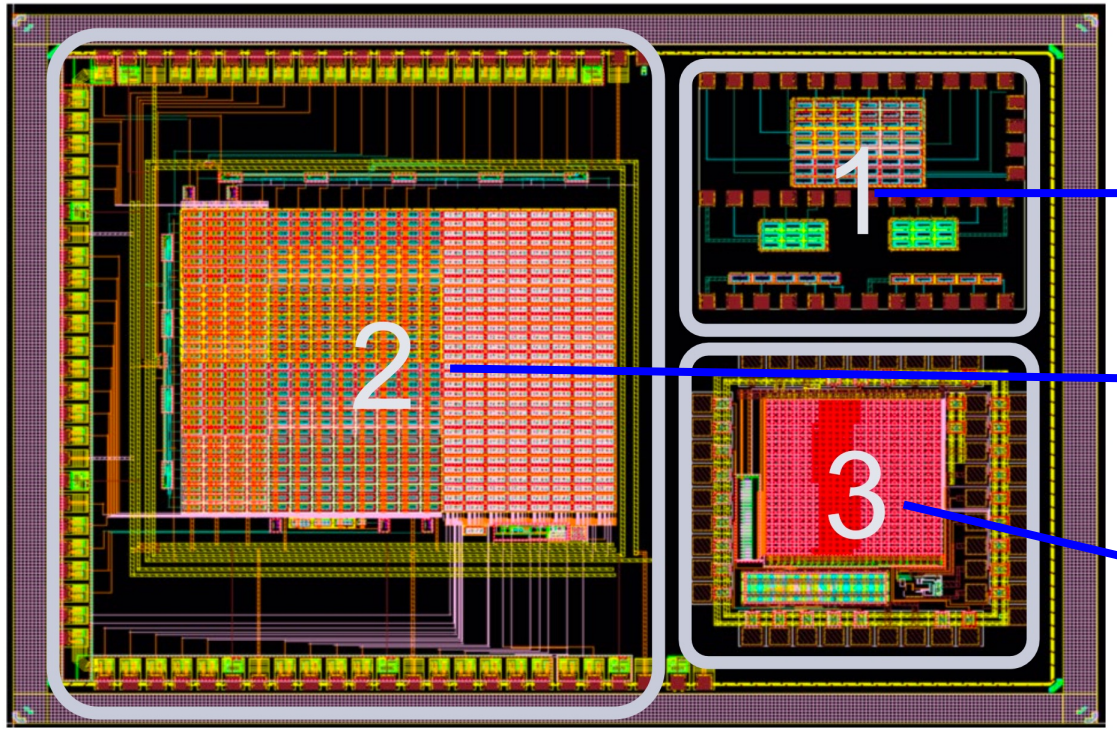
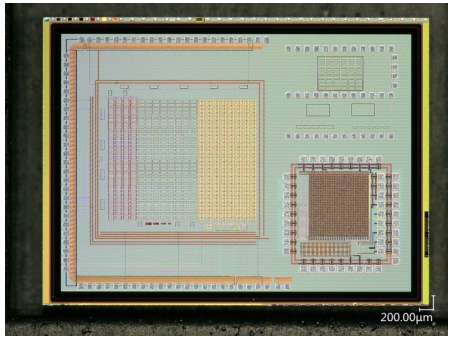


Figure 5.14

COFFEE

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS



COFFEE2

Three sections in the chip:

1: Passive diode arrays:

- Including 6 different signal collection structures for studying diodes and charge sharing.

2. Pixel arrays with diodes and in-pixel circuits:

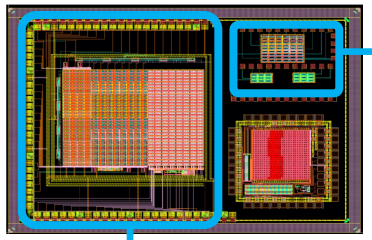
- Features 6 types of diodes and 3 types of in-pixel electronics.

3. Pixel arrays with peripheral digital readout:

- Used for validating readout strategies for imaging application, which are not directly relevant to the CEPC use case.

HVCMOS (COFFEE2) Chip Test

5.3.1.1 HV-CMOS pixel R&D



- Tests have been performed
  - IV (breakdown at –70 V)
  - CV (single pixel ~30-40 fF)
  - Leakage current increased from 0.01 nA to ~1 nA after 10^{14} n_{eq}/cm^2 radiation
  - Laser response observed
  - Radioactive source (^{55}Fe) observed
- Circuit test

COFFEE2 has successfully verified the sensor process and in-pixel analog front-end.

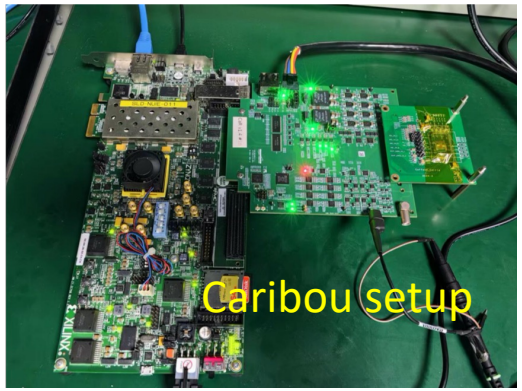
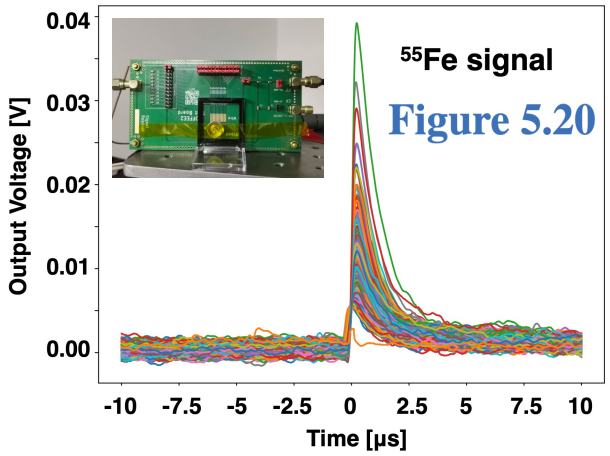
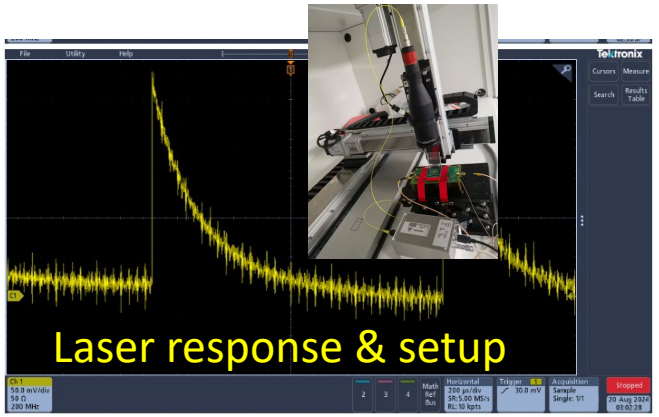
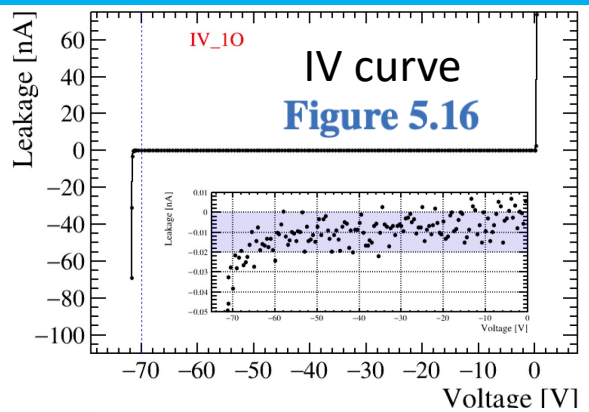
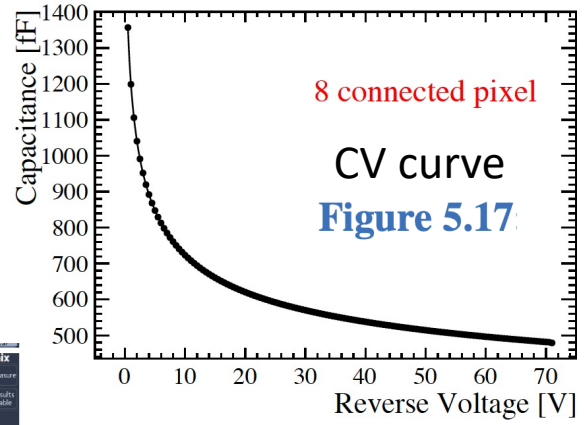


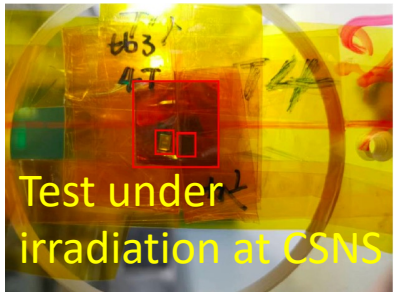
Figure 5.18







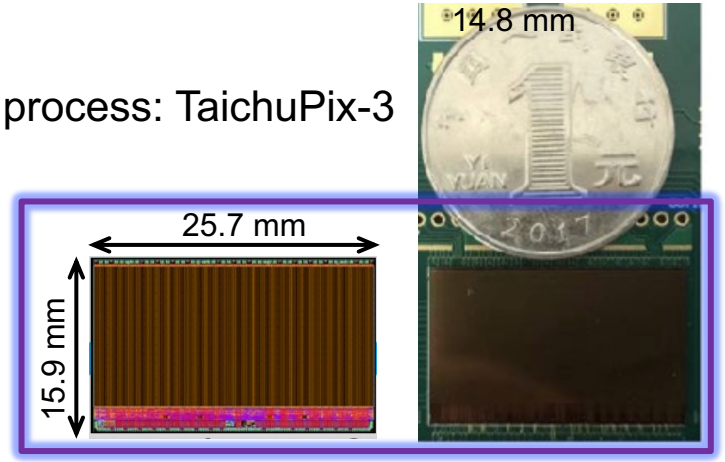




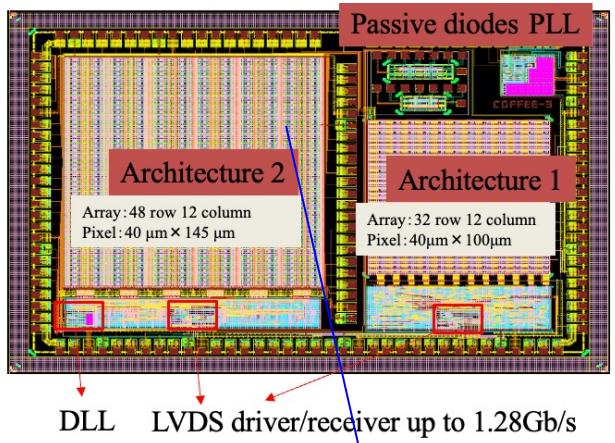
Experience in Silicon Detector Development

- The CEPC team has successfully developed several fully functional MAPS:
  - JadePix, TaichuPix, CPV, etc.
- Major contributions to silicon detector construction, testing, integration, and operation:
  - AMS L0 upgrade, ATLAS ITk, ATLAS HGTD, CMS HGCAL, LHCb UT, etc.

CIS process: TaichuPix-3

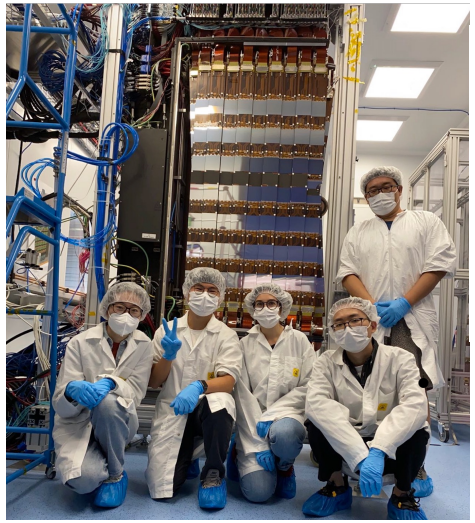


HV-CMOS process: COFFEE3

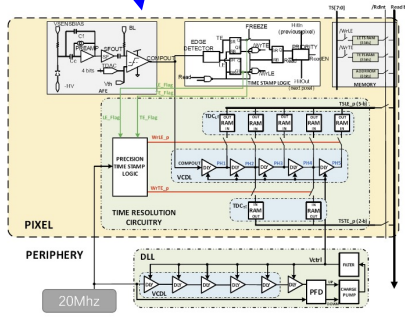


AMS L0 ladder production

ATLAS ITK strip module



LHCb UT A-side assembly



In-pixel coarse-fine TDC

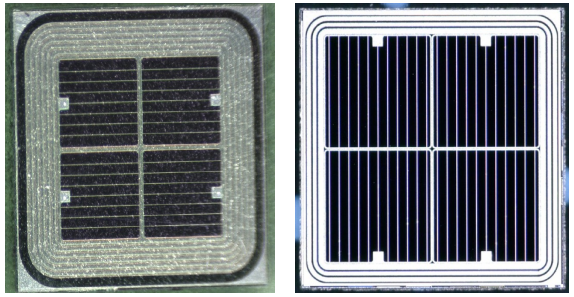
The tape-out of the new HV-CMOS (COFFEE3) chip has been submitted in Jan 2025 and expected to receive in May 2025.

LGAD Development at IHEP

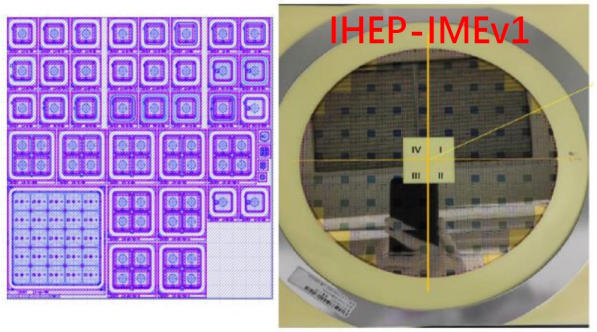
- The LGAD (Low Gain Avalanche Detector) sensor developed by IHEP achieves both precise position and time measurements.

5.4.1.1 AC-LGAD Sensor R&D

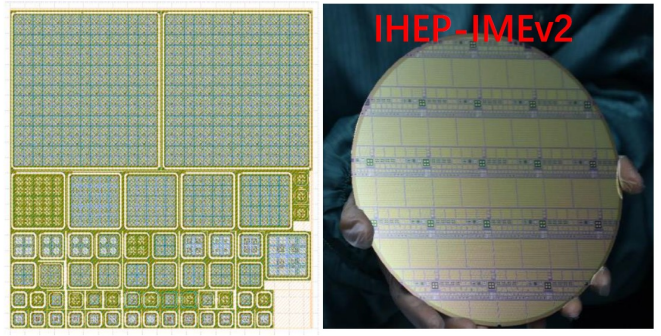
IHEP-NDL(2019)



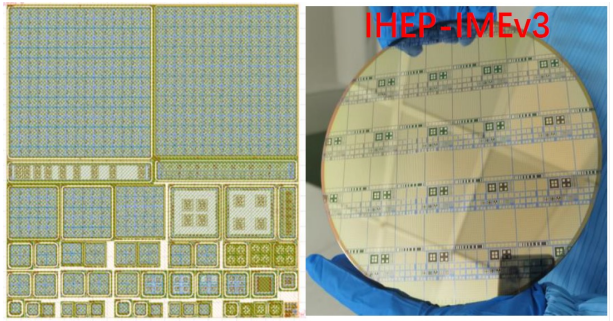
IHEP-IMEv1(2020.9)



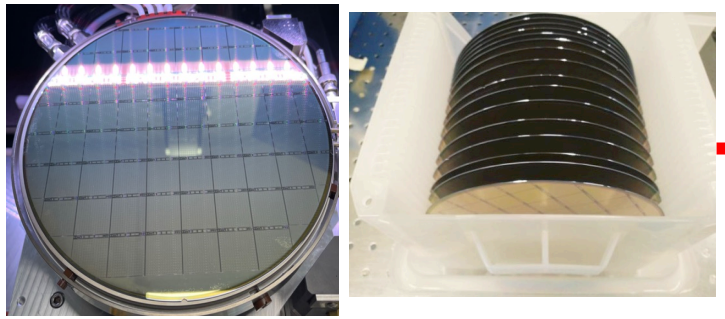
IHEP-IMEv2(2021.6)



IHEP-IMEv3(2022.5)



Pre-production for ATLAS (2023.7)



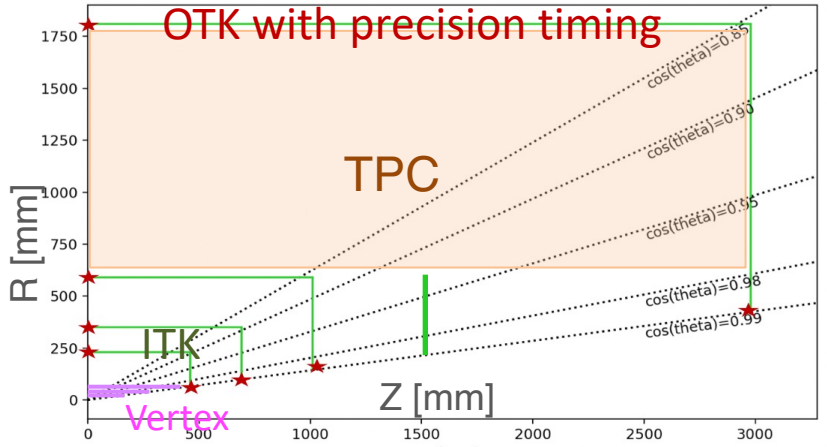
Mass production for ATLAS (2024.6)

- In May 2023, CERN selected IHEP-IME in the HGTD sensor tendering process:
  - First time a domestic silicon sensor was chosen by CERN for an LHC experiment.

AC-LGAD for OTK with Precision Timing

- Key parameters of AC-LGAD microstrip sensor for OTK:
  - Sensor size: (3-4.5) cm × (3-5) cm
  - Strip number: 512 or 384
  - Pitch size: ~100 μm
  - Spatial resolution: 10 μm
  - Time resolution: 50 ps
  - Power consumption: 300 mW/cm^2

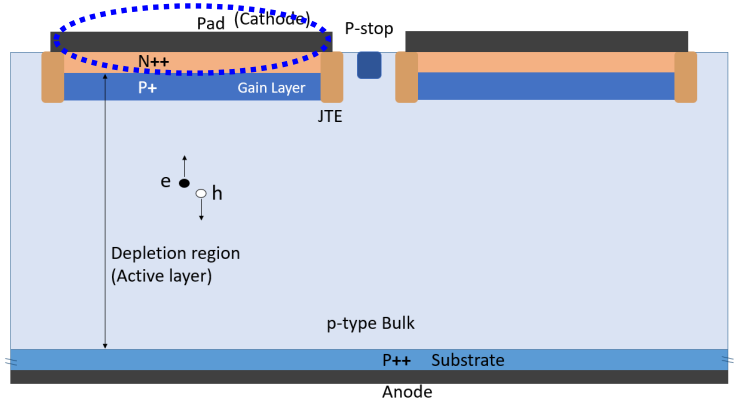
5.4.1.1 AC-LGAD Sensor R&D



LGAD (Low-Gain Avalanche Detector)

Segmented gain layer

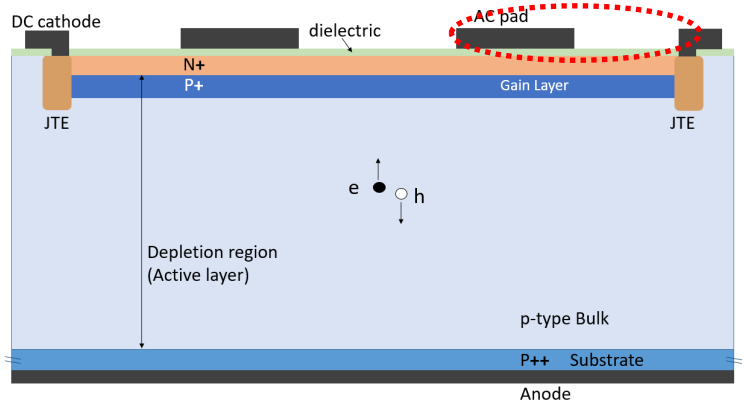
Figure 5.63



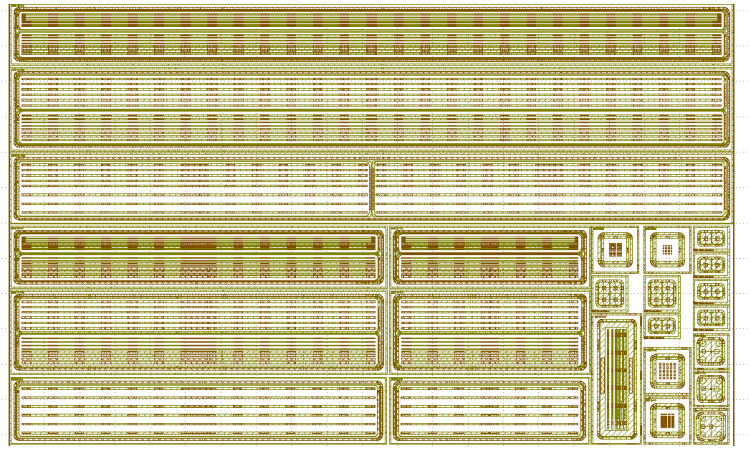
- The read-out electrode is connected to the N++ layer.

AC-LGAD (AC-coupled LGAD)

Continuous gain layer (less dead area)



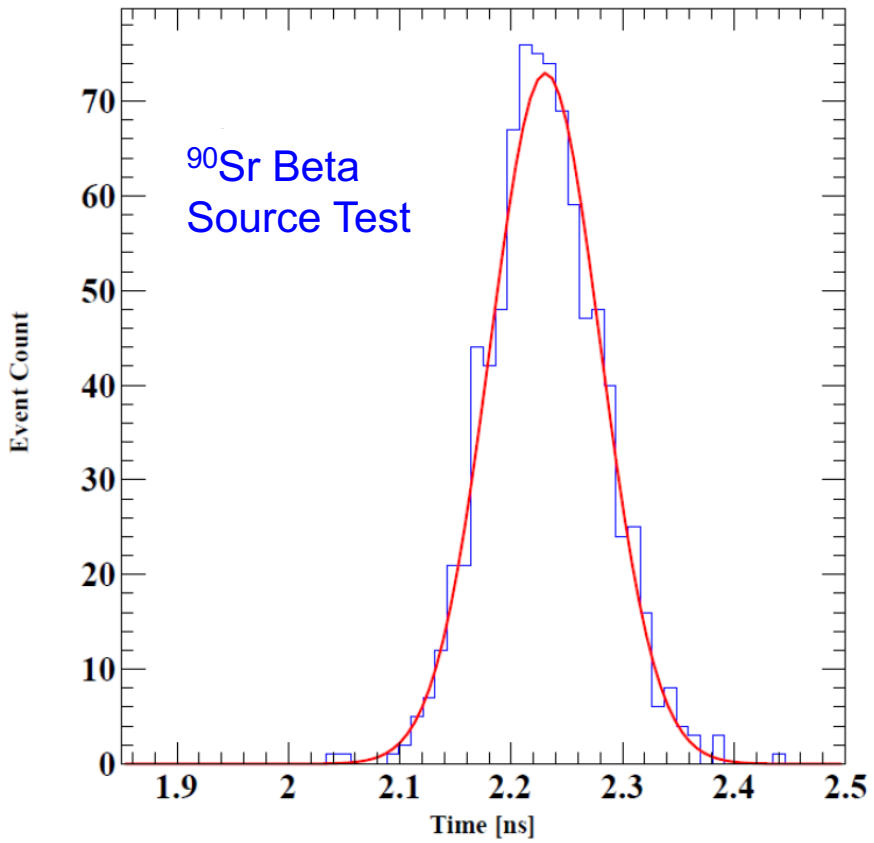
- A thin dielectric layer (Si_3N_4 or SiO_2) separates the metal AC pads from the N+ layer.



The latest AC-LGAD layout (submitted for tap-out in Feb 2025)

AC-LGAD Performance: Time and Spatial Resolution

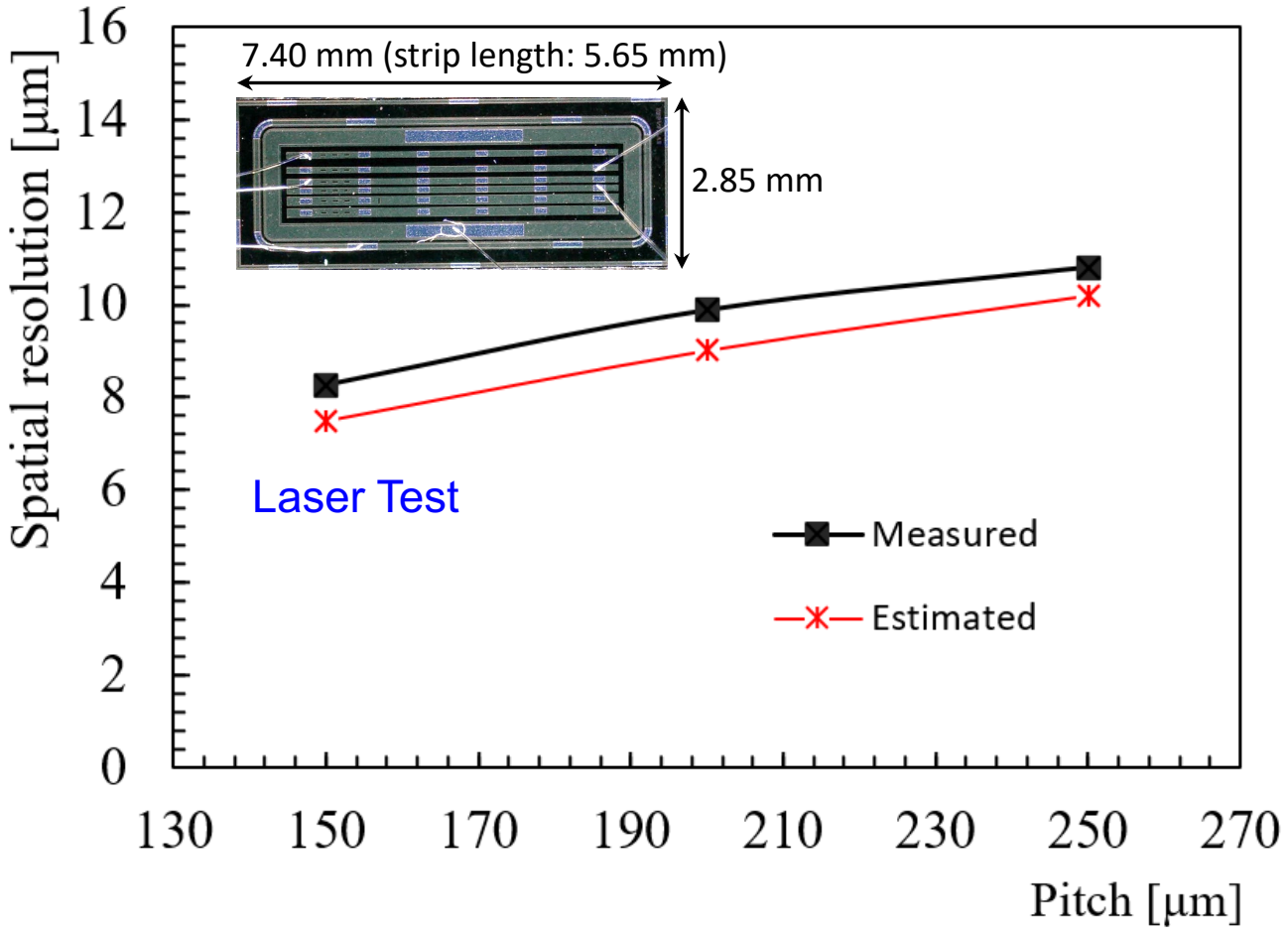
Figure 5.73



Time residual sigma: 47.1 ps

Time resolution: 37.5 ps

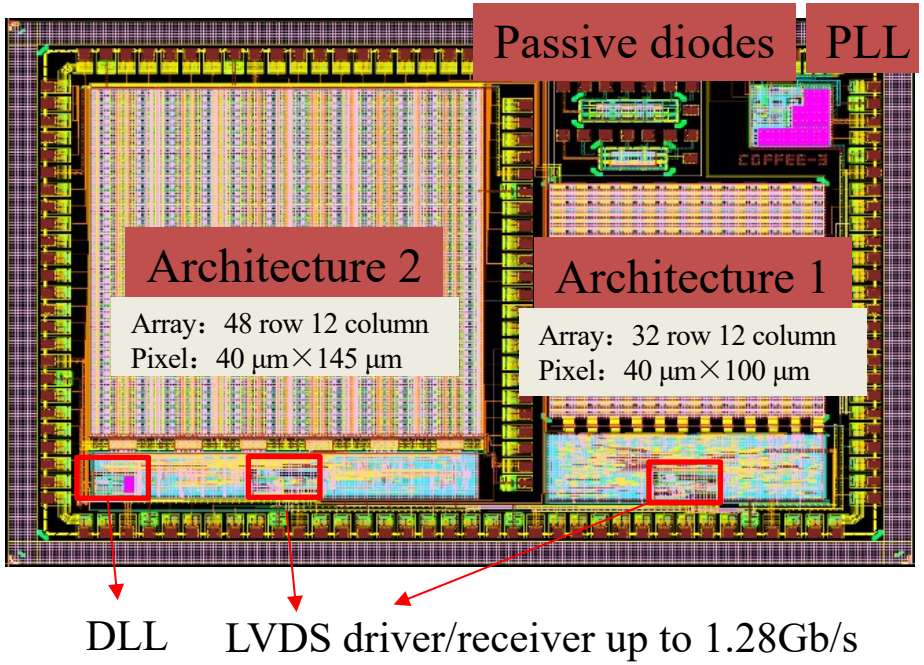
5.4.1.1 AC-LGAD Sensor R&D



Spatial resolution: 8 μm for 150 μm strip pitch size

Progress after 2024 IDRC Review (1)

- HV-CMOS Pixels (COFFEE2 and COFFEE3):
  - HV-CMOS pixel sensor chip (COFFEE2) has successfully completed critical verification, providing crucial input for the final chip design and prototyping.
  - The new COFFEE3 chip design was submitted for tape-out in Jan 2025 and is expected to be received in May 2025:
    (COFFEE3 incorporates two readout architectures, both featuring nearly a complete ASIC readout framework. This solution can be extended to final chip.)

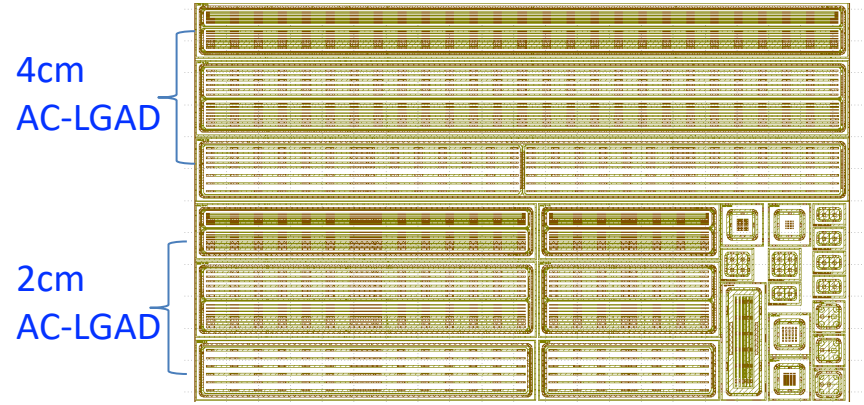


- **Architecture 1:** An optimized design framework based on the current process conditions (Triple-well process)；
- **Architecture 2:** An improved solution that requires process modification (Deep P-well required) to fully utilize the advantages of the 55 nm process node.

Progress after 2024 IDRC Review (2)

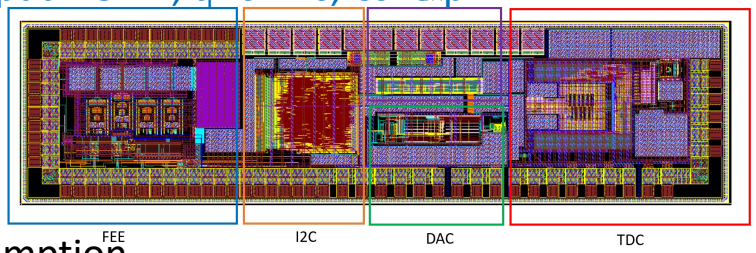
- New IHEP AC-LGAD strip sensor prototype: summitted for tap-out in Feb 2025. The new layout and design include:
  - Strip lengths： 1 cm, 2 cm, and 4 cm
  - Strip pitch sizes: 100 µm, 200 µm, and 500 µm
  - Optimized isolated structure design to reduce sensor capacitance
  - Process design optimization (n+ layer dose) for better spatial resolution

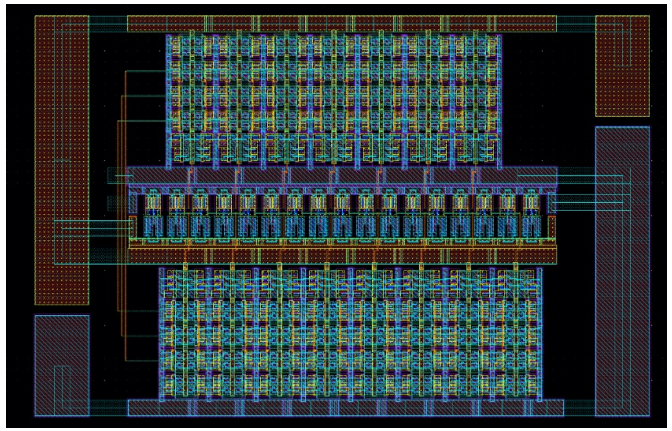
This study addresses the IDRC comment:
- Reevaluate the size of the AC-LGADs, carefully balancing performance factors—such as rate effects, time resolution, and achievable position accuracy …
- Sensors may have high capacitance …



1cm AC-LGAD

- Pre-phototype for AC-LGAD ASIC (LATRIC): designed has been completed and is schedule for submission in April.
  - Several key elements in the design are shared and verified with FPMROC (10 ps) chip
    - FEE: Preamplifier+Discriminator: jitter<7.8ps @ input 2.5mV, t_r=0.1ns, Cs=0 pF
    - PLL, Serializer, SPI is verified
  - I2C Slave: ASIC parameter configuration
  - 12-bit DAC: threshold and calibration
  - TDC design:
    - Event driven delay line to reduce the power consumption
    - Power consumption： average current for single event: 443 µA, static current: < 5 µA
    - Real time calibration for PVT (Process, Voltage, Temperature)
    - LSB ~36 ps based on preliminary layout post-simulation




TDC Delay line layout

ITK Barrel Design with HV-CMOS Pixels

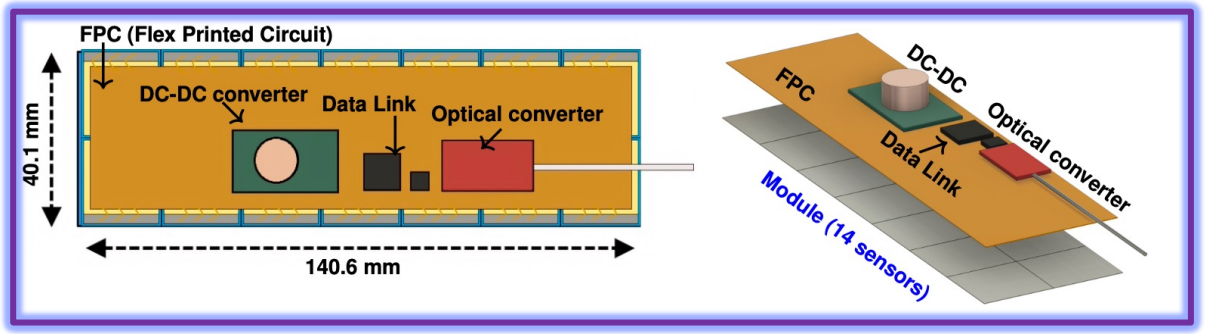
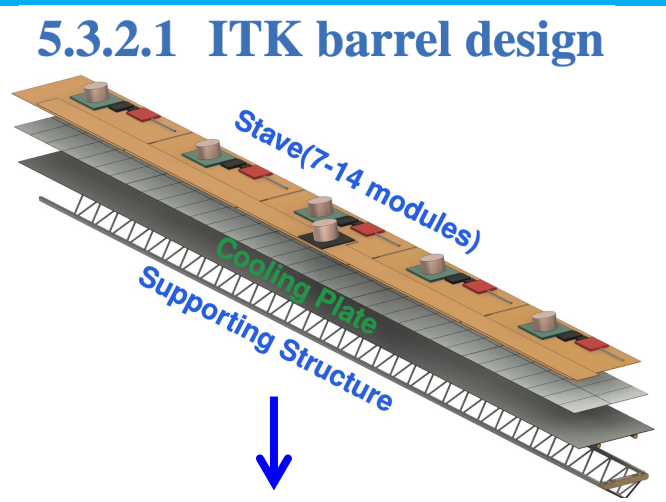


Figure 5.37



- HV-CMOS pixel sensor:
  - Sensor size: 20 mm × 20 mm
  - Pixel size: 34 μm × 150 μm (spatial resolution: 8 μm × 40 μm)
- Module:
  - 14 sensors (2 rows × 7 columns)
  - Module dimensions: 140.6 mm × 40.1 mm
- Stave length: 986.6 mm (ITKB1), 1,409.6 mm (ITKB2), and 1973.2 mm (ITKB3)
- Barrel radii: 235 mm (ITKB1), 345 mm (ITKB2), and 555.6 mm (ITKB3)

The designed 3 ITK barrel layers has a total surface area of 13.3 m², including 33,264 sensor chips, with a power consumption of ~26.6 kW.

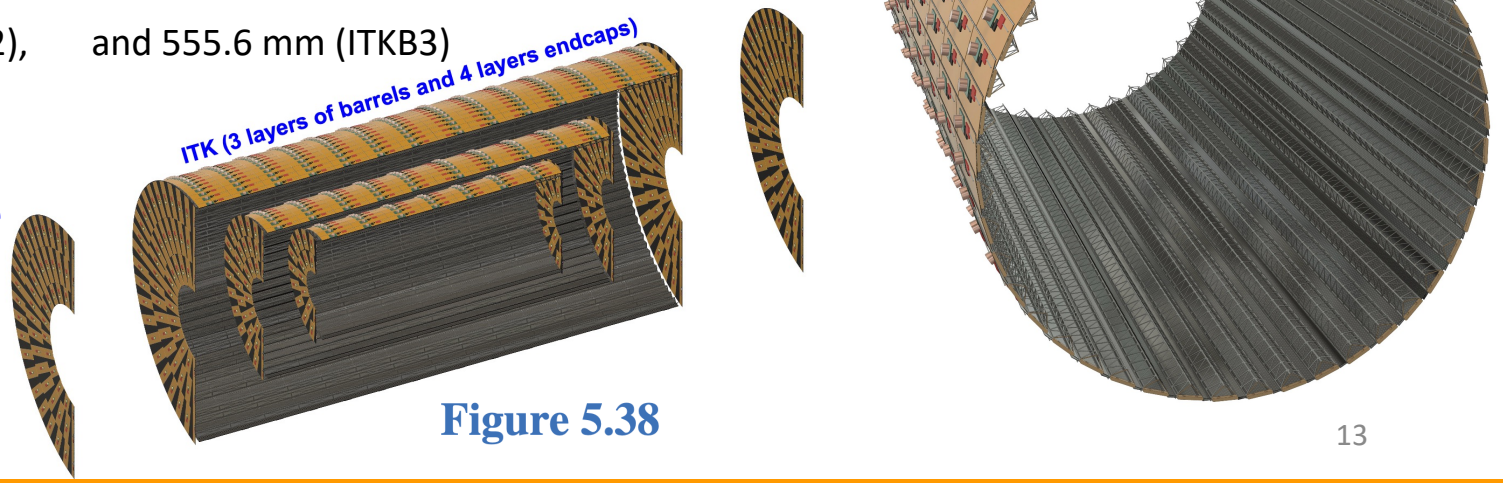
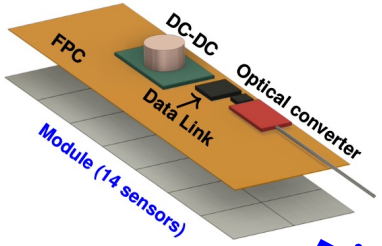


Figure 5.38

ITK Endcap Design with HV-CMOS Pixels



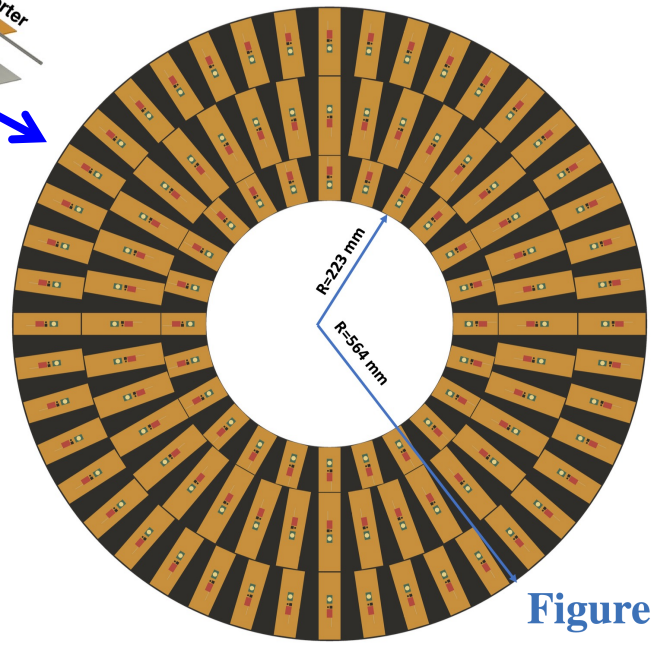


Figure 5.40

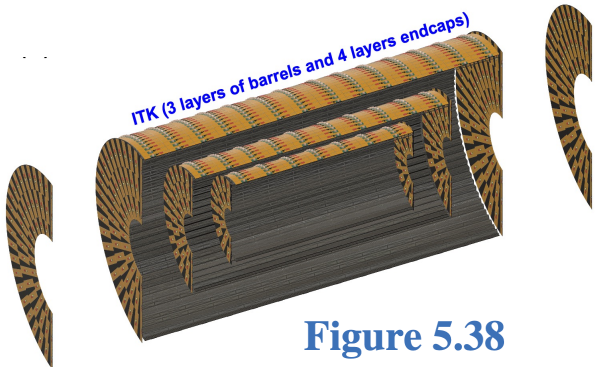
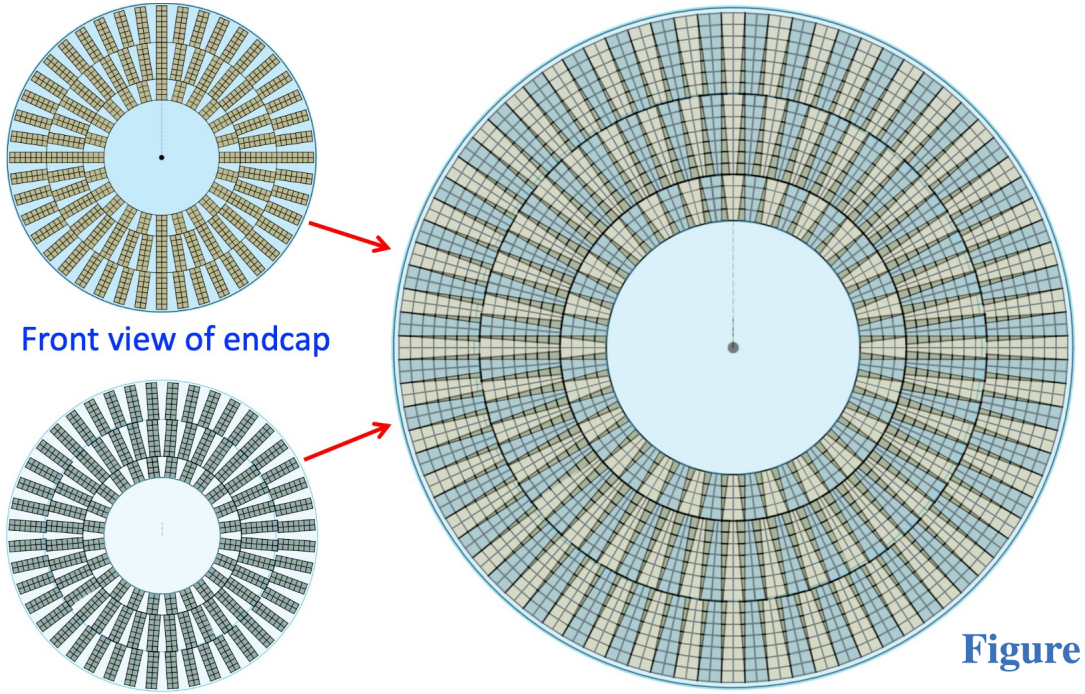


Figure 5.38

5.3.2.2 ITK endcap design

- Module:
  - 3 types of modules : 8, 12, and 14 sensors for all 4 ITK endcaps
- Endcap active area radii:
  - 81.5 mm<r<242.5 mm (ITKE1), 110.5 mm<r<352.3 mm (ITKE2), 163 mm <r<564 mm (ITKE3), and 223 mm<r<564 mm (ITKE4)



Front view of endcap

Back view of endcap

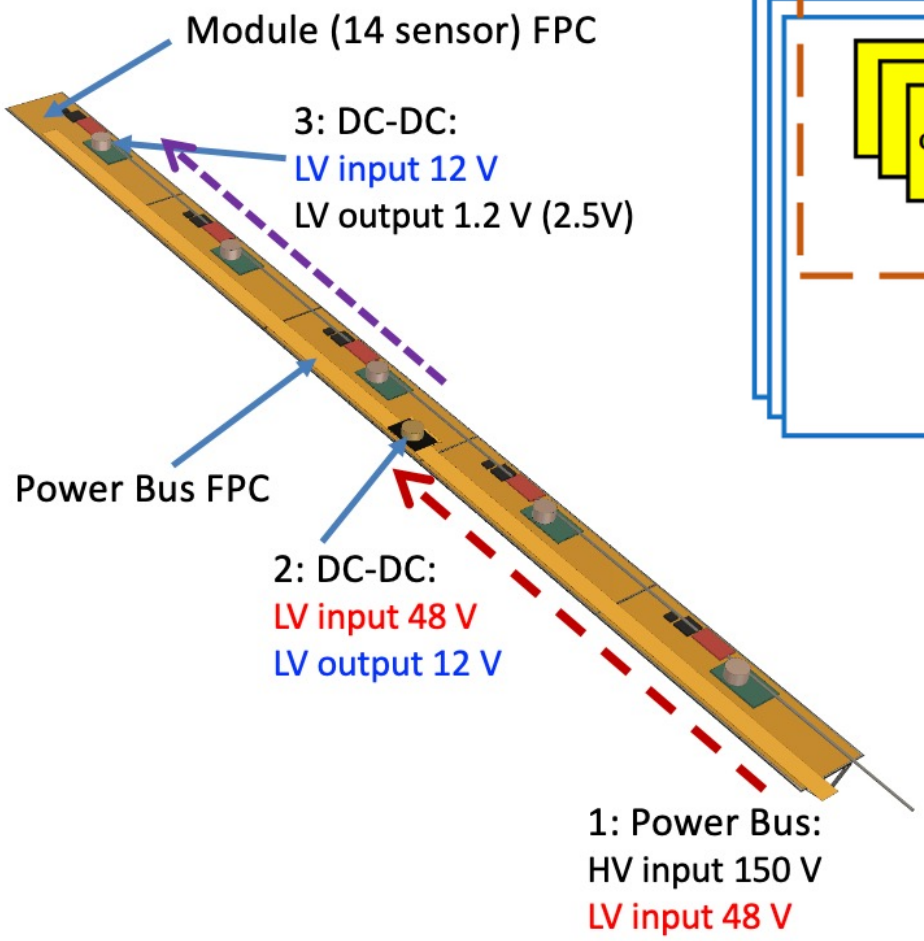
Perspective view of full endcap

Figure 5.39

Each ITK endcap has 2 faces. Four pairs of ITK endcaps have a total surface area of 5.5 m², including 13,760 sensor chips, with a power consumption of ~11 kW.

ITK Power Supply and Readout Electronics

5.3.3 Readout electronics



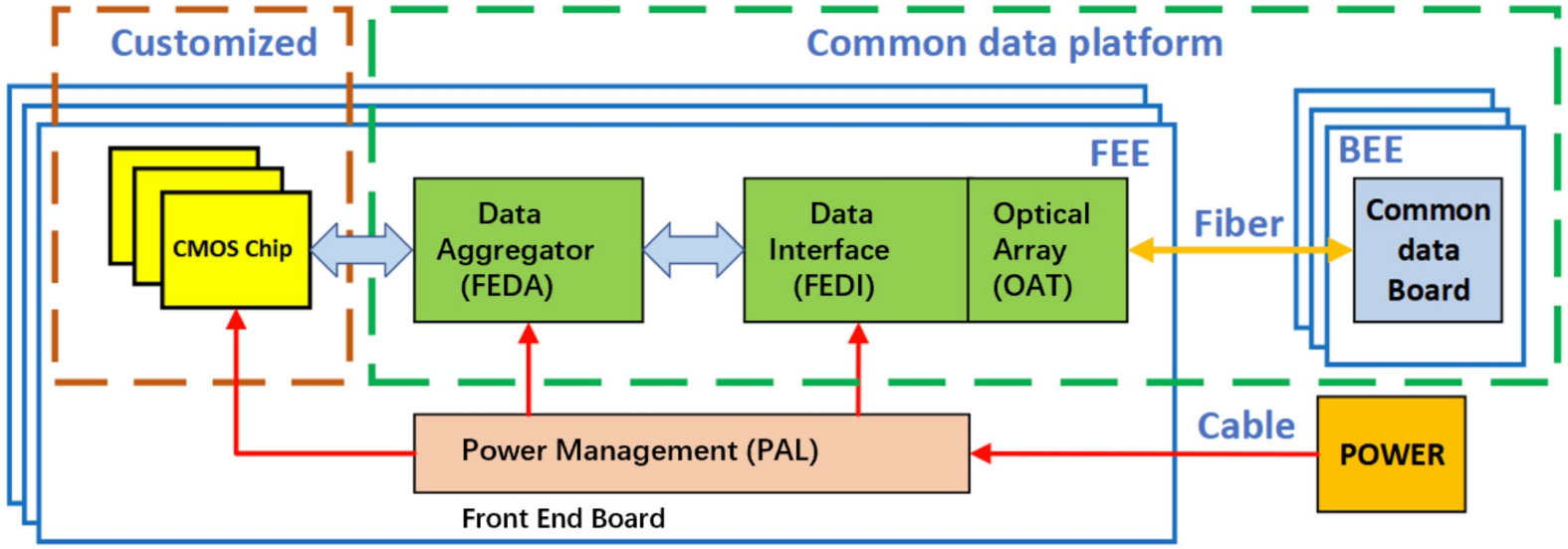


Figure 5.44

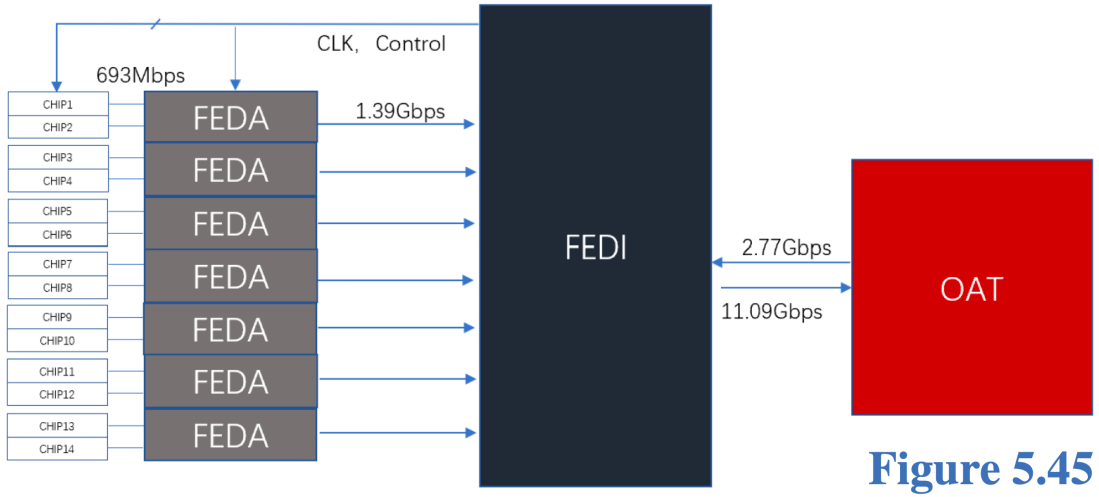
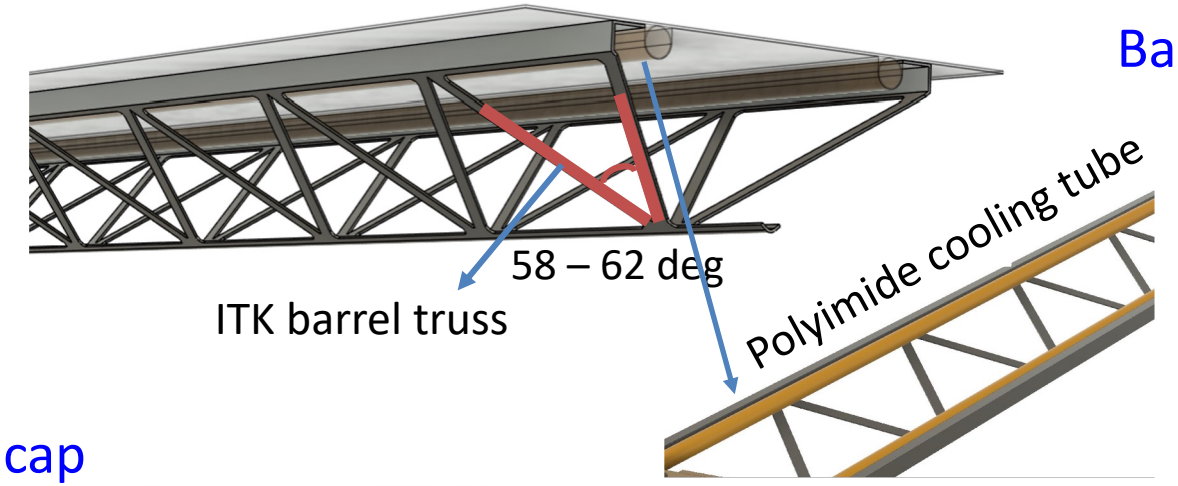


Figure 5.45

Mechanical and Cooling Structure of the ITK



Barrel stave

Endcap

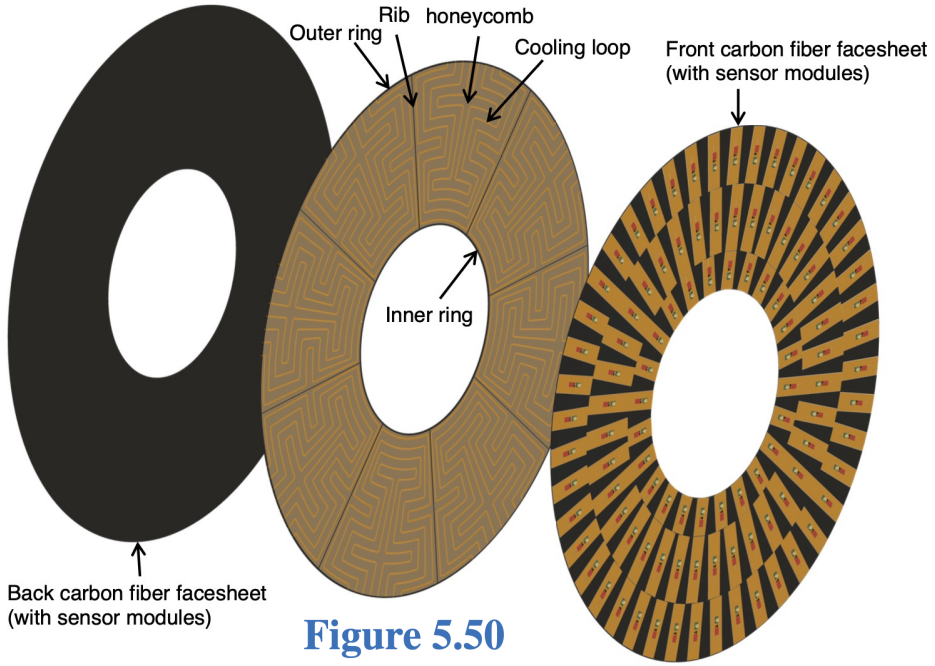


Figure 5.50

5.3.4 Mechanical and cooling design

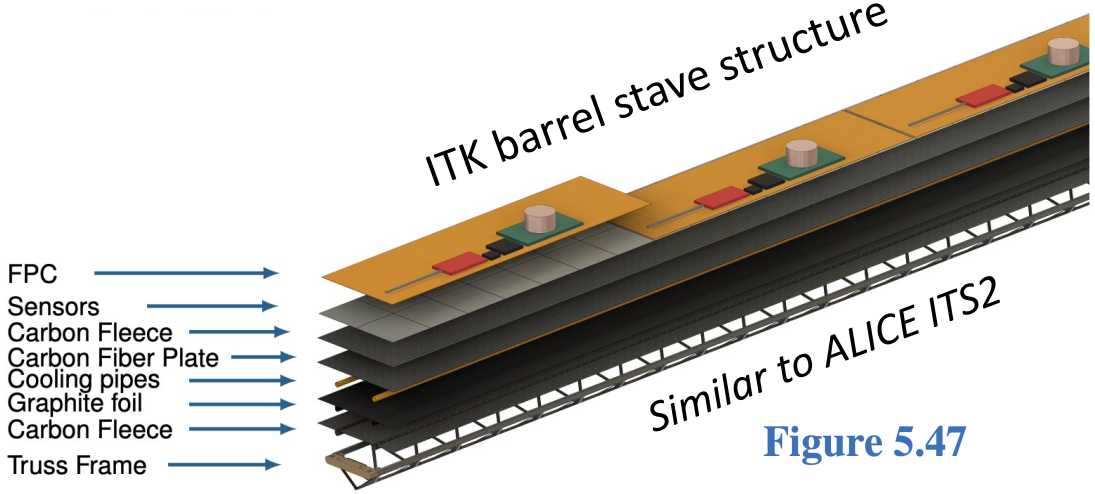


Figure 5.47

Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	150	28.41	0.053
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64	28.41	0.006
	Cooling fluid	Water		35.76	0.028
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Truss Frame	Carbon rowing				0.080
Power Bus FPC					0.070
Total					0.677

Table 5.8

Mechanical and Thermal Analysis of the ITK

5.3.4 Mechanical and cooling design

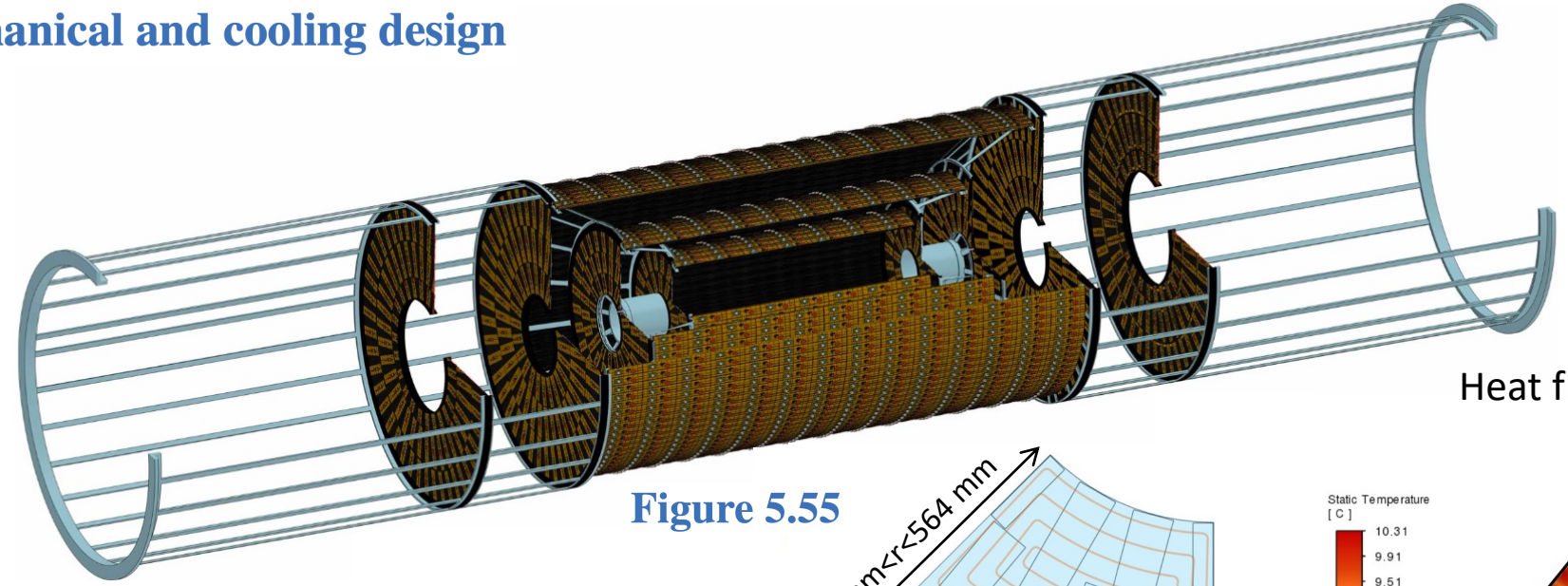


Figure 5.55

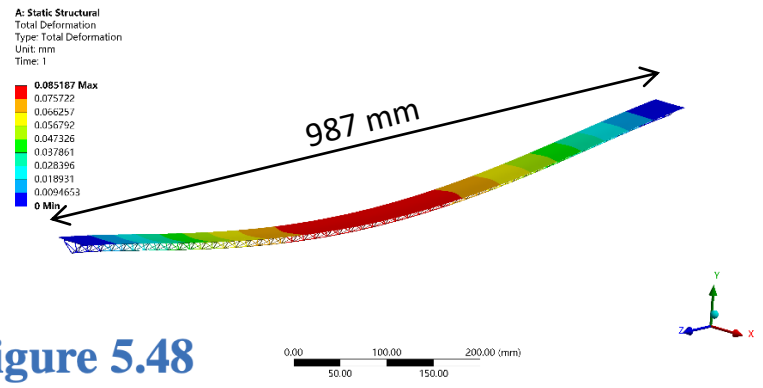
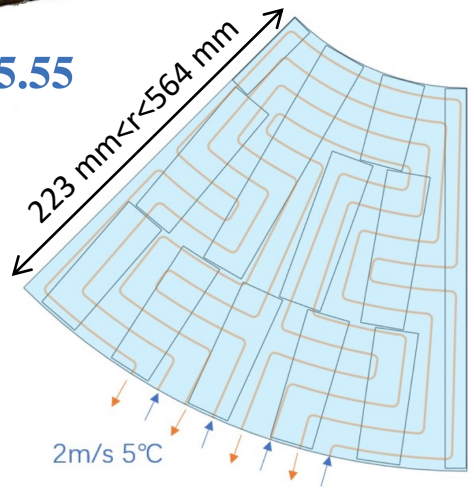
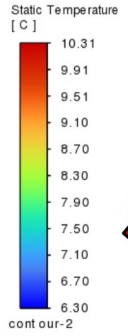


Figure 5.48

Maximum sag for first ITK barrel stave is 85 µm

Heat flux: 200 mW/cm^2





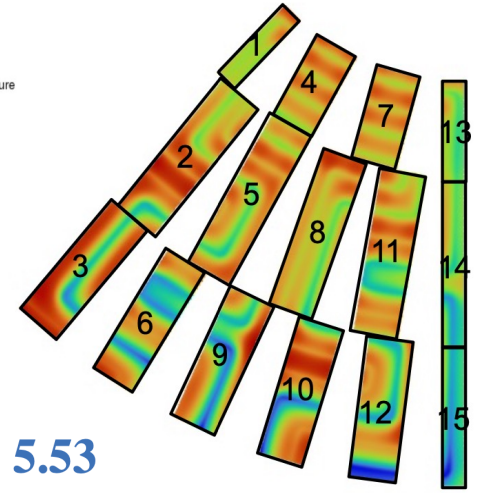
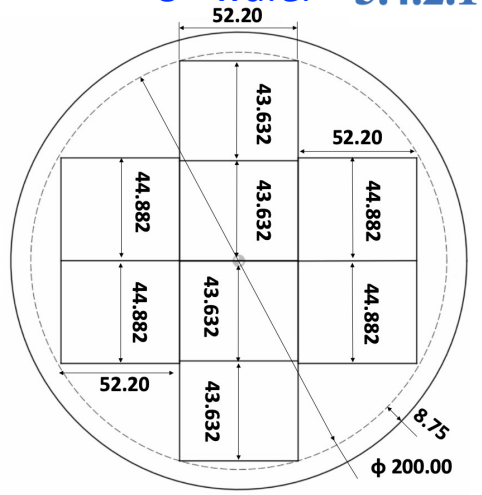


Figure 5.53

4-loops cooling for 1/8 endcap: with a cooling water flow of 2 m/s, a pipe inner diameter of 1.6 mm, and inlet temperature of 5°C, the temperature gradient across the endcap plane is <4°C, and the temperature difference for a single sensor is <2.5°C.

OTK Barrel Design with AC-LGAD Strips

8’’ wafer **5.4.2.1 OTK barrel design** Module (2×2 sensors)



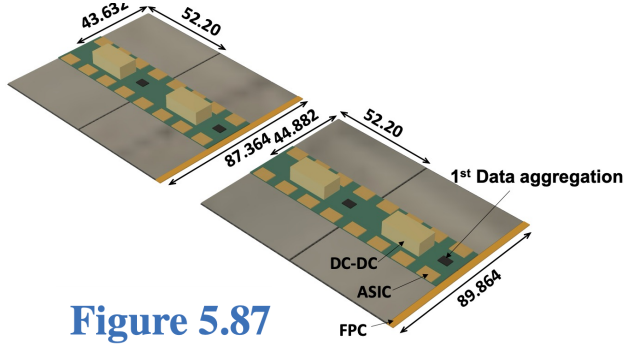


Figure 5.87

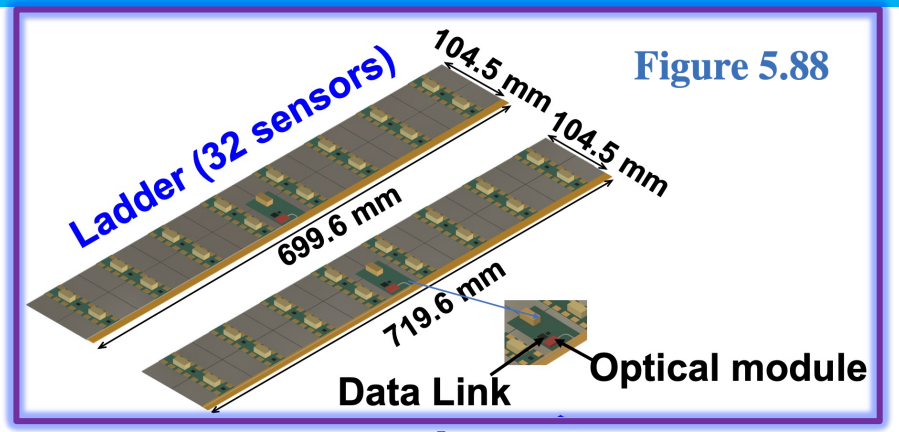


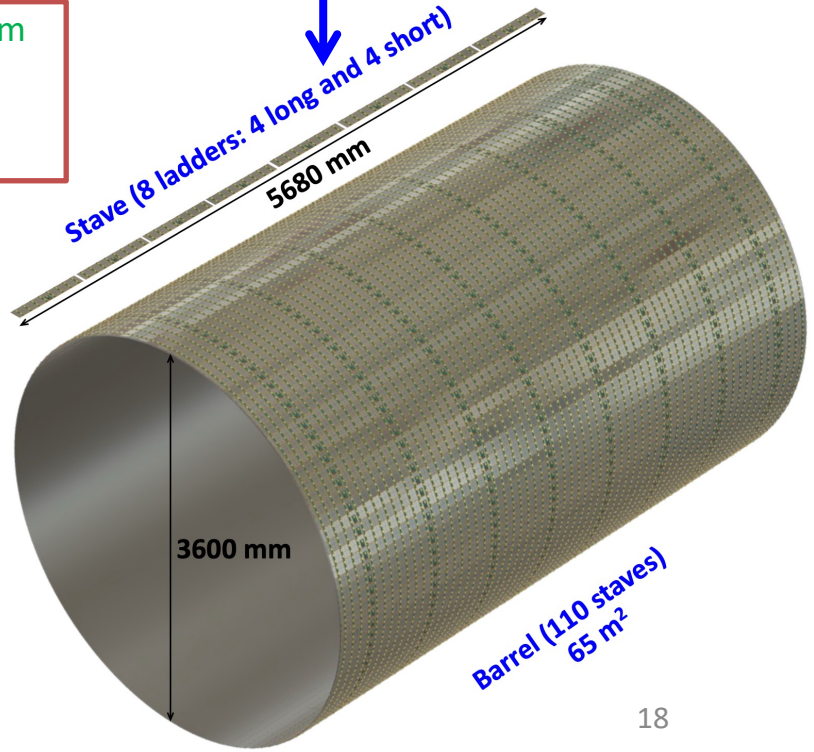
Figure 5.88

Following the 2024 IDRC review, the baseline sensor size was reduced from ~8 cm×5 cm to ~4 cm×5 cm, addressing the IDRC recommendation:

– Reevaluate the size of the AC-LGADs, carefully balancing performance factors—such as rate effects, time resolution, …

- AC-LGAD strip sensor（Each readout by 4 128-channels ASICs）:
  - Sensor size: 43.632 mm × 52.20 mm
    44.882 mm × 52.20 mm
  - Strip pitch: 100 μm (spatial resolution 10 μm)
- Module: 4 sensors (16 readout ASICs)
- Ladder: 8 modules (32 sensors)
- Stave: 8 ladders (4 short+4 long)

The designed OTK barrel has a total surface area of 65 m², including 28,160 sensors and 112,640 readout ASICs (LATRIC) developed by IHEP, with a power consumption of ~195 kW.



OTK Endcap Design with AC-LGAD Strips

Endcap (16 sectors, 10 m^2)

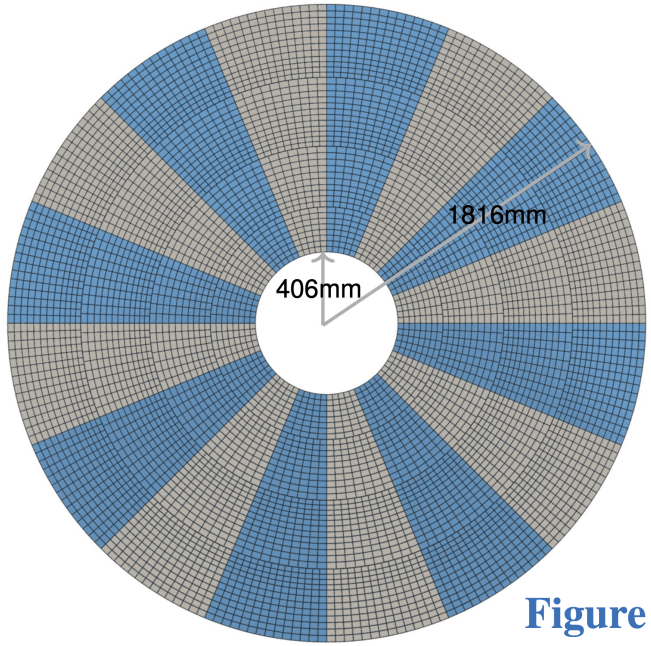
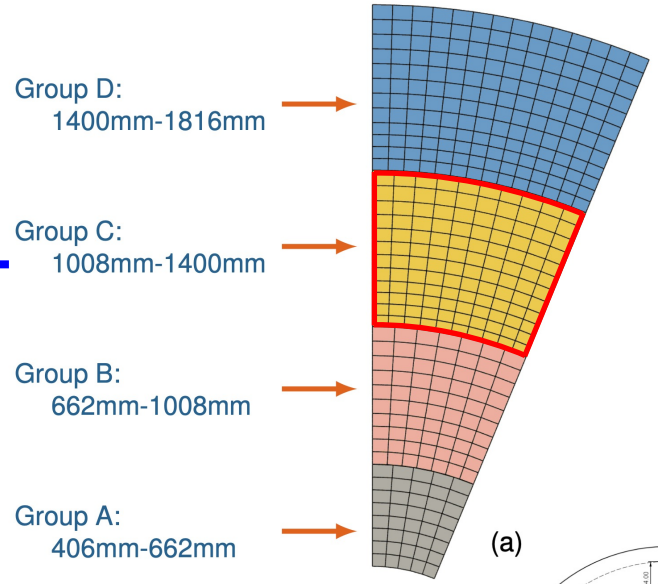


Figure 5.89

5.4.2.2 OTK endcap design

1/16 Sector



Sensor: 8'' wafer (group C sensors)

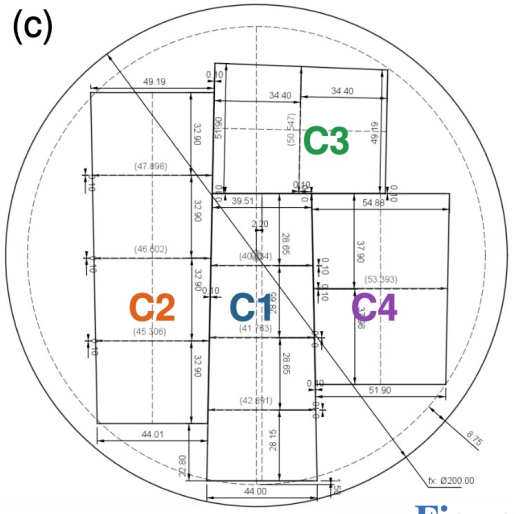
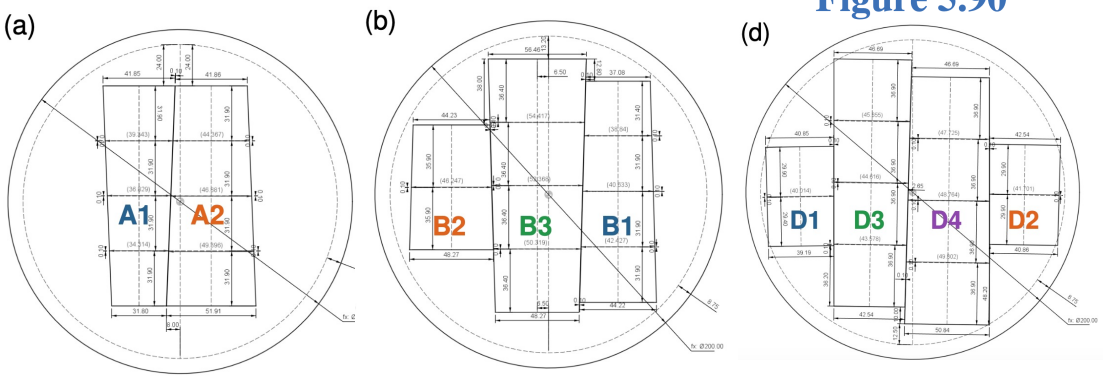


Figure 5.90



8'' wafer (group A, B, D sensors)

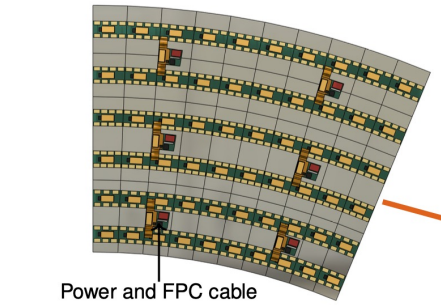
- OTK endcap consists of 42 rings, arranged into 4 groups.
- Each group contains 2-4 subgroups of trapezoid sensors, dicing from one 8'' silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
  - Strip pitch : 80.59-113.026 µm
  - Strip length : 28.05-36.3 mm

OTK endcap has a total surface area of 20 m^2, including 12,736 sensors and 46,336 ASICs, with a power consumption of ~60 kW.

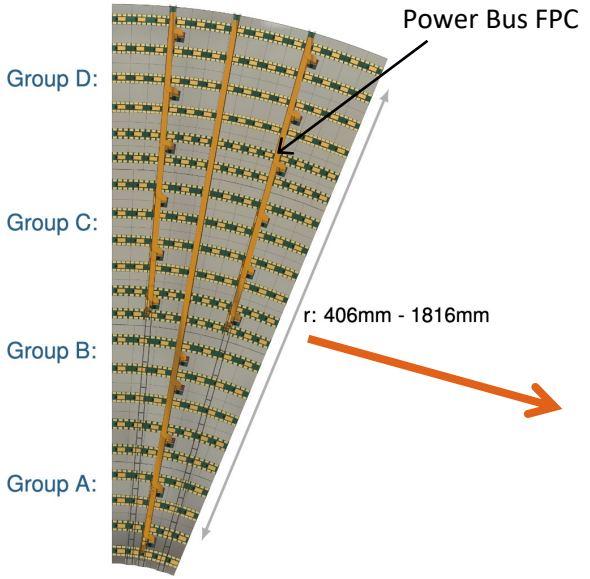
Maximize the use of silicon wafers and masks (only 4 required), and facilitate detector assembly.

OTK Endcap Sensors with Readout Electronics

Group C sensors



1/16 Sector



Endcap (16 sectors) 5.4.3 Readout electronics

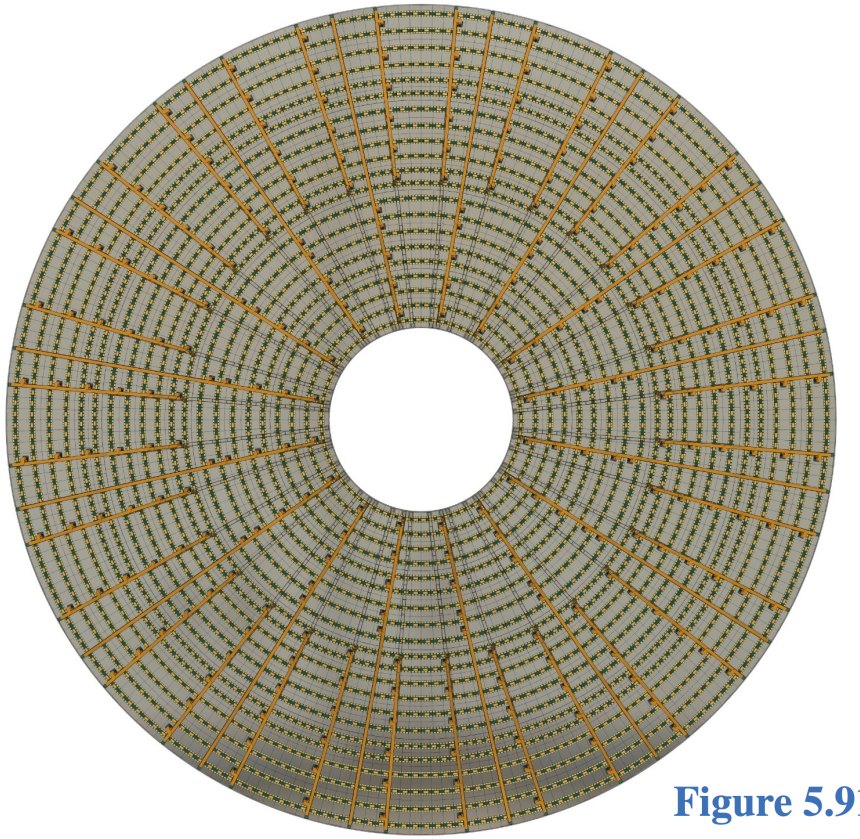


Figure 5.91

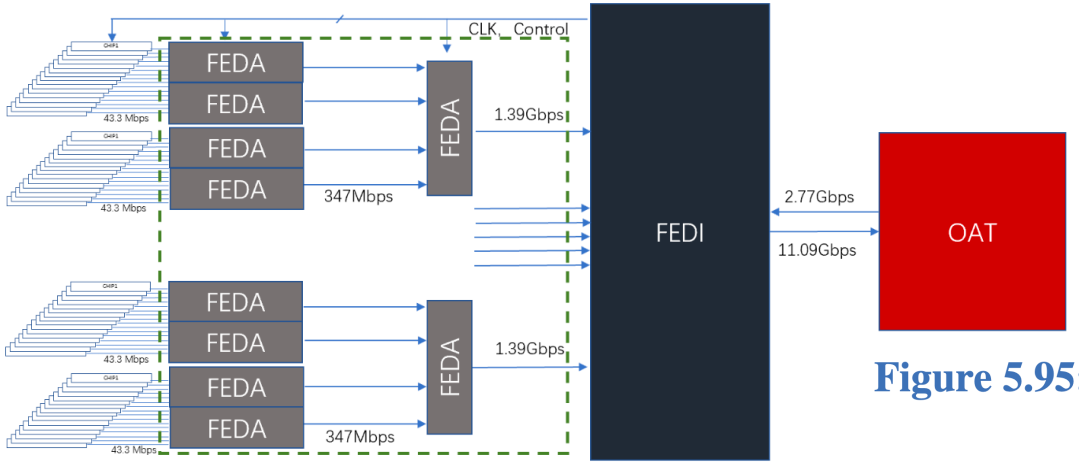


Figure 5.95

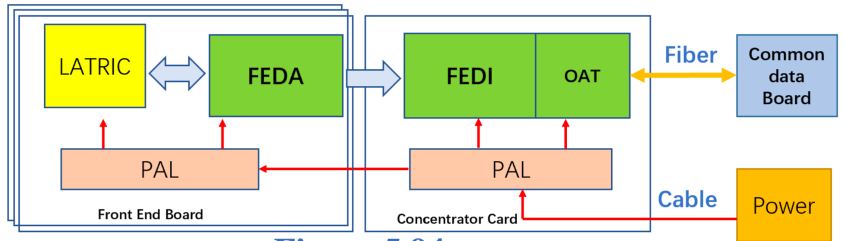
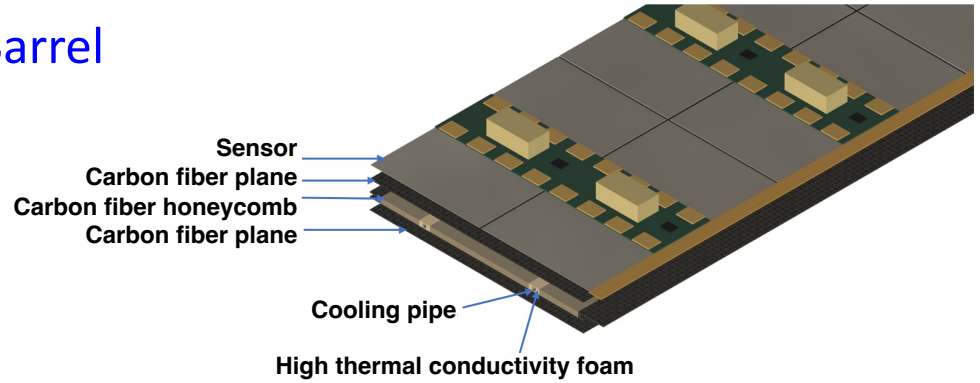


Figure 5.94

Mechanical and Cooling Structure of the OTK

Barrel



5.4.4 Mechanical and cooling design

Stave Installation

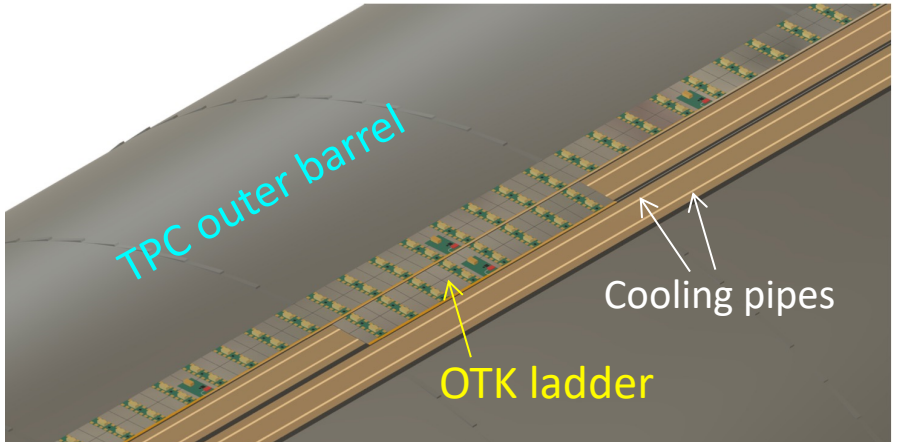


Figure 5.97

Endcap

1/16 OTK endcap sector

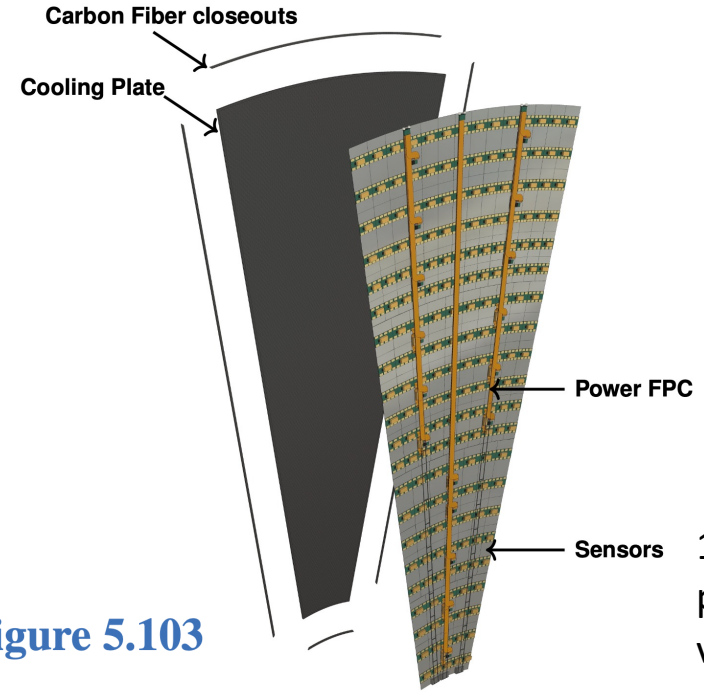


Figure 5.103

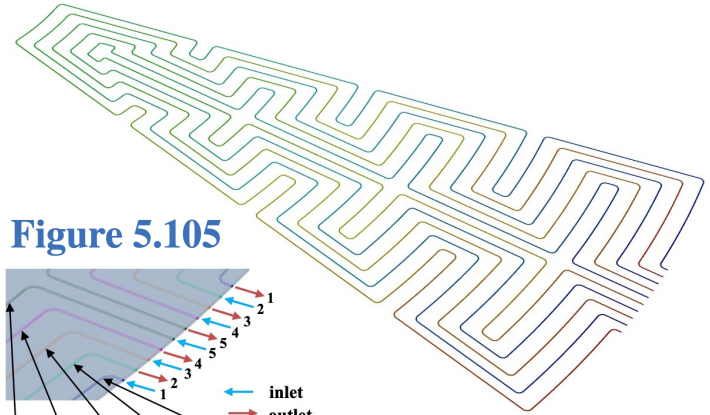
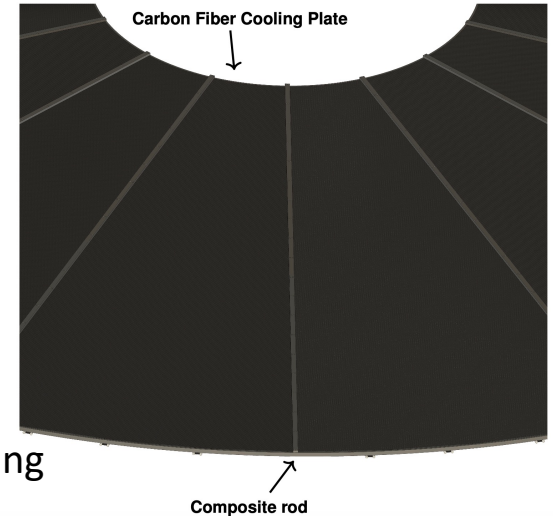


Figure 5.105

1/16 sector of the endcap uses 5-loop water cooling pipes: a pipe inner diameter of 2.3 mm, a flow velocity of 2 m/s, and an inlet temperature of 5°C.



Mounting 1/16 sectors

Mechanical and Thermal Analysis of the OTK

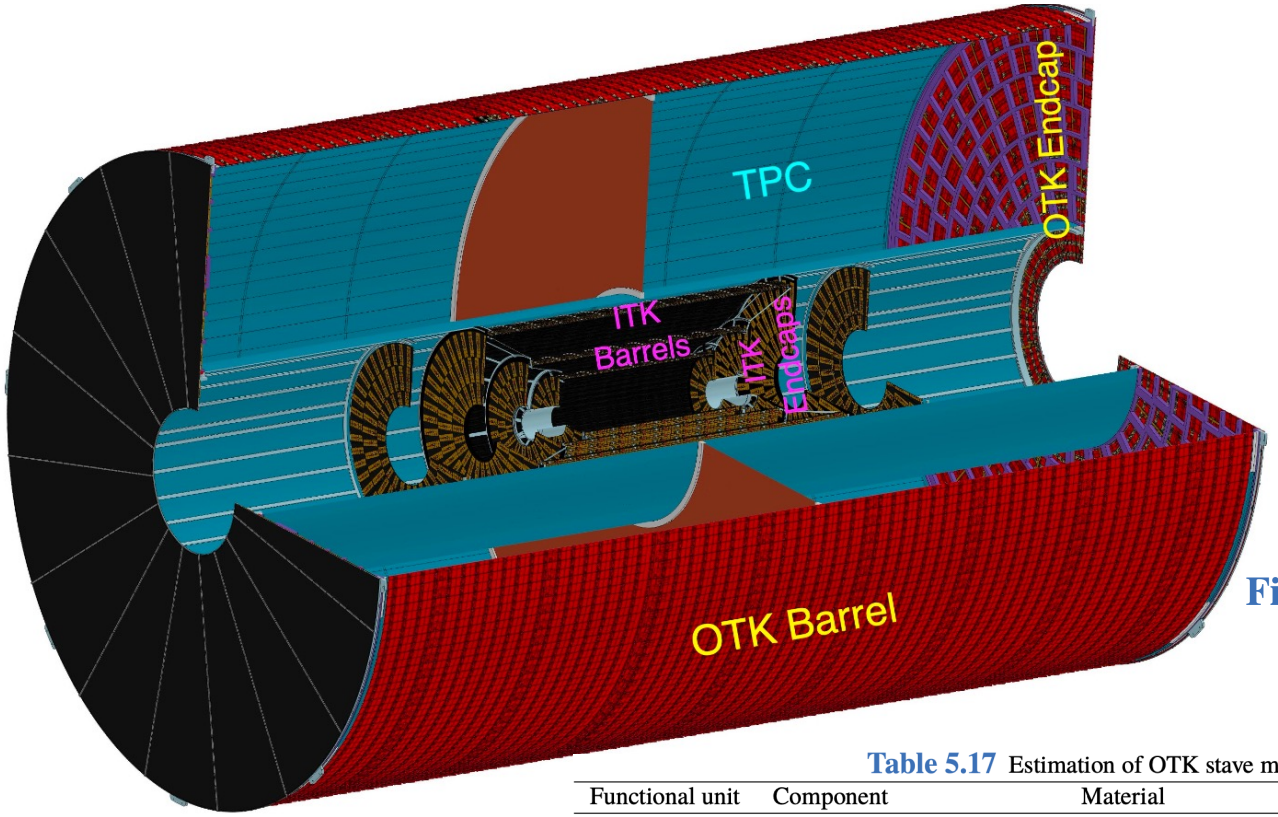


Figure 5.107

5.4.4 Mechanical and cooling design

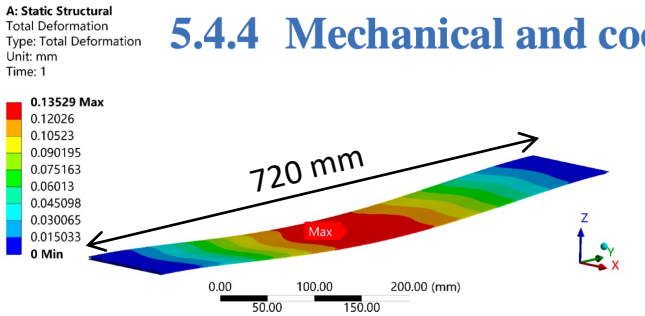


Figure 5.99

Maximum sag for OTK ladder is 135 µm

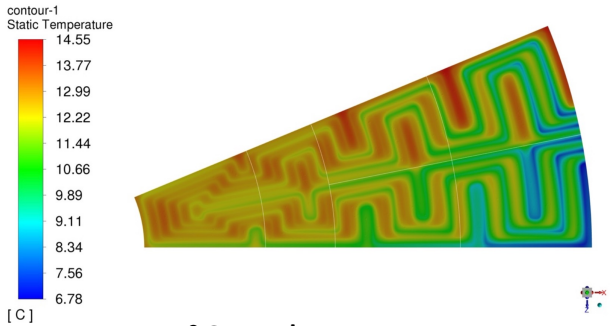


Figure 5.106

Sensor temperature <15°C and senor temperature gradient <4°C
(Heat flux: 300 mW/cm^2)

Table 5.17 Estimation of OTK stave material contributions

Functional unit	Component	Material	Thickness [µm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	PCB metal layers	Cu		1.436	0.200
	PCB Insulating layers	Polyimide		28.41	0.070
	Sensor	Silicon	300	9.369	0.320
	Glue		100	44.37	0.023
	Other electronics				0.100
Structure	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Cooling tube wall	Titanium	200	3.560	0.169
	Cooling fluid	Water		35.76	0.105
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	6000	186	0.322
	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Glue	Cyanate ester resin	200	44.37	0.045
Total					1.584

Estimation of Detector Counting Rate

Table 5.20 Estimated hit rates of the silicon trackers [10^3 Hz/cm^2]

	Low Lumi Z		Higgs		High Lumi Z	
	Average	Max	Average	Max	Average	Max
ITKB1	3.11	4.70	0.592	0.904	24.2	34.8
ITKB2	1.85	4.21	0.438	1.11	13.1	21.2
ITKB3	0.948	1.94	0.265	0.500	5.98	10.2
OTKB	0.617	0.914	0.231	0.346	3.30	4.82
ITKE1	11.2	51.0	2.72	12.1	98.7	487
ITKE2	7.01	41.6	1.89	9.65	50.3	327
ITKE3	3.13	29.0	0.915	7.53	17.6	131
ITKE4	2.23	10.1	0.694	2.52	13.1	59.1
OTKE	0.976	4.00	0.368	1.45	5.45	23.9

The CEPC will operate in different modes: the Z boson mode (91 GeV), the W^+W^- mode (160 GeV), the ZH mode (240 GeV), and the $t\bar{t}$ mode (360 GeV).

In the high-luminosity Z mode, the collision luminosity reaches 192×10^{34} cm^{-2}s^{-1}, with a bunch spacing of 23 nanoseconds. The main contribution to the detector counting rate comes from beam background, and the design of the detector should meet the requirements for high counting rates.

5.7 Beam background estimation

OTK tolerable hit rate

For the AC-LGAD strip sesnor used in the OTK, each fired strip generates 48 bits of data, with an average of ~2 strips firing per hit. Data from 6 or 8 sensor readout ASICs (6 ASICs are used only in specific parts of the OTK endcap) is aggregated by a primary data aggregation chip. In the OTK barrel, 16 primary data aggregation chips (e-links) are connected to a common data link chip (ChiTu) on the second aggregation board, with each primary data aggregation chip connecting via a 346.67 Mbit/s e-link. In the OTK endcap, 10 to 14 primary data aggregation chips (e-links) are connected to a common data link chip on the second aggregation board, with each primary data aggregation chip connecting via a 693.33 Mbit/s or 346.67 Mbit/s e-link.

The supported data rate per sensor readout ASIC is up to 43.33 Mbit/s for the barrel and up to 86.67 Mbit/s for the endcap, corresponding to a maximum hit rate of 8.0×10^4 Hz/cm^2 for the barrel (detector active area ~1.28 cm × 4.4 cm per ASIC) and 2.1×10^5 Hz/cm^2 for the endcap (detector active area ~1.28 cm × 3.3 cm per ASIC). This detector's tolerable hit rate is ~17 times larger than the estimated maximum background hit rate for the OTK barrel (OTKB, 4.82×10^3 Hz/cm^2) and ~9 times larger than that for the OTK endcap at High Lumi Z (OTKE, 23.89×10^3 Hz/cm^2), as summarized in Table 5.20.

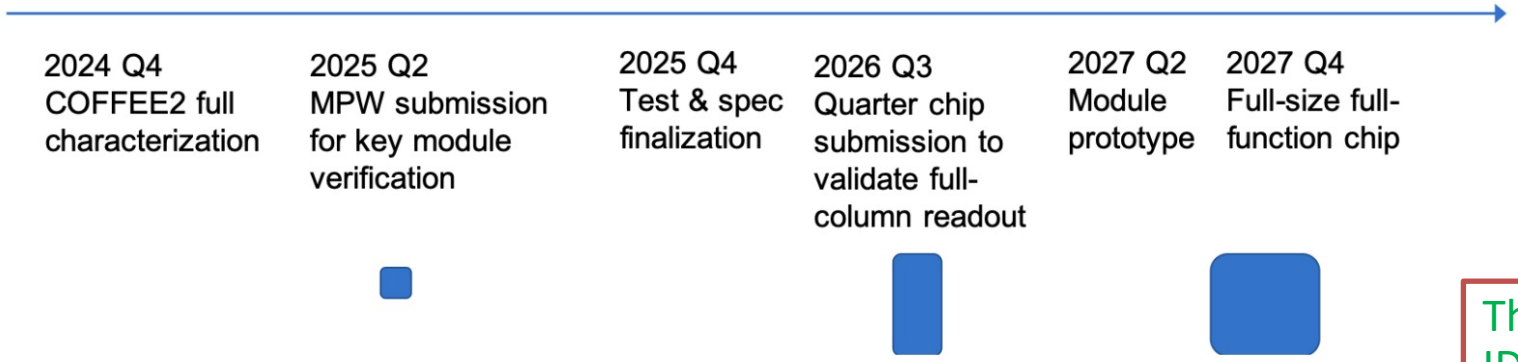
Our Research Team

- Currently active: 27 institutes, 50 staff, and 50+ postdocs & students

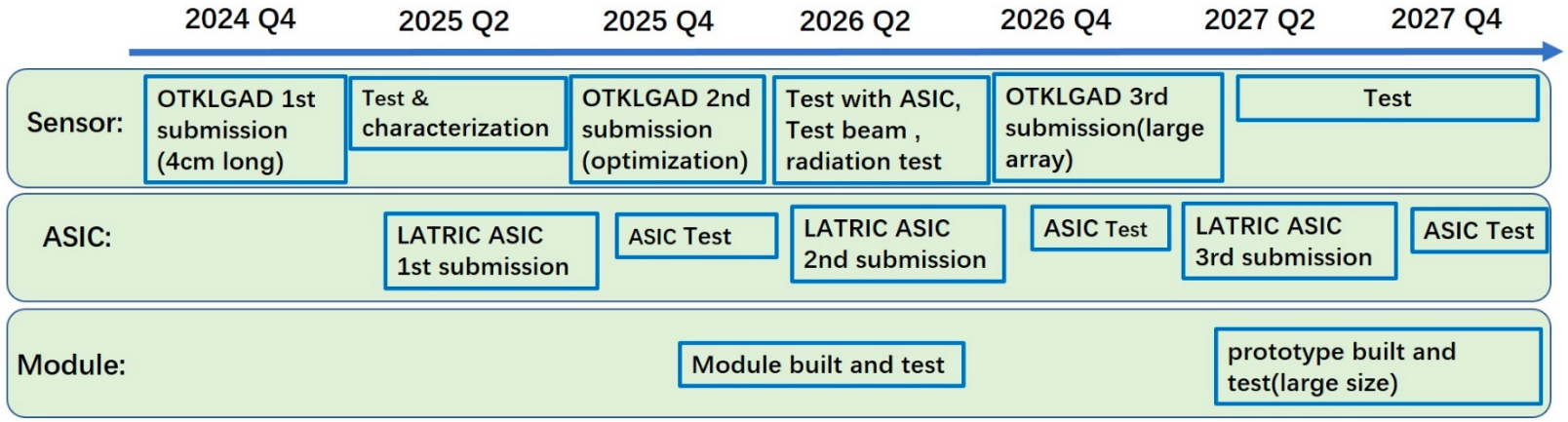
We welcome collaborations with domestic research institutions and industry, as well as international partners.

R&D Plan Following the Ref-TDR

- HV-CMOS pixels:



- AC-LGAD strips+ASIC:



This addresses the IDRC recommendation:

A detailed plan for the development of the ASICs … and seamless integration with the sensors is critical. ASIC development should proceed in parallel with sensor design ...

Development of the mechanical and cooling systems is progressing in parallel, with the goal of delivering a prototype detector by the end of 2027.

Costs

Table 5.21: Costs of the Silicon Trackers (kCHF)

	Inner Silicon Tracker (ITK)	
1.1	CMOS sensor	3,184
1.2	Module electronics	161
1.3	Readout electronics and DAQ	1,097
1.4	Module assembly	946
1.5	Mechanics and cooling	695
	Sub-total	6,083
	Outer Silicon Tracker (OTK)	
2.1	AC-LGAD sensor and readout ASIC	14,341
2.2	Module electronics	469
2.3	Readout electronics and DAQ	2,890
2.4	Module assembly	714
2.5	Mechanics and cooling	2,914
	Sub-total	21,327
	Silicon Tracker common items	
3.1	Common mechanics for Silicon Trackers	1,168
3.2	Detector safety and environmental system	253
3.3	Installation	865
	Sub-total	2,286
Total excluding backend electronics		29,696
	Extra	
4.1	Backend electronics	6,185
Total		35,881

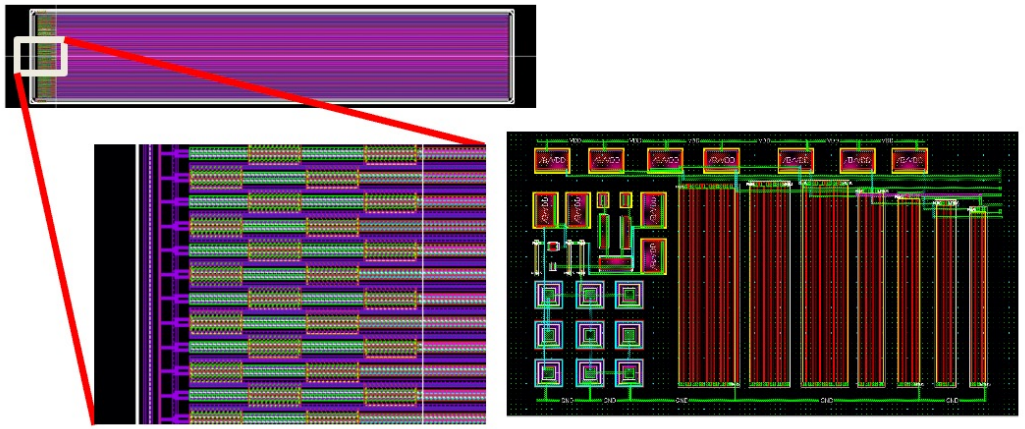
Summary

- The Silicon Tracker is a vital detector system for the CEPC, essential for precise particle trajectory determination and particle identification.
- The ongoing development spans from prototype detector creation to the refinement of the final design, gradually transitioning into the engineering phase.
- Continuous innovations in sensor technology, readout electronics, mechanical design, and the development of the cooling system will ensure that the Silicon Tracker meets the high demanding requirements of CEPC physics. These advancements will enhance tracking performance and contribute to the success of the CEPC project.

Summary of Answers to Review Comments

- There is currently no dedicated effort focused specifically on developing CMOS strip sensors for the Inner Tracker (ITK).

In our upcoming Ref-TDR, we delicate an entire Section to describe efforts for the development CMOS strip sensor. In addition, the tape-out for the first CMOS chip (CSC1) is scheduled in April.



CSC1 chip for CEPC

The design of the strip sensor and ASIC (preamplifier, the 1st stage amplifier, shaper, discriminator, and bandgap) has been completed.

- The 180 nm process may face limited availability in the coming years, presenting a potential risk.

We spoke with the CSMC foundry, and they preliminarily confirmed that 180 nm process will be maintained for a least the next 20 years. In parallel, we also have a plan to migrate to 55 nm or 28 nm, after the functional test of the 180 nm process.

ITK

Comments

- Additionally, integrating readout circuitry within the periphery of strip CMOS sensors is an innovative approach, likely to bring unforeseen challenges.

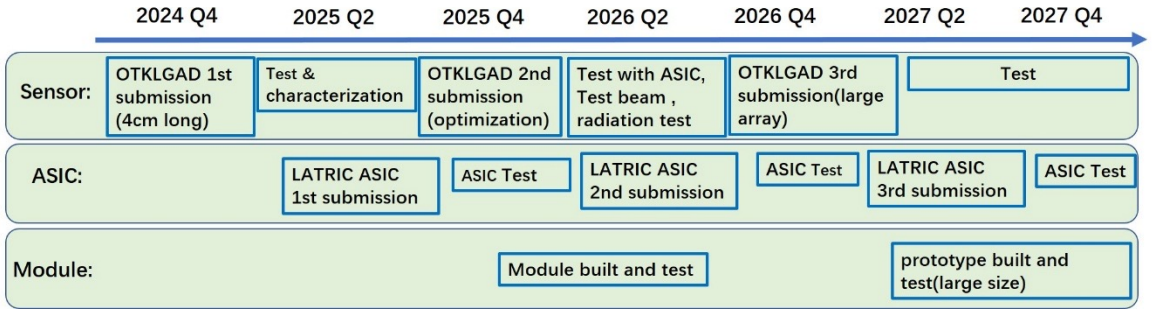
There are no fundamental barriers to the development of readout circuits in the periphery of strip sensors, as the key components for the strip CMOS sensor has already been incorporated into CSC1 design (full wafer). After the CSC1 tape-out, we will have further insights into the details of the readout circuitry and validate the electric isolation design.

Recommendations

OTK

- A detailed plan for the development of the ASICs for both CMOS strips and AC-LGAD (for OTK in this case) is essential. Given the demanding R&D timelines for these low-dissipation, high-time-resolution technologies, careful optimization of power consumption, timing precision, and seamless integration with the sensors is critical. ASIC development should proceed in parallel with sensor design. The process of designing, fabricating, and testing these ASICs is time-intensive, often requiring multiple iterations to achieve the desired performance. Any delays in this pipeline risk cascading effects on the broader project schedule.

We fully agree on the importance of having a detailed plan for the development of ASICs for both CMOS strips and AC-LGAD. To ensure that ASIC development aligns with sensor design, we have established parallel development tracks for both ASICs and sensors, as outlined in the development of AC-LGAD schedule for the next 3 years:



We are also leveraging existing R&D work to accelerate the process. Our ASIC development team has prior experience in developing high-performance time measurement ASICs, such as FPMROC. Many key design components from these previous projects are incorporated into the current ASIC design (Page 12), helping to shorten the development timeline.

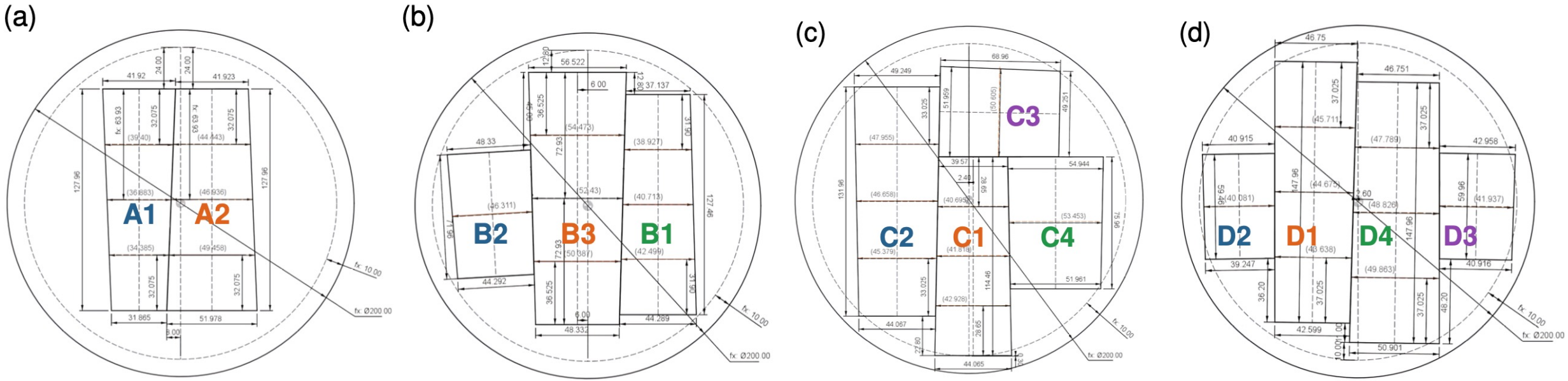
Given the time-intensive nature of ASIC design, fabrication, and testing, we conduct regular reviews and maintain close coordination between the various ASIC teams and sensor teams to mitigate potential risks, ensuring smooth progress and preventing delays that could impact the broader project timeline.

Comments (1)

OTK

- The large variety of sensor designs required for the endcap adds complexity to the construction process.

The complexity of OTK endcap construction has been carefully considered in the design. With dimensions ranging from 406 mm to 1,816 mm in radius, the OTK endcap is quite substantial (covering 10 m^2 per endcap). To simplify sensor production and assembly, the current design uses only 4 masks for the silicon wafers, with trapezoidal-shaped sensors (Page 19). This approach reduces the complexity of sensor production and assembly, as well as the costs, while ensuring effective full detector coverage.



Comments (2)

OTK

- Radiation damage may affect electron discharge through the n+ layer, potentially altering sensor performance over the detector's lifespan.

The devices used in the ATLAS High-Granularity Timing Detector (HGTD) are DC-LGADs, optimized for n+ layer depth and carbon doping, with a primary focus on achieving high tolerance to both Total Ionizing Dose (TID) and Non-Ionizing Energy Loss (NIEL). These sensors have demonstrated sufficient capability to operate in the high-radiation environment of proton-proton collisions, as confirmed by both TID and neutron irradiation tests.

For electron-positron colliders such as the CEPC, the radiation environment is significantly more favorable, particularly for the OTK with its low hit rate (Page 23). Our estimates show that the expected NIEL in the OTK is $<10^{10}$ n_{eq}/cm^2 and the TID is <0.1 kGy over the full CEPC operational lifetime. For the AC-LGAD sensors used in the OTK, the dominant radiation effect could from TID-induced surface damage, which leads to charge accumulation near the n^+ region and dielectric layers, potentially affecting performance, as noted by the Referee.

We have conducted dedicated studies on the TID tolerance of AC-LGADs. Existing strip-type AC-LGAD devices with a strip length of 5.65 mm were irradiated using an X-ray source at various doses (500 Gy, 1 kGy, 10 kGy, 100 kGy, and up to 1 MGy), and subsequently characterized through IV, CV, and timing/position resolution measurements. At a TID dose of 1 kGy, a slight increase in leakage current was observed, but the device maintained its timing and position resolution. These results indicate that AC-LGAD sensors, with TID levels <0.1 kGy, are expected to provide reliable performance throughout the full lifetime of the detector.

Comments (2)

- Sensors may have high capacitance (up to ~10 pF), which could impact noise jitter and rise time, making it challenging to achieve the desired time resolution.

We appreciate the referee's concern. Indeed, the relationship between time resolution and capacitance requires further study. To address this, we plan to tape out several prototypes in the coming years to explore this effect more thoroughly. Additionally, our latest sensor design includes options to reduce capacitance, such as increasing the thickness of the EPI layer or introducing an isolated structure (Page 12).

- The operation of AC-LGADs may be susceptible to effects from high particle rates, which should be thoroughly understood, especially regarding the size of the LGADs.

In our Ref-TDR, we have a dedicated section discussing the estimated particle rates in the ITK and OTK. The highest OTK anticipated hit rate during operation at CEPC (High Lum Z) is ~10^3 hits/cm^2/s (Page 23). For a sensor with dimensions of ~4 cm×5 cm, if a hit has already occurred, the probability of having a second hit within the same LGAD sensor and within sensor's charge collection window (~2 ns) is <10^{-4}, which should not pose any issues.

Comments (3)

OTK

- With the specified pitch and thickness, a charge-sharing mechanism is expected to enhance position resolution; however, this should be carefully evaluated for different electrode dimensions, considering potential gain layer variations across the detector.

Our latest AC-LGAD tape-out includes a range of electrode width and pitch size variations to study their effects on charge sharing and position resolution. Specifically, the electrode widths are 25, 50, and 100 μm, and the pitch sizes are 100, 200, and 500 μm (Page 12). The optimal electrode dimensions will be determined based on the test results. And a comprehensive discussion is provided in our Ref-TDR.

Gain layer variation is indeed an important factor. Significant differences in gain between adjacent strips can affect the accuracy of hit position reconstruction. However, such non-uniformities can be corrected through offline calibration, as demonstrated in "Nucl. Instrum. Methods Phys. Res. A **869**, 29 (2017)". To further improve gain uniformity, we are also working to enhance process control during fabrication. Our team is establishing cooperations with other semiconductor foundries to explore more advanced and stable production capabilities.

- The localized power dissipation at the ASIC level should be factored into the cooling design and overall performance assessment.

We appreciate referees' suggestion. Localized power dissipation at the ASIC has been considered in our cooling design, including the use of thermal vias in PCBs.

Recommendations (1)

OTK

1. Reevaluate the size of the AC-LGADs, carefully balancing performance factors—such as rate effects, time resolution, and achievable position accuracy—with expected manufacturing yield to arrive at a cost-effective solution.

We appreciate the referees' suggestion. Considering the various factors mentioned, along with the evolution of detector technology, we have reduced the sensor size to ~4 cm x 5 cm in the baseline design (Page 18), while accommodating the 2 cm x 2 cm size as a backup for the OTK in the Ref-TDR (Section 5.4.2.3).

In our latest AC-LGAD tape-out, we have already included sensor with various strip lengths and overall dimensions (Page 12). These will be evaluated systematically in terms of timing resolution, position accuracy, and yield. The sensor design will be further refined based on the test results. In parallel, we are working to improve process control during fabrication to enhance sensor quality.

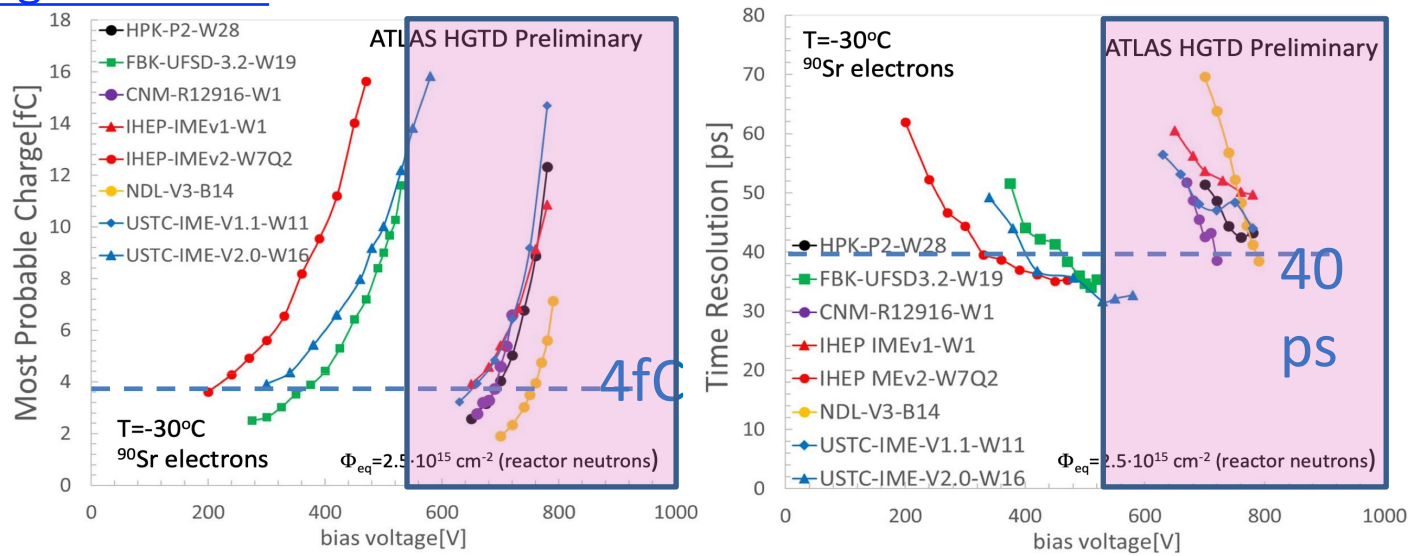
Given the CEPC project timeline of over 5 years from construction, the project remains flexible enough to adjust its technical approach and has robust backup plans in place for the engineering phase.

Recommendations (2)

OTK

2. Determine if redundancy is needed in the OTK barrel system.

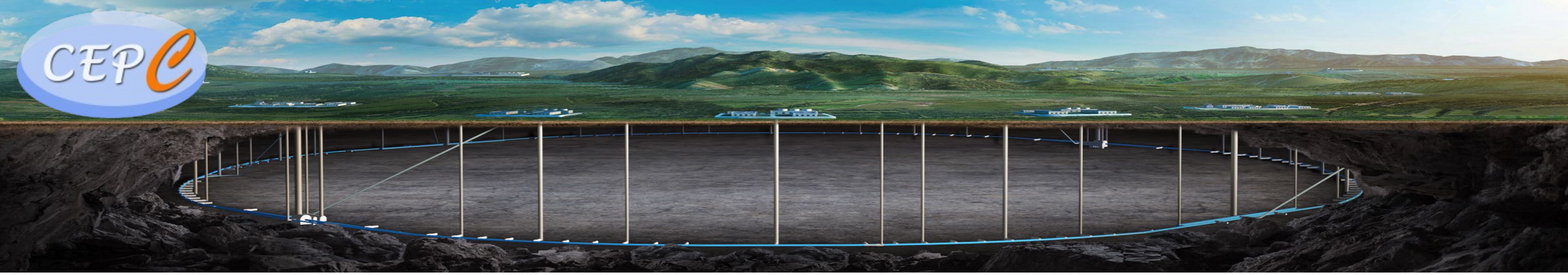
The necessity of redundancy in the OTK system has been carefully assessed. Recent advancements in LGAD technology by IHEP-IME have shown significant progress. These sensors used in the ATLAS HGTD, have exhibited good charge and timing resolution even after irradiation to a fluence of 2.5×10^{15} n_{eq}/cm^2, as illustrated in the figure below:



Furthermore, recent irradiation tests on AC-LGAD sensors by C. Bishop *et al.* from BNL and UCSC at a fluence of 1×10^{14} n_{eq}/cm^2 showed only a minor impact on performance. Considering the expected fluence in the OTK is $<10^{10}$ n_{eq}/cm^2 (and TID <0.1 kGy) over the full CEPC operational lifetime, AC-LGAD sensors are expected to maintain reliable performance throughout the detector's lifetime.

In addition, the OTK mechanical and electrical design features a modular structure. The barrel consists of 880 ladders, while each endcap is divided into 16 replaceable sectors (Page 21). This design ensures convenient maintenance when necessary, providing a substantial safety margin and enhancing the system's operational reliability.

The combination of robust sensor performance and the flexibility of the modular design ensures sufficient system reliability. Further redundancy measures are not deemed necessary for the OTK system.



Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

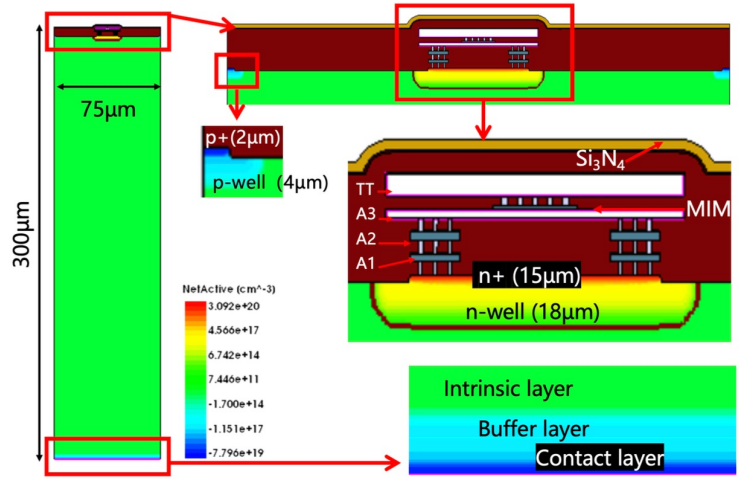
Technology Survey and Backup Choice for ITK

5.3.1.2 CMOS strip R&D

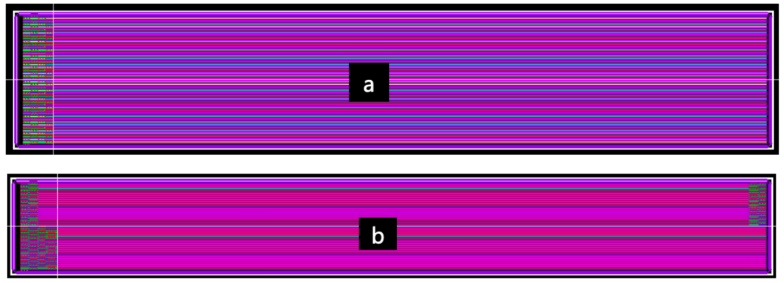
- CMOS strips compared with CMOS pixels:
  - Simpler readout with a relatively lower technical barrier for development.
  - Comparable spatial resolution, suitable for high charge resolution and a large dynamic range.

- Key parameters of CMOS Strip Chip (CSC) for CEPC :
  - Process node: 180 nm
  - Chip size: 2 cm × 2 cm
  - Strip number per chip: 1024
  - Strip pitch: 20 μm
  - Spatial resolution: 5 μm
  - Time resolution: 3 ns

Figure 5.25

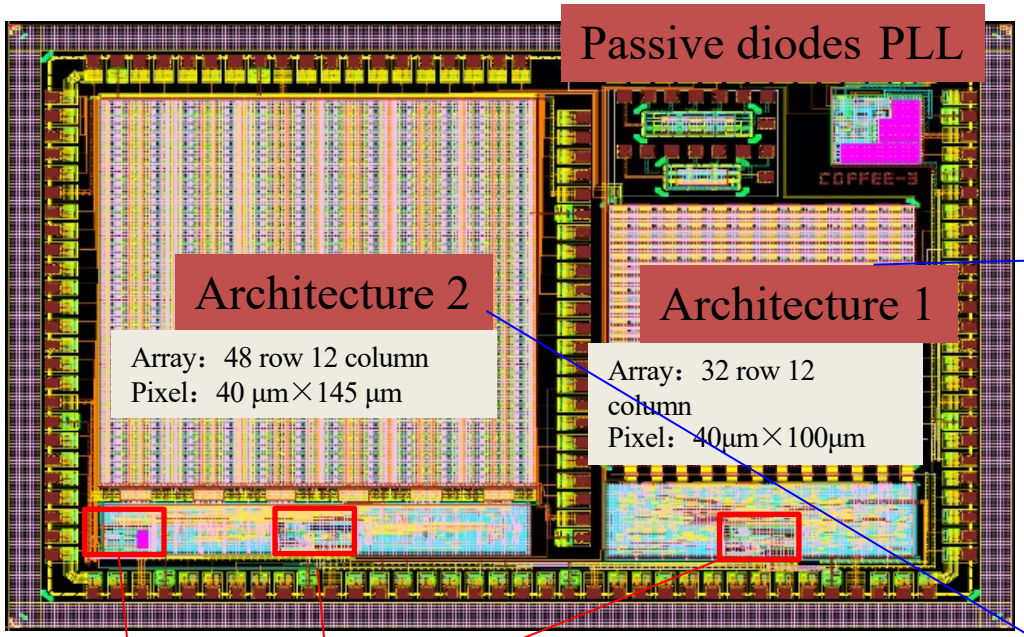


- HV-CMOS as ITK baseline and CMOS strip as backup:
  - Compared to the HV-CMOS pixels, the CMOS strips for the ITK offers comparable and slightly better intrinsic spatial resolution.
  - However, achieving a 3D detector requires twice the number of strip sensors, which increases the overall detector material.
  - Considering the trade-off among intrinsic spatial resolution, detector material, and technology maturity, the CMOS strip sensor is used as a backup option for the HV-CMOS pixel sensor.



CSC1 chip for CEPC

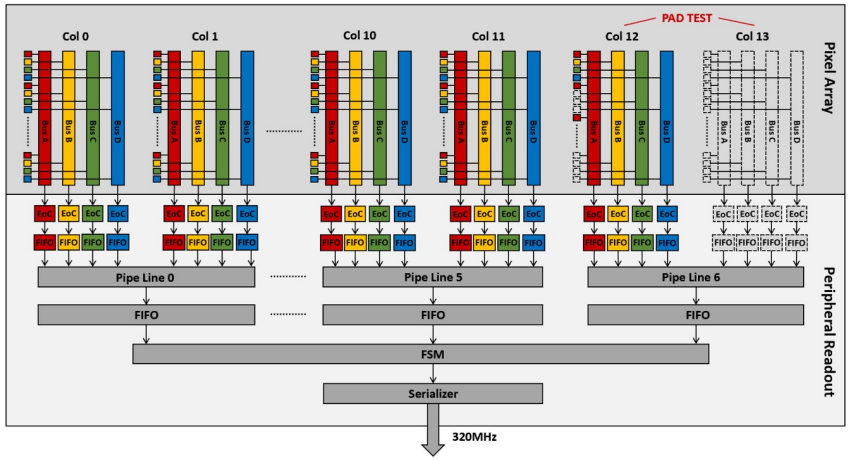
Progress on COFFEE3 Development



DLL LVDS driver/receiver up to 1.28Gb/s

- In-pixel Coarse-fine TDC and 4-bit threshold tuning;
- ToA and ToT information are saved in each pixel;
- Data-driven readout;

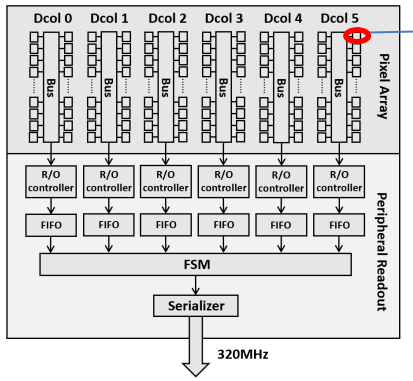
Architecture 1： NMOS Pixel Array Schematic Diagram

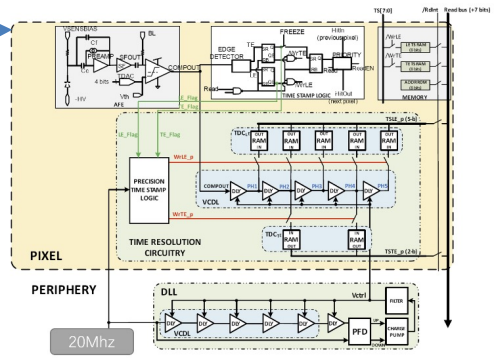


LVDS driver/receiver up to 1.28Gb/s

- In-pixel NMOS based comparator, in-pixel 4-bit DAC for threshold tuning;
- Time information （TOA, TOT…）and data formation in the end of each column;
- Improved capability to manage high incident conditions;

Architecture 2: an improved solution, fully utilize the advantages of the 55 nm process node



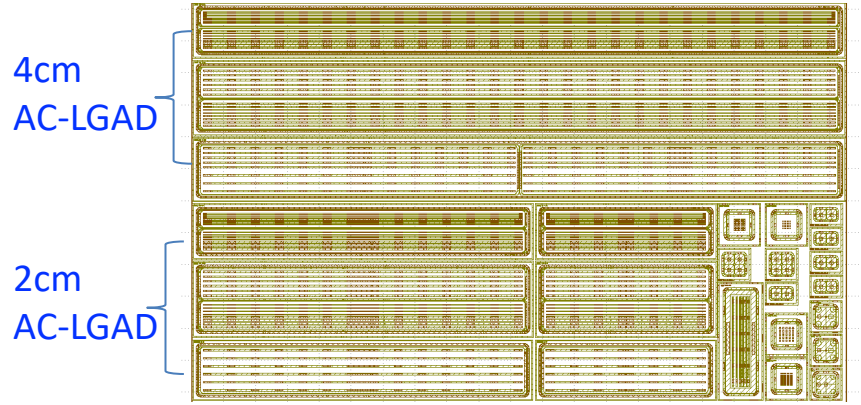


LVDS driver/receiver up to 1.28Gb/s

Progress after 2024 IDRC Review (2)

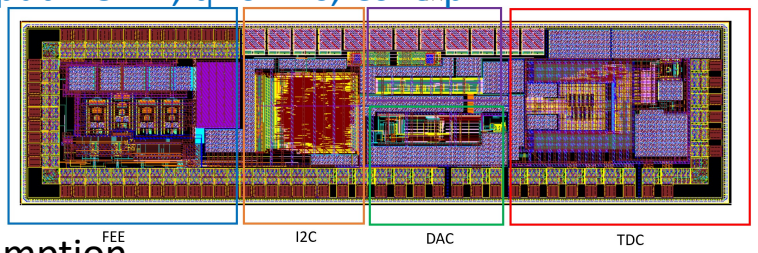
- New IHEP AC-LGAD strip sensor prototype: summitted for tap-out in Feb 2025. The new layout and design include:
  - Strip lengths： 1 cm, 2 cm, and 4 cm
  - Strip pitch sizes: 100 µm, 200 µm, and 500 µm
  - Optimized isolated structure design to reduce sensor capacitance
  - Process design optimization (n+ layer dose) for better spatial resolution

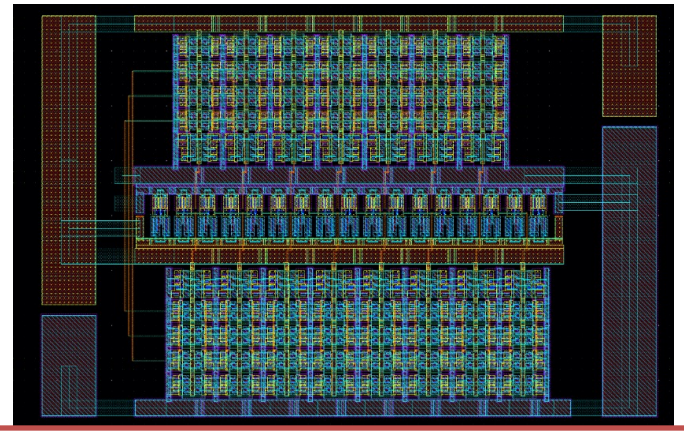
This study addresses the IDRC comment:
- Reevaluate the size of the AC-LGADs, carefully balancing performance factors—such as rate effects, time resolution, and achievable position accuracy …



1cm AC-LGAD

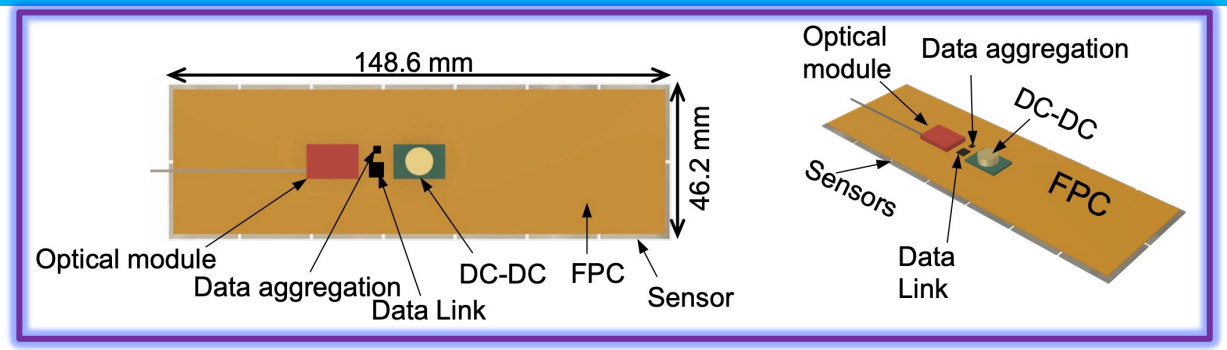
- Pre-phototype for AC-LGAD ASIC (LATRIC): designed has been completed and is schedule for submission in April.
  - Several key elements in the design are shared and verified with FPMROC (10 ps) chip
    - FEE: Preamplifier+Discriminator: jitter<7.8ps @ input 2.5mV, t_r=0.1ns, Cs=0 pF
    - PLL, Serializer, SPI is verified
  - I2C Slave: ASIC parameter configuration
  - 12-bit DAC: threshold and calibration
  - TDC design:
    - Event driven delay line to reduce the power consumption
    - Real time Calibration for PVT (Process, Voltage, Temperature)
    - LSB ~36 ps based on preliminary layout post-simulation
    - Power consumption： average current for single event:

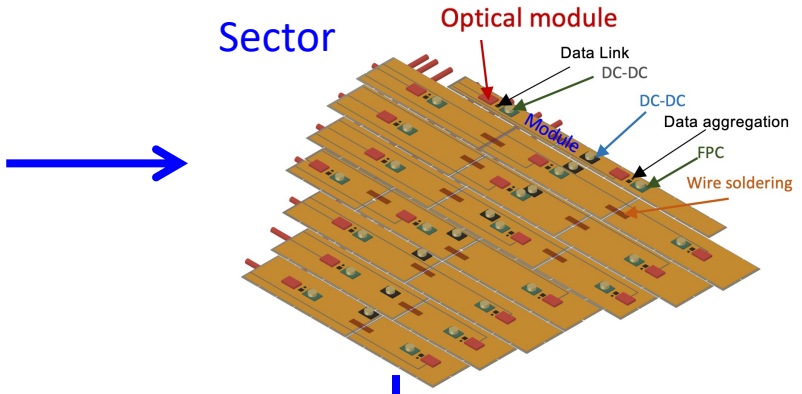




This study addresses the IDRC comment:
- Reevaluate the size of the AC-LGADs, carefully balancing performa
such as rate effects, time resolution, and achievable position accura

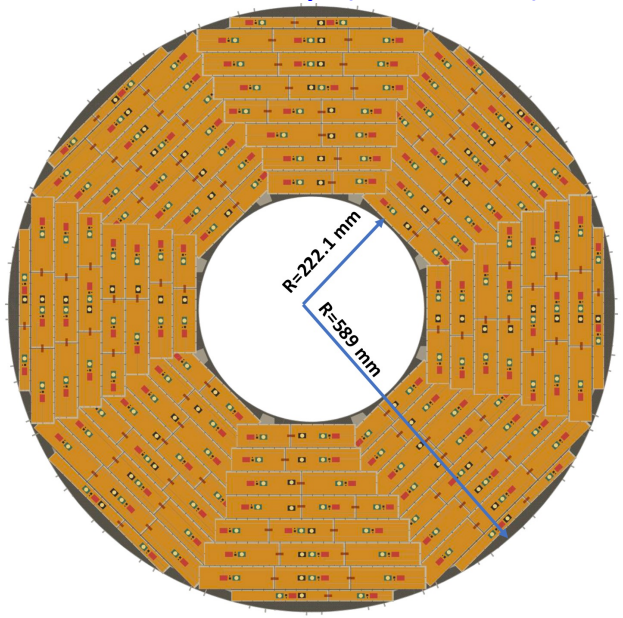
Alternative ITK Endcap Design with CMOS Strips

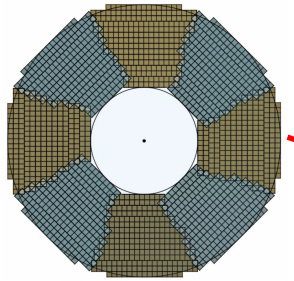




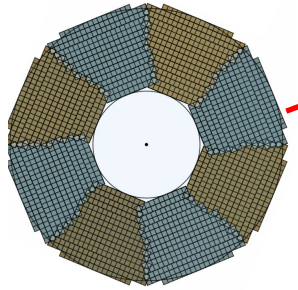
- CMOS Strip Chip (CSC) for CEPC:
  - Chip size: 20 mm × 20 mm
  - Strip pitch size: 20 μm (spatial resolution 5 μm)

Half Endcap (8 sectors)

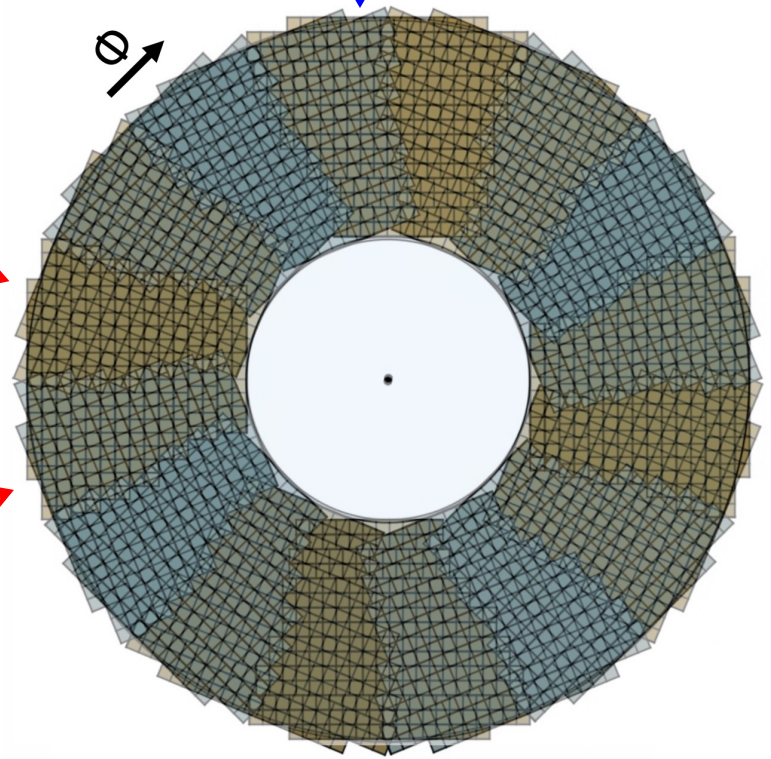


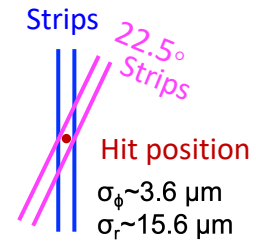


Normal half endcap



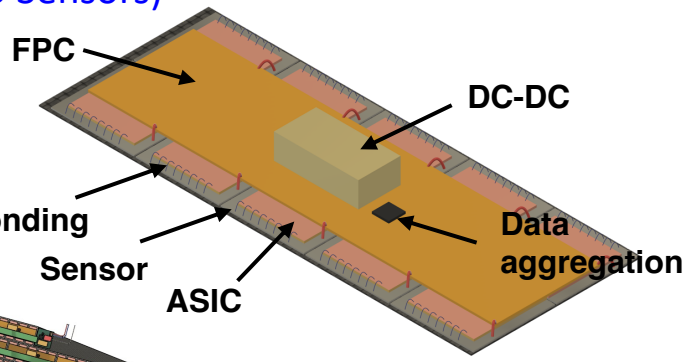
22.5◦ half endcap

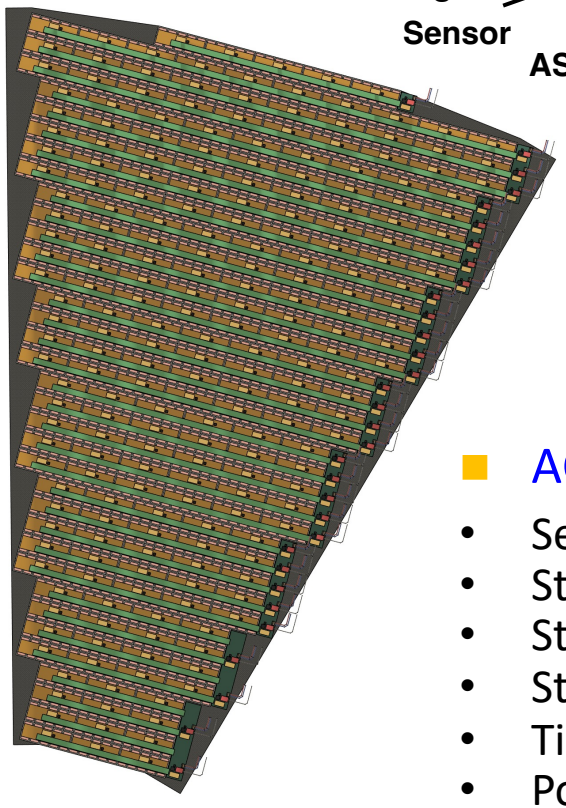




OTK Backup Design

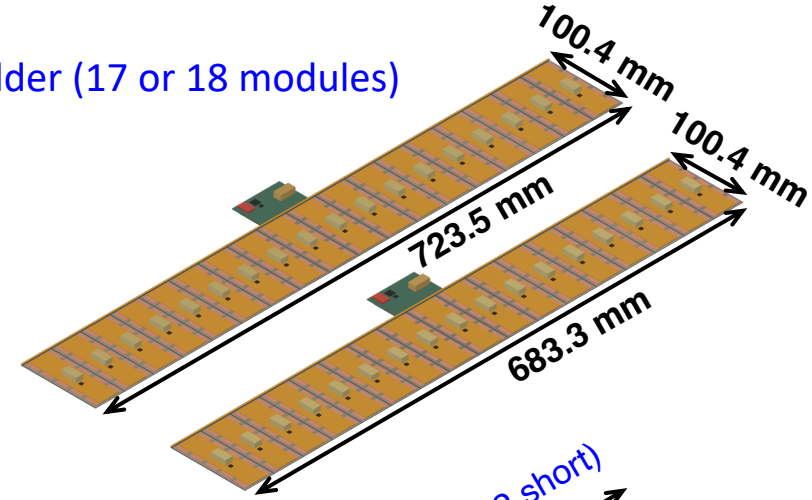
Module (2×5 Sensors)

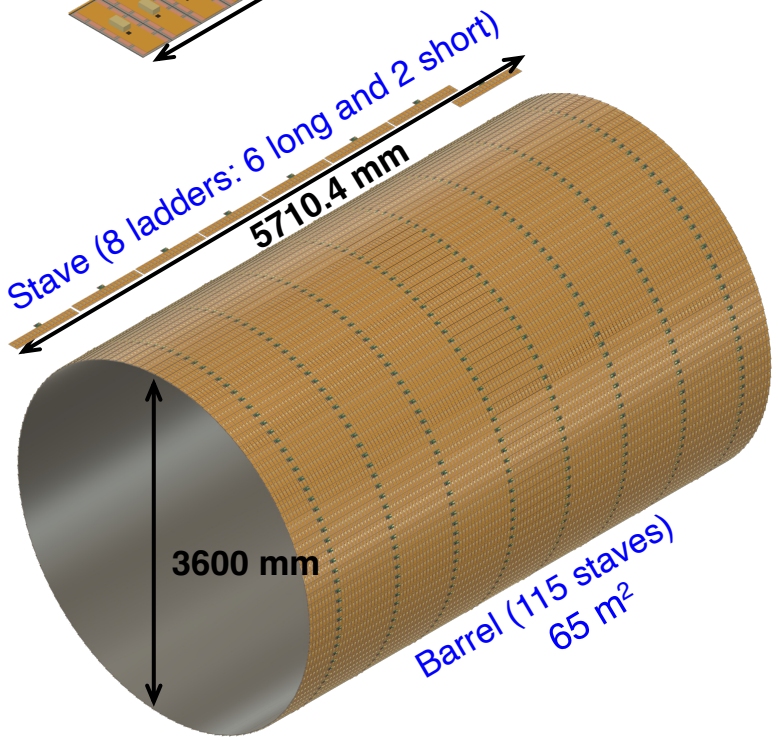




1/12 Endcap Sector

Ladder (17 or 18 modules)





- AC-LGAD strip sensor:
  - Sensor size: 20 mm × 20 mm
  - Strip length: 19.4 mm
  - Strip number: 128
  - Strip pitch: 151.6 μm
  - Time resolution: 50 ps
  - Power consumption: 300 mW/cm²

Simulation of the Tracker Performance

Momentum resolution in the barrel region:

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{Si}} = ap_t \oplus \frac{b}{\beta\sqrt{\sin\theta}}$$

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{TPC}} = as_1 p_t \oplus \frac{bs_2}{\beta\sqrt{\sin\theta}}$$

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{Combined}} = \frac{1}{\sqrt{\left(\frac{\sigma_{p_t}}{p_t}\right)^{-2}_{\text{Si}} + \left(\frac{\sigma_{p_t}}{p_t}\right)^{-2}_{\text{TPC}}}}$$

where $a = 1.5 \times 10^{-5}$, $b = 1.4 \times 10^{-3}$, $s_1 \approx 6$, and $s_2 \approx 0.8$.

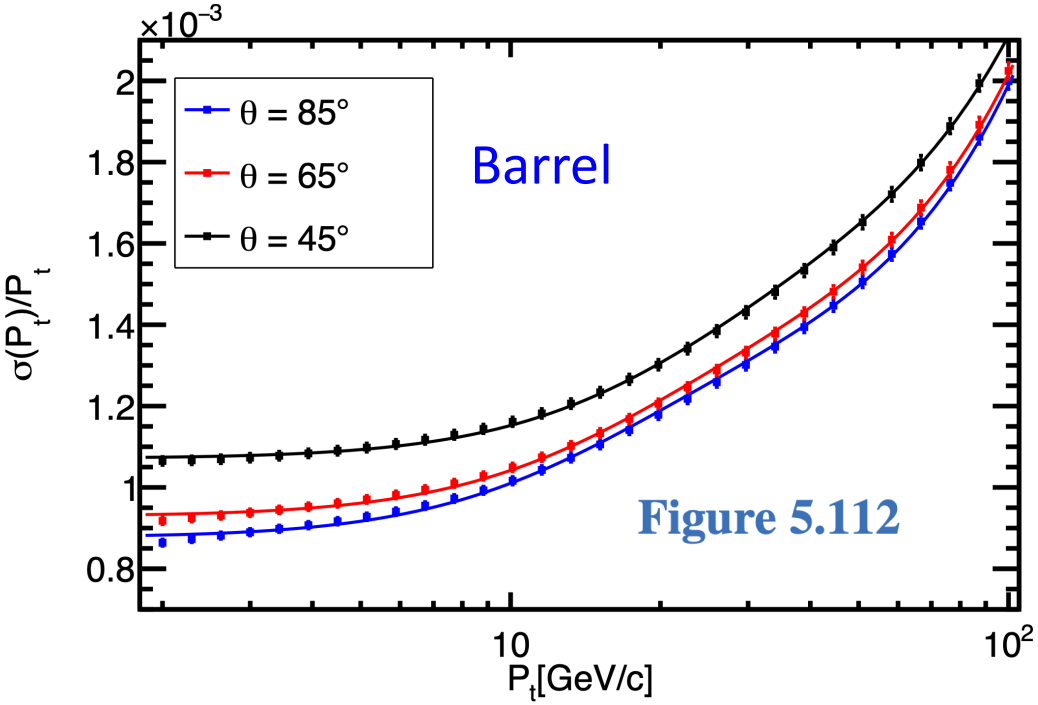
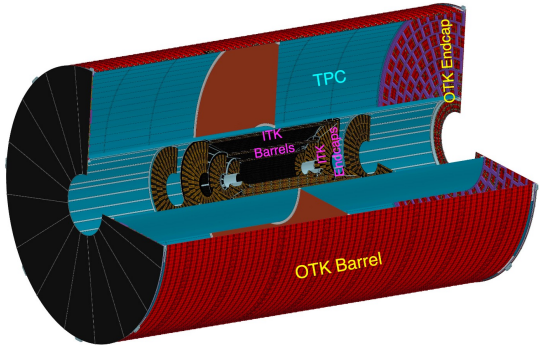


Figure 5.112

5.8 Performance

Systematic understanding of the tracker design and its performance



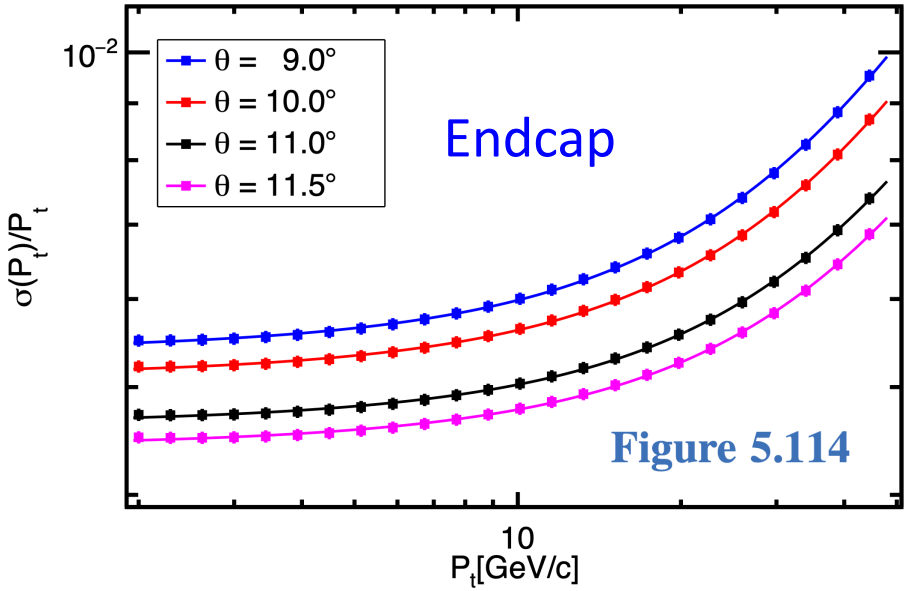


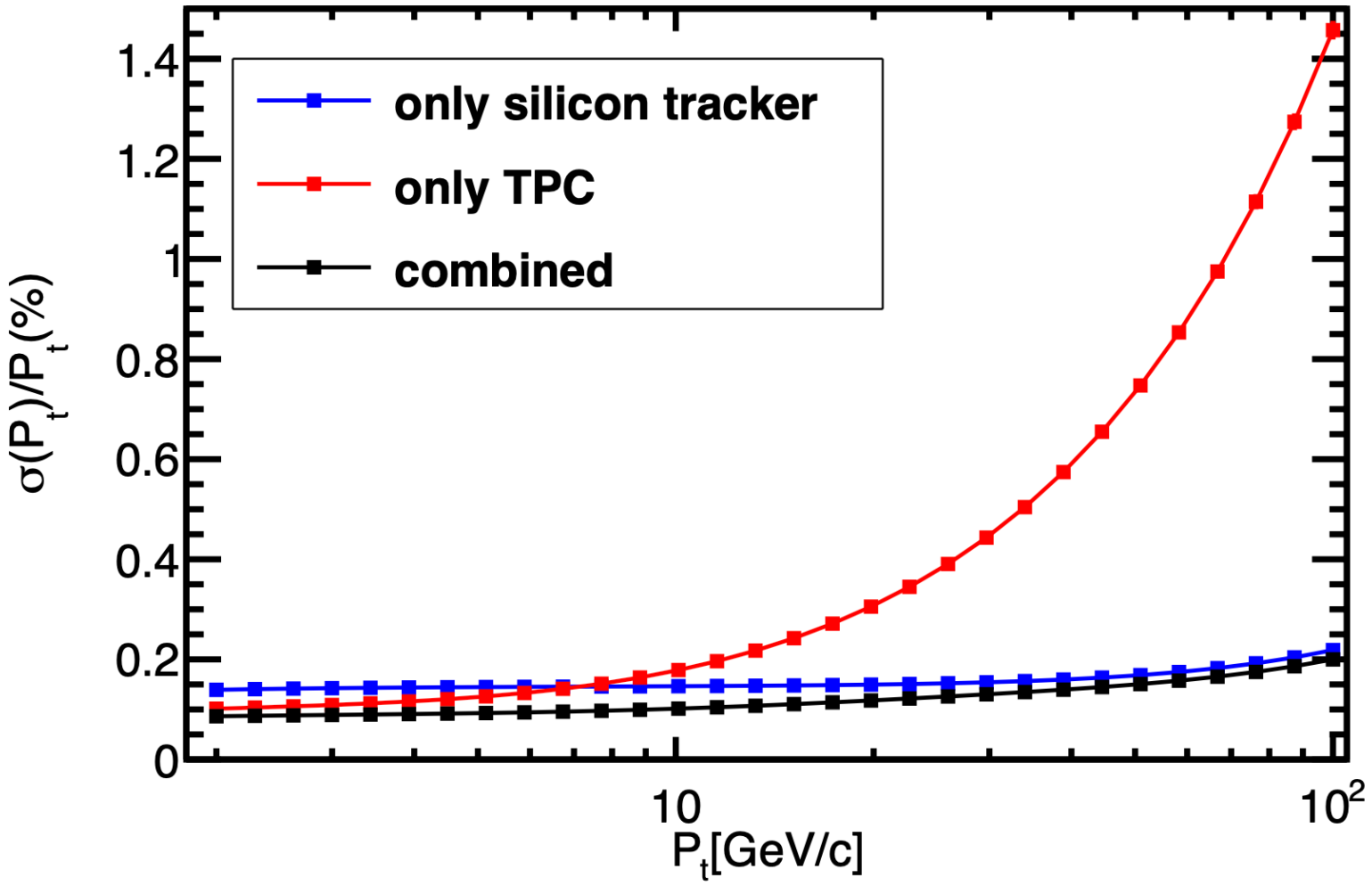
Figure 5.114

Momentum resolution in the endcap region:

$$\frac{\sigma_{p_t}}{p_t} = \frac{a' p_t}{(tan\theta)^2} \oplus \frac{b'}{\beta tan\theta\sqrt{\cos\theta}} \oplus \frac{c'\sqrt{p_t}}{\sqrt{\beta}(\tan\theta)^{\frac{3}{2}}(\cos\theta)^{\frac{1}{4}}}$$

where $a' \approx 0.4 \times 10^{-5}$, $b' \approx 0.9 \times 10^{-3}$, and $c' = 4.5 \times 10^{-5}$.

Momentum Resolution



PID Performance