2025 MicroTCA/ATCA International Workshop
for Large Scientific Facility Control

Programs

ORGANIZER: CHONGQING UNIVERSITY (CQU)

SEP.15-SEP.17, 2025   CHONGQING, CHINA

2025 MicroTCA/ATCA International Workshop For Large Scientific Facility Control

2025 MicroTCA/ATCA International Workshop for Large Scientific Facility Control will be hosted by Chongqing University (CQU), in Chongqing, China on Sep.15-Sep.17, 2025. The workshop will be held on-site and online at the same time.

The workshop promotes and coordinates the development of MicroTCA/ATCA standards and systems in China and East Asia, especially in data acquisition, digital signal processing, measurements, instrumentations, controls, and analog circuit (Microwave/RF) applications in research facilities and industry. The workshop also provides a platform to discuss technologies and collaborations.

The workshop's main topics include:

- Applications in research facilities (accelerators, high energy physics, plasma, fusion, laser, photon beamlines, etc.)
- Applications in industry
- New products
- New technologies
- Future of standard and interoperability
- Software and firmware
- Industry exhibition - presentation of modules and systems from industry and research

Organization

Program Committee

Bocheng Jiang (Chair)	CQU
Holger Schlarb (Co-chair)	DESY
Bo Liu (Co-chair)	SARI
Paul Chu (Co-chair)	NJU/Suzhou Lab
Rong Liu	BNU
Zeran Zhou	USTC
Xinpeng Ma	IHEP
Lei Shi	IASF
Hongrui Cao	ASIPP
Junqiang Zhang	CQU
Min li	IMP
Fang Liu	IHEP

Local Organizing Committee

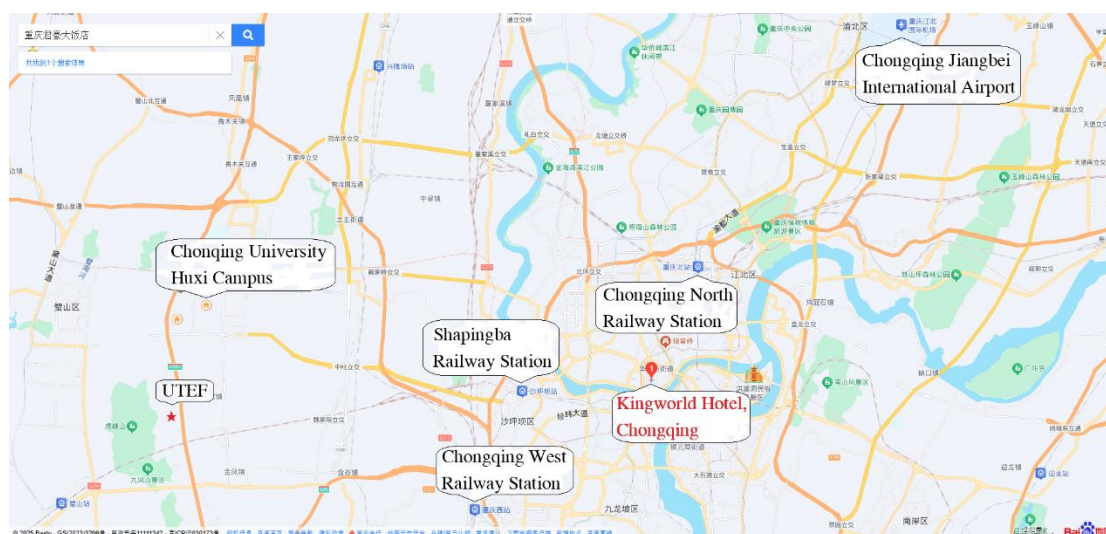|	
Junqiang Zhang (Chair)	CQU
Zhongquan Li (Co-chair)	CQU
Chen Zhang	CQU
Yuting Qian	CQU
Lingxi Ye	CQU
Ziyang Xu	CQU
Xue Yang	CQU

Venue Location

Kingworld Hotel, Chongqing, China (重庆君豪大饭店).

Registration

Sep. 14 14:00-20:00, Kingworld Hotel
Sep. 15 8:00-18:00, Kingworld Hotel

Transportation and Accommodation

Workshop participants are recommended to stay at the Kingworld Hotel, which serves as the main venue hotel. Some alternative hotels near the main venue have also been listed below for your reference.

I. Kingworld Hotel, Chongqing
■ Address: No. 9 Jinyuan Road, Jiangbei District, Chongqing, China
■ Telephone: 023-86338888

2. Seeker boutique Hotel (Chongqing Jiangbei Technology and Business University Branch)
■ Address: No. 70, Building 62, Eshibao Hill, Jinyuan Road, Jiangbei District, Chongqing
■ Telephone: 023-88516509

3. JI Hotel (Chongqing Century Golden Resource Shopping Center Branch)
■ Address: No. 23-24, Building 62, Eshibao Hill, Jinyuan Road, Jiangbei District, Chongqing
■ Telephone: 15703061082

4. Home Inn (Chongqing Century Golden Resource Shopping Center Branch)

- Address: No. 26, Building 62, Eshibao Hill, Jinyuan Road, Jiangbei District, Chongqing
- Telephone: 023-88163366-9

Meals and Banquet

Sep. 15	Lunch	Kingworld Hotel
Sep. 15	Dinner	Kingworld Hotel
Sep. 16	Lunch	Kingworld Hotel
Sep. 16	Banquet	Jingxige Hotpot
Sep. 17	Lunch	Kingworld Hotel

Contact Information

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Organizer

Chongqing University

Workshop agenda

September 15, 2025

| Time	Title	Speaker	Host
09:00 - 09:15	Tutorial Welcome	Rong Liu	Rong Liu
09:15 - 09:45	LHX Liquid Cooling Solutions and Multiple Industry Application Scenarios	Alex Mao	
09:45 - 10:15	Low-Level RF Systems Based on MicroTCA.4	Nan Gan	
10:15 - 10:45	Coffee Break		
10:45 - 11:15	Timing System in MicroTCA	Fang Liu	Rong Liu
11:15 - 11:45	MicroTCA Management - how to become a MicroTCA expert in 30 minutes	Heiko Koerte	
11:45 - 13:30	Lunch		
13:30 -13:40	Welcome Speech	Bocheng Jiang	Junqiang Zhang
13:40-14:10	Progress of the UTEF Low Energy Light Source		
14:10-14:30	Summary and Highlights of the 13th MicroTCA Workshop at DESY in Hamburg	Holger Schlarb	
14:30 - 14:50	Progress in the Localization of MTCA Platforms and Applications	Hongrui Cao	
14:50 - 15:10	The Update of CSNS-II RCS LLRF System Based on MTCA.4	Wei Long	
15:10 - 15:30	Development Progress of the Digital Low-Level RF system for the Hefei Advanced Light Facility	Kunlin Wu	
15:30 - 15:50	LO&CLK Distribution RTM Board Development Progress	Xinpeng Ma	
15:50 – 16:20	Coffee Break and Group Photo		
16:20 - 16:40	MicroTCA-based Motion Controller	Michael Randall	Holger Schlarb
16:40 - 17:00	Status Update on MicroTCA based Fast Orbit Feedback System for PETRA IV	Sven Pfeiffer	
17:00 - 17:20	Libera Brilliance X: MTCA.4 Readout Electronics for Electron Synchrotrons	Manuel Cargnelutti	
17:20 - 17:40	DESY MicroTCA Solutions: FPGA- and SoC-Based Platforms for Science Community and Next-Generation Research Facilities	Behzad Boghrati	
17:40 - 18:00	DESY MMC STAMP: Overview and recent improvements	Patrick Huesmann	
18:30 - 20:30	Dinner		

September 16, 2025

Time	Title	Speaker	Host
08:30 - 09:00	Development and New Progress of a Universal Signal Processing Platform for Beam Diagnostics and Control	Yongbin Leng	Hongrui Cao
09:00 - 09:20	RFSoC-Base LLRF Development for CSNS-II LINAC	Zhexin Xie	
09:20 - 09:35	The Development of the MTCA.4 Based LLRF System in the UTEF	Junqiang Zhang	
09:35 - 9:50	Construction and Testing of the Low-voltage Electronics Test Platform for Wuhan Advanced Light Source 1.0 GeV Linear Accelerator	Hongwei Yue	
9:50 - 10:05	Low-Level Radio Frequency Control System for HUST-UED	Changda Peng	
10:05 - 10:30	Coffee break		
10:30 - 10:50	MicroTCA for Photon Beamlines - on-the-fly scans with spec	Martin Tolkiehn	Chungming Chu
10:50 - 11:10	Universal Dual-channel FMC Carrier Board Based on the MTCA.4	Yajie Mu	
11:10 - 11:30	The Fast Protection System for CSNS-II	Peng Zhu	
11:30 - 11:50	Design of the HEPS FOFB System Based on an ATCA Platform	Guodong Gao	
11:50 - 12:10	Introduction to Control and Data Acquisition Systems for Shanghai Synchrotron Radiation Facility Experimental Stations	Ying Zhao	
12:10 - 13:30	Lunch		
13:30 - 17:00	UTEF Visit		
17:00 - 20:00	Banquet		

September 17, 2025

| Time	Title	Speaker	Host
08:30 - 09:00	Dual-Wheel Drive Accelerates the Development of the Artificial Intelligence Industry	Cong Tan	Martin Tolkiehn
09:00 - 09:20	Precision Timing & Advanced RF Solutions for Particle Accelerators	Jiaoni Bai	
09:20 - 09:35	The Latest Developments in the MTCA.4 Architecture and Corresponding Thermal Solutions	Alphonso Liu	
09:35 - 9:50	The Independently Controllable MTCA System Platform	Bo Li	
09:50 - 10:05	In collaboration with Struck Innovative Systeme GmbH	Rong Liu	
10:05 - 10:30	Coffee Break		
10:30- 10:50	The Design and Development of Control System in the UTEF	Mingtao Kang	Zeran Zhou
10:50 - 11:10	IOC Deployment and Management System Based on Container Technology	Junhua Zhu	
11:10 - 11:30	Introduction to Beamline Control at SSRF	Xuying Lan	
11:30 - 11:50	Detector Control System for CEE	Min Li	
11:50 - 12:10	Simulation of ADRC Application in High-Frequency Cavity	Xue Yang	
12:10 - 13:00	Lunch		
13:30 - 13:50	Introduction to DESY's Firmware Framework FWK	Michael Randall	Xinpeng Ma
13:50 - 14:10	Systemetic Approach for Accelerator Controls	Chungming Chu	
14:10 - 14:30	Introduction to Experimental Station Control at SSRF	Yongnian Zhou	
14:30 - 14:50	Research and Development of the Timing System for CSNS-II Accelerator	Sinong Cheng	
14:50 - 15:10	The Design of Timing System for S3FEL	Ting Liu	
15:10 - 15:30	MicroTCA Developments and History at DESY	Holger Schlarb	
15:30 - 16:00	Coffee Break		
16:00 - 17:00	Round Table Discussion		Holger Schlarb, Chungming Chu, Rong Liu
17:00 - 17:15	Close Out		Junqiang Zhang
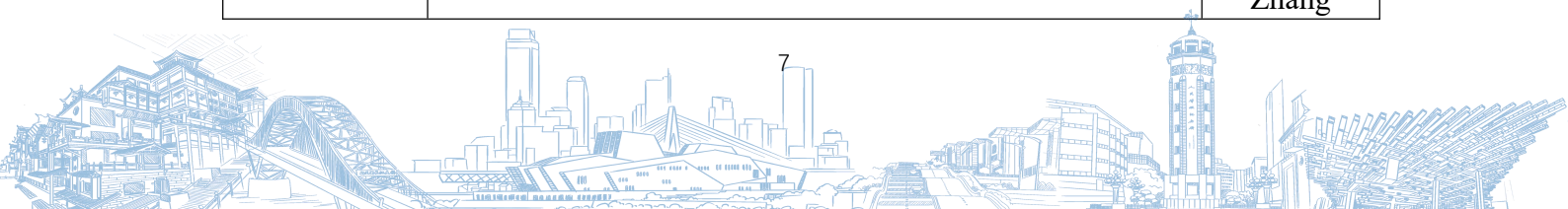
Leave

the engineering challenges to us

you can

focus on the next

Signal Microwave
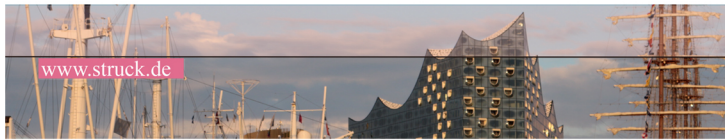
2/4 Channel 2.5 GSPS 14-bit Digitizer AMC
SIS8160 Dual FMC Carrier/SFMC01 Combination
(Kintex Ultrascale based)

new

SIS8160 FMC Carrier Functionality
• 4-lane PCI Express Gen3 Connectivity
• Xilinx XCKU40- or XCKU060-1FFVA1156C Kintex Ultrascale FPGA
• Dual Boot
• Front Panel MMCX Clock Input
• Front Panel MMCX Digital In-/Output (HW Configuration)
• Point to Point Links
• 4 MLVDS µTCA Ports (AMC Ports 17-20) → 8 MLVDS lines
• 2 HPC FMC Sites
• Variable FMC V_{ADJ} (1,0V - 1,8V)
• Low Jitter Clock Generation and Management
• 2 x 2 GByte DDR4 Memory with two Memory Controllers
• White Rabbit Option (over FMC 2)
• Stand Alone Operation Option
• MMC1.0 under DESY LV91

SFMC01 Functionality
• 2 Channels 2.5 GSPS 14-bit
• AC (Balun) or DC Coupled
• Up to 5 GHz AC Analog BW

Possible next JESD Digitizer FMCs
• 4 Channel GSPS 16-bit
• 8 Channel 500 MSPS 14-bit
• Project Driven ...

SIS8160 w. SFMC01

Product Announcement
SIS8164 64 Channel Digital I/O AMC
(Artix-7 based)

Functionality
• Single-lane PCI Express Gen2 Connectivity
• Xilinx XC7A15T-2FGG484C Artix-7 FPGA
• 2 x 32 Channels/Bits on 3M 10250-55H3PC Connectors
• Cable Present Detection Option with Front Panel LED
• LVTTL with TTL Tolerance
• Input/Output Enable in 8 Channel Groups
• One LEMO LVTTL Control Input with TTL Tolerance
• One LEMO LVTTL Control Output
• Flexible Interrupt Generation (Control Input, Input Status Change,...)
• Gigabit Link Port implemenation (AMC Port 0, AMC.2 type E1)
• 4 MLVDS µTCA Ports (AMC Ports 17-20) → 8 MLVDS lines
• MMC1.0 under DESY LV91
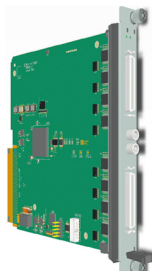
SIS8864 preview

Struck Innovative Systeme GmbH
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phone: ++49 40 60 87 305 0
rev: 08/18

2018 International Beam Instrumentation Conference
SEP 9-13, 2018   Shanghai, China
Organized by Shanghai Institute of Applied Physics, CAS (SINAP)

2018 marks our 20th year in business. We would like to take this opportunity to thank you for your patronage.
Feel free to inquire about customized versions of standard products or full custom designs in case our off-the-shelf product offerings do not meet the requirements of your application.

Kintex Ultrascale based
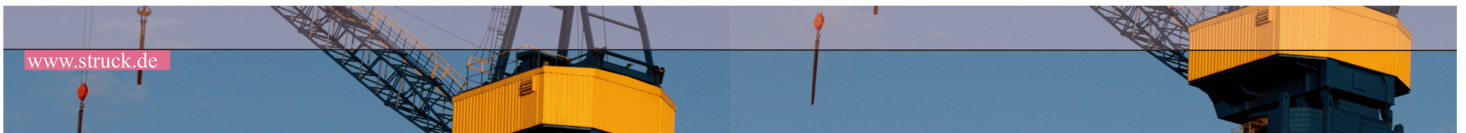## SIS8300-KU 10 channel 16-bit 125 MS/s MTCA.4 Digitizer

The SIS8300-x digitizer board family is in use for LLRF, BPM and controls applications in several accelerators. The new SIS8300-KU is targeted at users who would like to develop or customize firmware with the Xilinx Vivado toolchain. The higher MGT speeds of the Ultrascale family result in performance improvements on the PCI Express and link side.

Functionality
• 4-lane PCI Express Gen3 Connectivity
• 10 Channels 125 MS/s 16-bit (or 250 MS/s 14-bit) ADC
• 10 MS/s to 125 MS/s Per Channel Sampling Speed
• AC or DC Input Stage
• Internal, Front Panel, RTM and Backplane Clock Sources
• Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
• High Precision Clock Distribution Circuitry
• Programmable Delay of Dual Channel Digitizer Groups
• Multi Gigabit Link Port Implementation to Backplane
• Twin SFP+ Card Cage for High Speed System Interconnects
• White Rabbit Clock Option for SFP+ Ports
• Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
• Xilinx XCKU040-1FFVA1156C Kintex Ultrascale FPGA

SIS8300-KU MTCA.4 Digitizer

• 2 GByte DDR4 Memory (flexible partitioning scheme)
• Dual boot
• MMC1.0 under DESY license LV91
• In Field Firmware Upgrade Support
• Zone 3 class A1.0, A1.0C or A1.1CO Compatible

SIS8300-L2 10 channel 16-bit 125 MS/s MTCA.4 Digitizer

The SIS8300-L2 is the working horse of the European XFEL. It allows for flexible configuration of the Zone 3 and the analog performance was further enhanced for LLRF operation im combination with the DWC8300 Downconverter RTM.
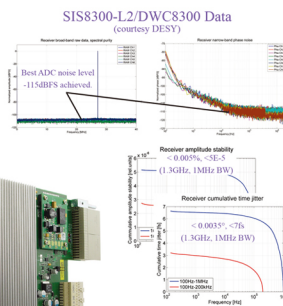
Functionality
• MTCA.4
• 4-lane PCI Express connectivity
• 10 channels 125 MS/s 16-bit ADC
• 10 MS/s to 125 MS/s per channel sampling speed
• Xilinx XC6VLX130T-2FFG1156C Virtex-6 FPGA
• Dual boot
• 2 GByte DDR3 memory
• AC or DC input stage
• ADC inputs through Rear Transition Module (RTM)
• internal, front panel, RTM and backplane clock sources
• Two 16-bit DACs for fast feedback implementation
• Front panel or Zone 3 DAC routing
• FPGA, RTM_CLK4, DIV0 and DIV1 DAC clock sources
• High precision clock distribution circuitry
• Programmable delay of dual channel digitizer groups
• Gigabit link port implementation to backplane
• 6.5 GBit/s on point to point links
• Extended MGT clocking scheme
• Twin SFP card cage for high speed system interconnects
• Front panel grounding block
• MMC 1.0 under DESY license LV91
• Zone 3 class A1.1 compatible (A1.0C and A1.1CO optional)

SIS8300-L2 MTCA.4 Digitizer

Model	FPGA Family	Channels/Sampling Speed/Resolution
SIS8300 V2	Virtex 5	10 x 125 MS/s 16-bit
SIS8300 V2	Virtex 5	8 x 250 MS/s 14-bit
SIS8325	Virtex 6	10 x 250 MS/s 16-bit
Related MTCA.4 Digitizer Boards		

SIS8300-L2/DWC8300 Data
(courtesy DESY)

Best ADC noise level -115dBFS achieved.

Receiver amplitude stability
< 0.005%, <5E-5
(1.3GHz, 1MHz BW)

Receiver cumulative time jitter
< 0.0035°, <7fs
(1.3GHz, 1MHz BW)

DWC8300 MTCA.4 Downconverter RTM

The DWC8300 is a MTCA.4 downconverter RTM. It was developed at DESY for LLRF applications under the designation DRTM-DWC10 and is built by Struck under license of DESY.

Functionality
• MTCA.4 RTM implementation
• 10 Channels
• 8 Channel FBM multi coax. connector (CH1 to CH8)
• CH0 and CH9 SMA
• 700 MHz - 4 GHz (350 - 500 MHz LF version)
• Various intermediate frequencies
• Switchable front end attenuators
• LO clock from front panel or RF backplane
• LO power level monitor
• Digitizer clock input (5 - 130 MHz) from front panel or RF backplane
• I²C support
• Zone 3 class A1.1 compatible

Production under DESY license LV 63

DWC8300 RTM

DS8VM1 Direct Sampling/Vectormodulator RTM

The DS8VM1 Downconverter/Vectormodulator RTM was developed at DESY for lower frequency single cavity LLRF applications under the designation DRTM-DS8VM1.

Functionality
• MTCA.4 RTM
• 8 Channels DC or AC on FBM multi coax. connector
• DC - 400 MHz or 5 MHz – 700 MHz
• 2 Channels DC on MMCX connectors
• Switchable front end attenuators
• VM output 50MHz - 1 GHz
• Switchable output attenuator
• REF power level monitor
• Digitizer clock input (10 - 700 MHz) from front panel or RF backplane
• MMCX clock, interlock and sync. reset input
• On board clock generation/distribution
• I²C support
• Zone 3 class A1.1 compatible

DS8VM1 RTM

Production under DESY license LV 74

SIS8900 MTCA.4 Single Ended Input RTM

The SIS8900 RTM is used to feed single ended -50 Ω terminated- signals to the SIS8300 digitizer. Access to RTM _CLK0, RTM_CLK1 and RTM_CLK2 and a couple of digital I/O lines is implemented in addition.

Functionality
• MTCA.4 RTM
• 8-Bit I/O expander for I²C-bus
• 10 LEMO 00 connectors (FBM option)
• 50 Ohm input impedance
• -1 V,...,+1 V default input range
• AC OR DC input configuration
• RJ45 jack for RTM clocks
• RJ45 jack for Digital I/O
• +5V, 250 mA power option for RJ45 jacks
• Two metric on board pin headers for 6 LVDS input/output signals each
• Zone 3 class A1.1 compatible

SIS8900 RTM

SIS8800 MTCA.4 Scaler/Digital I/O

The SIS8800 is the MTCA.4 follow up to our SIS3820 VME multi purpose scaler. It can be used standalone or in combination with the SIS8980 discriminator RTM or custom digital I/O RTMs.

Functionality
• MTCA.4
• 4-lane PCI Express connectivity
• Xilinx XC6VLX130T-2FFG1156C Virtex-6 FPGA
• Dual boot
• 2 GByte DDR3 memory
• 16 front inputs NIM or TTL/LEMO, TTL,ECL or LVDS/flat cable
• 4 control in-/4 control front outputs
• 42 LVDS I/Os to Zone 3
• two MGTs to Zone 3
• MMC 1.0 under DESY license LV91
• Zone 3 class D1.1 compatible

SIS8800 MTCA.4 Scaler

DWC8VM1 Downconverter/Vectormodular RTM

The DWC8VM1 Downconverter/Vectormodulator RTM was developed at DESY for single cavity LLRF applications under the designation DRTM-DWC8VM1.

Functionality
• MTCA.4 RTM
• 8 Channels Downconverter on FBM multi coax. connector
• 2 Channels DC on MMCX connectors
• 500 MHz - 4 GHz (HF Version 5.7 GHz)
• Various intermediate frequencies
• Switchable front end attenuators
• VM output 50 MHz - 6 GHz
• Switchable output attenuator
• LO clock from front panel or RFBP
• LO and REF power level monitor
• Digitizer clock input (5 - 130 MHz) from front panel or RF backplane
• MMCX clock and interlock input
• I²C support
• Zone 3 class A1.1 compatible

DWC8VM1 RTM
Production under DESY license LV 71

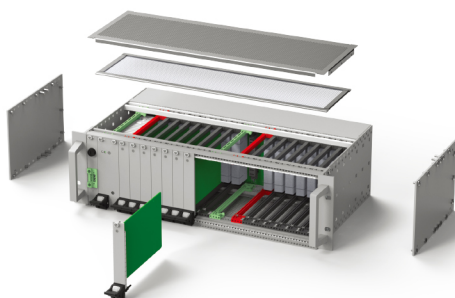| Model	f_{min} in MHz	f_{max} in MHz
DWC8VM1LF	350	500
DWC8VM1	500	3500
DWC8VM1HF	3500	6000
DWC8VM1 Overview Table		

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ELECTRIC

Company Introduction

Anhui Zooneng Measurement & Control Technology Co.,Ltd., established in 2022, is a national high-tech enterprise co-founded with the participation of the Institute of Energy, Hefei Comprehensive National Science Center.

The company's core team originates from the field of fusion reactor nuclear measurement, with deep involvement in fusion scientific research projects such as EAST and ITER. With extensive experience in nuclear electronics, measurement, and diagnostics, we are recognized as one of China's leading teams in this cutting-edge field.

Driven by our expertise in weak nuclear pulse signal processing, we have mastered key technologies including FPGA-based high-speed nuclear pulse identification and processing, real-time feedback control, and PXIe/MTCA high-speed communication protocols.

Applications

- ◆ Fusion Reactor Diagnostic and Measurement Systems
- ◆ Nuclear Measurement and Nuclear Technology Applications
- ◆ High-End Industrial Control Systems
- ◆ Complete Machine Electronics

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坤驰科技专注为大科学装置与工业领域客户提供基于MTCA、PCIe、光纤及以太网等高速总线技术的高性能数字化仪和数据采集解决方案。

系列	采样率	通道	精度	总线
ADQ7DC	10/5 Gsps	1/2通道	14bit	MTCA.4/PXIe/PCIe/USB3.0/10GbE
ADQ14	2/1/0.5 Gsps	1/2/4通道	14bit	MTCA.4/PXIe/PCIe/USB3.0/10GbE
ADQ1600TD	1.6 Gsps	1通道	14bit	MTCA.4/PXIe/PCIe/USB3.0
ADQ1600RF	1.6 Gsps	1通道	14bit	MTCA.4/PXIe/PCIe/USB3.0
ADQ8	1 Gsps	8通道	10bit	MTCA.4/PXIe

ADQ7DC

核心规格

- 14位垂直分辨率
- 2个5GS/s通道或1个10GS/s通道（软件可选）
- 直流耦合，输入带宽高达3GHz（1Vpp输入范围）
- 可编程直流失调
- 4GB板载内存
- 用于自定义实时信号处理的开放式FPGA需要DEVDAQ
- 特定于应用的固件选项
- 以7GB/s的速度点对点流式传输到 GPU
- 硬件触发器和 GPIO
- MTCA.4、PCIe、PXIe、USB3.0、10 GbE 外形尺寸

ADQ8-8C

核心规格

- 10位垂直分辨率
- 每个通道1GS/s采样率
- 8 个输入通道
- 直流耦合，输入带宽高达500MHz（5Vpp输入范围）
- 可编程直流失调
- 1GB板载内存
- 用于自定义实时信号处理的开放式FPGA需要DEVDAQ
- PXIe、MTCA.4 外形尺寸

ADQ14

核心规格

- 14位垂直分辨率
- 1、2或4通道
- 0.5、1或2GS/s采样率
- 输入带宽高达1.2GHz的交流和直流耦合型号
- 直流耦合，输入范围为0.5、1 Vpp
- 交流耦合，输入范围为1.9 Vpp
- 以 3.2 GB/s 的速度点对点流式传输到 GPU
- MTCA.4、PXIe、PCIe、USB3.0、10 GbE 外形尺寸

MORE TO
渺图科技 MIAOTU TECHNOLOGY

Shanghai Miaoto Technology Co.,Ltd.

AI service customization：

01

1.1 General AI Deployment & Development

Custom AI solutions that help experts work smarter, faster, and more effectively.
Our Facial Disease Recognition Framework: We built an AI tool that helps doctors detect diseases from facial photos. It's accurate, efficient, and works fairly across skin tones. By analyzing visual patterns, it speeds up early screening and supports clinical decisions. Visual Component:
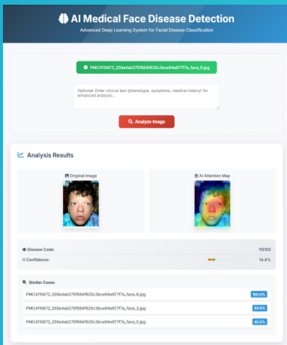
1.2 Specialized AI for Research & Professional Use

Your work is unique. Your AI should be too - we build tools designed just for you.
Here's how it works:
• You share the challenge in your area of expertise.
• We design an AI that understands the details, data, and language of your field.
• You get a custom tool that helps you analyze, discover, and move faster.
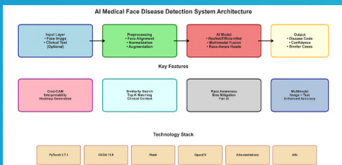
System Architecture

AI Face Disease Detection System

AI Computing Power Solutions

02

智算场景面临的挑战	"一套集群多种异构" 完美释放硬件算力	BioHPC 集群架构	智算场景下的流程化海量 数据处理

异构硬件 | **异构计算框架** | **异构存储**

承载不同架构的CPU以及不同类型的GPU；如何在同时兼容异构的CPU以及GPU的前提下，以可以充分释放算力？

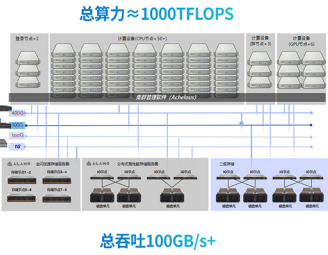承载不同的应用（人工智能、大数据、HPC等），面对不同种类的计算框架，如何使用一套系统支持异构计算框架，并且按需动态构建计算框架，避免异构资源壁垒带来的集群割裂？

1.存储类型多样：不但包含基于闪存的存储，也包含基于磁盘存储；有些应用数据由对象存储承载；有些应用要求访问文件存储，怎样让应用对于异构存储无感知？
2.IO模式多样：不同应用具有不同的IO模式，如何让存储智能去匹配不同IO模式？
3.数据多样：数据量庞大，数据类型多样，数据特征复杂，如何高效进行数据管理？

部署了Achelous的智算集群是异构计算资源、异构存储资源和异构计算框架的完美解决方案

总算力≈1000TFLOPS

总吞吐100GB/s+

• 管算协同，让工程师从计算闭环中解放出来，既提升计算性能，也方便用户
• 通过数据溯源让数据有据可循，有理可依

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Custom Software Development Services:

03

Bioinformatics Custom Development Services

Core Focus:
Specializing in genomics research and mass spectrometry scenarios, we provide end-to-end technical solutions from data processing to visualization.

Specific Services:
• Development of biology-related data analysis software: Utilizing C++/Python technology stacks to build specialized databases for genetic sequences and experimental data, enabling efficient storage, retrieval, and management.
• Assisting researchers in swiftly interpreting data patterns.

Control System Custom Development Services

Core Focus:
Addressing control needs in small-scale hardware scenarios with stable and efficient embedded control solutions.

Technology Stack:
C++ as the core development language, combined with the QT framework for interface development, ensuring both computational performance and a seamless visual operation experience for control systems.

Application Scenarios:
Suitable for laboratory-scale equipment, industrial auxiliary control modules, and other scenarios requiring precise hardware control, status monitoring, and data interaction.

Multi-Language Program Custom Development Services

Core Capabilities:
Leveraging expertise in both C++ and Python to flexibly adapt technology stacks based on project requirements.

Service Features:
• **C++:** Optimized for high-performance, low-latency scenarios such as hardware control and large-scale data processing.
• **Python:** Ideal for rapid development, data processing, and script automation, including scientific data analysis and tool development.
• **Cross-Scenario Adaptation:** Combining the strengths of both languages to deliver integrated development solutions for complex projects (e.g., "database + data analysis + visualization").

H3C Technologies Co., Ltd.

Company Profile

H3C is a global leader in digital solutions, specializing in ICT infrastructure and smart terminals. Headquartered in Hangzhou, China, it operates in 100+ countries, serving government, finance, education, and internet sectors to drive digital transformation.

Key Products

1. Networking: Switches, routers, wireless APs with SDN support.

2. Cloud Computing: H3C Cloud OS platform for hybrid/private cloud.

3. Servers & Storage: UniServer series and storage systems for high-performance computing.

4. Security: Firewalls, IDS to ensure network security.

5. Smart Terminals: Digital displays, IoT devices for smart campuses.

Advantages: Full-stack digital capabilities, proprietary IP, one-stop services.

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