2025 MicroTCA/ATCA for Large Scientific Facility Control International Workshop

Tutorial: Timing System in MicroTCA

Fang Liu

INSTITUTE OF HIGH ENERGY PHYSICS, CAS

Outline

1 *How to Build a Timing System*

2 *Introduction of HEPS Timing System*

3 *Other Timing System Based on MicroTCA*

Part I

How to Build a Timing System?

Part I: How to build a timing system

- **Definition of a Timing System**

  - ***Synchronization system***
  - ***Reference line***
  - ***Timing system***
  - ***Triggering system***
  - ***Global timing system***
  - ***……***

What's the difference?

Part I: How to build a timing system

- **Synchronization System and Reference Line**

  - ***Generally , Only RF Clock Signal, High Frequency***
  - ***Giving reference clock for kinds of Cavitie （RF cavity、Buncher、BI cavity……）、accelerator module、diagnostic module……***
  - ***Precision：Can Reach Less than 100fs***
  - ***Signal Type: Sine signal （One Point in Frequency Spectrum ）***
  - ***Phase can be adjusted***

Part I: How to build a timing system

- **Timing / Trigger / Global Timing system**

  - ***Control the accelerator operating logic :When to trigger e-gun?When to tirgger kicker?……***
  - ***Giving trigger signal to other system to define when to make sense for the beam***
  - ***Square one ， slow （may lager than several seconds ）***
  - ***Precision： Can reach sub-picoseconds***
  - ***Can implement Complex logic for accelerator***
  - ***Digital System， FPGA based system***

How to build a timing system？

Procedure

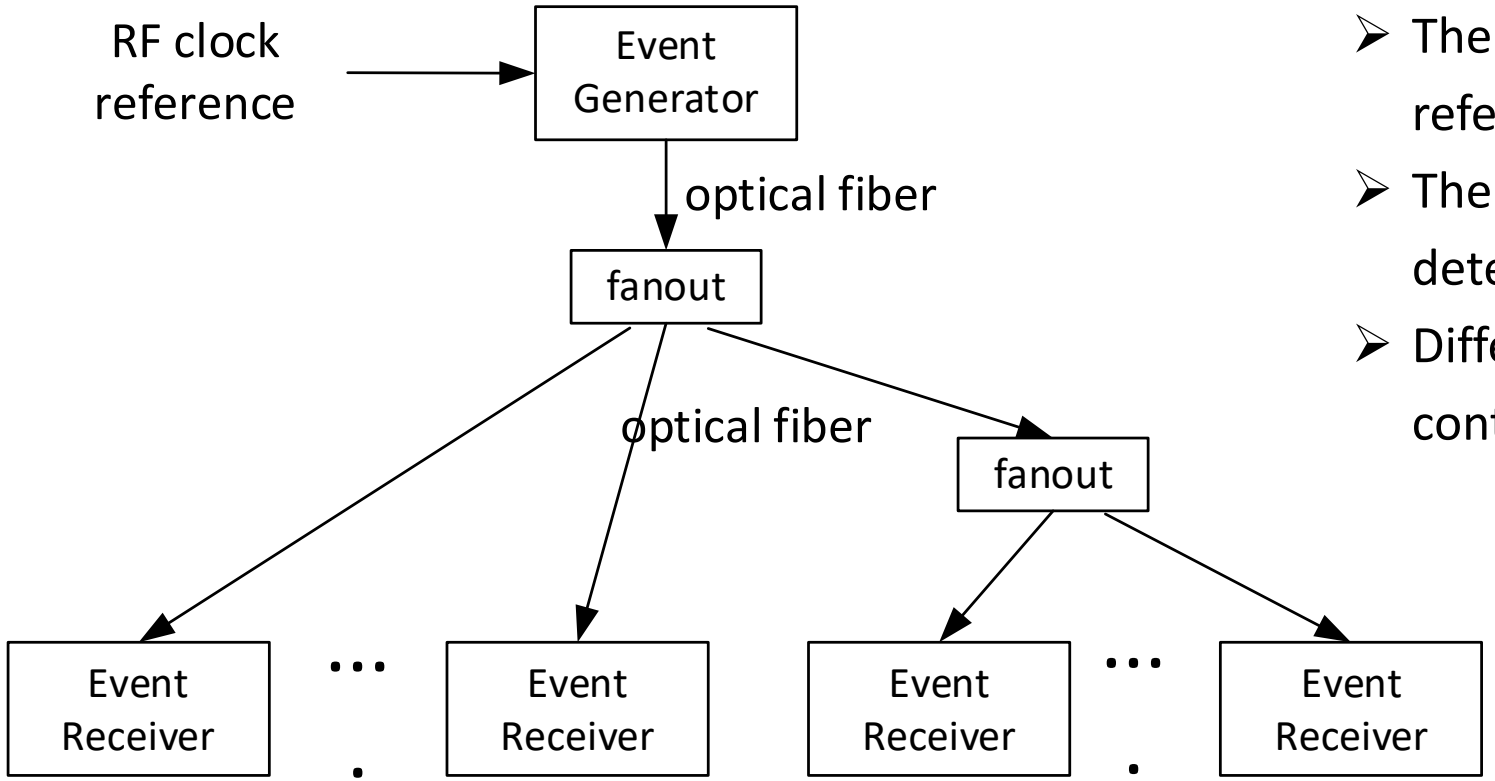
- ***Have to know the operating logic of your accelerator***
- ***Collecting requirements from other systems***
- ***Confirm your Design：requirements and budget***
- ***Build a test platform：key parameters***
- ***Start your program，take care with cables and connection***

Two commonly used timing systems in Accelerator

- **Event-Based Timing System**
  - ***The Most Famous： MRF***
  - ***EVG、FANOUT、EVR***
- **White Rabbite Timing System**
  - ***Earliest Developer： CERN***
  - ***The underlying technology is the same***

Event-Based Timing System

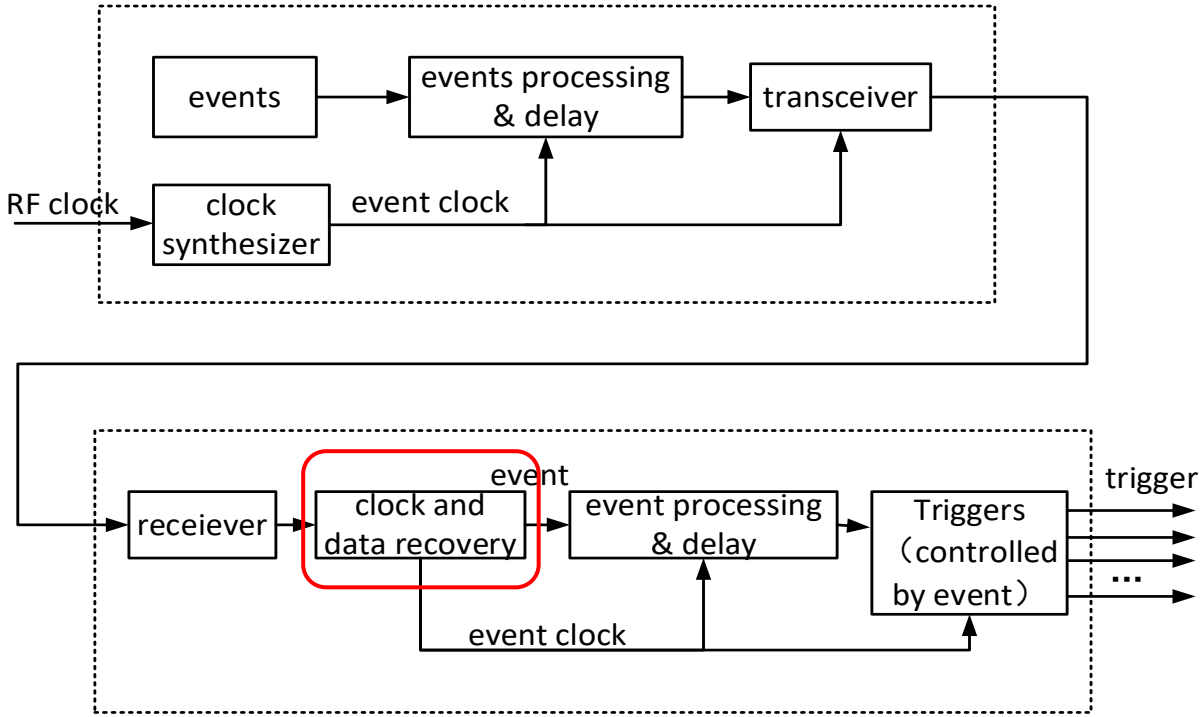
- Widely used：SSRF，HLS，TPS，NSLS-II，MAXIV，Diamond、APSU and so on
- Basic implementation:



- The event clock and the high-frequency reference clock are multiples
- The timing from the EVG to the EVR is determined
- Different triggering processes are controlled by different event codes

Event-Based Timing System

- Based on high-speed serial digital communication technology
- FPGA:MGT、GTX、GTH……
- CDR：Clock and Data Recovery

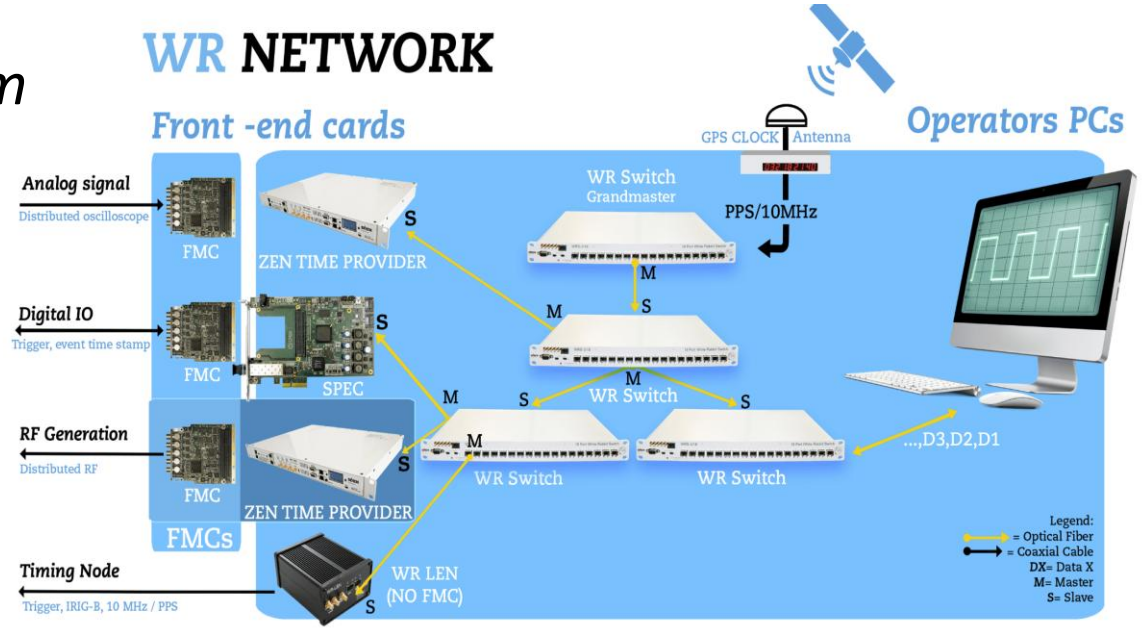


- The Jitter between RF clock and output trigger can reach sub picoseconds.
- Delay step: event clock, sub-nanoseconds ; Can make a Fine Delay Module， Less than 10ps
- Delay compensation

White Rabbite Timing System

Gigabit Ethernet-based synchronization system

- **Synchronous Ethernet（Sync-E）+Precision Time Protocol（IEEE1588）+Digital Dual-Mixer Time Difference（DDMTD）；**
- Sub-nanosecond synchronization accuracy(UTC and PPS, Timestamp,125MHz Clock)
- Jitter between outputs also can reach sub-picoseconds
- Delay compensation；

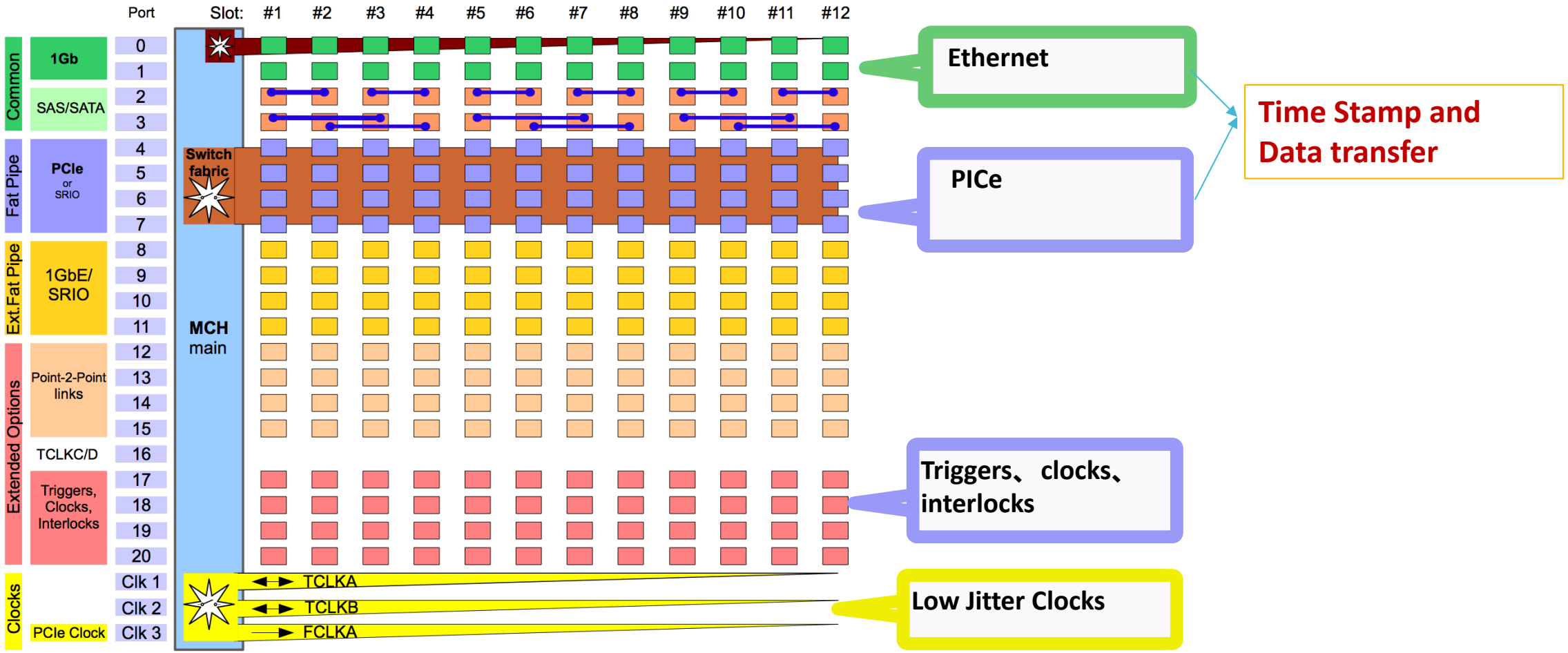


Problem：

- Based on Ethernet, with a fixed 125MHz operating frequency, which **cannot** be directly **synchronized with RF frequency**
- The delay is adjusted in 8ns steps, and it is **not possible** to **achieve specific injection control**

The Benefit of a Timing System using MicroTCA

- The Backplane provides extensive connectivity

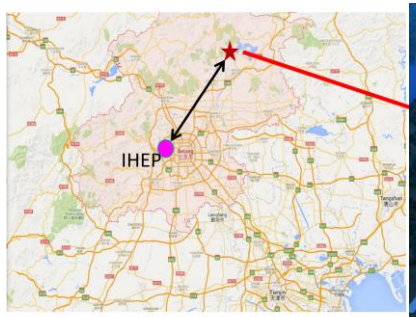


Part II

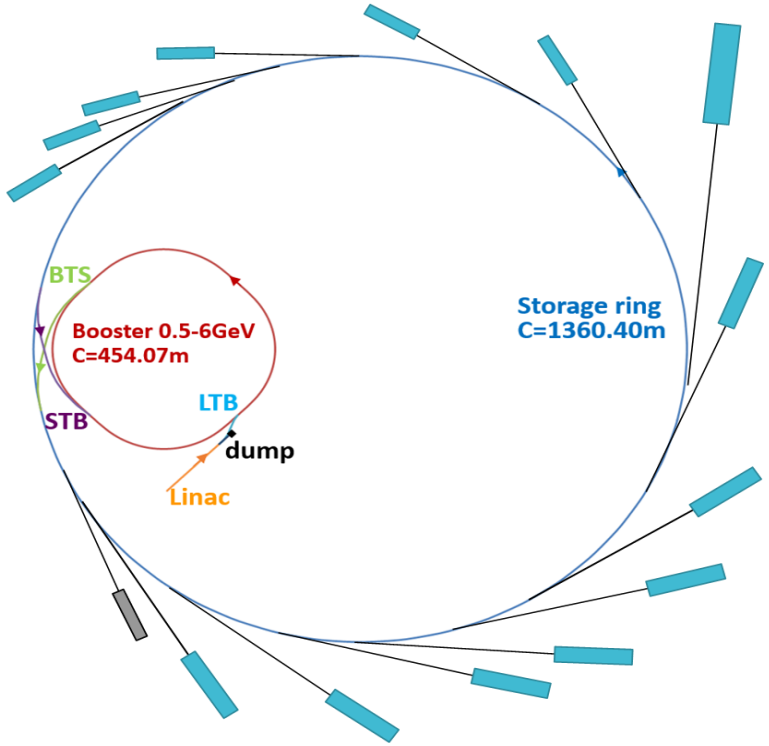
Introduction of HEPS Timing System

HEPS Project Introduction

- HEPS– 4th generation synchrotron light source, 7BA-lattice
  - 14+1 beamlines for phase 1
- Construction period – Jun. 2019 – Dec. 2025
- Huairou District, Beijing area, ~80 km, northeast to IHEP

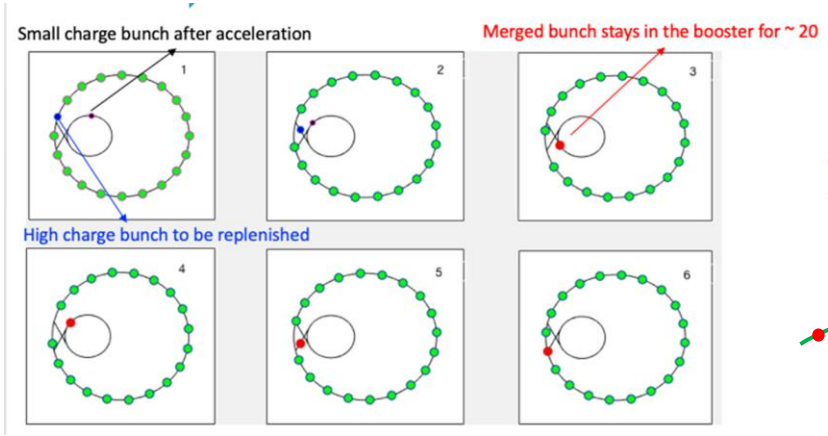


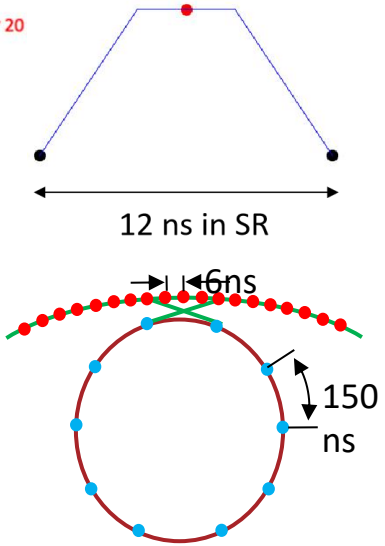
Main parameters	Value	Unit
Beam energy	6	GeV
Circumference	1360.4	m
Emittance	< 60	pm·rad
Brightness	$>10^{22}$	ph/s/mm^2/mrad^2/0.1%BW
Beam current	200	mA



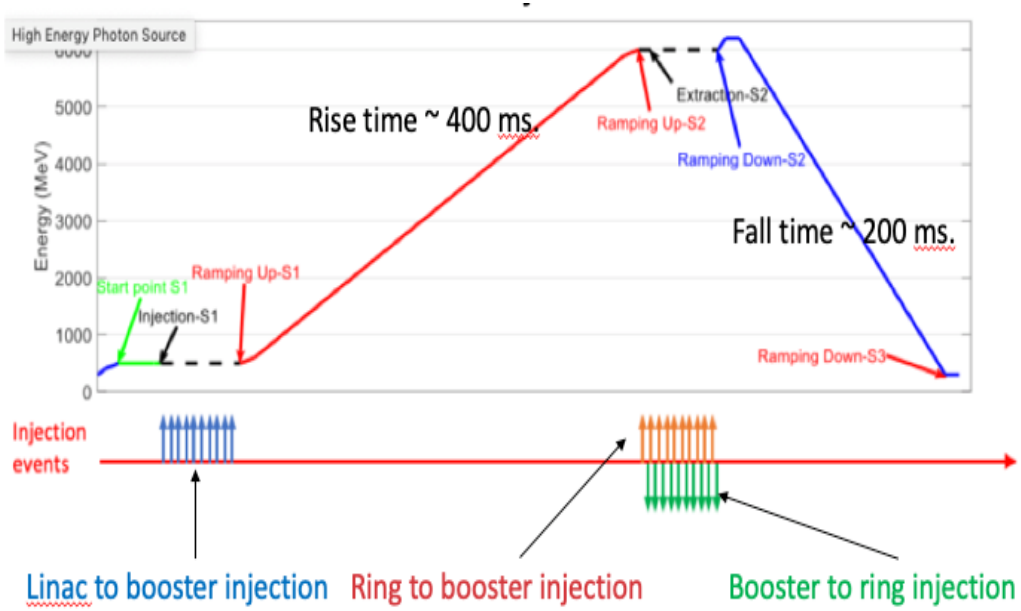
Challenge

- Due to small dynamic aperture of Storage ring , the baseline injection scheme for HEPS : **On-axis swap-out injection**
- **Three Injection Processes**; SR and BST: The bunch in the storage ring will go back to the booster and merge with a specific bunch in boosterm, then go back to the same bucket in the storage ring.
- Beam deflection/ SR kicker pulse is within 12 ns, the timing trigger **jitter** should be **less than 10ps** , also **delay** adjustment step need to reach **10ps/step.** To align the microwave optimized phase, maintain optimal beam gathering and acceleration**, e-Gun jitter** also requires less than **10ps, Delay** adjustment step **size:≤10ps**

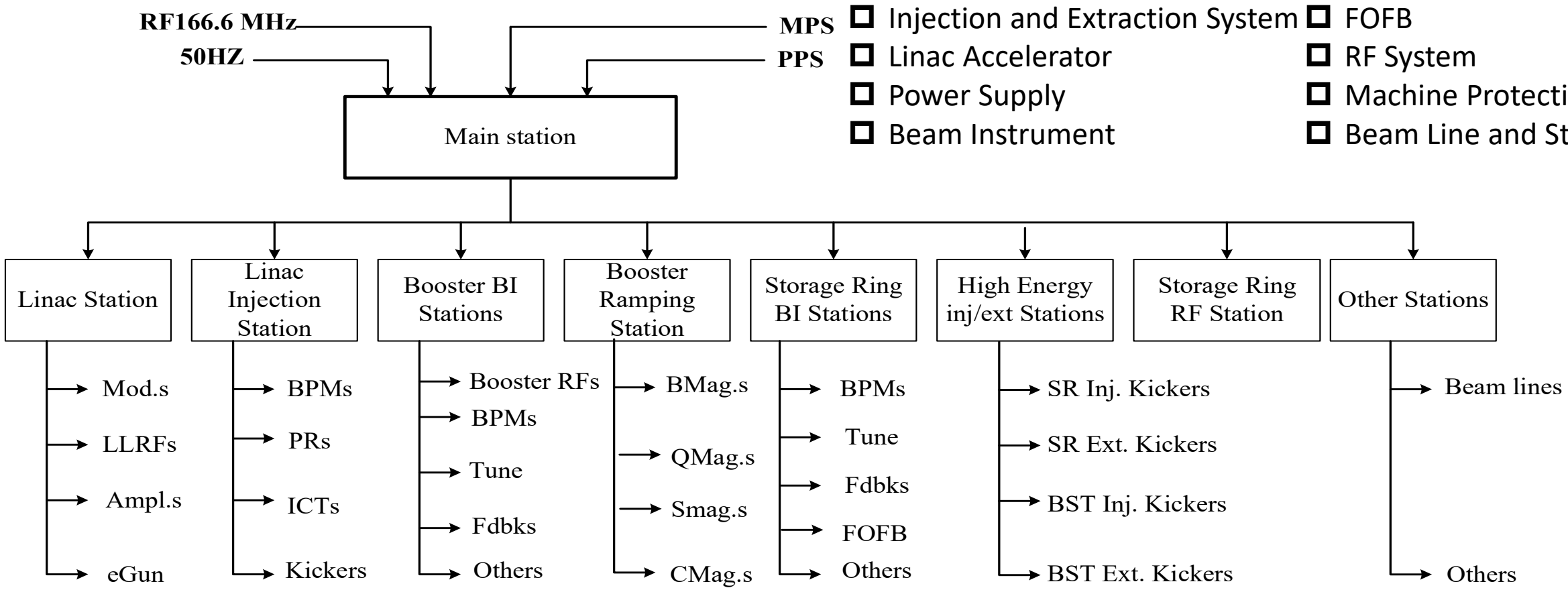




Single bunch swap-out



Overview of HEPS Timing System



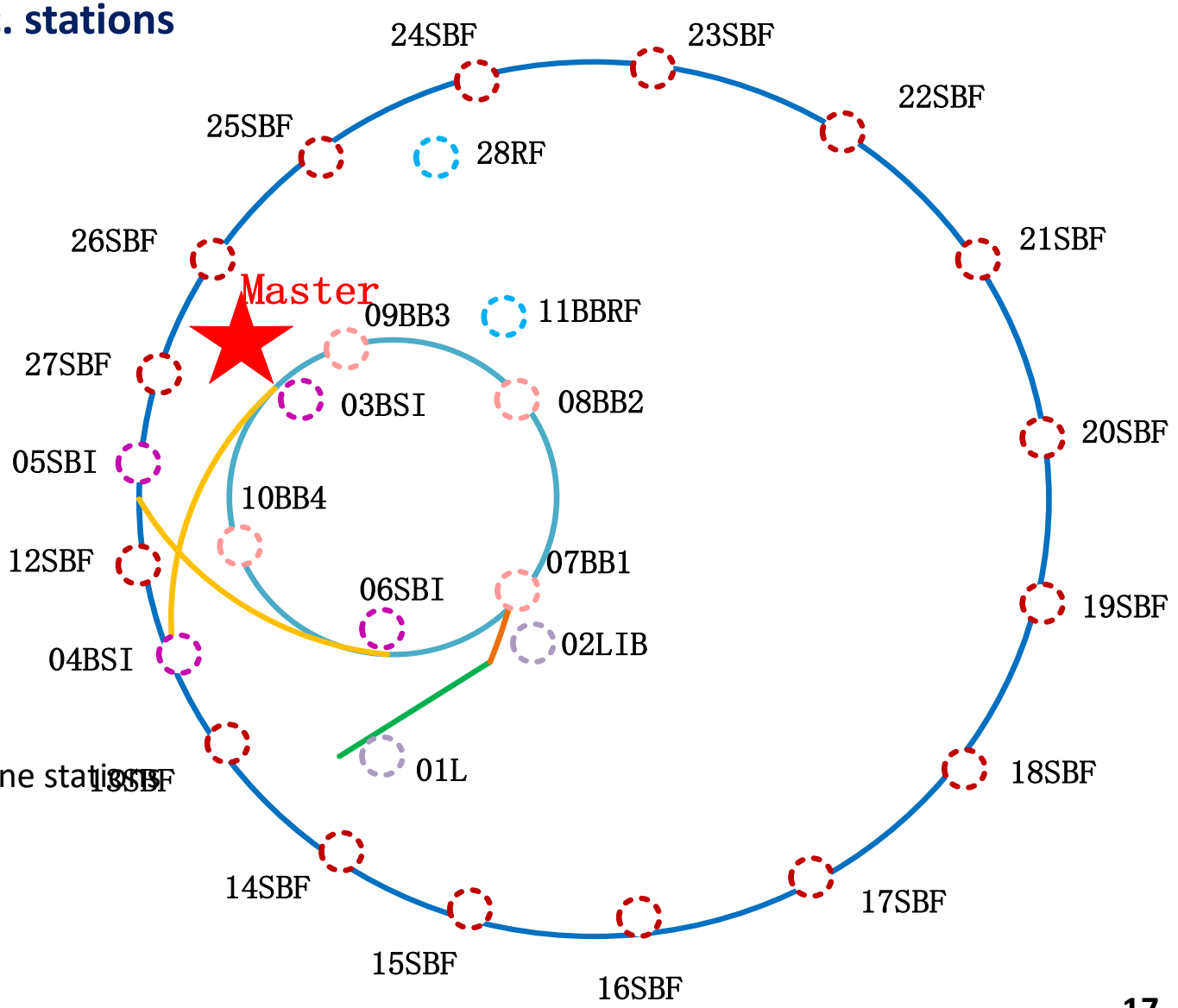
- Injection and Extraction System
- Linac Accelerator
- Power Supply
- Beam Instrument
- FOFB
- RF System
- Machine Protection
- Beam Line and Station

- Provides a trigger signal that is synchronized with RF frequencies and has a certain time relationship
- Provides distributed clock signals for revolution frequency and synchronization frequency
- The overall system jitter must be less than 30 ps, triggers for e-Gun and SR kicker <10ps

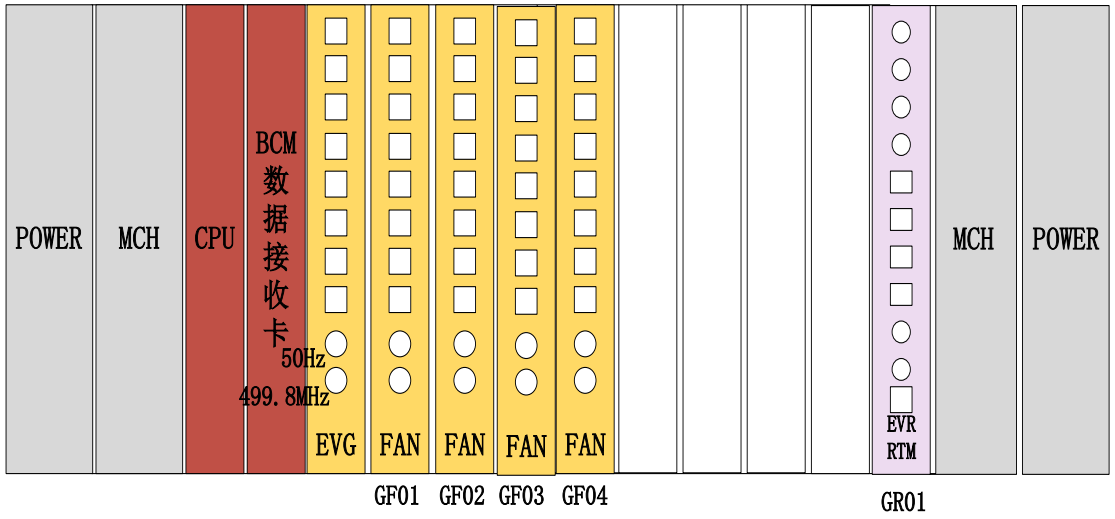
Layout

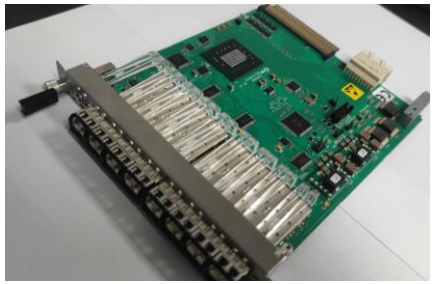
36 timing stations： 1 Master station, 28 Acc. stations 7 beamline stations

- **Linac station： 2**
  - ✓ 01 station： E-Gun、 Linac Klystron and LLRF
  - ✓ 02 station： Low energy injection kicker、 Linac, low energy transport line and part booster BI
- **High energy injection and extraction station： 4**
  - ✓ 03: Booster extr. kicker and bumper
  - ✓ 04: Storage ring injection kicker
  - ✓ 05: Storage ring pre-kicker、 kicker
  - ✓ 06: Booster injection kicker
- **Booster Stations： 5**
  - ✓ 07-10 stations： Booster BI (BPM and others)
  - ✓ 11 station： Booster BI and Booster RF
- **Storage ring BI and FOFB stations: 16**
  - ✓ 12-27 stations： 3 straight section's BI and FOFB in one station
- **Storage ring RF station： 1**
  - ✓ 28 stations： SR RF
- **Beamline stations： 7**



Main Station



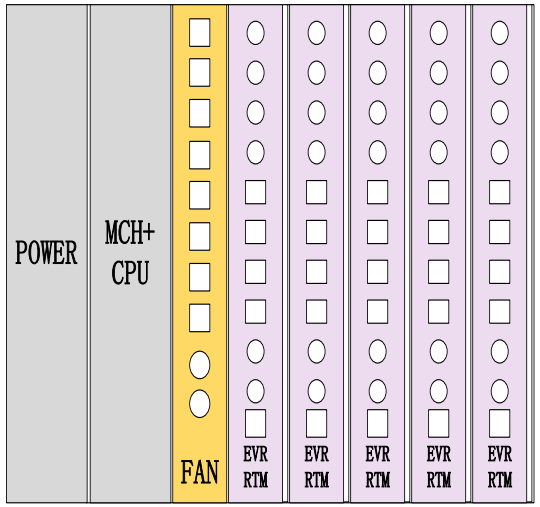


mTCA-EVM-300

AMG64/472

- MTCA.4 Crate： Native-R9(11850-028)9U
- Double Power Supply，double MCH：NAT-MCH-PHYS80
- CPU：AMG64/472 4-core (4.0 GHz) (45W) Xeon E3-1505M v6,32GB DRAM，CentOS—>Debian linux，
- EVG：mTCA-EVM-300
- FANOUT：mTCA-EVM-300
- DATA TRANSFER：DAMC-Z7IO +DFMC-SFP4

Slave Station



9U chassis

2U chassis

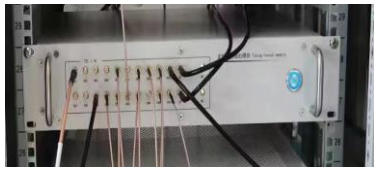
mTCA-EVR

EVRTM

TTL-FineDelay

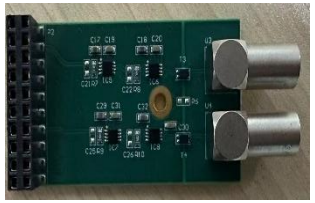
HFBR-1414

3U chassis



1-10 TTL FANOUT

1-10 HFBR-1414



TTL5V

TTL3.3V

■ Crate

- 9U：12 slots
- 2U：6 slots

  MCH+CPU：

  4 Core Core E3 (E3-1505LV5 25W 4c/8t HDP530 2.0GHz 8MB incl. ECC 16 GB DDR3-1066)
- 3U :beamline

■ Timing Board

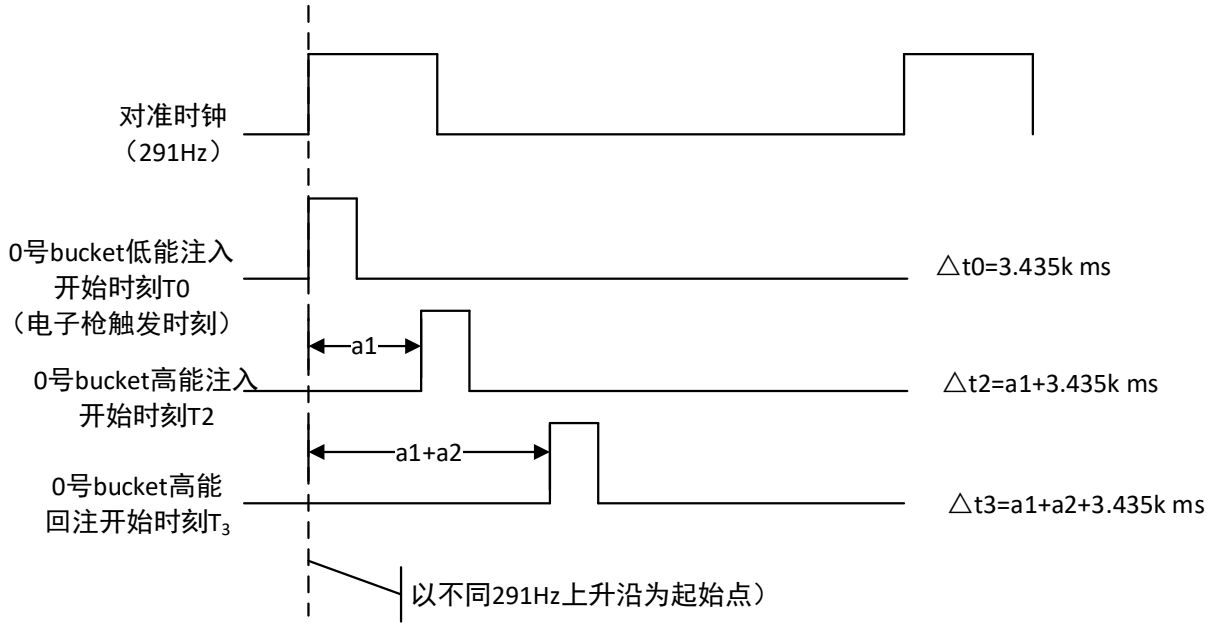
- FANOUT：mTCA-EVM-300
- EVR：mTCA-EVR-300
  - TTL:4
  - UNIV：4
  - Pulser 16
- RTM：UNIV：10

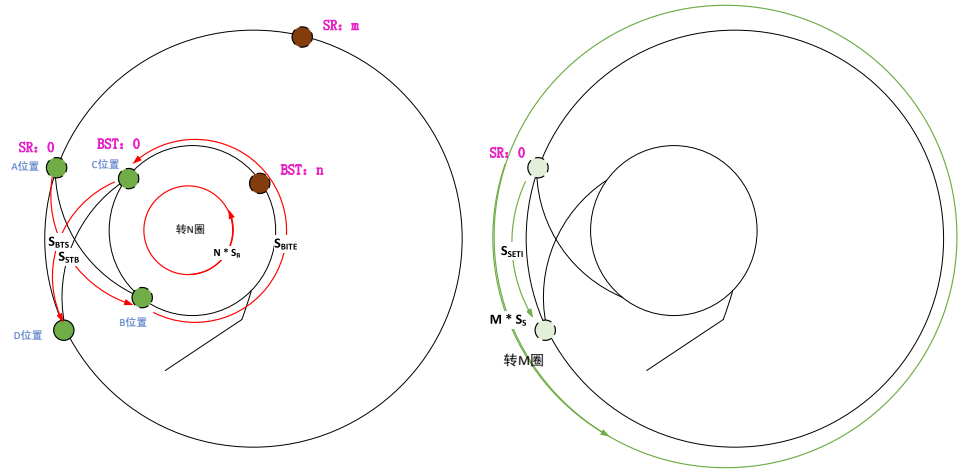
■ Output

- UNIV-TTL5V：LEMO
- UNIV-HFBR-1414：ST
- UNIV-TTL-DLY： 10p delay step size
- 1-10 TTL FANOUT
- 1-10 HFBR-1414 FANOUT

Alignment of the three Injection&Extraction processes

- 0th bucket alignment for the three IE processes; Each IE process needs to run independtly;
- Coincidence clock:291Hz;





(a)　　(b)

$$\Delta t * c = S_{STB} + N \times S_B + S_{BITE} + S_{BTS} = M \times S_S + S_{SETI}$$

$$\Delta t_0 = 6\text{ns} \times (\text{m} + 756\text{M1}) = 2\text{ns} \times (\text{n} + 757\text{N1})$$

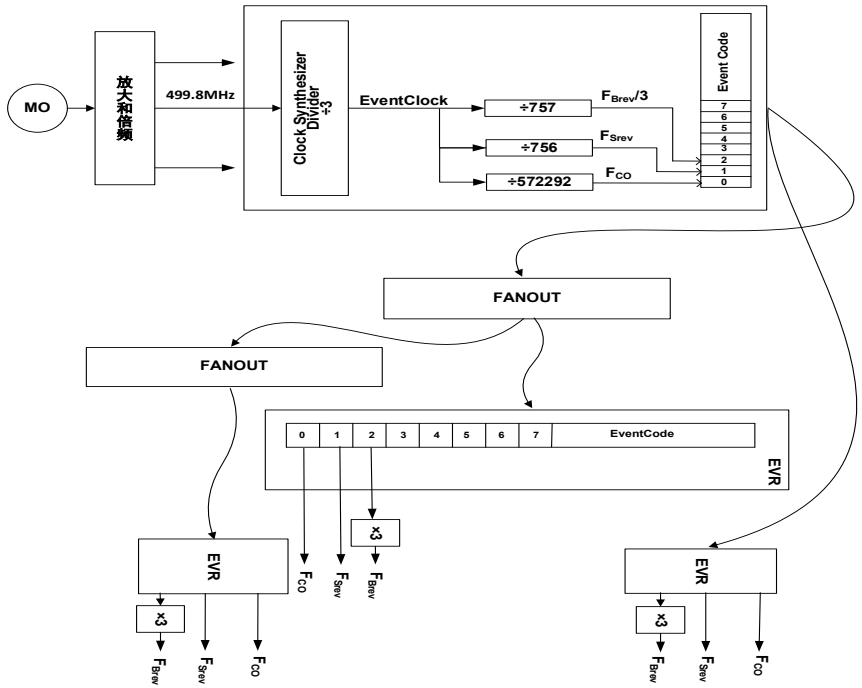
$$\boldsymbol{\Delta t_0 = 6ns \times \text{mod}(190512\text{n} + 757\text{m}, 572292)}$$

- After finding the start time of bucket 0 in each injection process, buckets in other locations can be injected into the specified bucket with an integer multiple delay of 6ns.
- The timing system will use different event codes to control each independent process, and each process can be controlled independently or combined to meet the various needs of operation.

Distributed clocks

- Three distributed clocks are provided through DBUS: SR revolution frequency, Booster revolution frequency, and alignment clock

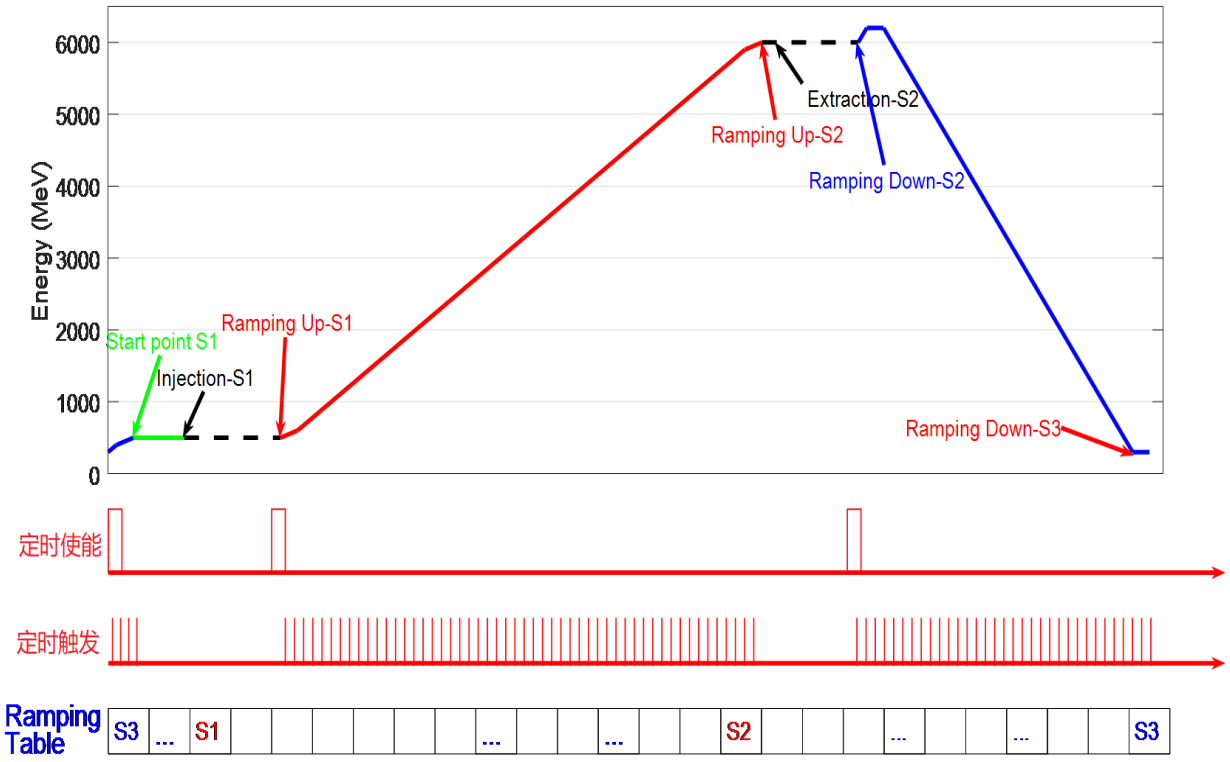
Name	Definition	Value	Unit	Comment
$f_{SR,rev}$	f_{ref} / 2268	220.371	kHz	SR revolution frequency
$f_{BST,rev}$	f_{ref} / 757	660.239	kHz	BST revolution frequency
f_{CO}	f_{ref} / 2268 / 757	291.11	Hz	Coincidence rate of BST -> SR 0-th bucket



- Coincidence clock
  - obtained by dividing the event clock by dividing it by 572292
- SR revolution Frequency
  - event clock/756
- Booster revolution Fre
  - Solution：event clock/756，EVR+ Triple multiply

Synchronous Ramping Control

- The timing system provides an synchronous enable and step-by-step trigger signals, and controls the booster magnet and the RF system to ramping synchronously.

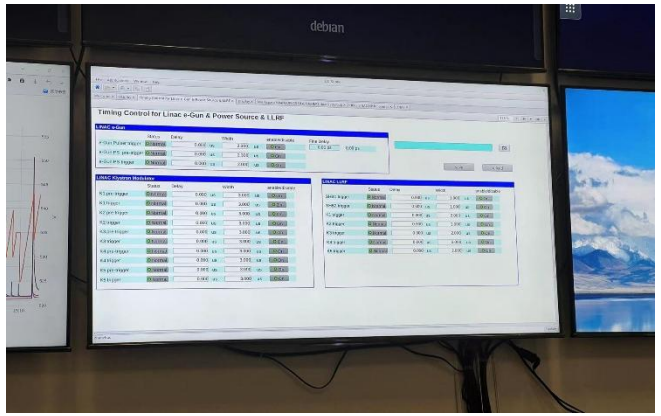


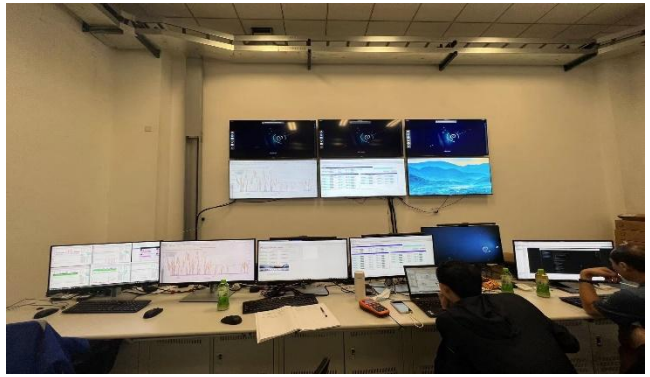
The HEPS injection cycle is 1 second. Among them, there are 3 ramping processes

- When it is necessary to raise or lower energy, the timing system will receive the control system RAMPING start signal, the frequency and number of triggers that need to be provided.
- After an timing enable signal is sent to the participating devices , each device is enabled to the RAMPING state.
- After a fixed period of time, a trigger signal is sent at a regular interval, and each time the ramping device receives a timing trigger signal, it advances one point according to the direction determined above.
- When the Ramping reaches the specified value, the Ramping device will automatically disable and enable the device, and maintain the current set value, even if there is a timing trigger signal, it will no longer operate.
- When the Ramping reaches the end of the Ramping Table, the current index value of the device will automatically jump to the start point of the Table, waiting for subsequent control.
- If the device receives the control force disable command, it does not act on the enable signal sent from timing system.

HEPS LINAC Timing System

- Adopted the MicroTCA.4 structure.





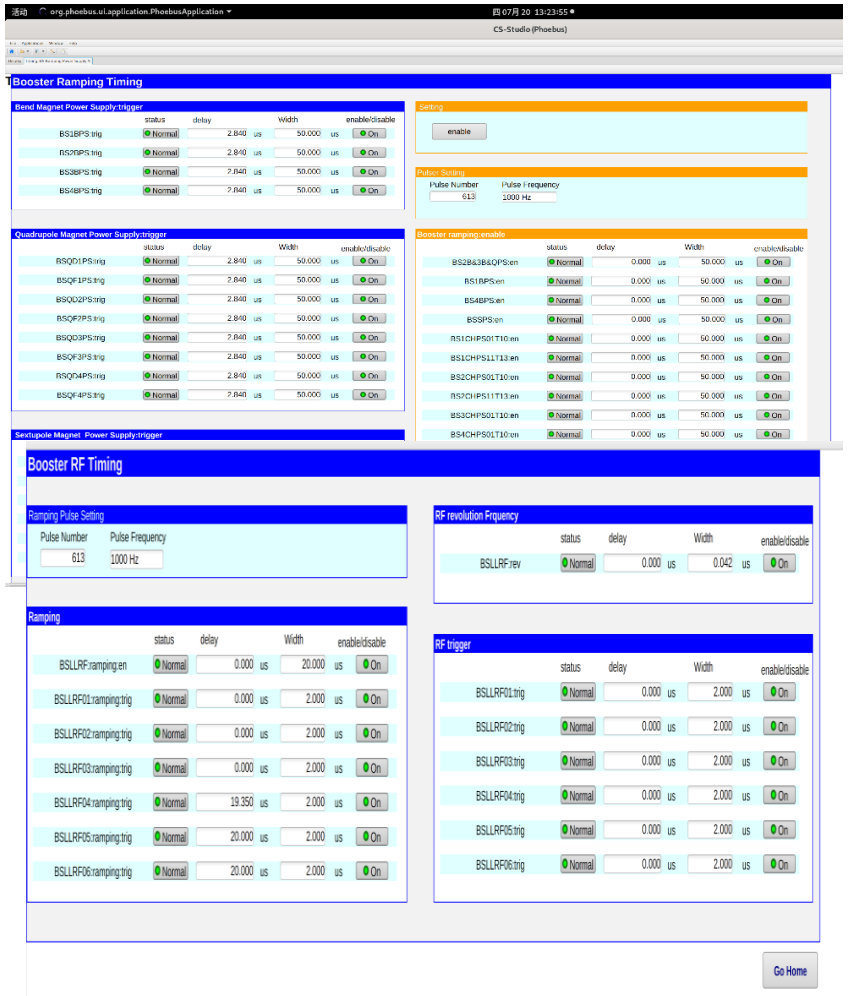
Temporary Linac Control Room

Temporary Main Timing Station &
Microwave and Power Source Timing Station

Linac BI Timing Station

Booster Timing

•Booster RF and Power Supply Timing

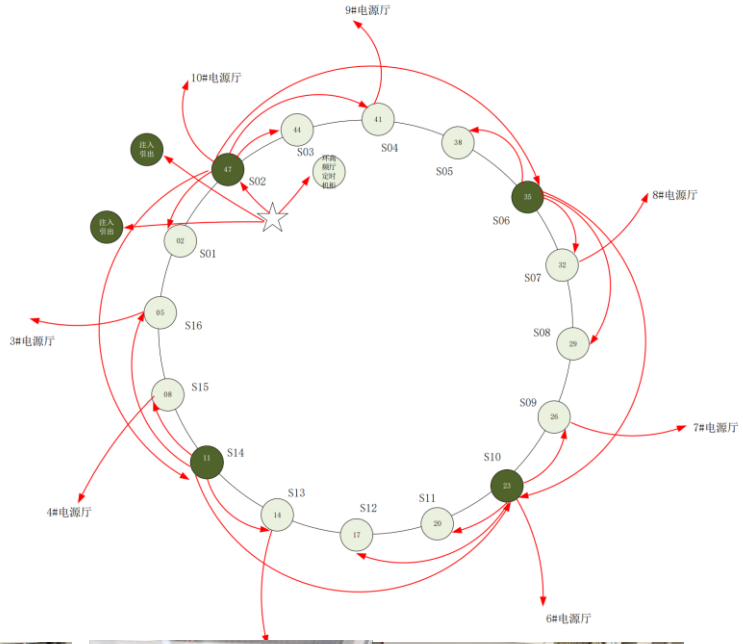


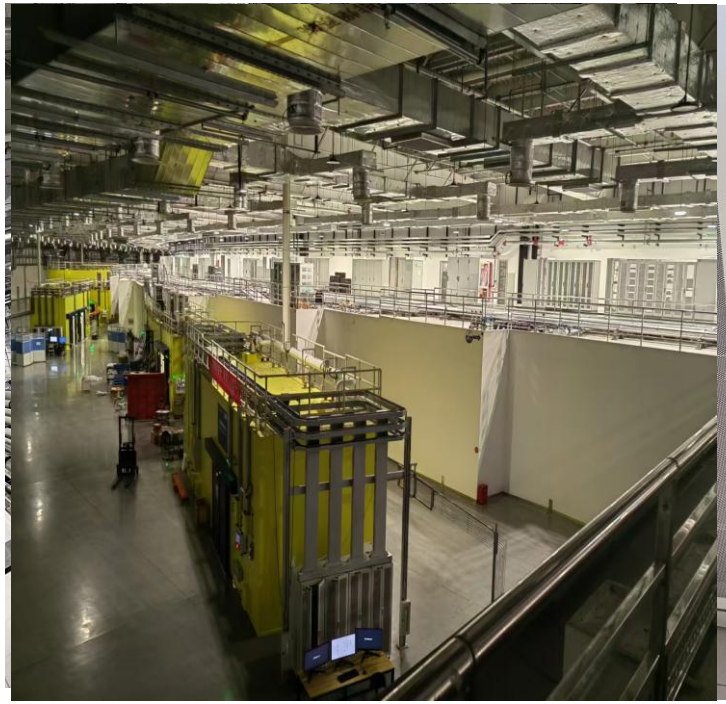
Booster Timing

- **BI Timing**
- 4 stations are located under the vacuum pipes in Booster tunnel

SR Timing

- BI：576 BPM，~200 BLM，BCM，TUNE……
- PS：~2700 power supplies，Postmortem
- IE、FOFB、RF





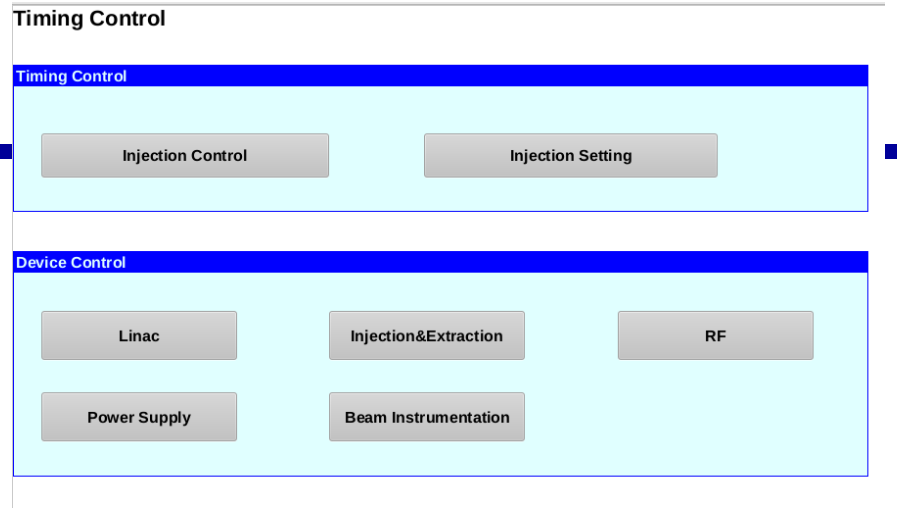
Control Interface

- Low energy injection 、 BTS and STB injection control
- Ramping： Power Supply Ramping、 RF voltage& Phase Ramping

- Top-up Mode
- Normal Mode
- Flexible combine each injection process
- Can set the delay between each injection or ramping process

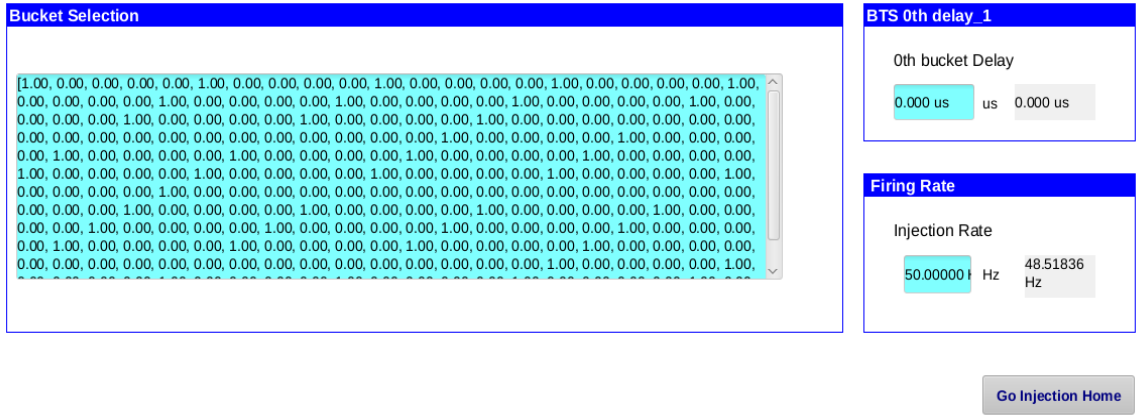
Bucket Select

- Max Booster bucket : 10 Select in Control inteface
- SR bucket: 756 download using a waveform



Booster Low Energy Injection Timing Control

Booster To Storage Ring Injection Timing Parameters



- th0 can delay
- giving pre-trigger for Linac LLRF
  - ✓ Pulse number and Frequency can set

Tigger for BI、e-Gun、LLRF……

Timing Control for Linac e-Gun & Power Source & LLRF

LINAC e-Gun

	Status	Delay		Width		enable/disable	Fine Delay	
e-Gun Pulser trigger	Normal	152.570	us	1.000	us	On	0.00 ps	0.00 ps
e-Gun PS pre-trigger	Normal	0.000	us	2.000	us	Off		
e-Gun PS trigger	Normal	149.000	us	2.000	us	On		

LINAC Klystron Modulator

	Status	Delay		Width		enable/disable
K1 pre-trigger	Invert	0.000	us	4.000	us	Off
K1 trigger	Normal	147.310	us	4.000	us	On
K2 pre-trigger	Invert	0.000	us	4.000	us	Off
K2 trigger	Normal	145.630	us	5.000	us	On

LINAC LLRF

	Status
SHB1 trigger	Normal
SHB2 trigger	Normal
K1 trigger	Normal
K2 trigger	Normal

Linac Beam Instrumentation Timing Control

Linac BI Timing

LINAC ICT

	status	delay		Width		enable/disable
ICT01	Normal	157.150	us	2.000	us	On
ICT02	Normal	157.150	us	2.000	us	On
ICT03	Normal	157.118	us	2.000	us	On
ICT04	Normal	157.100	us	2.000	us	On
ICT05	Normal	157.088	us	2.000	us	On
ICT06	Normal	157.098	us	2.000	us	On

LINAC PR

	status	delay		Width		
PR01	Normal	50.000	us	35.000	us	On
PR02	Normal	50.000	us			
PR03	Normal	50.000	us			
PR04	Normal	50.000	us			
PR05	Normal	50.000	us			
PR06	Normal	50.000	us			

LINAC BPM

	status	delay		Width		enable/disable
BPM01	Normal	155.120	us	2.000	us	On
BPM02	Normal	155.100	us	2.000	us	On
BPM03	Normal	155.127	us	2.000	us	On
BPM04	Normal	155.250	us	2.000	us	On
BPM05	Normal	155.240	us	2.000	us	On
BPM06	Normal	155.290	us	2.000	us	On
BPM07	Normal	155.260	us	2.000	us	On
BPM08	Normal	155.230	us	2.000	us	On

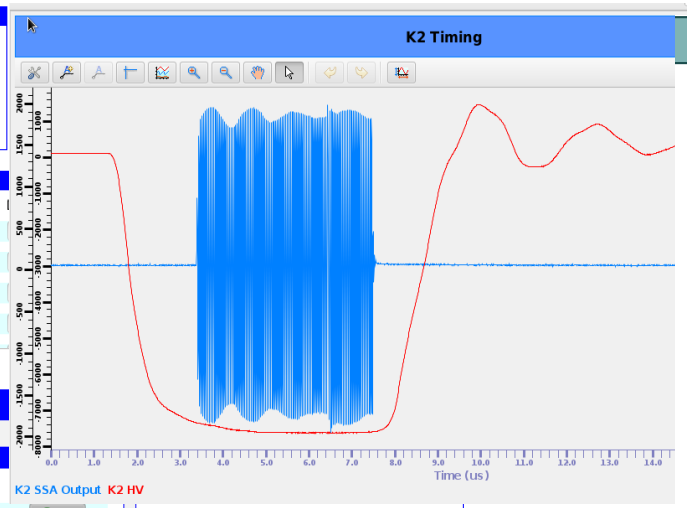
BPM SYN

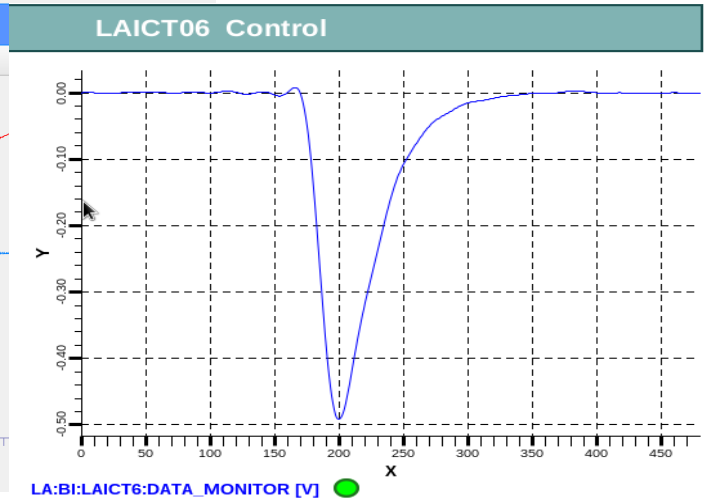
	status	delay		Width
BPMSYN	Normal	0.000	us	

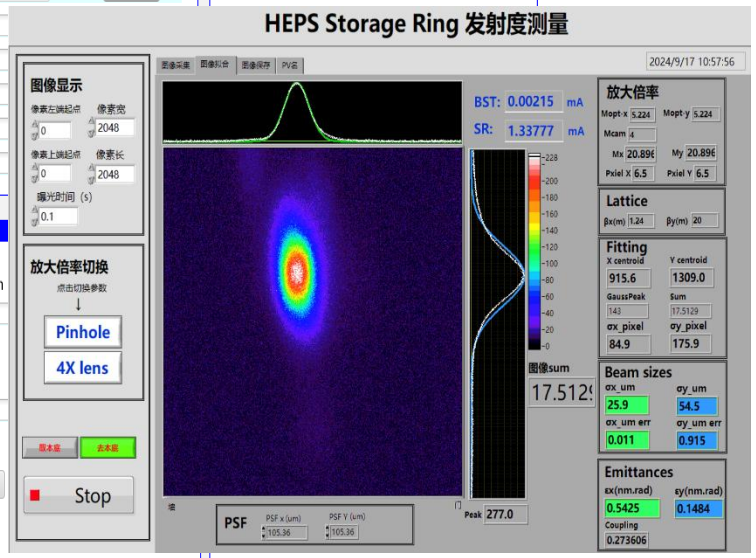
BPM TEST

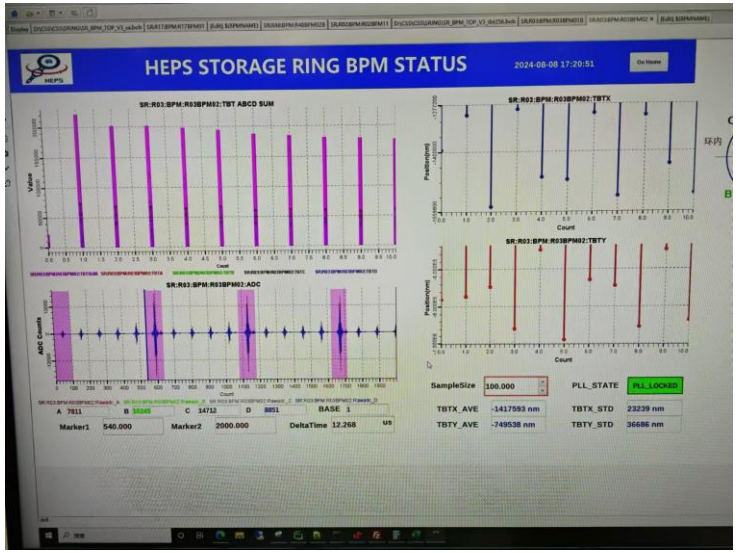
	status	delay	
BPMTST	Normal	0.000	us

Save Reload





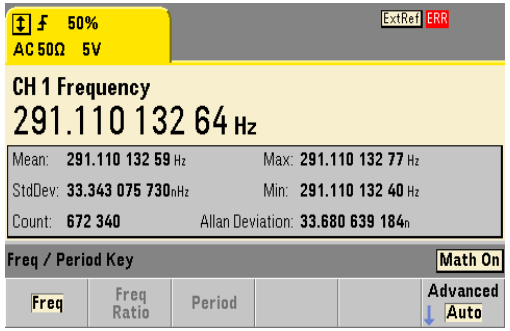


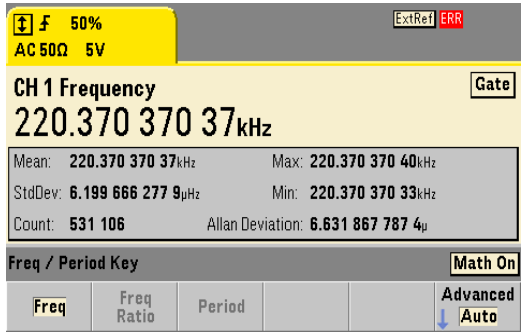


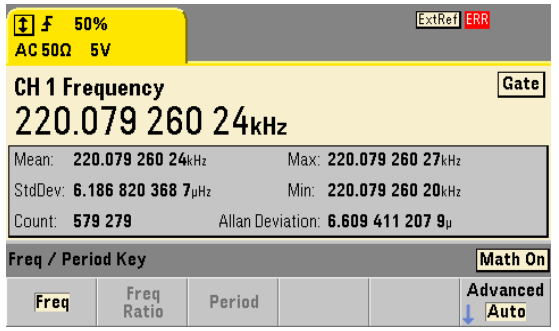
Testing for Distributed Clock

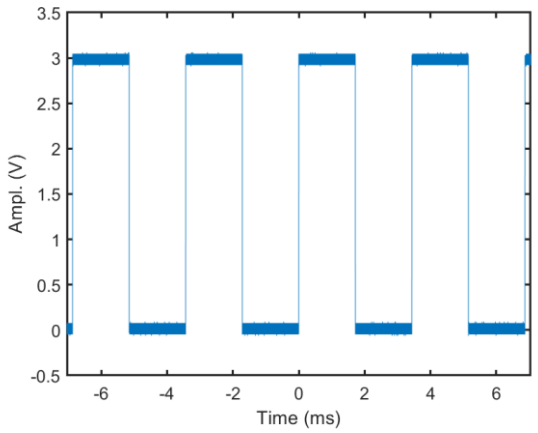
Name	Frequency	Divider
F_{CO}	291.11Hz	572292 （756×757）
F_{Srev}	220.370Hz	756
F_{Brev}	660.239Hz	757/3

- Teledyne LeCroy SDA 820Zi-B oscilloscope measures the time-domain waveform of the output signal. The LeCroy oscilloscope has a bandwidth of 20GHz and a sampling rate of 80GS/s
- KEYSIGHT 53220A frequency meter measures the frequency and frequency stability.

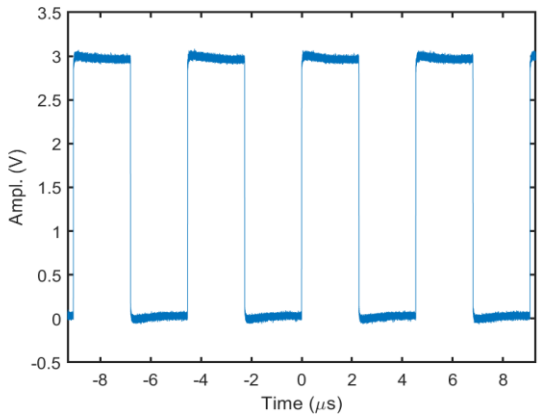




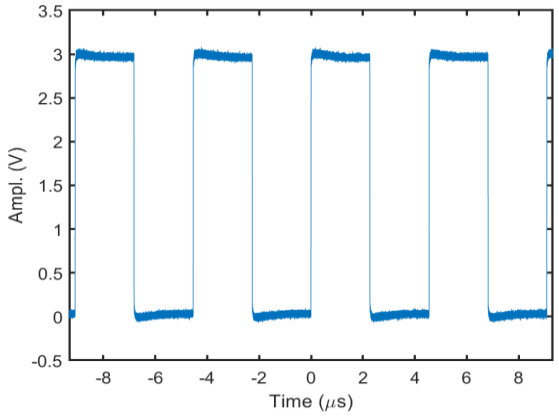




DBUS0： Aligment clock



DUBS2： SR revolution clock

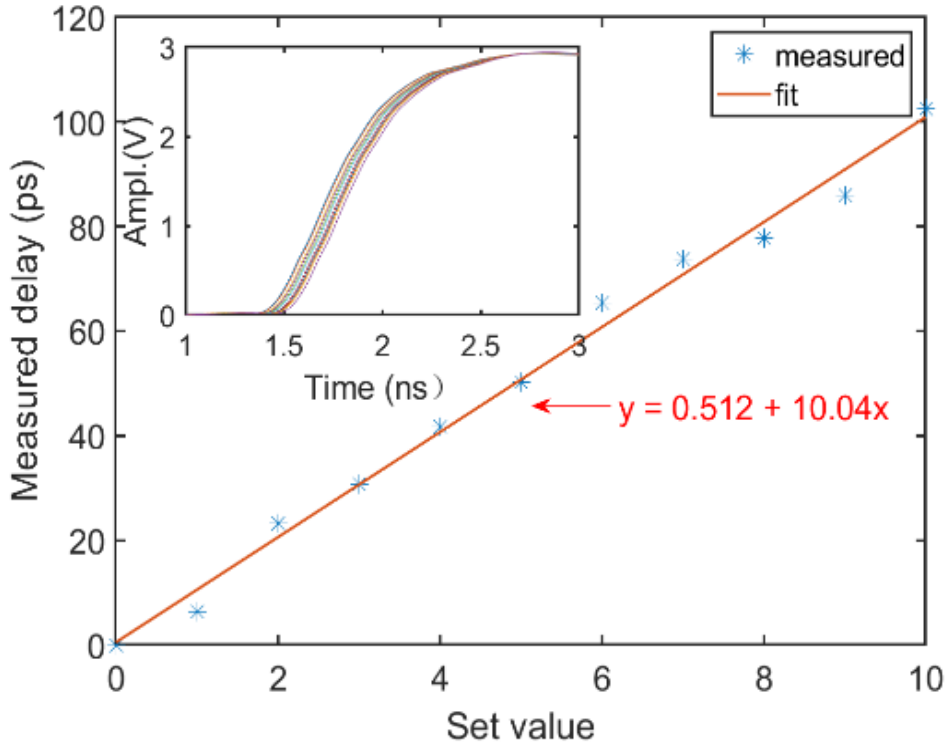


DUBS1： BST revolution clock/3

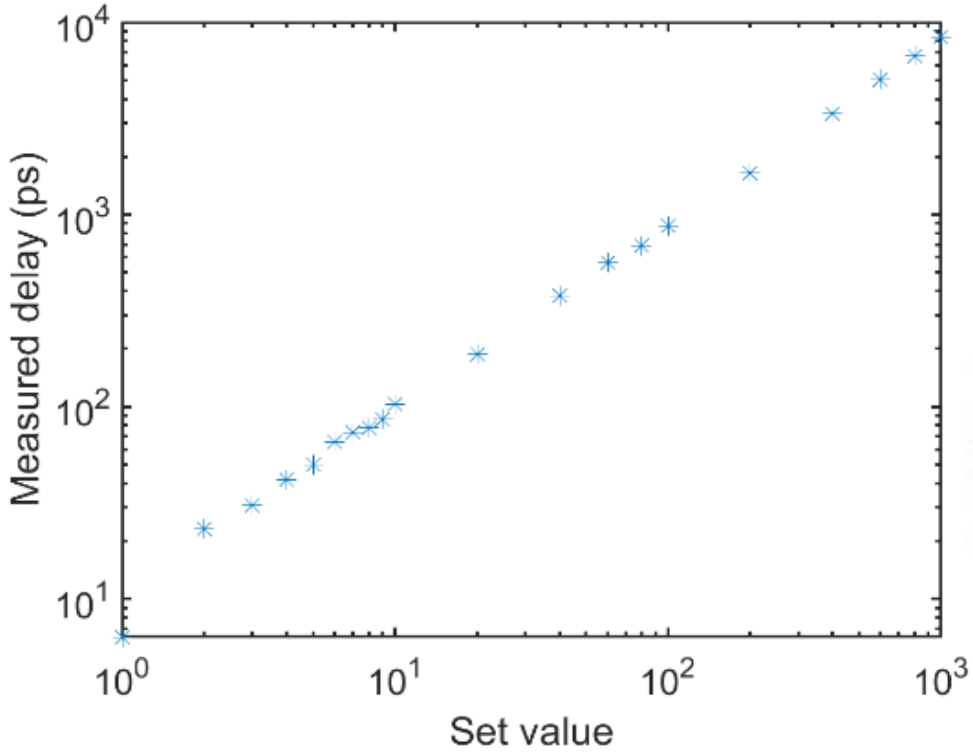
- Coincidence Clock: 291.11013264Hz resolution 34nHz
- SR revolution clock: 220.37037037 kHz resolution 7μHz
- BST revolution clock/3: 220.07926024 kHz resolution 7μHz。

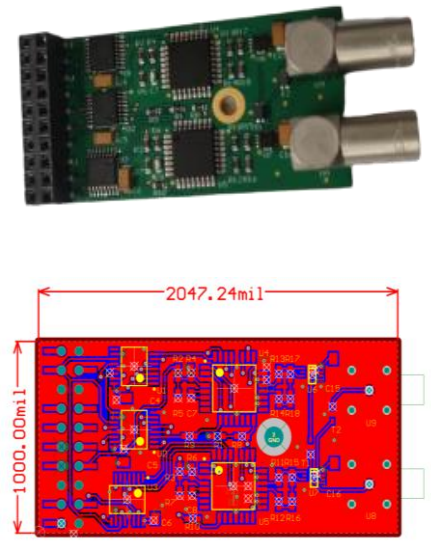
Delay Adjustment Test

- Since 6ns is a digital counting implementation, only 10ps adjustment accuracy is tested here.
- The delay adjustment is performed by adjusting the delay step size of the delay module in the EVR. For each delay value, 1000 waveforms are measured with an oscilloscope and averaged over the 1000 sets of data.



10ps step size adjustment 10 times, adjust 100ps

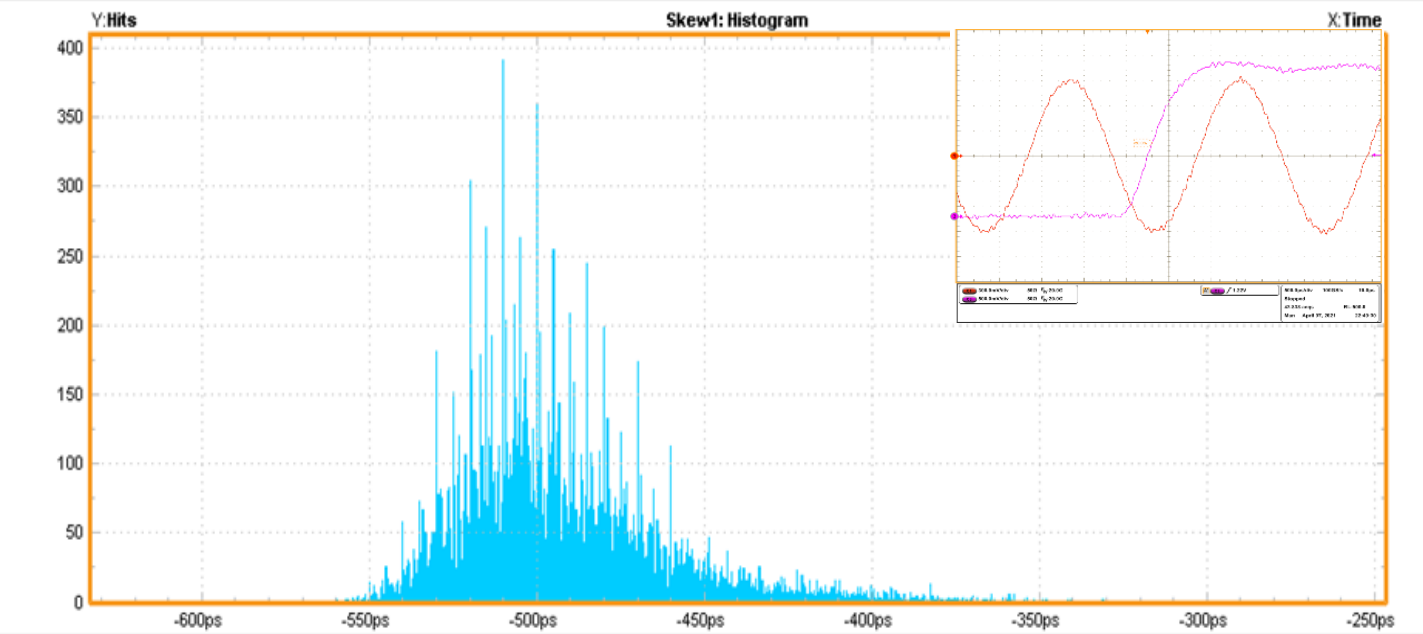




10ps delay step size, adjustment close to 10ns

Delay Compensation Test

- Optical fiber networks are susceptible to temperature and humidity, and are prone to slow drift due to diurnal temperature and seasonal changes
- All our timing modules equipt with delay compensation function
- The system does not require the use of contour wires, has an automatic measurement function

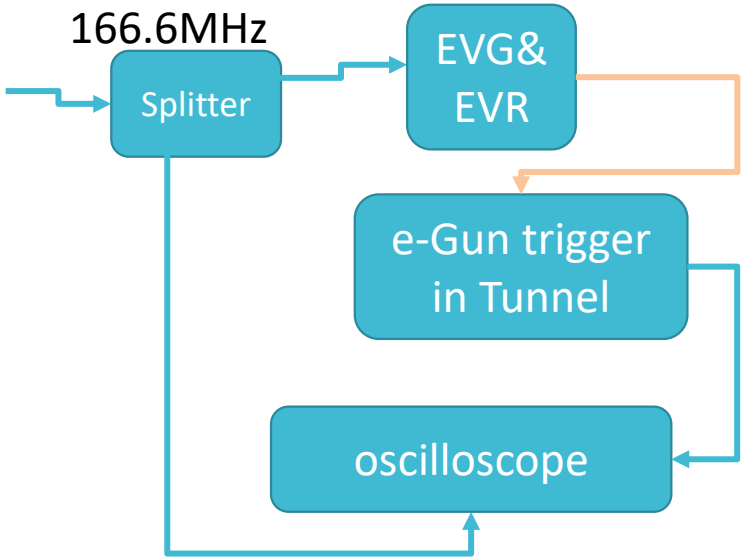


Description	Mean	Std Dev	Max	Min	Peak-peak	Points
Skew, ch1,ch3	-491.93ps	27.353ps	-357.93ps	-560.00ps	202.08ps	43827

- Due to the influence of experimental conditions, only qualitative experiments were conducted
- In the experiment, a heater was used to heat the 400m fiber from 27 degrees to 46 degrees (fiber surface temperature) for two hours, while the output jitter was measured.
- Test result: The output RMS jitter is 27.353ps

Jitter Test

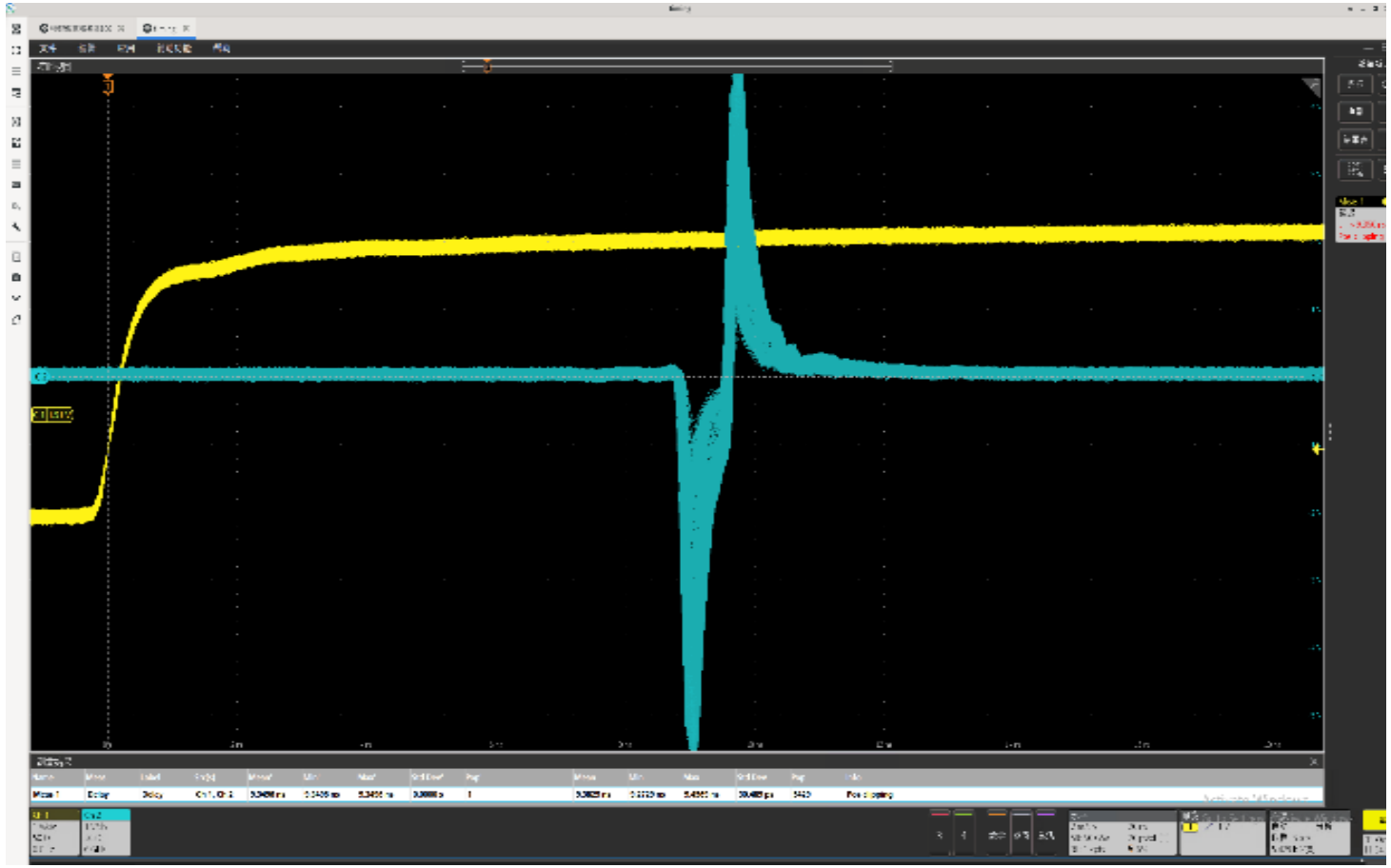
- e-Gun trigger jitter test, RMS jitter <10ps



➢ RMS jitter 9.687ps

Jitter Test

- BRBP08 trigger jitter



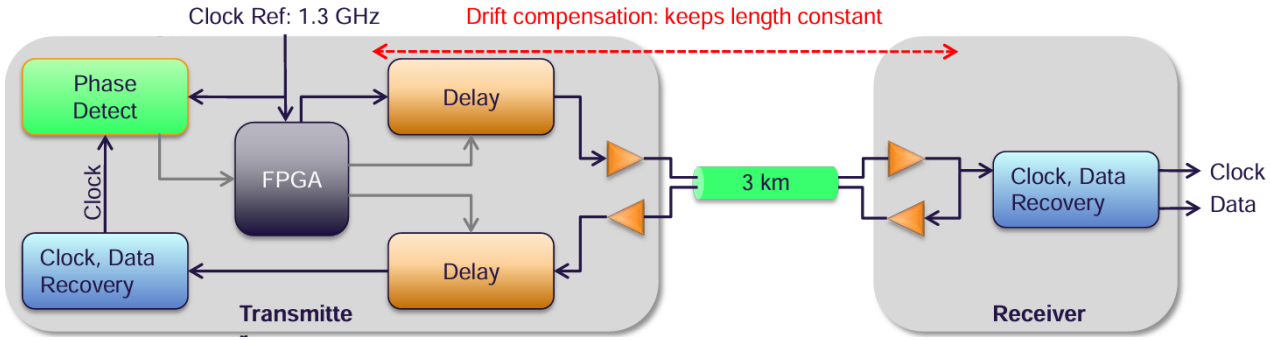
RMS jitter is 22.352ps

long term is 30.489ps （5 days）

Part III

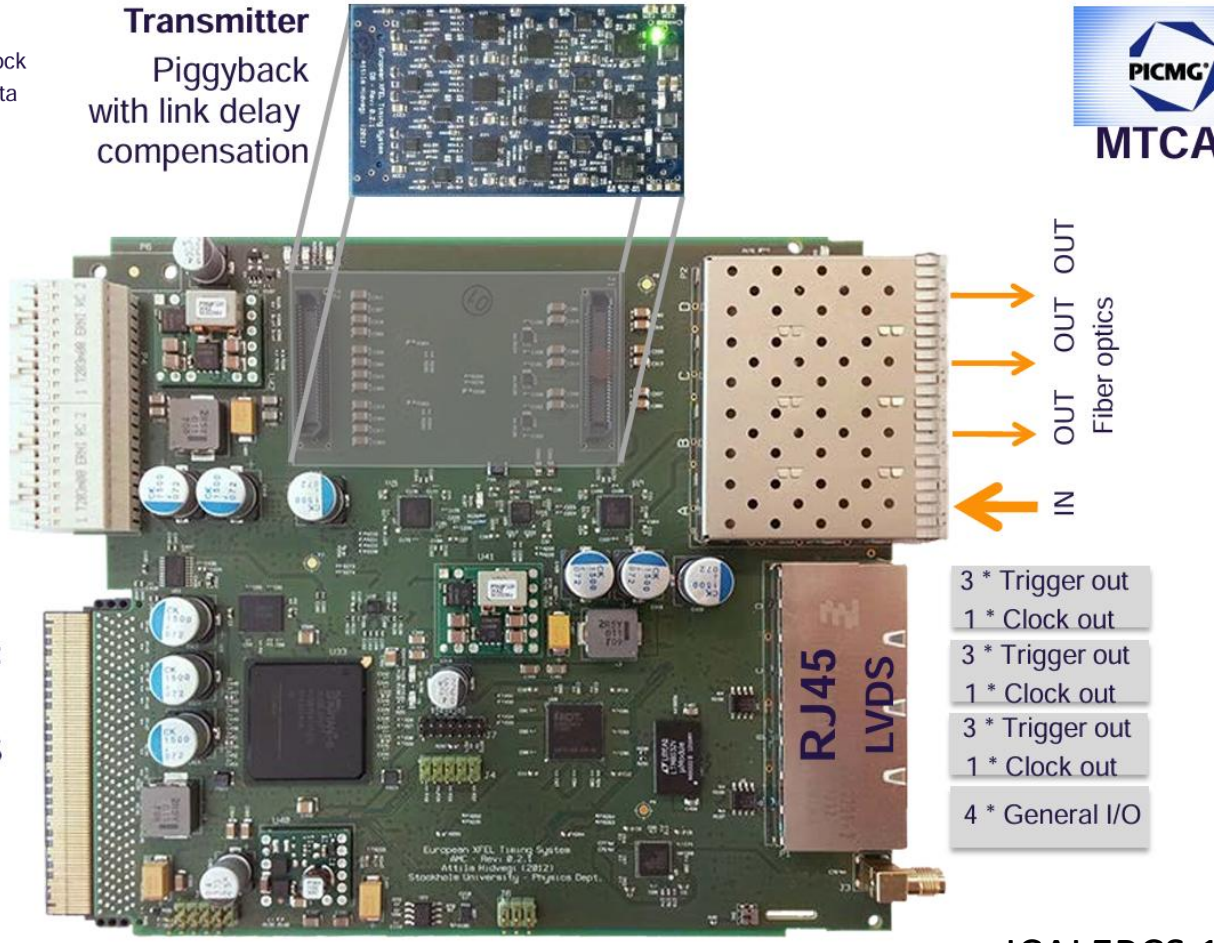
Some Other Timing System Based on MicroTCA

European XFEL



- Fiber optic links @ 1.3GHz
- AMC module is a receiver:
  - It retransmits on one link
  - Or transmits on 3 fiber links with drift compensation (piggyback)
- ps stability (5 …10 ps RMS)
- Clock, trigger and event distribution
- Distribution of data words and tables

X2Timer

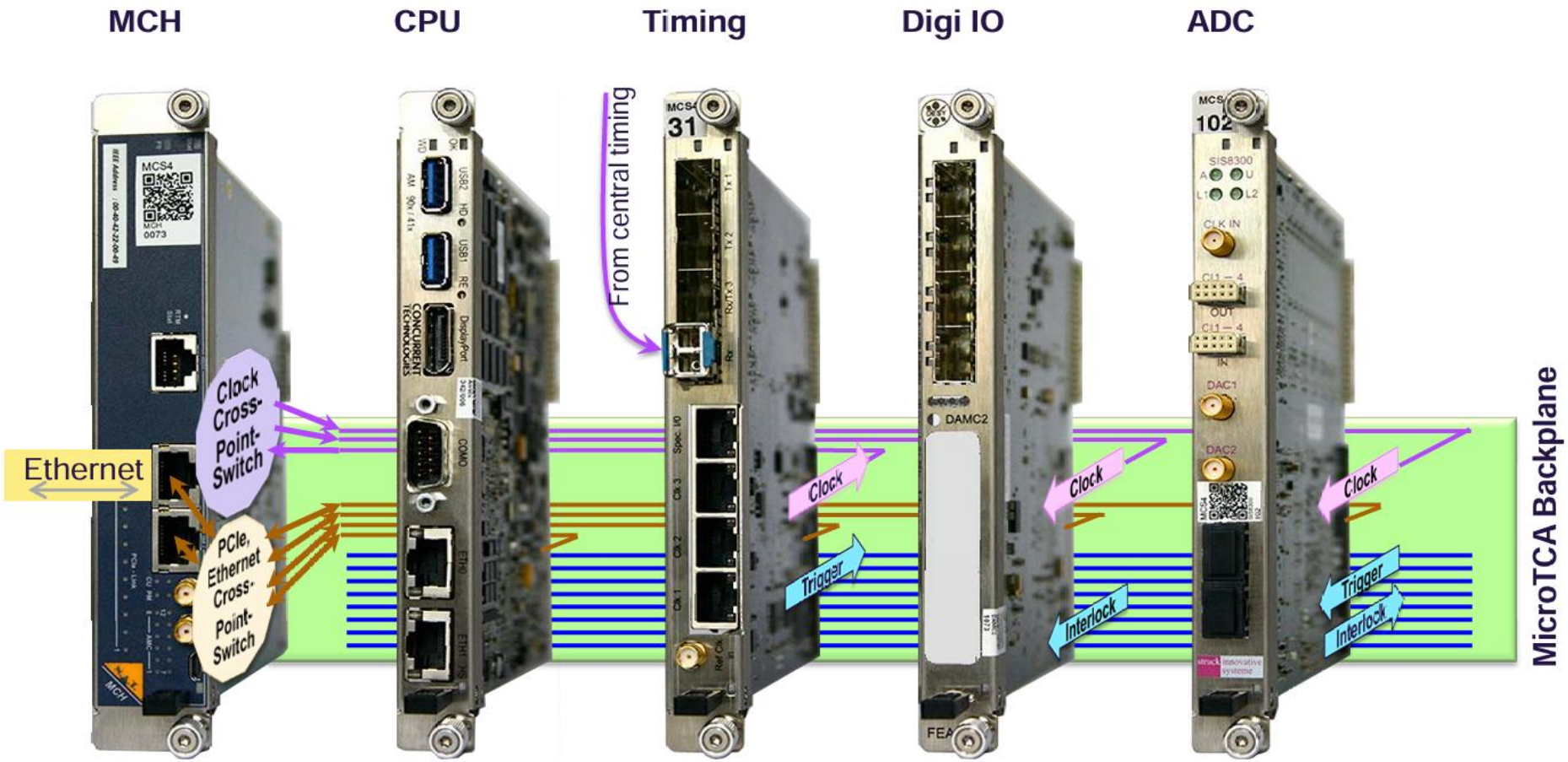


Optional **RTM**:
9 transmitters,
Further triggers or clocks

MicroTCA **backplane**:
TCLKA and TCLKB,
8 * M-LVDS

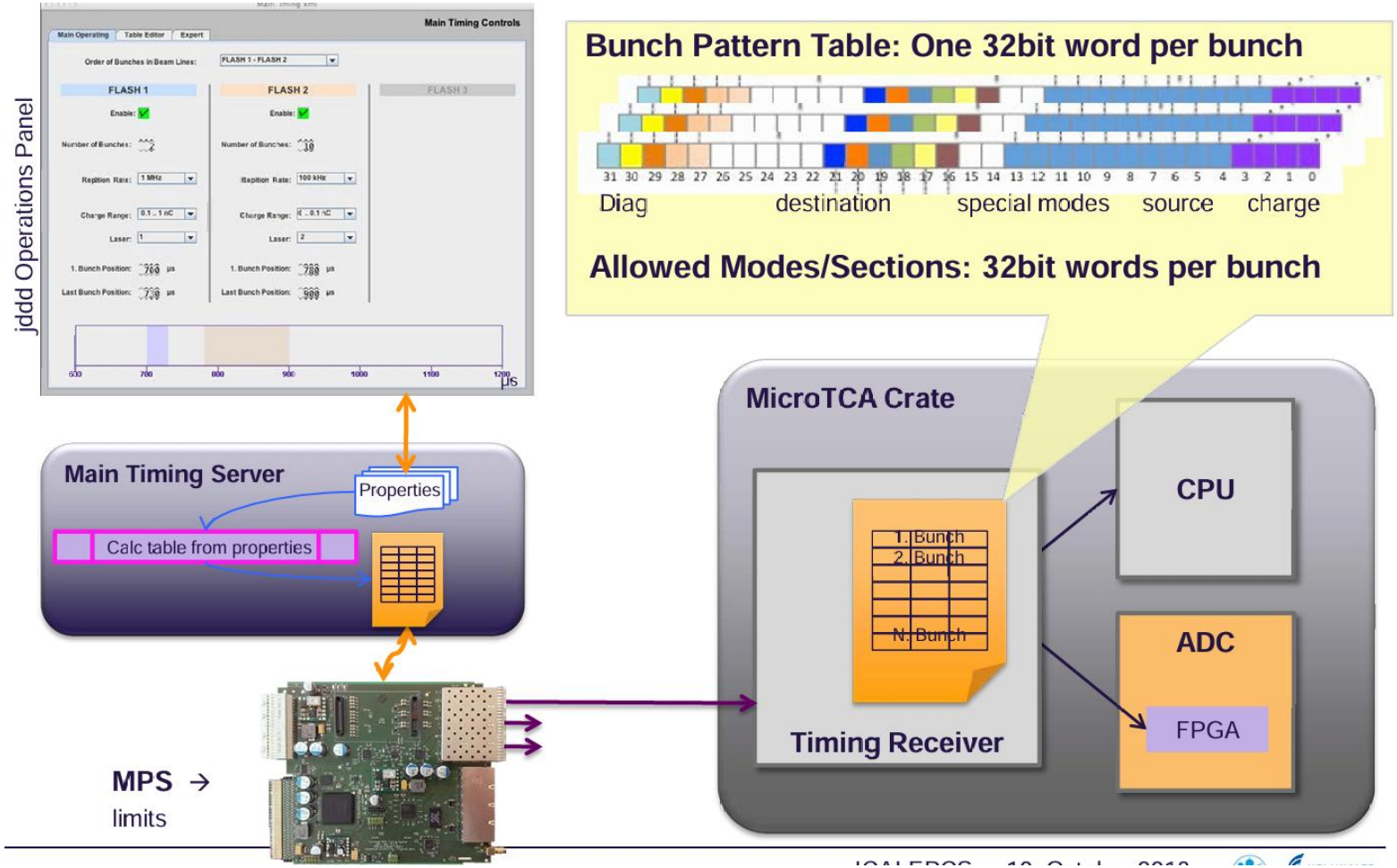
Can be used as transmitter or receiver

MicroTCA.4: Clock and Trigger Distribution

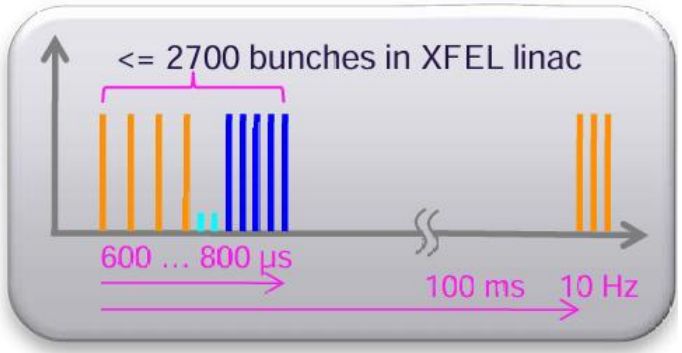


ICALEPCS 13， THCOBB02

Real Time Configuration Data

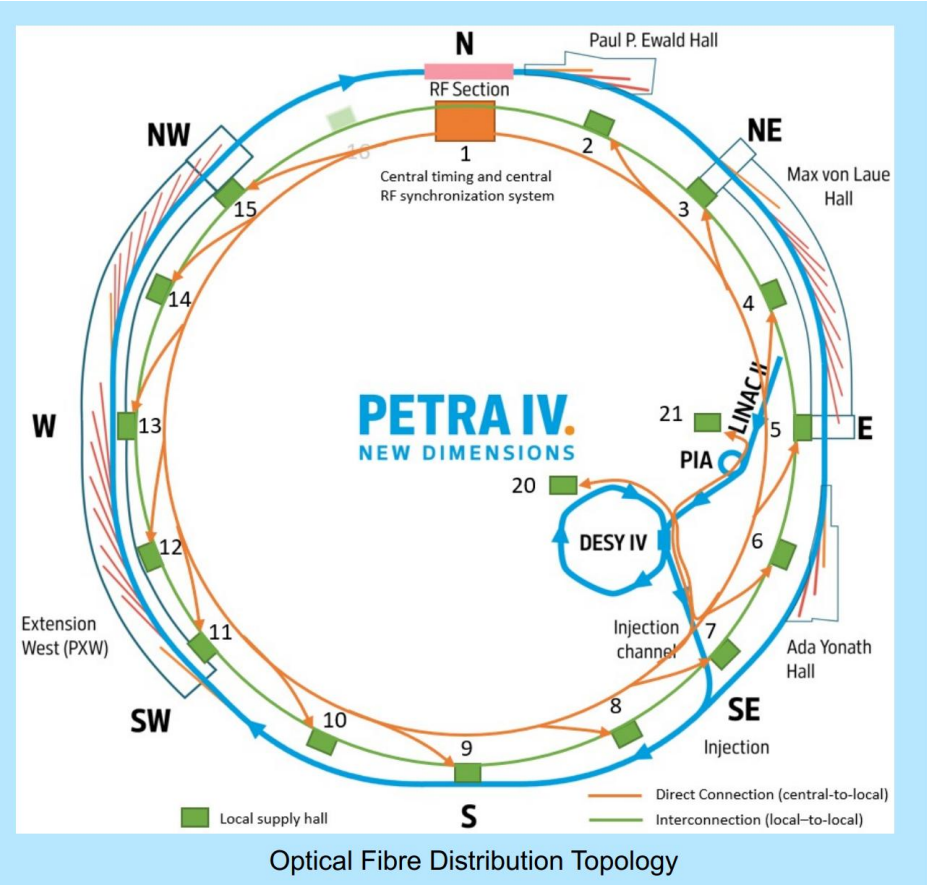


- The XFEL can produce 27 000 bunches per second
- Variable bunch pattern for the users

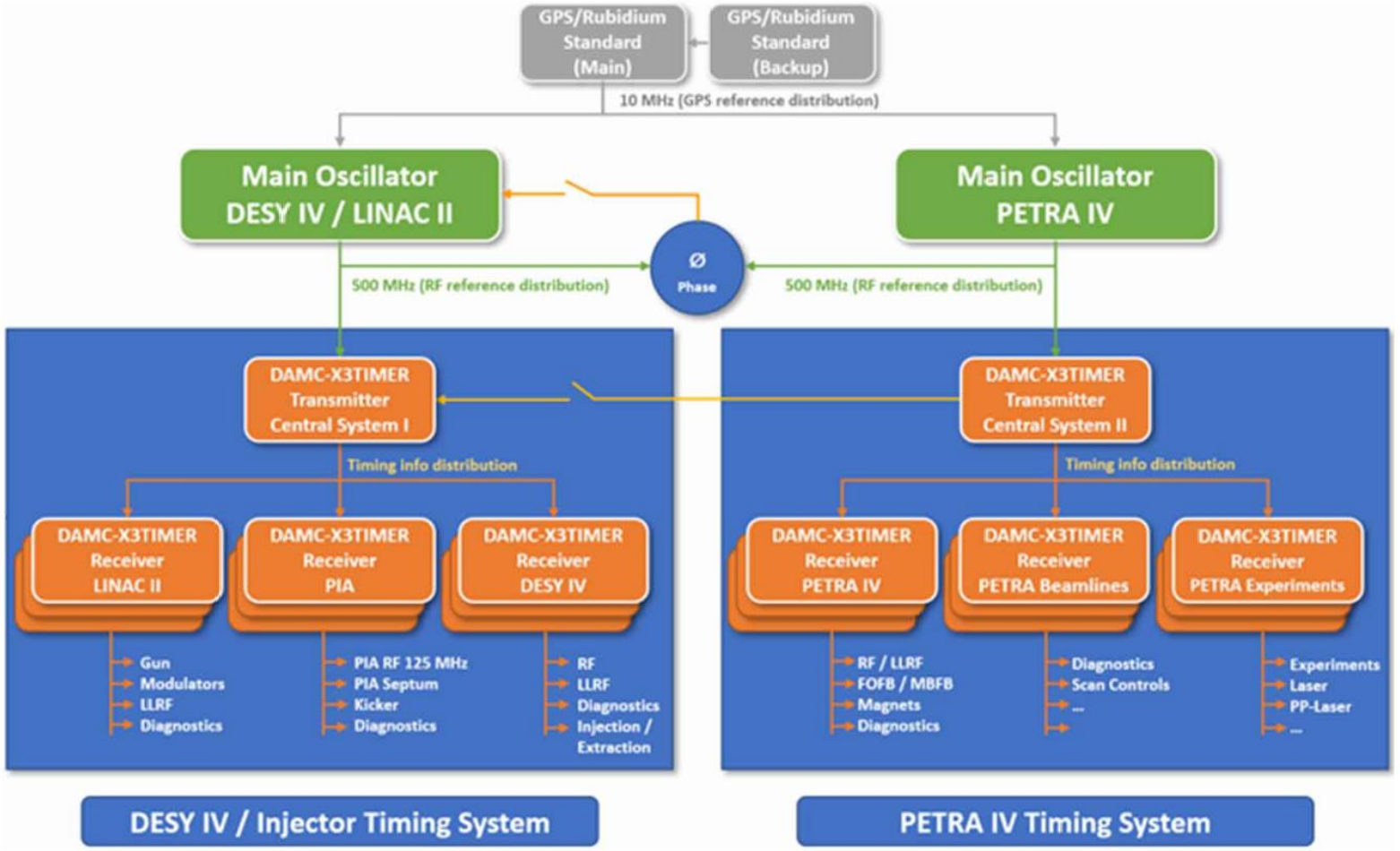


PETRA IV

- PETRA IV： Timing



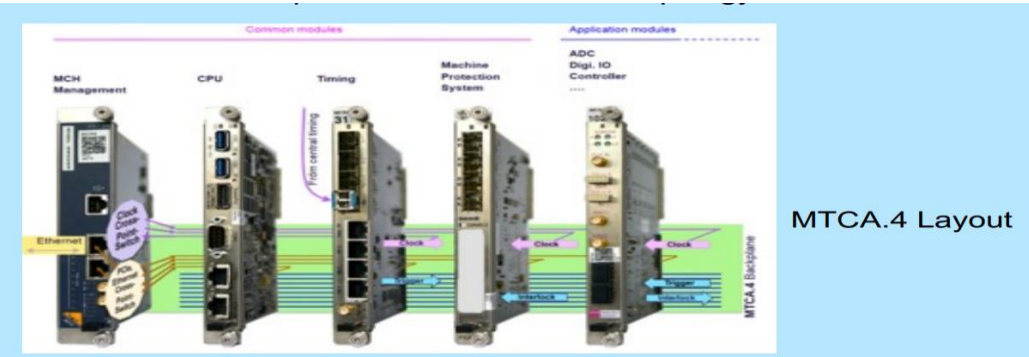
Optical Fibre Distribution Topology



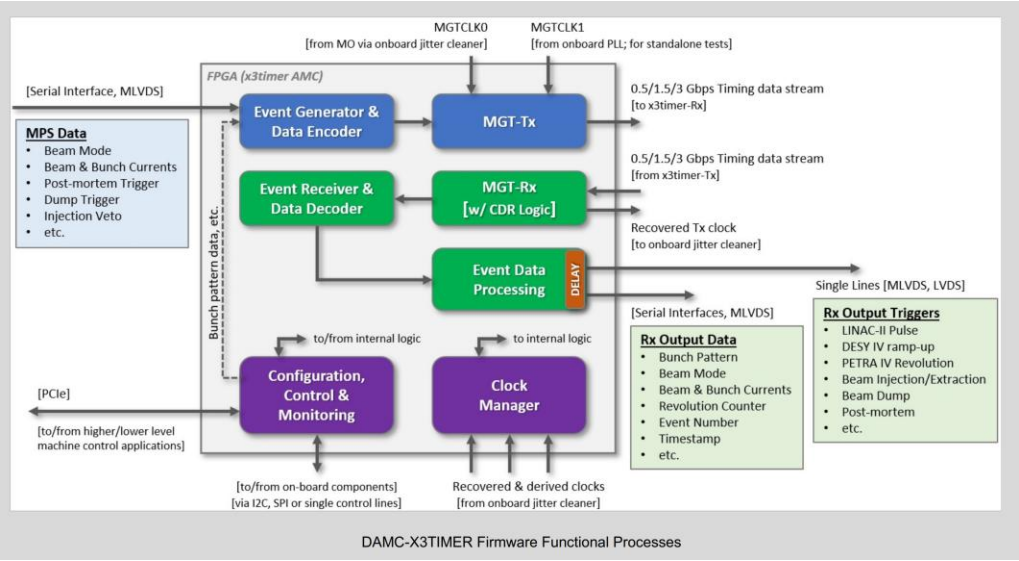
https://accelconf.web.cern.ch/icalepcs2021/papers/thpv025.pdf

PETRA IV

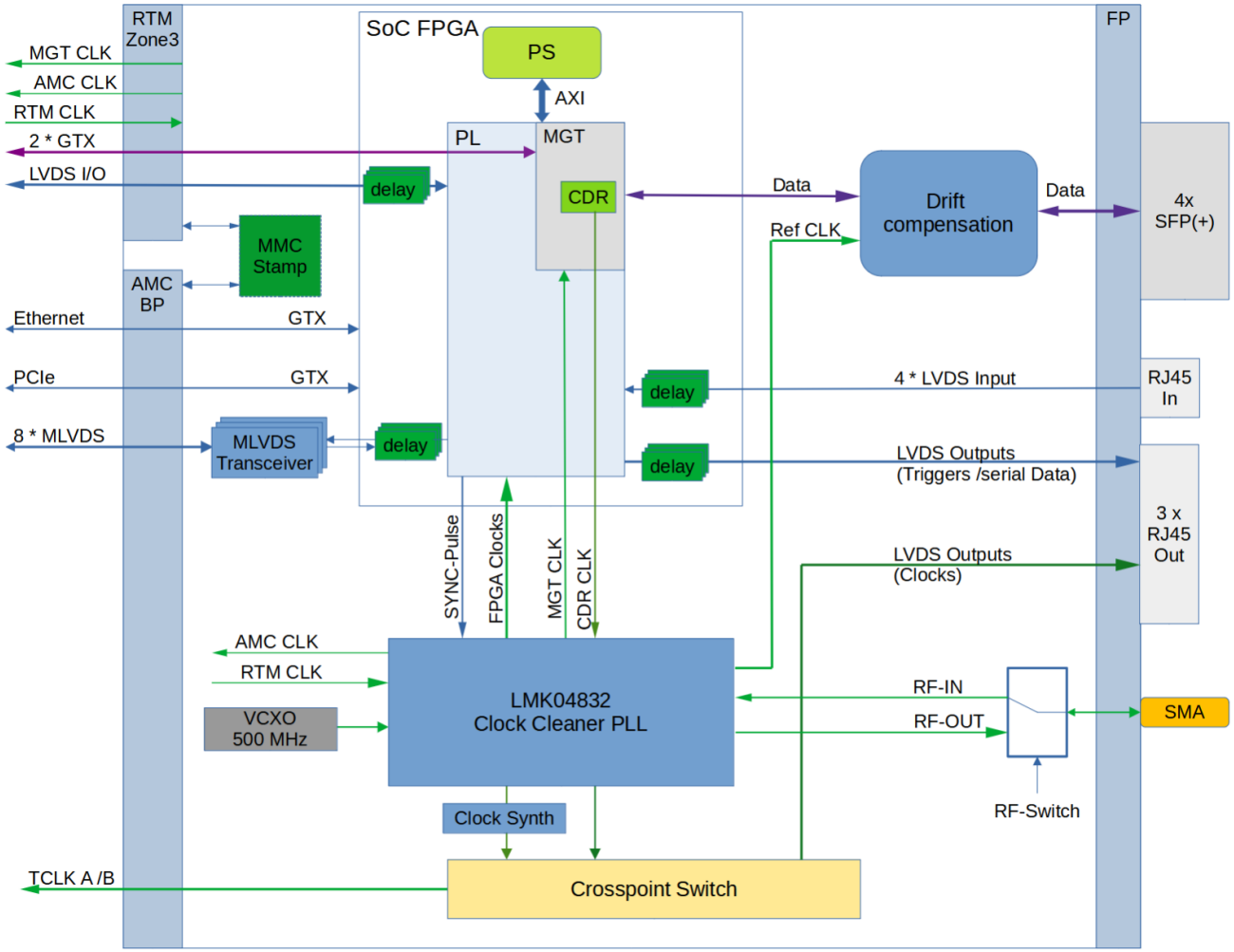
- PETRA IV： DAMC-X3TIMER



MTCA.4 Layout



DAMC-X3TIMER Firmware Functional Processes



DAMC-X3TIMER Hardware Schematic

https://accelconf.web.cern.ch/icalepcs2021/papers/thpv025.pdf

SIRIUS：A MicroTCA.4 TIMING RECEIVER

- Developed a timing receiver board to provide triggers and synchronized clocks for Sirius BPM electronics and other devices
- Timing Receiver： AFC + RTM with 8SFP， can output trigger and clock by FMC board
- BPM and FOFB: same AFC

Figure 1: AFC board with two FMC 5 POF mounted.

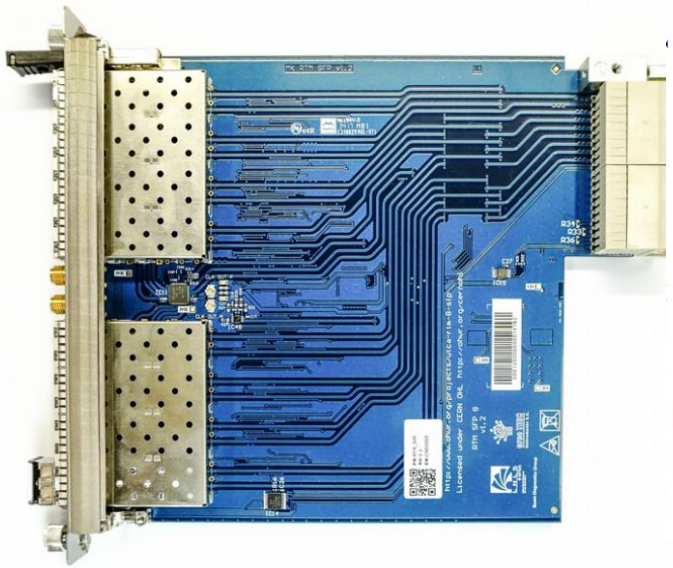


Figure 3: RTM with 8 SFP slots.

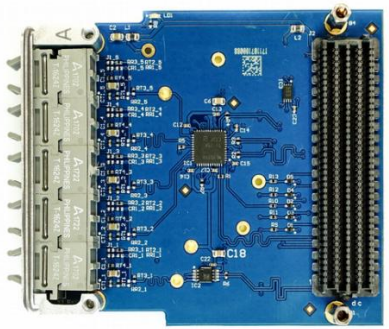
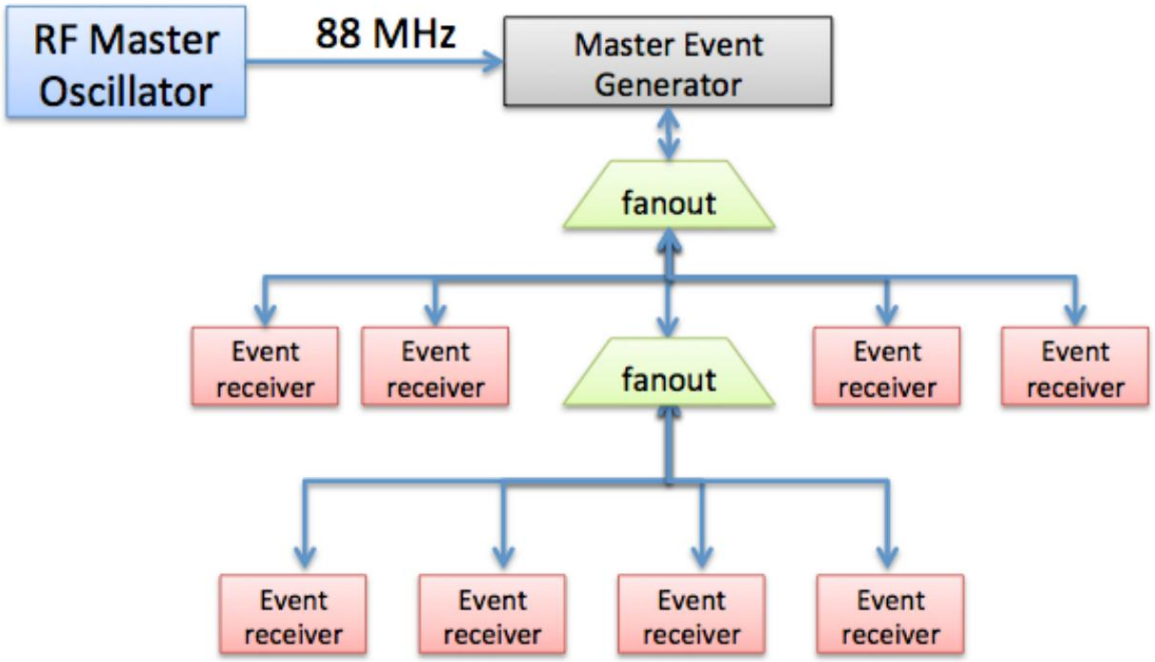


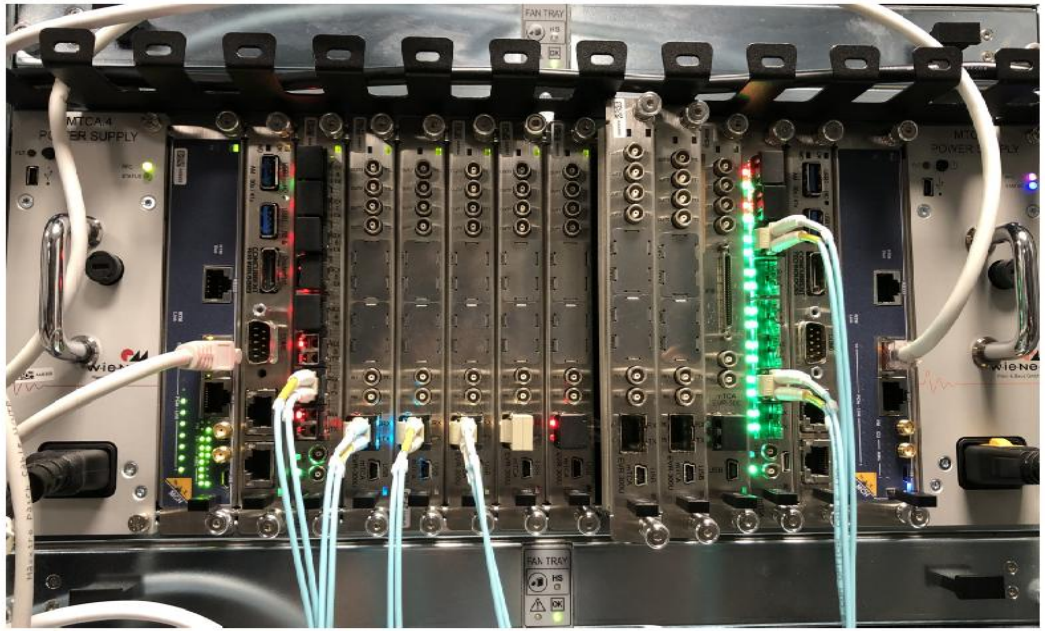
Figure 2: FMC 5 POF, a FMC board with 5 plastic optical fiber outputs.

a general purpose 10- 280MHz I2C programmable XO oscillator (Silicon Labs Si570, 570BCC000121G) that outputs a reference clock to the FPGA GTP transceivers

IBIC2018， WEPA01

European Spallation Source(ESS) Timing System





- The event clock frequency is 88.0525 MHz, divided down from the bunch frequency of 352.21 MHz.
- An integer number of ticks of this clock defines the beam macropulse full length, around 2.86 ms, with a repetition rate of 14 Hz.
- ESS uses the MTCA-EVR-300 and PCIe-EVR-300DC EVRs provided by Micro-Research Finland (MRF)

Proceedings of IPAC2017, Copenhagen, Denmark THPVA064

https://proceedings.jacow.org/icalepcs2023/papers/thmbcmo21.pdf

Summary

- The timing system is one of the most critical systems controlling the operation of the entire accelerator.
- To design and implement such a system, one must understand the machine's operational principles, master relevant timing technologies, and be familiar with performance requirements.
- The High Energy Photon Source (HEPS) timing system has adopted MicroTCA technology, which is increasingly being used in accelerator facilities worldwide.

Thank you!