The development of the MTCA.4 based LLRF system in the UTEF

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Outline

1. Brief introduction of UTEF
2. The development of LLRF
3. Relevant tests
4. Summary

1. Brief introduction of UTEF

Ultrafast Transient Experimental Facility (UTEF) is composed of a synchrotron radiation light source and an electron microscope.

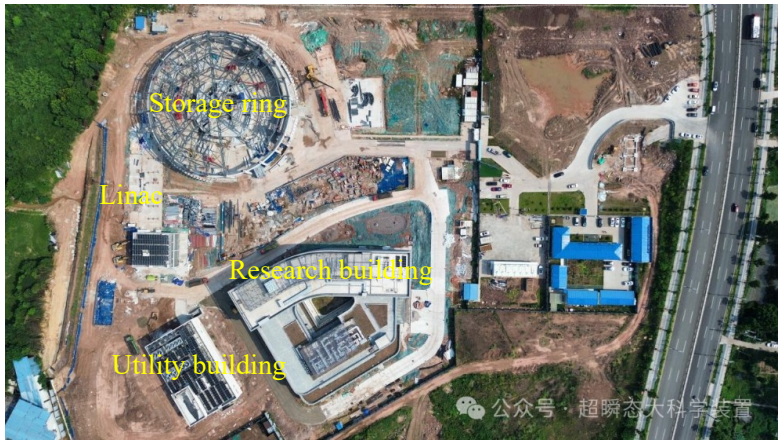
UTEF is developed in 2 phases, phase I is a pre-research project, including a 500MeV light source and an electron microscope platform; phase II including a 3GeV light source and an electron microscope cluster。

Parameters of 500MeV ring

Parameters	Value	Unit
Energy	0.5	GeV
Ring circumference	76.78	m
Beam current	0.5~1	A
Focusing type	QBA	
Natural emittance	8.56	nm rad
Working point（x, y）	6.198, 3.357	-
Length of straight section	8*4	m
Working frequency	499.8	MHz
Energy loss per turn	4.34	keV
Natural energy spread	0.37×10^{-3}	

Timeline of UTEF:

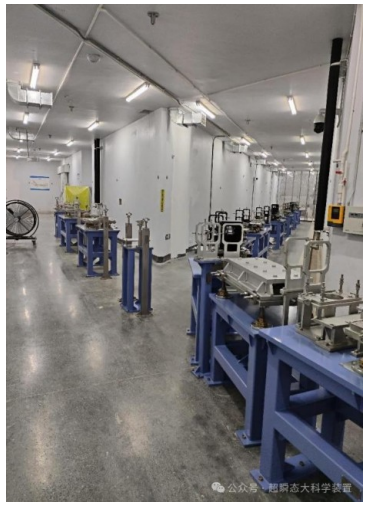
2024/04
Facility construction starts
2025/05
Linac starts install
2026/01
Storage ring starts install
2026/12
Project completed



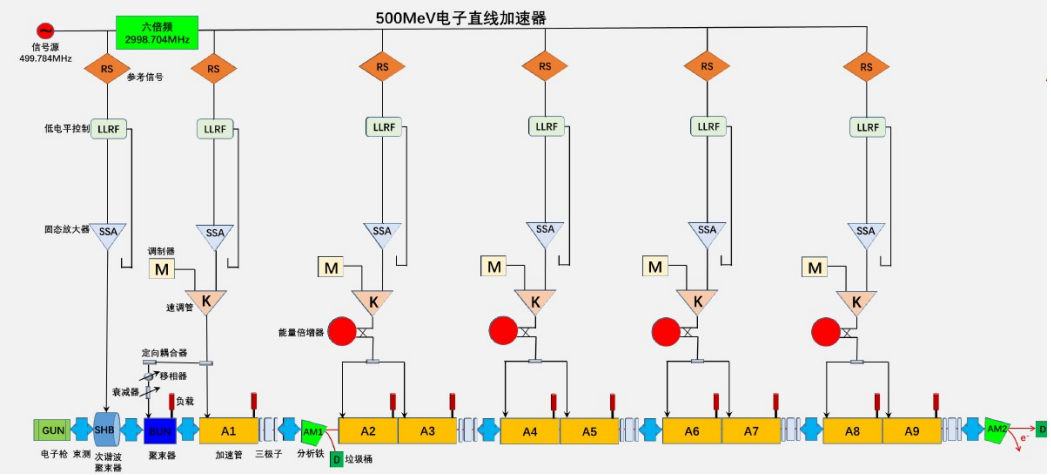
Aerial view


Storage ring


Linac


Beam transport line

2. The development of LLRF



The layout of the Linac

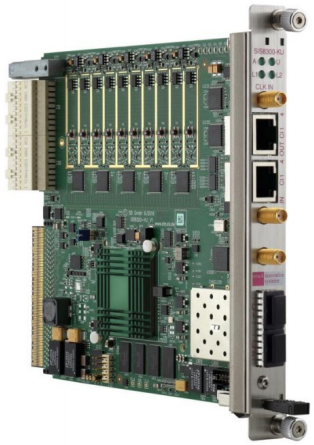
Parameters of 500MeV Linac

Parameters	value	unit
Beam energy	500	MeV
Beam charge	≥1	nc
Beam length	≤1	ns
Energy spread	≤0.5 (rms)	%
Normalized emittance	≤50 (rms)	mm.mrad
Repetition rate	2	Hz
Working frequency	499.79/2998.74	MHz
Amplitude stability	0.2 (rms)	%
Phase stability	0.1 (rms)	°

2.1 MTCA.4 LLRF

NATIVE-R2

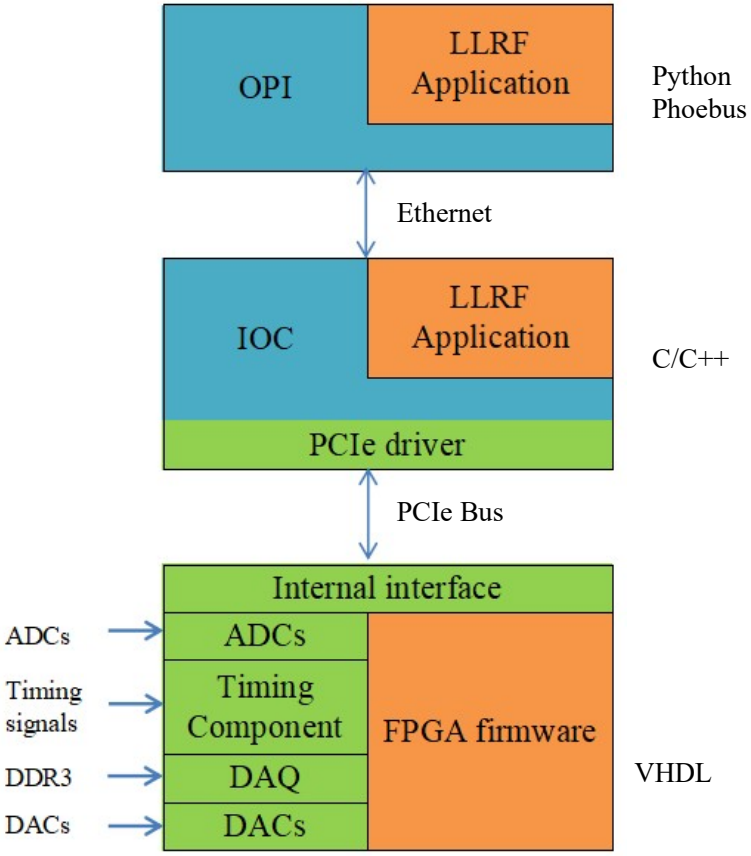
DWC8VM1



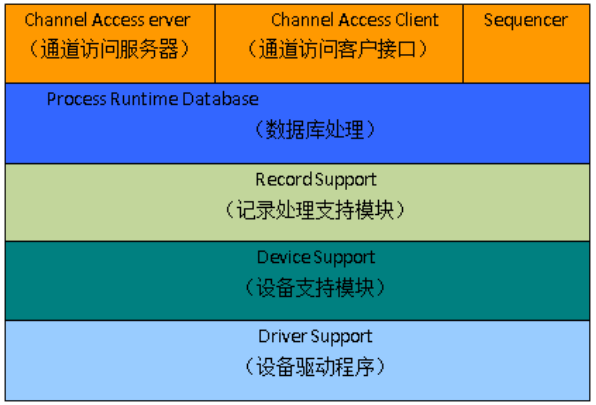
SIS8300KU

SIS8300-KU Properties

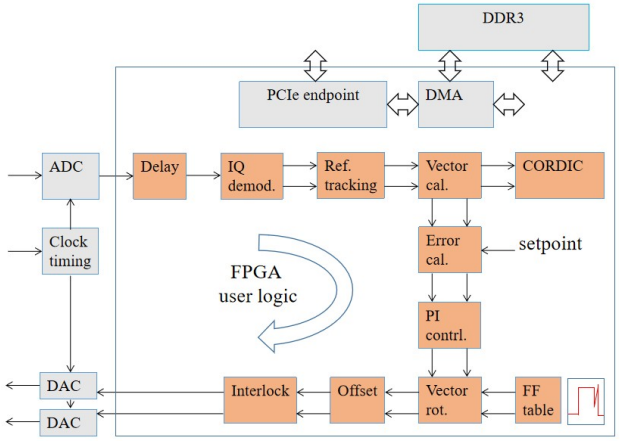
- 10 Channels 125 MS/s 16-bit or 250 MS/s 14-bit ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- White Rabbit Clock Option for SFP+ Ports
- Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
- XCKU040-1FFVA1156C Kintex Ultrascale FPGA
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual boot
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- Vivado Project for Custom Firmware Development
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible



Software and firmware

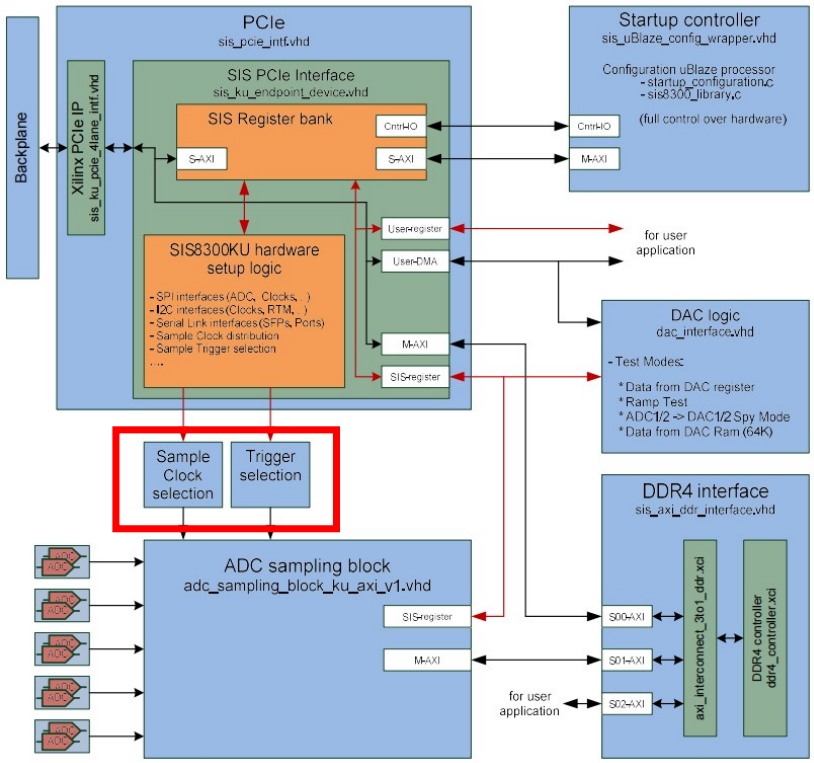


EPICS IOC software diagram
Debian11， EPICS base7



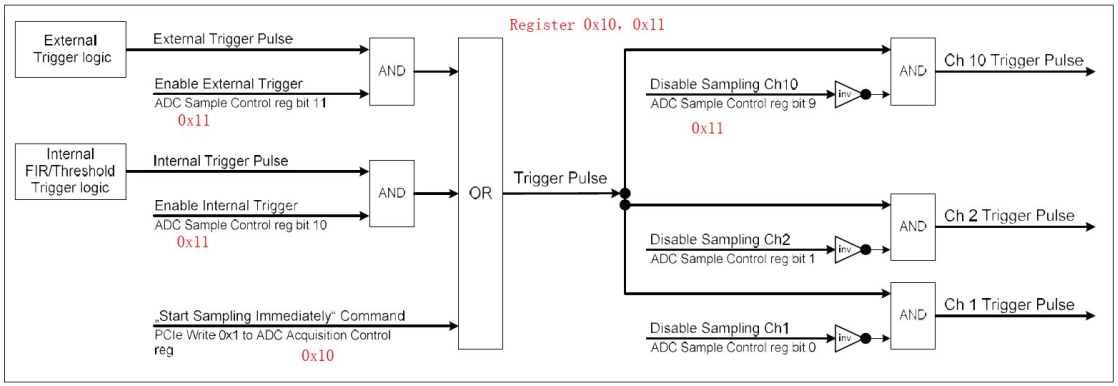
LLRF firmware

Sample clock/Trigger selection

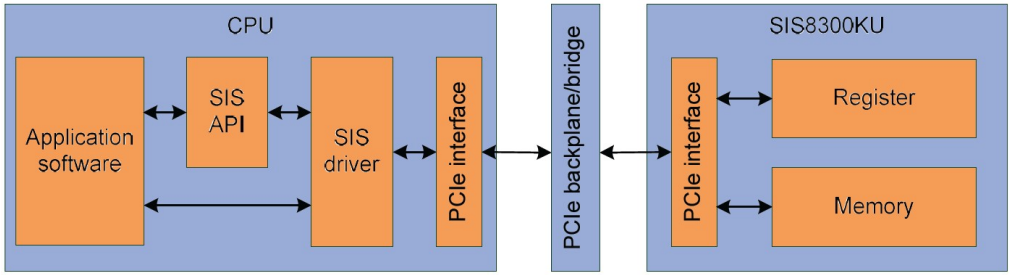


SIS8300KU
AXI-based Xilinx FPGA framework

```
/*****************************************************************************************/
/* initialize clock distribution multiplexer                                             */
/*****************************************************************************************/
// clock_source = 0:            internal 250MHz clock oscillator
// clock_source = 1:            external SMA clock
// clock_source = 2:            external HARLINK clock
// clock_source = 3:            external RTM clock 0 1 (no MUX setting necessary
// clock_source = 4:            external RTM clock 2
// clock_source = 5:            external TCLKA
// clock_source = 6:            external TCLKB
// else:                        internal 250MHz clock oscillator

clock_source = 0 ;   // internal 250MHz clock oscillator

*(pcie_register_axi_ptr + SIS8300_USER_CONTROL_STATUS_REG) =  0x00001;  // set user Led U
initialize_process_state = INITIALIZE_CLOCK_MUX_STATE ; //
sis_write_control_reg(0x80000000 + (initialize_process_state & 0xff)); // enable pcie register access

initialize_clock_distribution_multiplexer(pcie_register_axi_ptr,  clock_source);

*(pcie_register_axi_ptr + SIS8300_USER_CONTROL_STATUS_REG) =  0x10000;  // clr user Led U

#ifdef DEBUG_PRINTS
       print("initialize clock distribution multiplexer finished\n\r");
#endif
```



Register space



Offset	Access	Function	Note
0x00	R	Module Identifier/Firmware Version register	
0x01	R	Serial number register	
0x02	R/W	reserved	
0x03	R/W	reserved	
0x04	R/W	User Control/Status register (JK)	
0x05	R	Firmware Options register	
0x06	R/W	ADC Temperature Sensor interface register	
0x07	R	PCIe Status register	1
0x10	R/W	ADC Acquisition Control/Status register	
0x11	R/W	ADC Sample Control register	
0x12	R/W	MLVDS Input/Output Control/Status register	
0x13	R/W	RJ45 Connector Input/Output Control/Status register	1
0x14	R/W	SFP1 Link Control/Status register	1
0x15	R/W	SFP2 Link Control/Status register	1
0x16	R/W	Port 12 Link Control/Status register	1
0x17	R/W	Port 13 Link Control/Status register	1
0x18	R/W	Port 14 Link Control/Status register	1
0x19	R/W	Port 15 Link Control/Status register	1

Register for hardware configuration:
Address map from 0x00-0x3FF

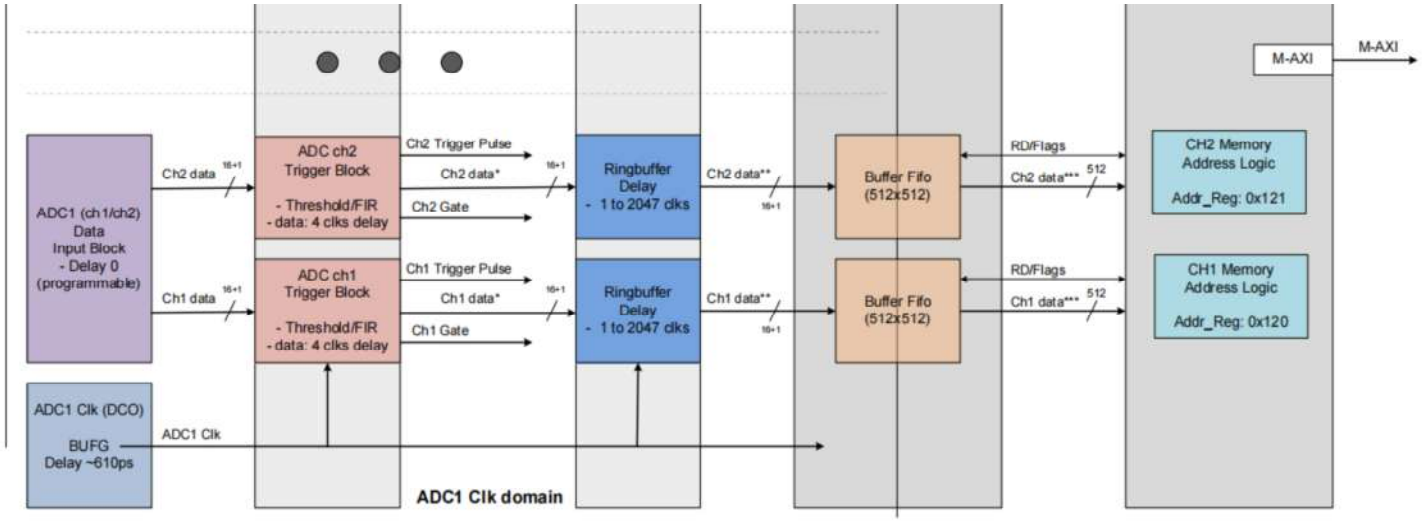
No.	Offset	Function	Bit	RW	PV name
1	0x400	Ch1 delay	(15 downto 0)	R/W	SET_CH1_DELAY
		Ch2 delay	(31 downto 16)		SET_CH2_DELAY
2	0x401	Ch3 delay	(15 downto 0)	R/W	SET_CH3_DELAY
		Ch4 delay	(31 downto 16)		SET_CH4_DELAY
3	0x402	Ch5 delay	(15 downto 0)	R/W	SET_CH5_DELAY
		Ch6 delay	(31 downto 16)		SET_CH6_DELAY
4	0x403	Ch7 delay	(15 downto 0)	R/W	SET_CH7_DELAY
		Ch8 delay	(31 downto 16)		SET_CH8_DELAY
5	0x404	Ch9 delay	(15 downto 0)	R/W	SET_CH9_DELAY
		Ch10 delay	(31 downto 16)		SET_CH10_DELAY
6	0x405	Trigger delay	(15 downto 0)	R/W	SET_TRG_DELAY
7	0x406	ch1 start time	(15 downto 0)	R/W	CH1_SETTIME
		Ch2 start time	(31 downto 16)		CH2_SETTIME
8	0x407	Ch3 start time	(15 downto 0)	R/W	CH3_SETTIME
		Ch4 start time	(31 downto 16)		CH4_SETTIME

The external register interface provides the user with the possibility to implement up to 3072 32bit registers on the top level of the HDL design. The registers are embedded into the devices regular register space from address 0x400 to 0xFFF.

DDR4 Memory

Address 0x0 - 0x7FFFFFFF: DDR4 selected Memory

Each ADC channel has its own Memory Address Control Logic
Memory Sample Start Block Address of each channel
ch1-ch10: 0x000000，0x100000……0x900000



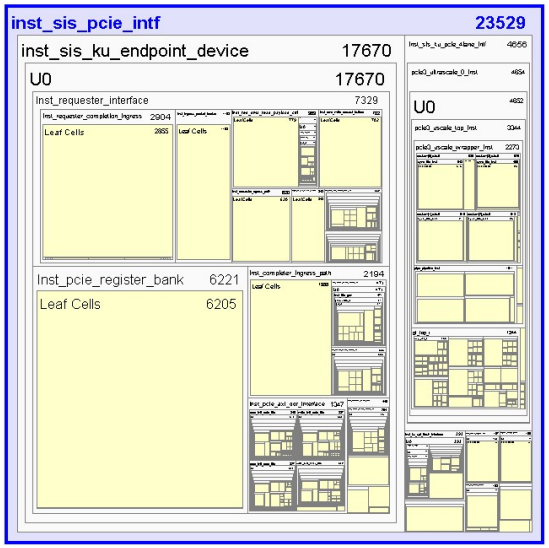
ADC sampling logic

DMA Space

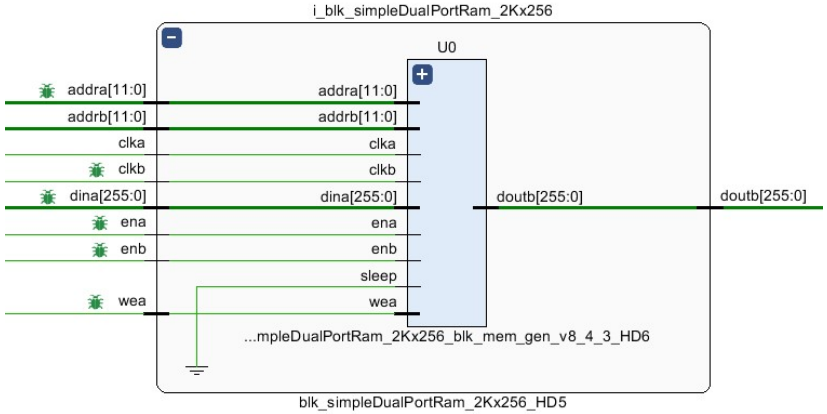
User DMA space:
Address 0x80000000 - 0x9FFFFFFF: free User DMA space
Address 0xA0000000 - 0xAFFFFFFF: Test-BRAM User DMA space
Address 0xB0000000 - 0xB000FFFF: DAC-RAM
Address 0xC0000000 - 0xC7FFFFFF: SFP1-BRAM User DMA space
Address 0xC8000000 - 0xCFFFFFFF: SFP2-BRAM User DMA space
Address 0xD0000000 - 0xD3FFFFFF: PORT12-BRAM User DMA space
Address 0xD4000000 - 0xD7FFFFFF: PORT13-BRAM User DMA space
Address 0xD8000000 - 0xDBFFFFFF: PORT14-BRAM User DMA space
Address 0xDC000000 - 0xDFFFFFFF: PORT15-BRAM User DMA space

DMA address for Feedforward Table:

I	:	0XA0000000-0XA00001FFF
Q	:	0XA00002000-0XA00003FFF
Amplitude	:	0XA00004000-0XA00005FFF
Phase	:	0XA00006000-0XA00007FFF

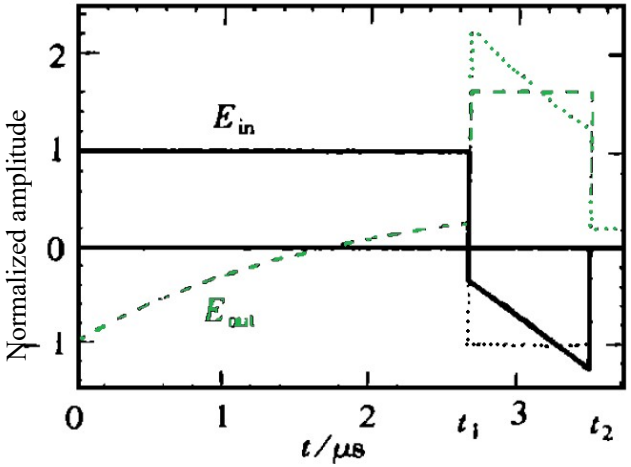


Hierarchy of sis_pcie_intf



Schematic of simpleDualPortRam

Pulse compressor

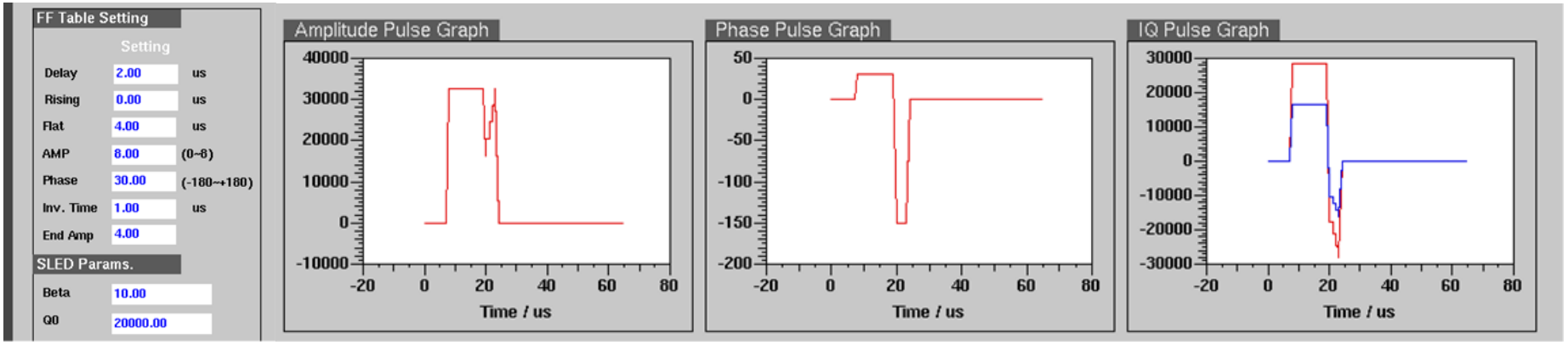


Waveform of output of Pulse compressor

To get a flat-top pulse, amplitude of SLED input pulse should follow the equations below

$$E_{in}(t_1 \le t < t_2) = \frac{C}{\alpha - 1} + \left(1 - e^{-t/T_c} - \frac{C}{\alpha - 1}\right) \alpha e^{\frac{(\alpha-1)(t-t_1)}{T_c}}$$

$$c = -\frac{\left[1 + (1 - e^{-t_1/T_c})\,\alpha e^{(\alpha-1)(t_2-t_1)/T_c}\right](\alpha - 1)}{1 - \alpha e^{(\alpha-1)(t_2-t_1)/T_c}},$$



Feedforward table


Amplitude/Phase Settings
Trigger delay
Sample start time
A/P correction
Attenuator settings
Interlock settings
Attenuation compensation
Waveforms of AP and IQ
Feedforward Table
Feedback Control

Phoebus OPI

2.2 SSA, CLK&LO

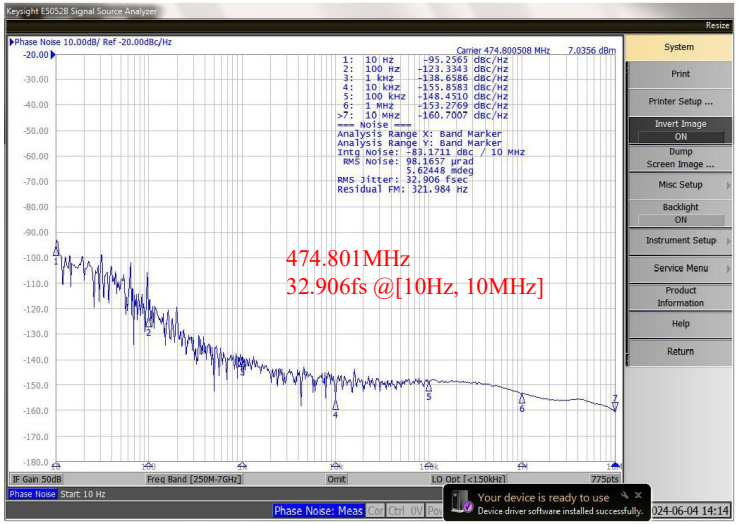
Solid state amplifier

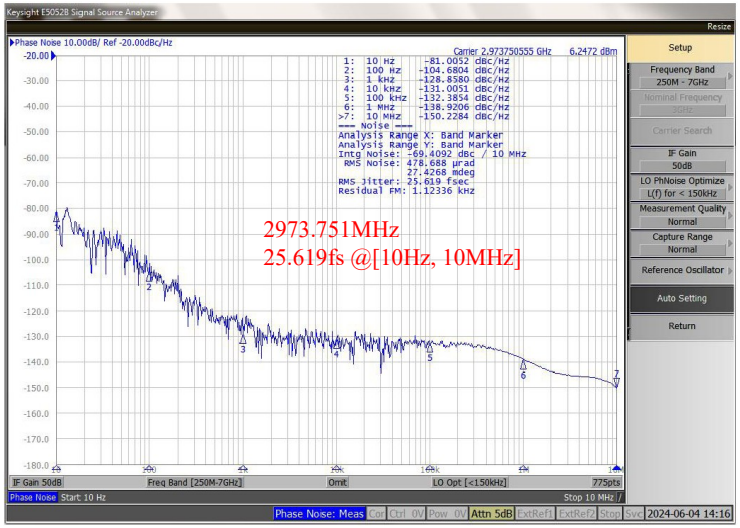
1.Working frequency：499.784MHz/2998.704MHz
2.Bandwidth：≥±2.5MHz@1dB
3. Pulse width：0.5-30μs/0.5-4μs
4.Repetition rate：1-50Hz
5. Output power：≥ 2000W/1000W
6.Rising edge/Falling edge：≤0.1/0.1μs
7.Rising edge jitter：≤ 5ns
8. Pulse flatness：≤ 0.2% (rms)
9. Pulse phase shift：≤ 1 ° (rms)
10. Amplitude stability：≤ 0.02% (rms)
11. Phase stability：≤ 0.02 ° (rms)

CLK & LO

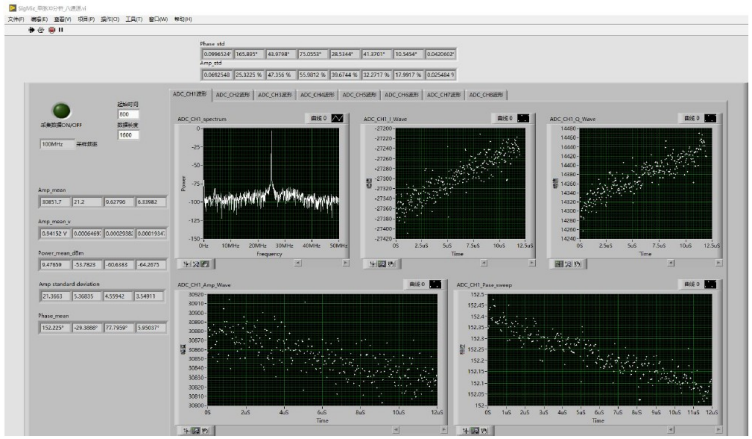
No.	Items	Frequency
1	Main RF	499.79/2998.74MHz
2	LO	474.80/2973.75MHz
3	IF	24.99MHz
4	ADC Clock	124.95MHz

1. Working frequency：499.790/2998.74MHz
2. Input power（CW）：0-3dBm
3. Ref. signal power（CW）：≥ 15dBm
4. LO signal power（CW）：≥ 15dBm
5. Clock signal power（CW）：≥ 15dBm
6 .LO phase noise：<50/36fs @[10Hz, 10MHz]
7. Harmonic suppression：> 50dBc
8. Spurious noise suppression：> 65dBc
9. Power stability：< ±0.1dB（1min）

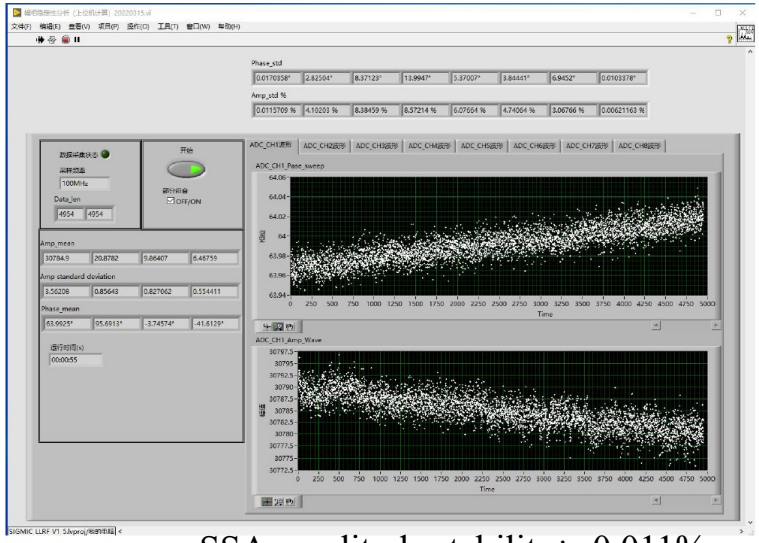




The phase noise of LO signals

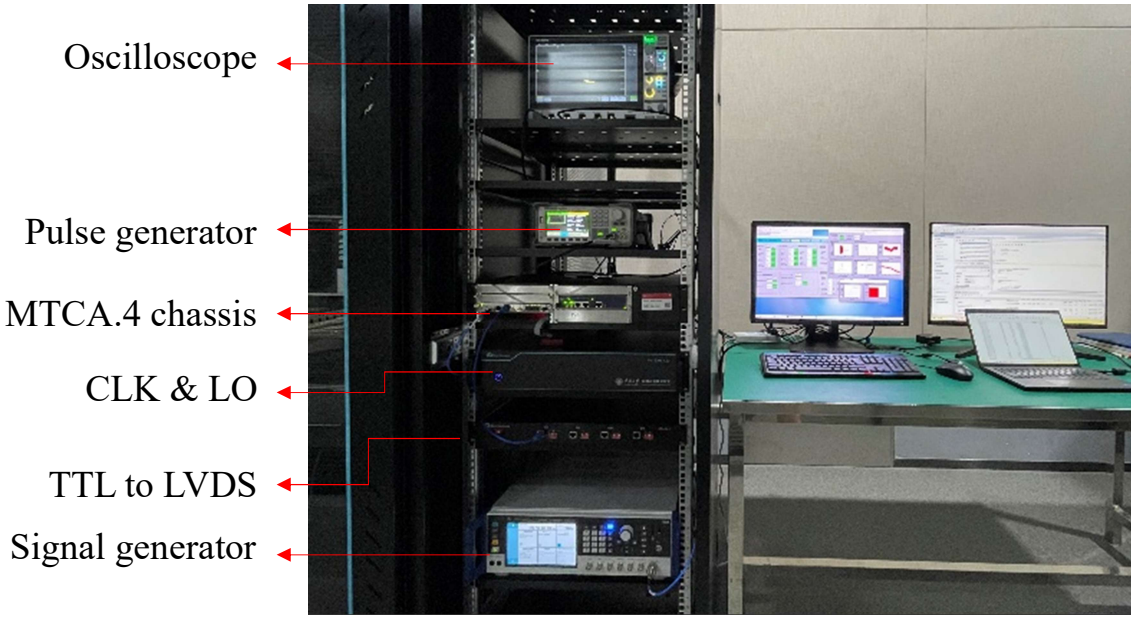


SSA pulse flatness:0.2% (rms)
SSA phase shift:1° (rms)

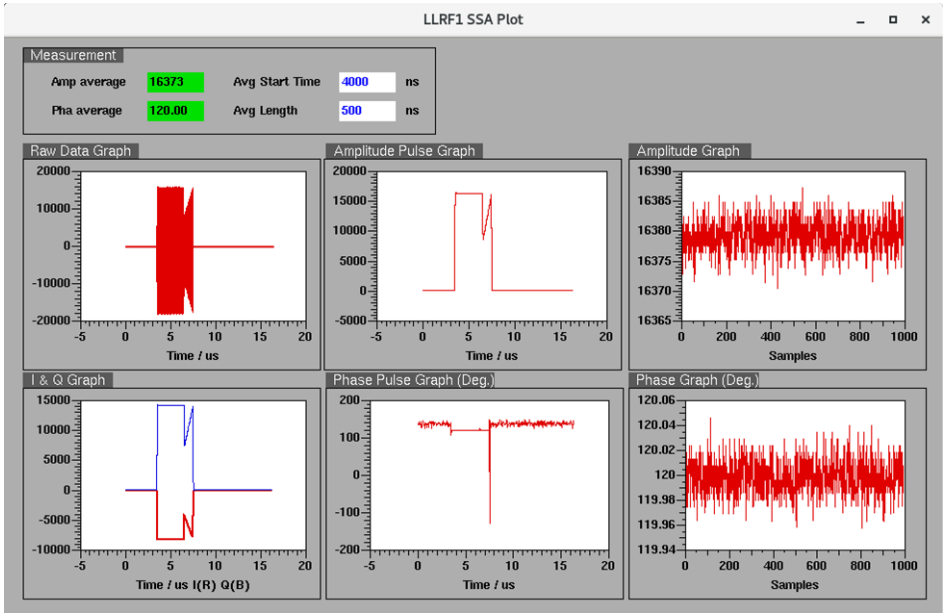


SSA amplitude stability： 0.011%
SSA phase stability： 0.017

3. Relevant tests



Desktop testing



A/P stabilities(rms): 0.01%, 0.01°

3.1 Klystron acceptance test

Klystron
E37302A, 45MW, 2998MHz
Canon electron tubes & devices Co., LTD

Modulator

Pulse generator,
LVDS Converter,
MTCA.4 LLRF,
CLK&LO

Power meter

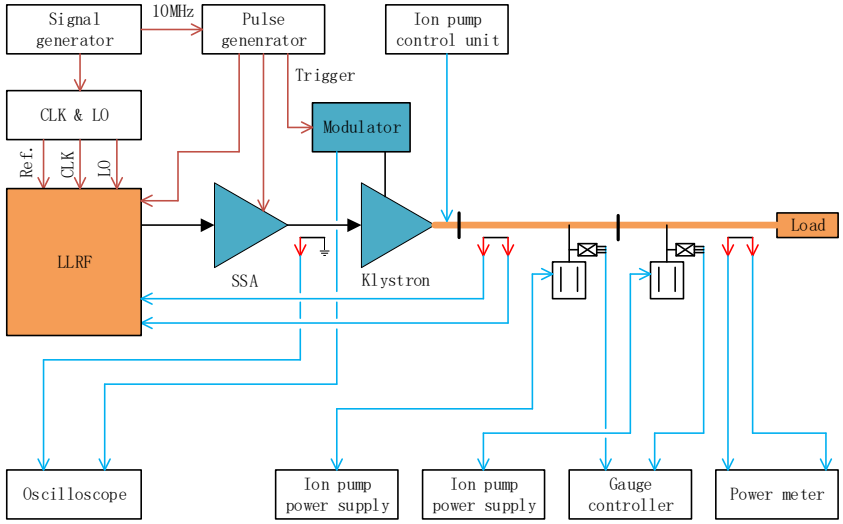
Solid
state amplifier

Vacuum

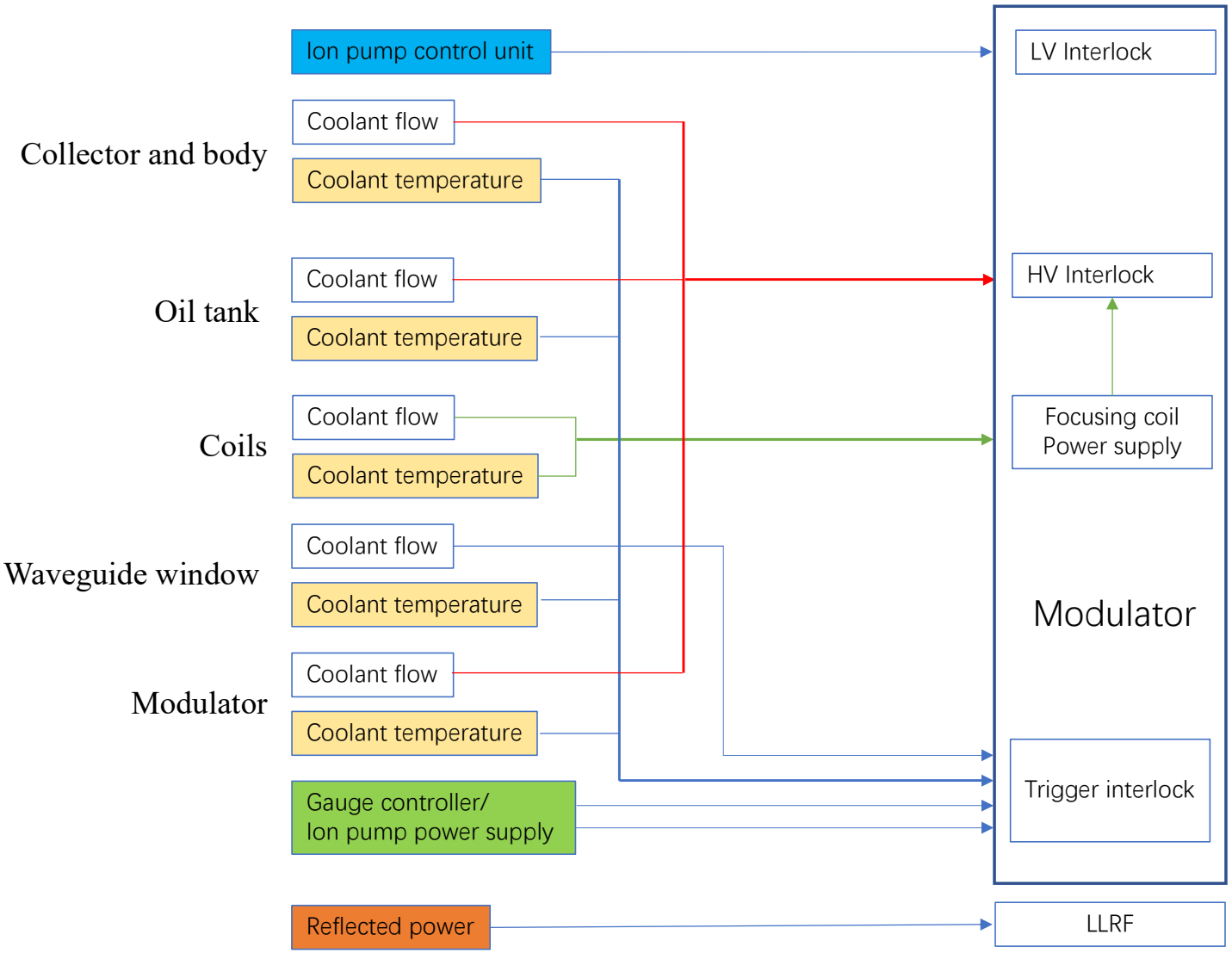
Modulator
control

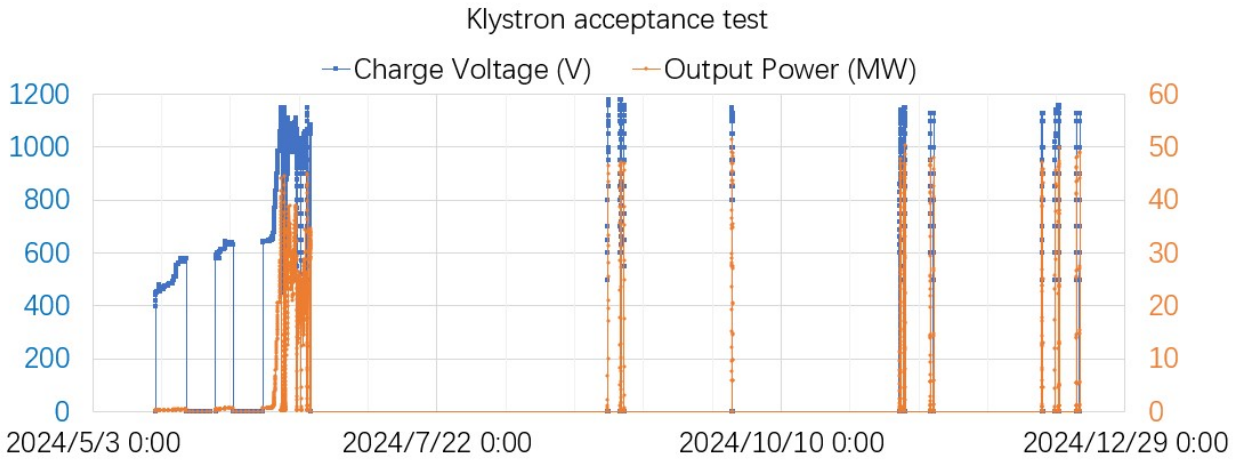
Oscilloscope

Signal
generator

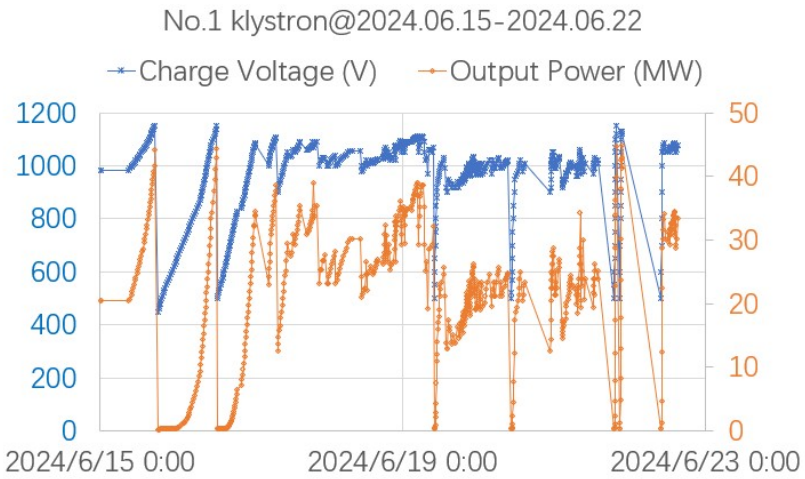


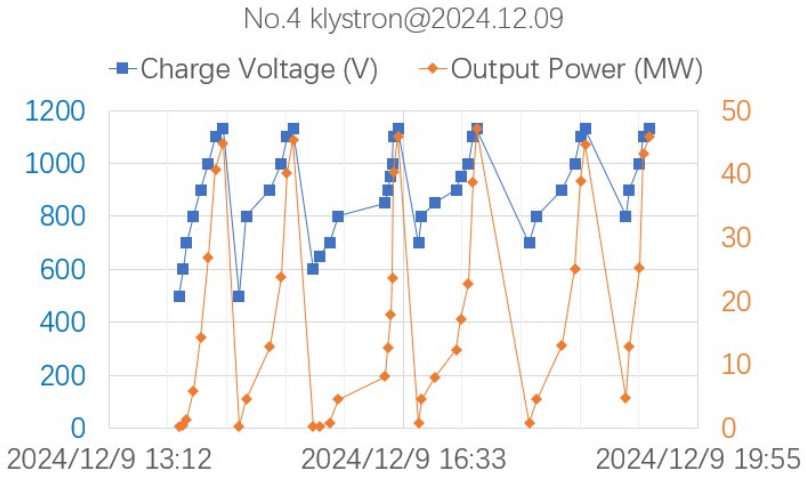
Blocks of test platform


Ion pump control unit
Collector and body
Coolant flow
Coolant temperature
Oil tank
Coolant flow
Coolant temperature
Coils
Coolant flow
Coolant temperature
Waveguide window
Coolant flow
Coolant temperature
Modulator
Coolant flow
Coolant temperature
Gauge controller/
Ion pump power supply
Reflected power
LV Interlock
HV Interlock
Focusing coil
Power supply
Modulator
Trigger interlock
LLRF

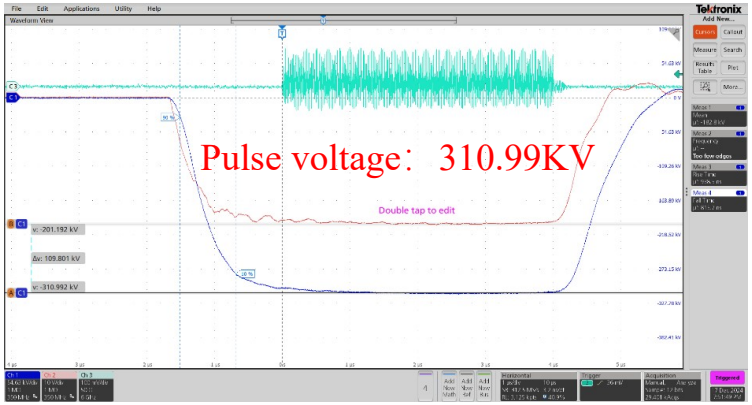


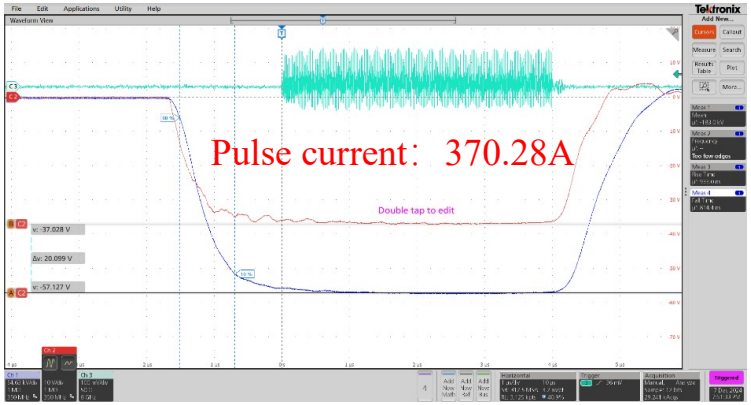
Klystron	RF conditioning time
No.1	2024.5.17-9.3
No.2	2024.9.28-11.7
No.3	2024.11.13-11.14
No.4	2024.12.9
No.5	2024.12.12-12.13
No.6	2024.12.17-12.18

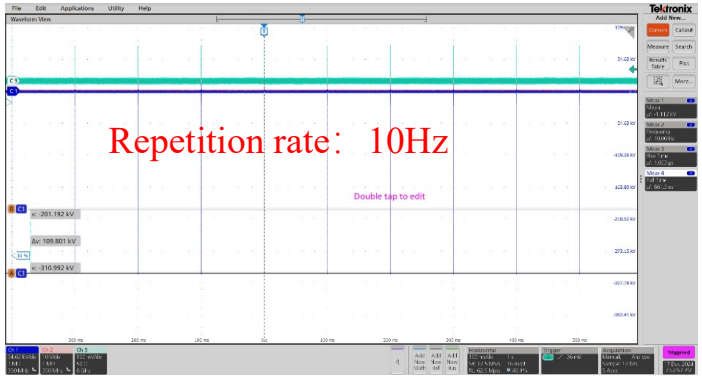


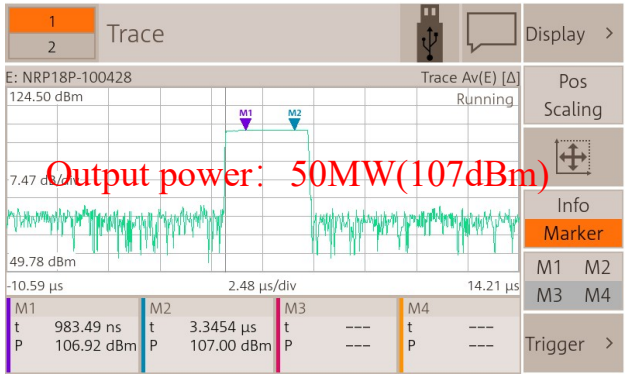


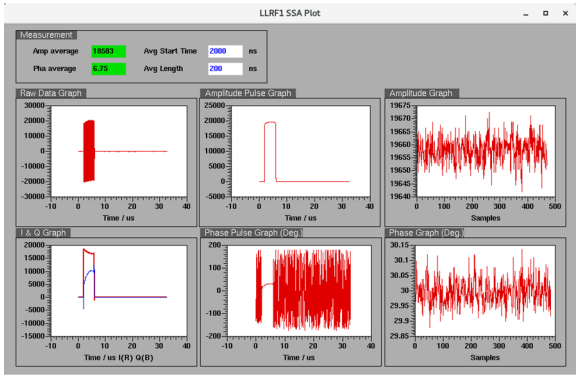
Vacuum data@ 2024.06.19







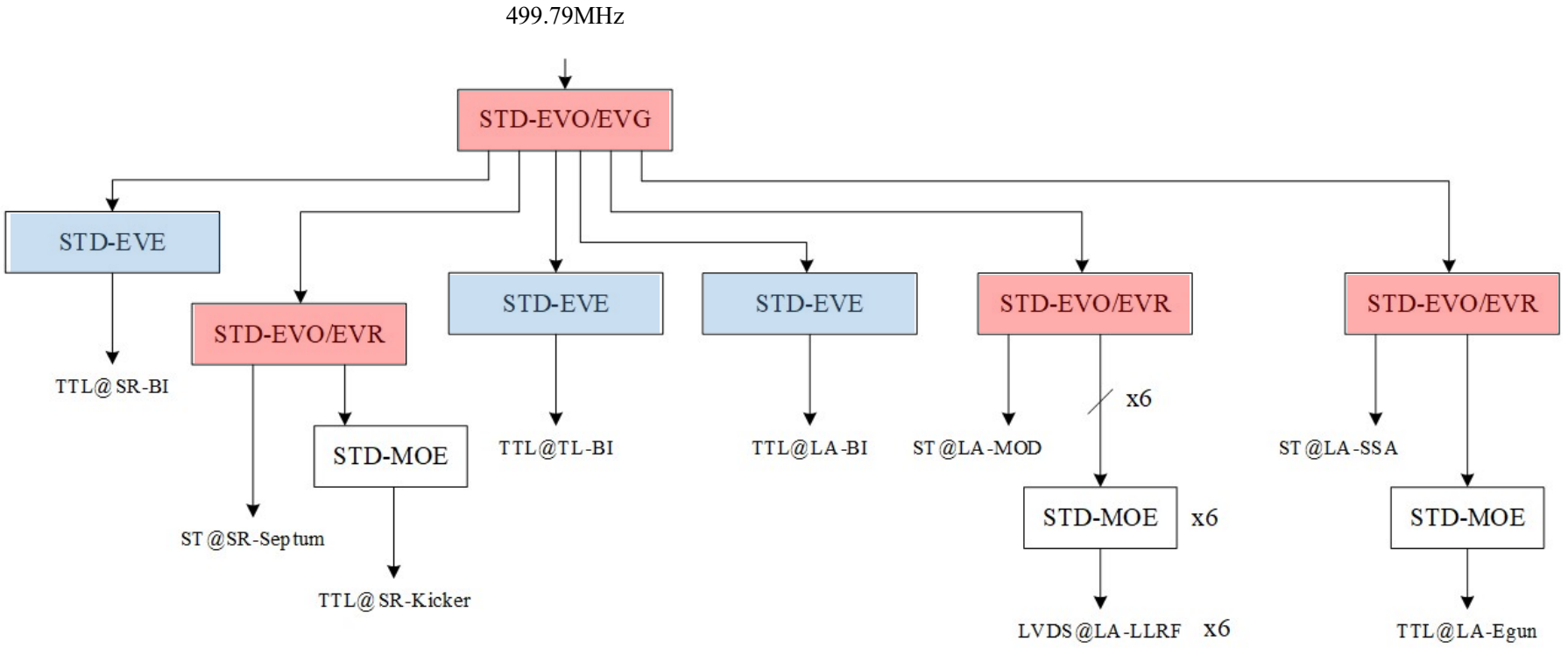




Amplitude/Phase stability (rms):
0.02%， 0.03°

Final status of the acceptance test

3.2 Test with timing system



The layout of timing system

STD-EVO

19 inches 1U standard chassis,
110/220V 50-60Hz AC power supply
■ Configured as EVR, EVG and FANOUT by software
■ event clock delay, 1/20 event clock delay, 5ps/step delay
■ event clock frequency range is 60 – 135MHz
■ RF clock frequency range is 60 – 500MHz,
■ Support cascaded EVG function with different event clock frequency
■ Embedded IOC installed (uclinux 2.6.30.4)
In front panel:
■ 1 RF clock input (0–10dBm)
■ 1 interlock / AC-line input (TTL)
■ 1 fiber input (SFP module)
■ 8 fiber output (SFP module)
In rear panel:
■ 1 10/100Mbit Ethernet port
■ 10 optic trigger output (HFBR-1414/ST)

STD-EVE

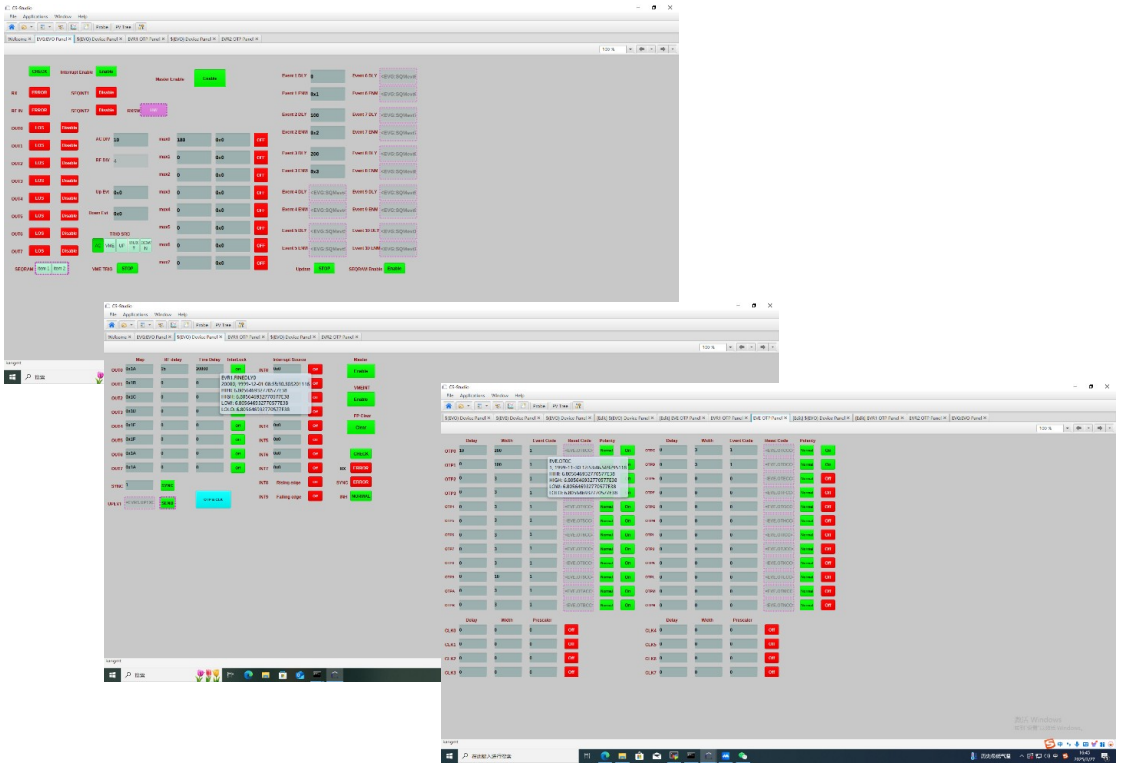
19 inches 1U standard chassis,
110/220V 50-60Hz AC power supply
■ event clock delay, 1/20 event clock delay, 5ps/step delay
■ recovery RF clock frequency range is 60 – 500MHz,
■ Embedded IOC installed (uclinux 2.6.30.4)
In front panel:
■ 1 RF clock output (-3dBm)
■ 1 interlock input (TTL)
■ 1 fiber input (SFP module)
■ 8 TTL output (SFP module)
In rear panel:
■ 1 10/100Mbit Ethernet port
■ 12 TTL trigger output (8 NIM trigger output optional)

STD-MOE

19 inches 1U standard chassis
110/220V 50-60Hz AC power supply
In front panel:
■ 4 fiber inputs (SFP module)
■ 4 TTL outputs
In rear panel:
■ 4 interlock inputs (1 interlock input/channel)

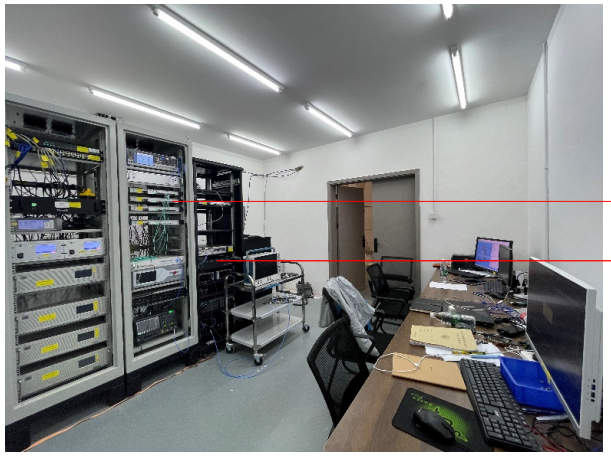
Facility	Equipment	Num.	Pulse width	Delay step	Jitter(RMS)	Connector
Linac	E-gun	1	1ns	5ps	30ps	BNC
	Modulator	5	4μs	10ns	150ps	ST
	Solid state amplifier	6	4μs	10ns	150ps	ST
	LLRF	6	4μs	10ns	150ps	*RJ45
	Beam inspection	3	4μs	10ns	150ps	SMA
Transport line	Beam inspection	3	4μs	10ns	150ps	SMA
Storage line	LLRF	2	4μs	10ns	150ps	SMA
	Septum	1	60μs	10ns	150ps	ST
	NLK	1	0.5μs	5ps	150ps	BNC
	Beam inspection	9	4μs	10ns	150ps	SMA
	Beam inspection	7	4μs	10ps	150ps	SMA
	Beam line					

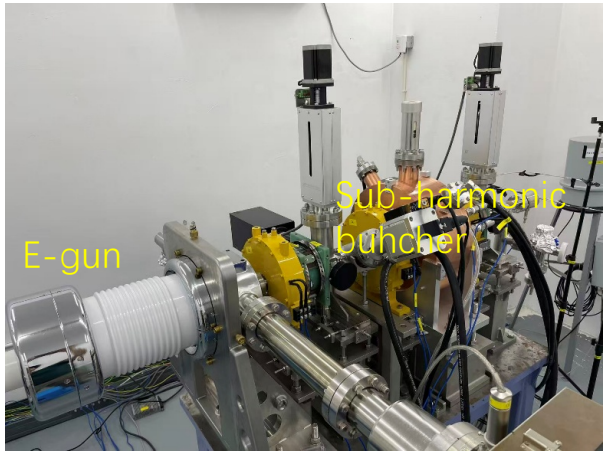
Integration test of LLRF & Timing system

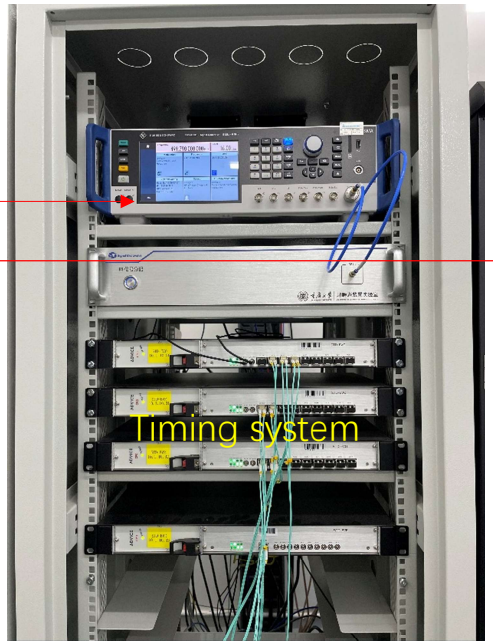


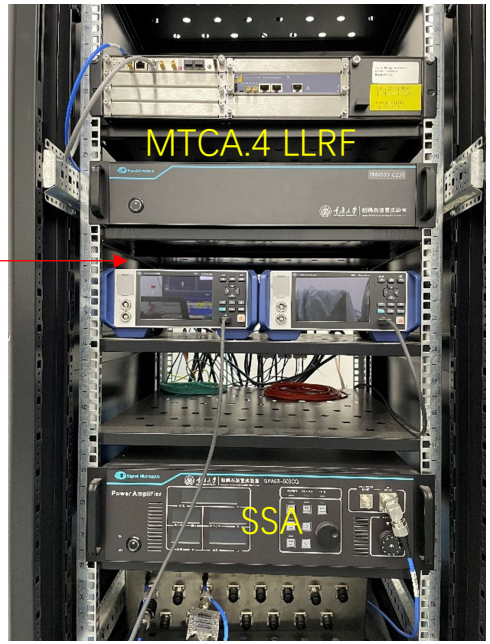
Timing OPI

3.3 E-gun commissioning

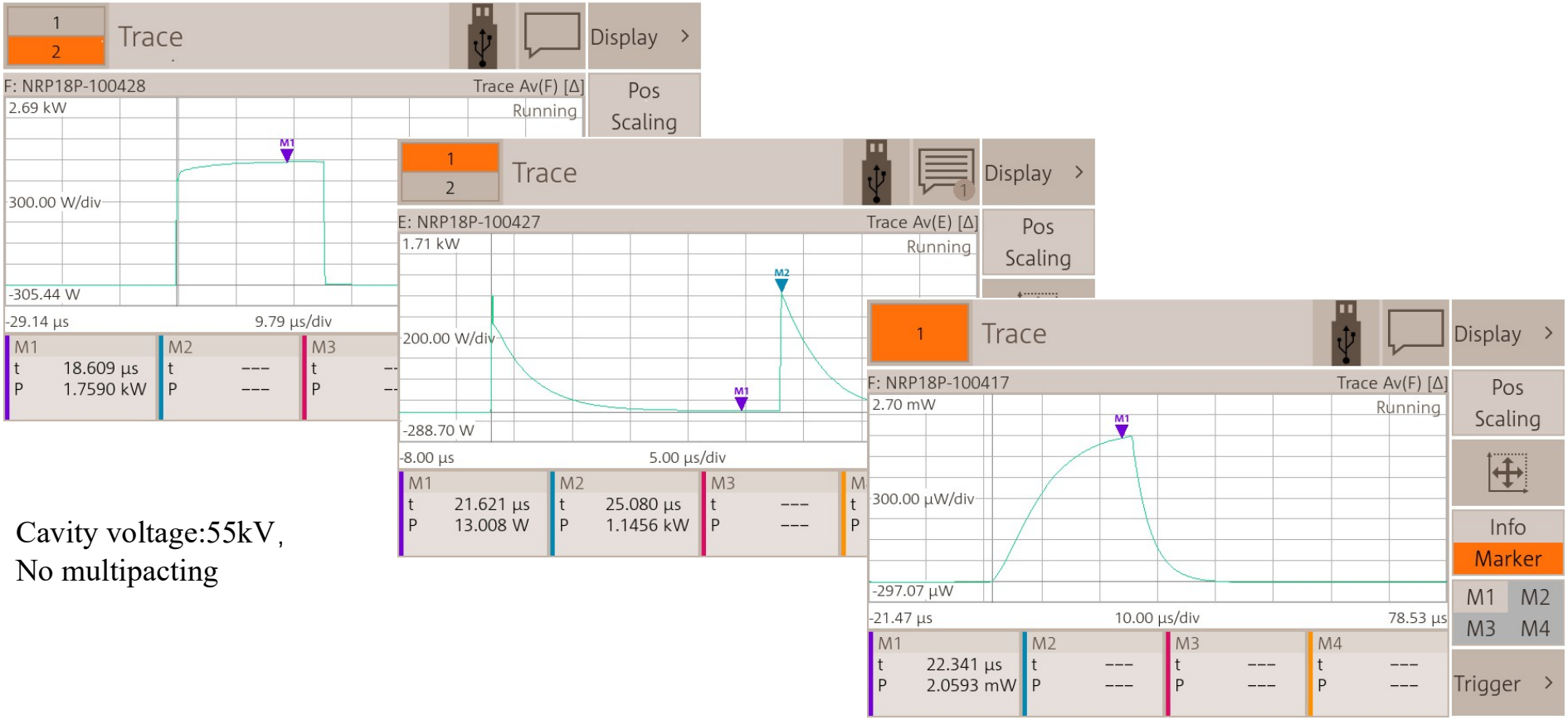




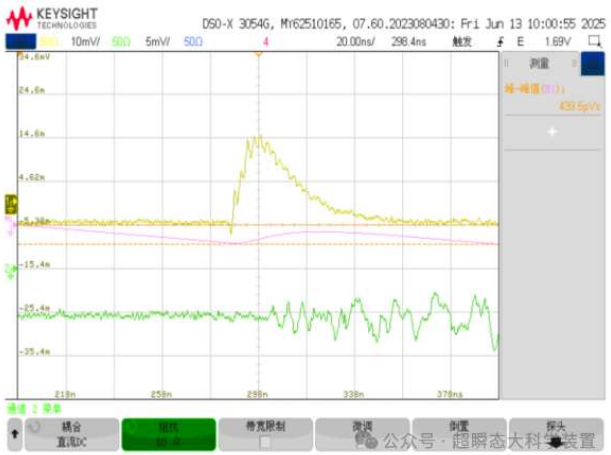


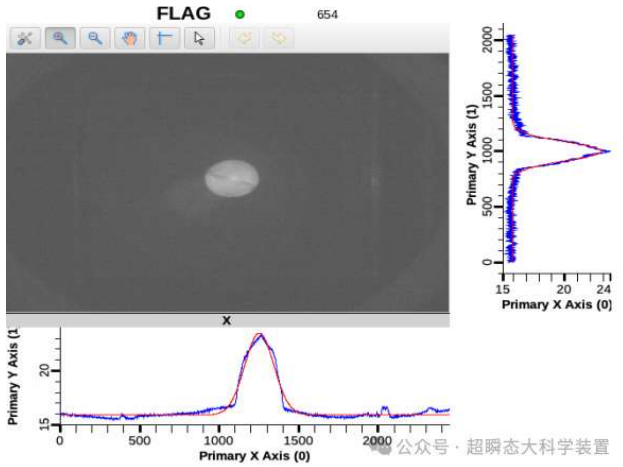


Field conditions is limited, space Interference is severe， good grounding is necessary.

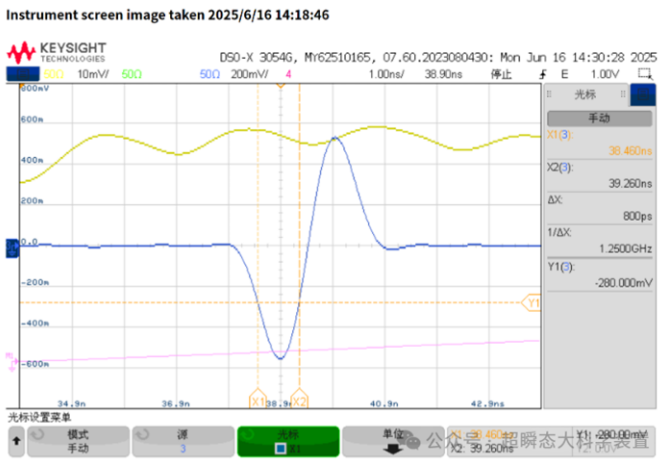


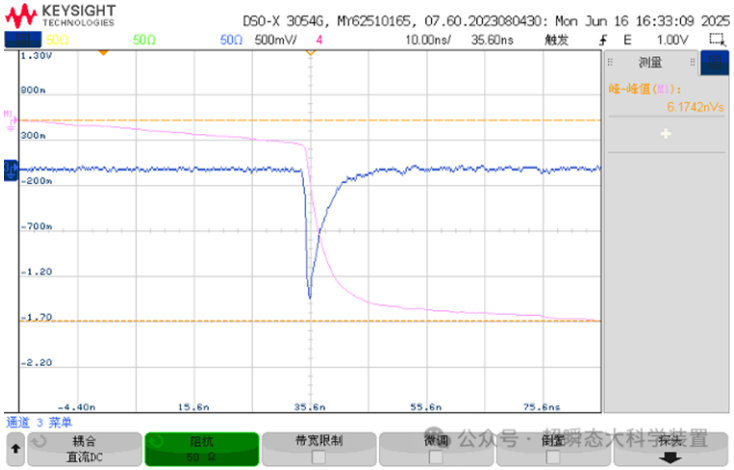
Cavity voltage:55kV,
No multipacting





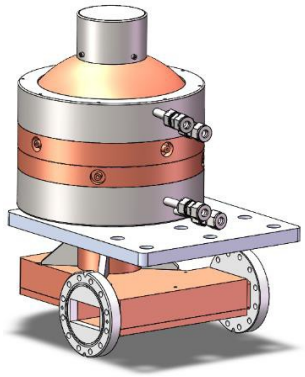
Beam @ ICT & profile



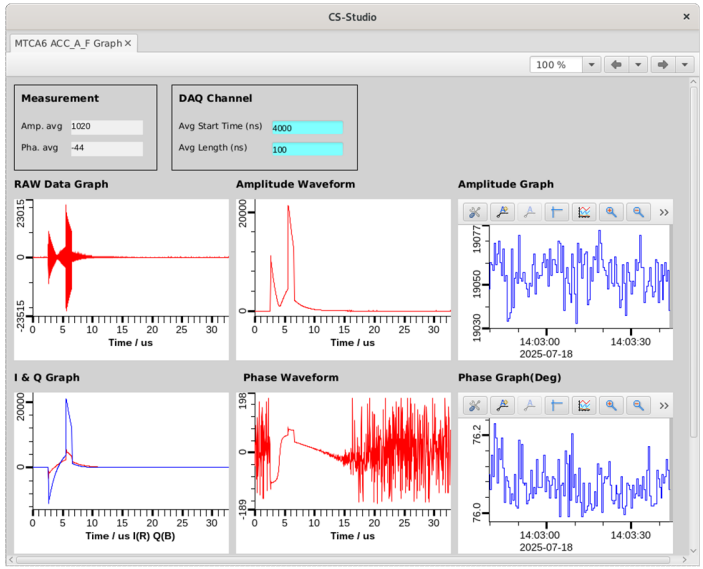


Pulse width & pulse charge @ BPM & Faraday cylinder

3.4 Pulse compressor



Parameters	Value
Working frequency (MHz)	2998.74
Input power (MW)	45
Pulse width (μs)	3
Q_0	1×10^5
Coupling factor	5
Multipaction factor	> 1.5
Effective pulse width (μs)	1



Test with pulse compressor

4. Summary

1. The development of MTCA.4 based LLRF is finished.

2. Relevant tests with klystron, timing system, sub-harmonic buncher, pulse compressor have been done, the performance meets our requirements.

3. Next step: installation and commissioning at the linac.

Thanks for your attention