Status Update on MicroTCA based Fast Orbit Feedback System for PETRA IV

2025 MicroTCA/ATCA International Workshop for Large Scientific Facility Control,

Chongqing, China, Sep.15-Sep.17, 2025

Sven Pfeiffer, Sajjad Mirza (DESY - MSK) on behalf of the PETRA IV - WP2.08

Hamburg, 15.09.2025

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

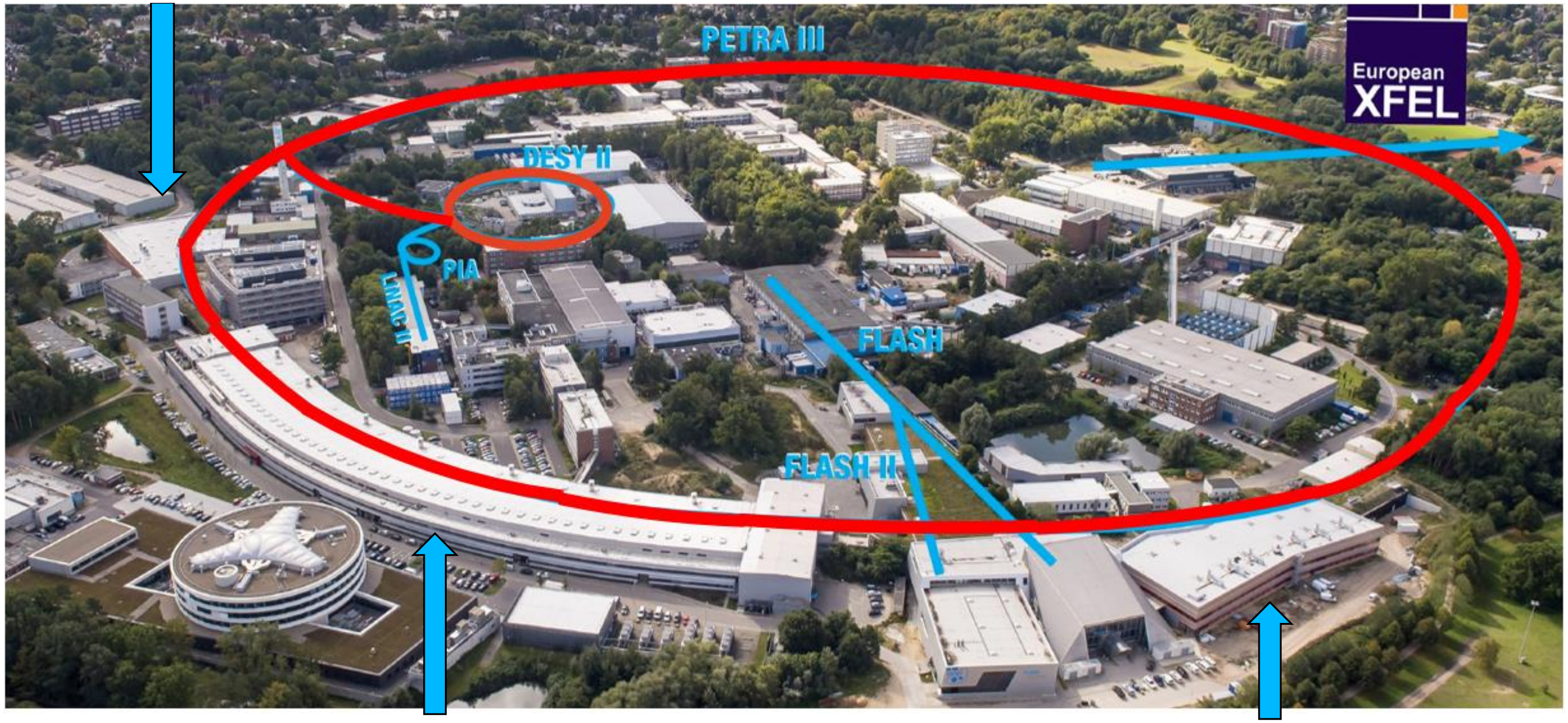
DESY.

PETRA III is one of the core facilities at DESY

PETRA IV. NEW DIMENSIONS

Each year ~5000h users operation serve more than 2000 users

Ada Yonath Hall
Extension Hall East



Max von Laue Hall

Paul P. Ewald Hall
Extension Hall North

Parameter	PETRA III
Energy [GeV]	6
Circumference [m]	2304
Emittance (hor./vert.) [nm]	1.3 / 0.013
Total current [mA]	100

PETRA III emittance 1300 pm

65 times smaller

PETRA IV emittance 20 pm

enabling 500 times larger X-ray beams brightness

PETRA IV project:

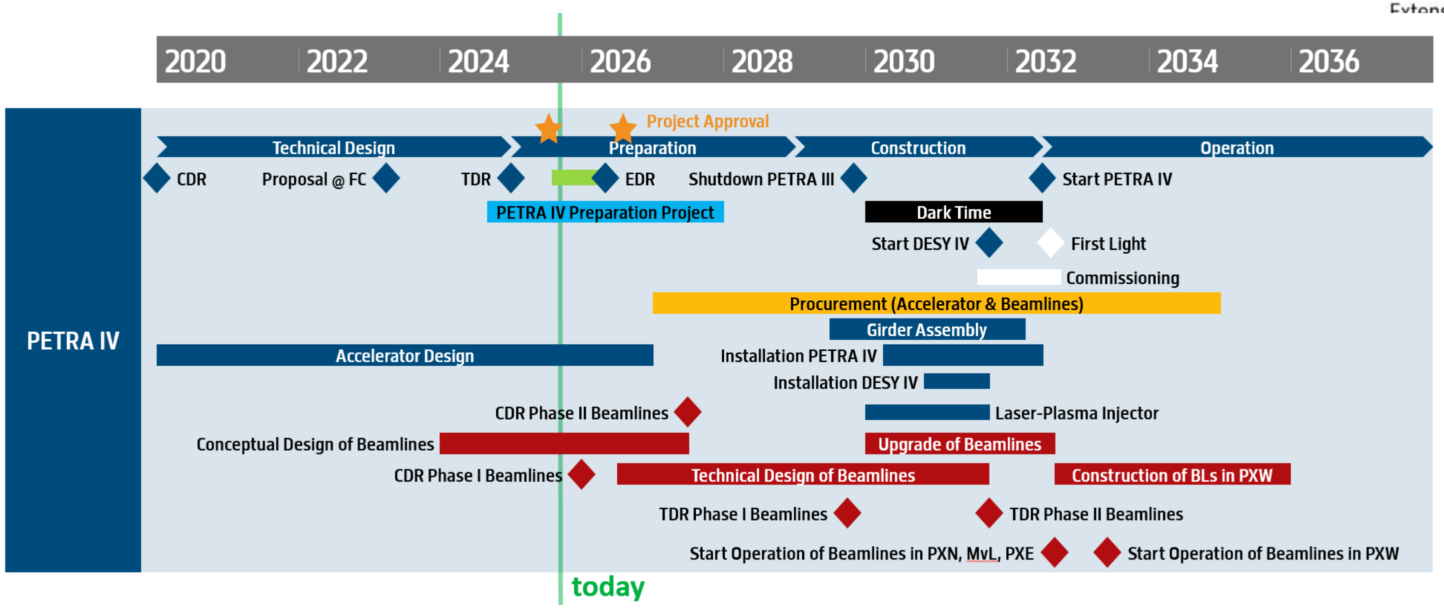
replacing PIII with an ultra-low emittance ring (20 pm), adding a new Experimental Hall in two more octants, replacing DESY II with a new low emittance booster

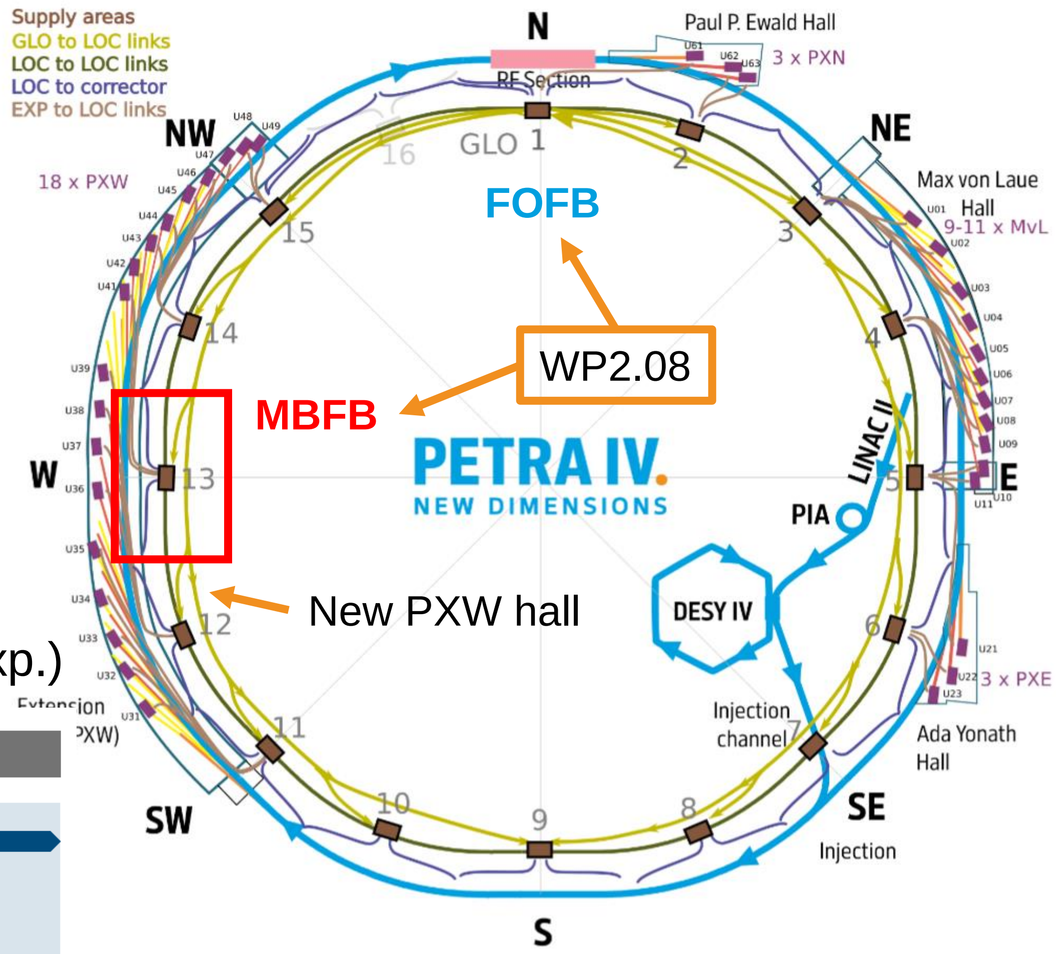
Introduction

PETRA III → PETRA IV upgrade status

PETRA III since 2009 3rd gen. light source → 4th generation

- Brightness*   480b@120mA   → 1920b@120mA
- Timing*   40b@100mA   → 80b@80mA
- Electronics   VME/SEDAC etc → MicroTCA.4
- Control system   Tine   → DOOCS (TANGO at exp.)





* PETRA IV non-baseline values:

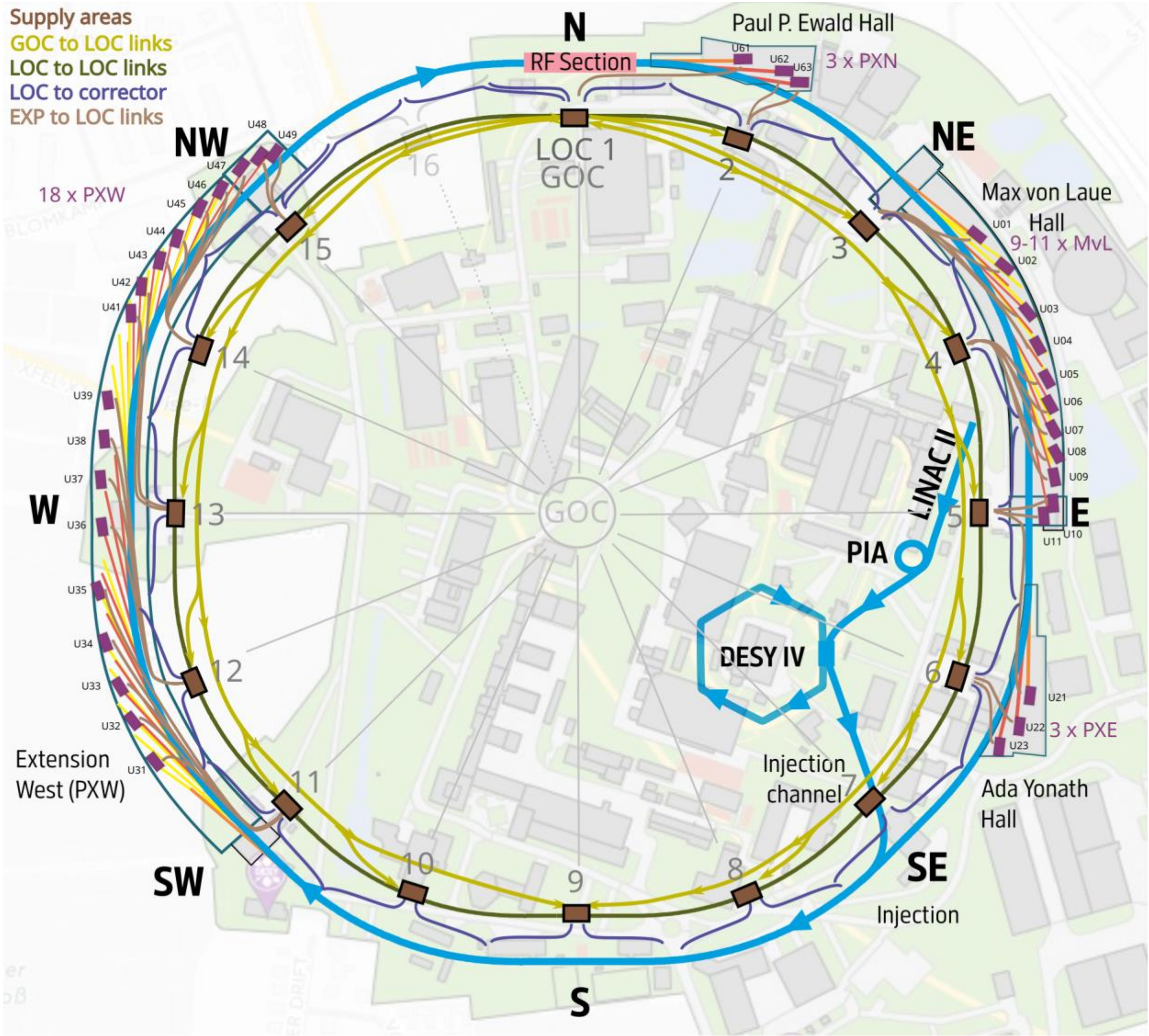
- 3840b@200mA
- 80b@200mA

FOFB system topology

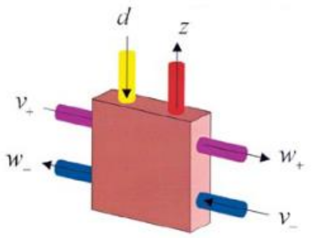
Latency optimized topology

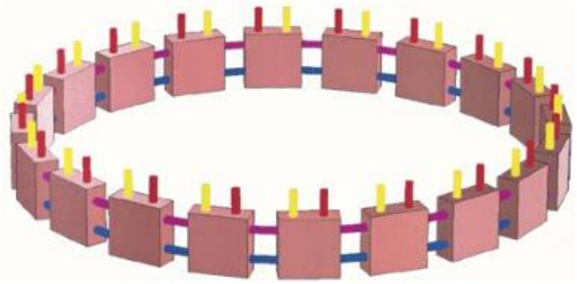
Ring: **2.3km, 790 BPMs, 560 fast correctors,**
FOFB: **10% (5%, 3%) beam stability, DC to 1kHz**

- **1 global orbit control unit (GOC)**
  - Close to RF system / timing system
  - Short path from GOC to LOC in experimental halls
- **16 (15) distributed local controllers (LOC)**
  - Collection of BPM information
  - Transmission of updated magnet current to power supplies
- **Optical fiber communication links**
  - Global to all local systems → classical regulation (star topology)
  - Local to local system
    - For local control scheme integrating experiments
    - *Redundant system mode (decentralized) as future upgrade*



R.D'Andrea, IEEE TRANSACTIONS ON AUTOMATIC CONTROL, VOL. 48, NO. 9, SEPTEMBER 2003



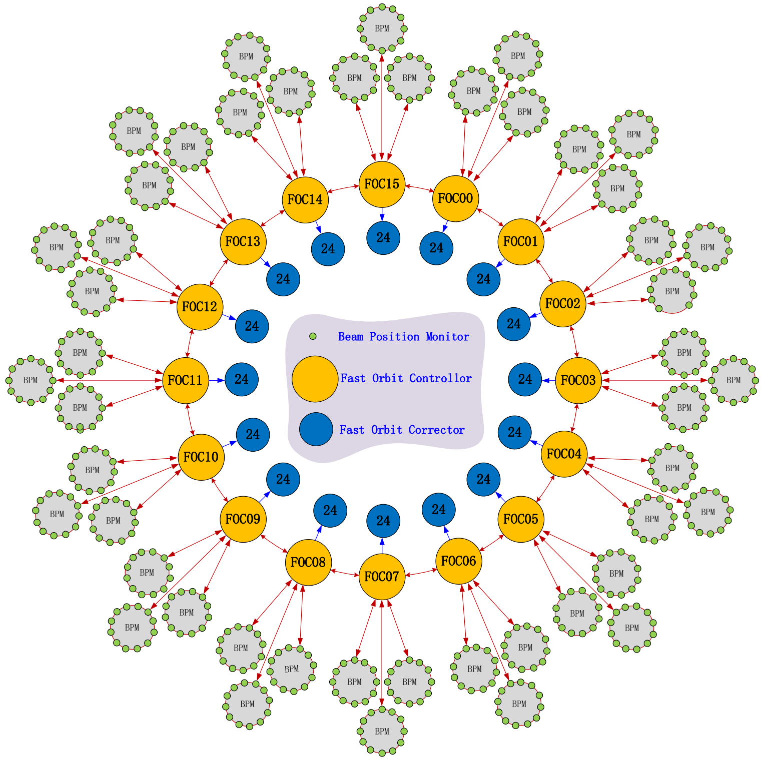


FOFB - Latency optimized topologies

Sector distributed and Central node

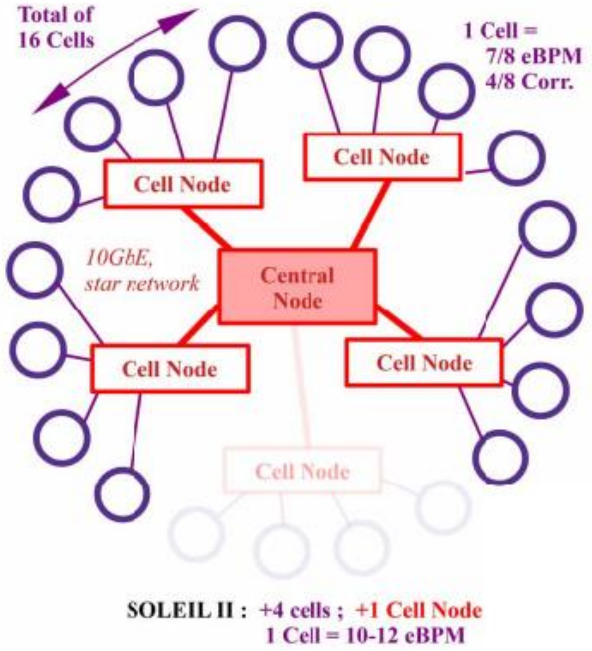
Sector distributed

HEPS, MAX IV, SIRIUS



Central node

ESRF-EBS, APS-U, Diamond-II



Each sector

- Hosts a local node to receive BPM positions and communicates with nearby nodes
- Calculates corrector strengths locally for nearby correctors

→ Saves FPGA resources and latency towards corrector's communication

A single global node

- Interacts with all local nodes for BPM data and sending corrector strengths.
- Calculates the new corrector strengths globally

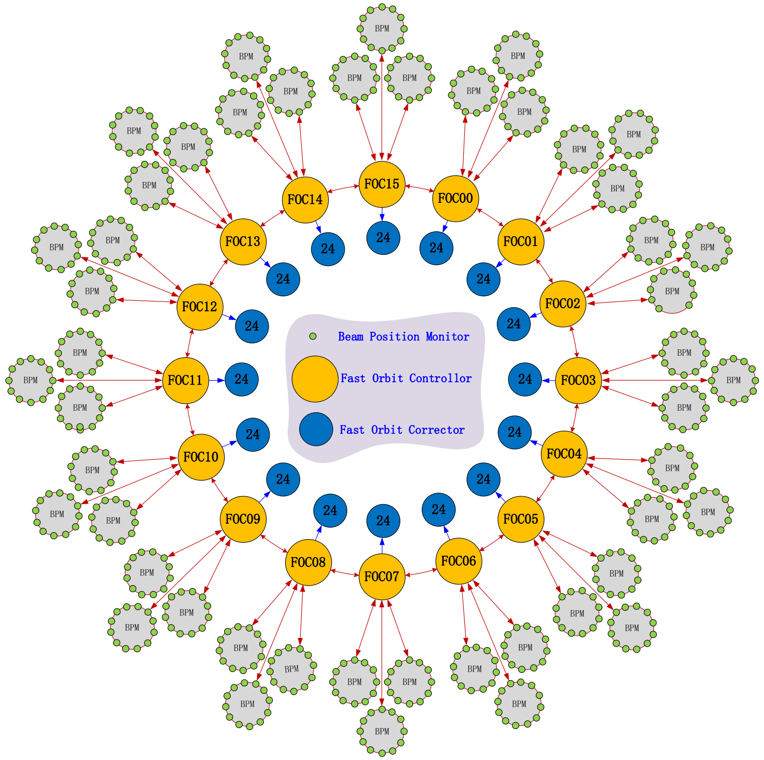
→ For larger facilities, better for latency optimization.

FOFB - Latency optimized topologies

Sector distributed and Central node

Sector distributed

HEPS, MAX IV, SIRIUS



Each sector

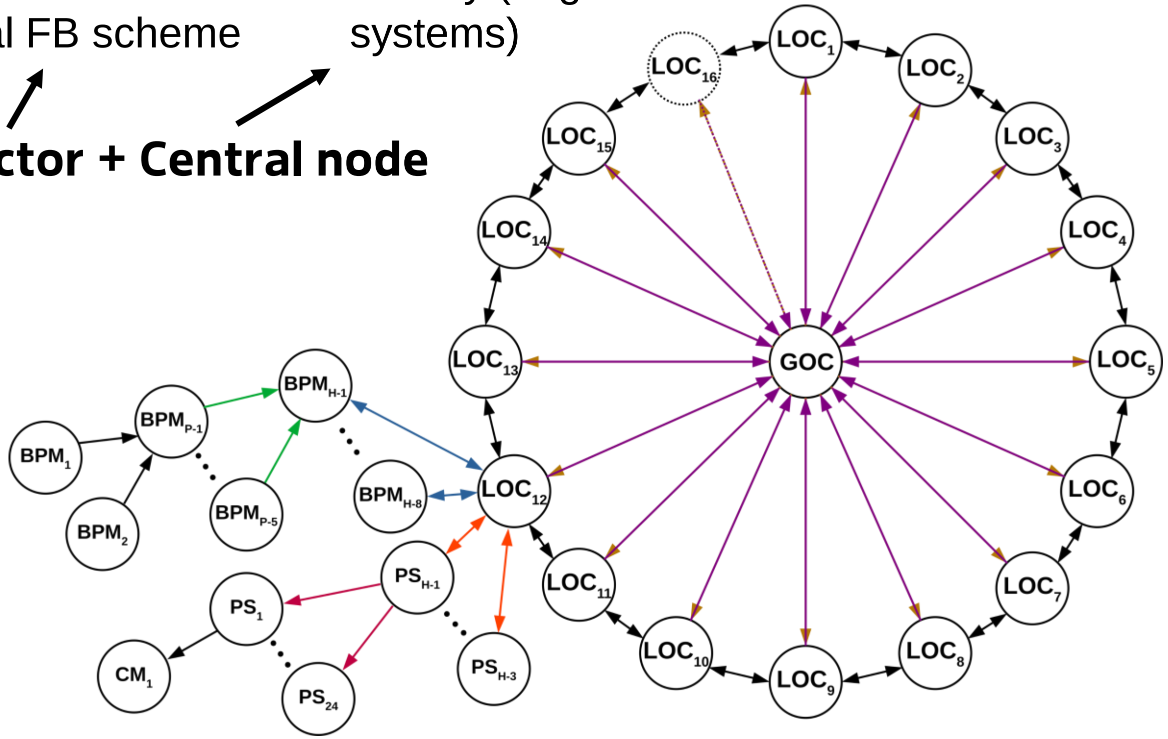
- Hosts a local node to receive BPM positions and communicates with nearby nodes
- Calculates corrector strengths locally for nearby correctors

→ Saves FPGA resources and latency towards corrector's communication

Ideal for photon based feedback in local FB scheme

Ideal for minimal latency (large scale systems)

Sector + Central node



A single global node

- Interacts with all local nodes for BPM data and sending corrector strengths.
- Calculates the new corrector strengths globally

→ For larger facilities, better for latency optimization.

FOFB - a cross-directional problem

A two dimensional control problem

The goal is to maintain the beam position

- **Throughout the ring** → spatial domain
- **Over time** → temporal domain

$$G(s) = \begin{pmatrix} r_{11}G_{11}(s) & \cdots & r_{1n}G_{1n}(s) \\ \vdots & \ddots & \vdots \\ r_{m1}G_{m1}(s) & \cdots & r_{mn}G_{mn}(s) \end{pmatrix}$$

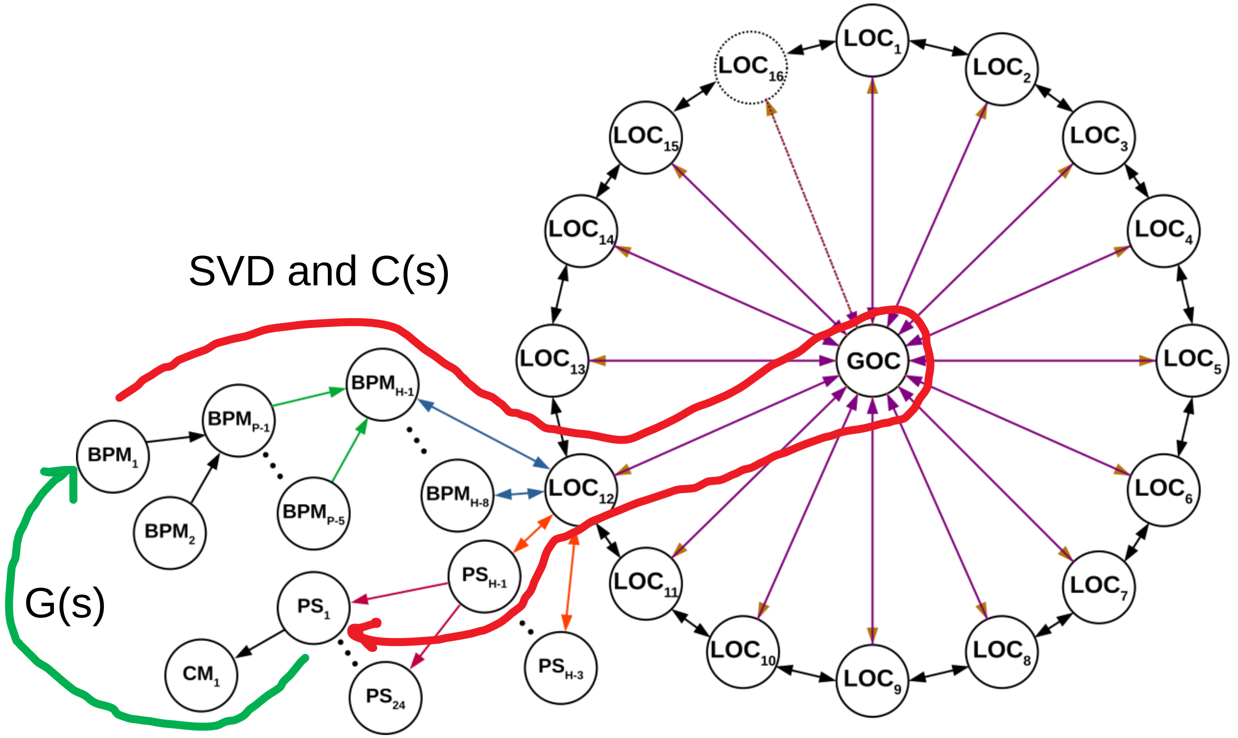
with $r_{mn} = \frac{\sqrt{\beta_m(z)\beta_n(z)}}{2\pi Q}\cos(\pi Q - |\phi_m(z) - \phi_n(z)|)$

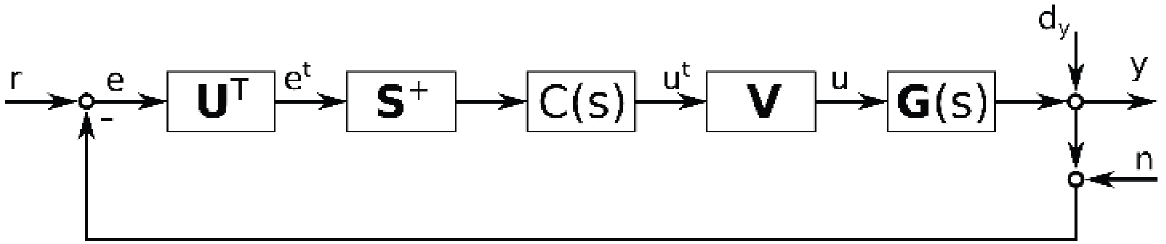
- All corrector channels with identical temporal response

$$\mathbf{G(s)} = G(s)\mathbf{R} \longrightarrow \mathbf{C(s)} = C(s)\mathbf{R}^{+}$$

2 step simulation

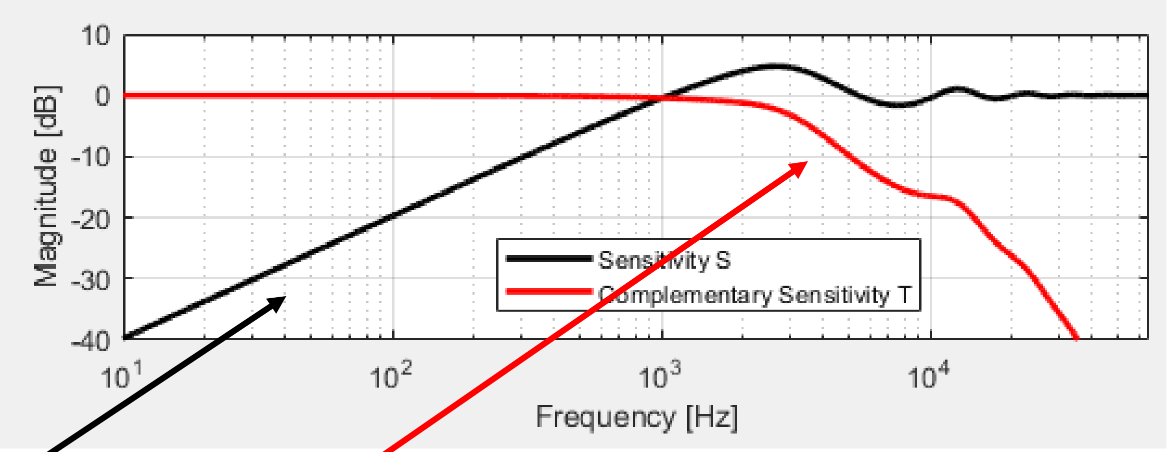
- SISO dynamical system (1 location with all TFs)
  - Worst case scenario → best case for MIMO
- MIMO system (spatially distributed) with main dynamics



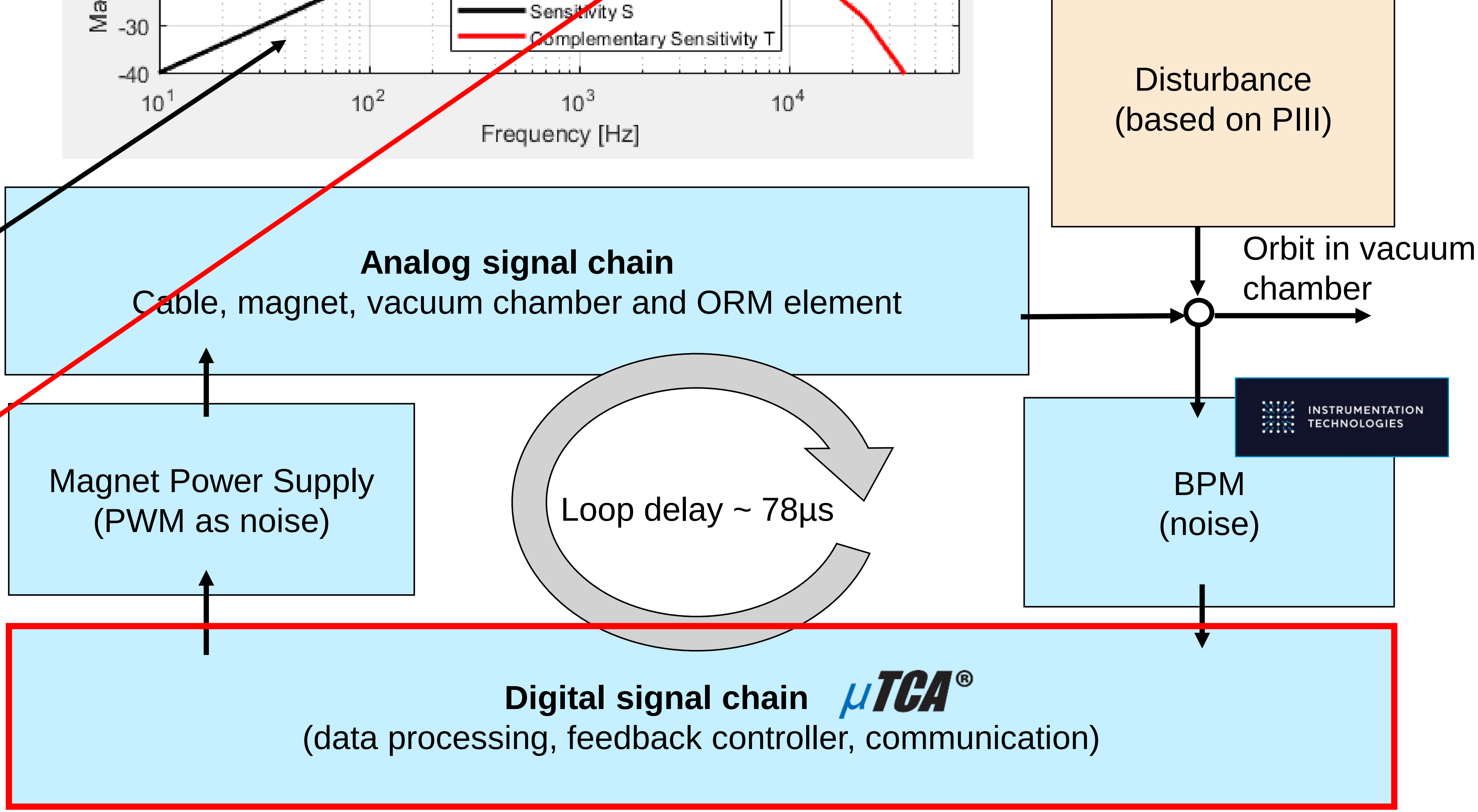


FOFB sub-systems

SISO modelling and simulation



- Subsystems based on PETRA IV design
- Disturbance spectra approximated with measurement at PIII
- PI controller optimized for disturbance rejection
  - Goal: 1kHz
- PI controller optimized for reference tracking
  - Integration of experiments (photon diagnostics)



Digital signal chain

Baseline concept

Talk: M. Cargnelutti

Standard support modules/boards per crate

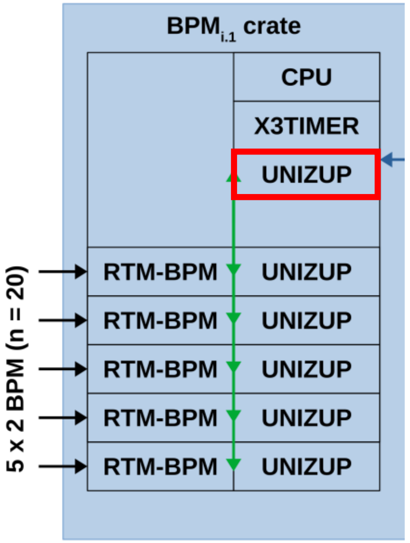
- 2x PS (redundant)
- MCH, CPU, x3timer

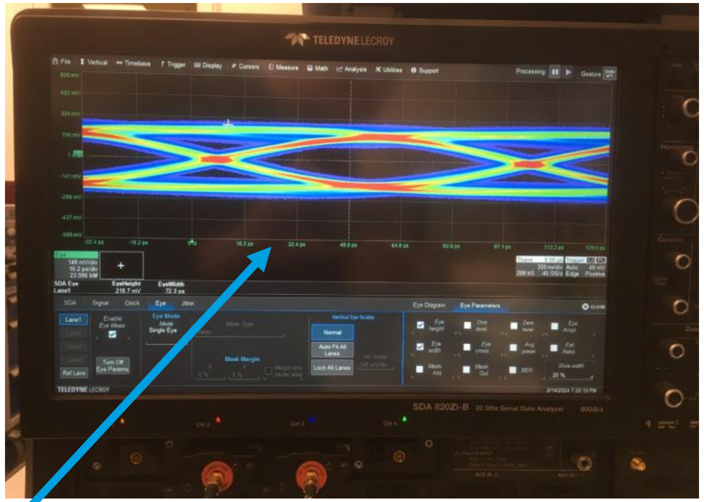
2 versions of AMC boards only (no options)

- DAMC-UNIZUP as BPM data collector

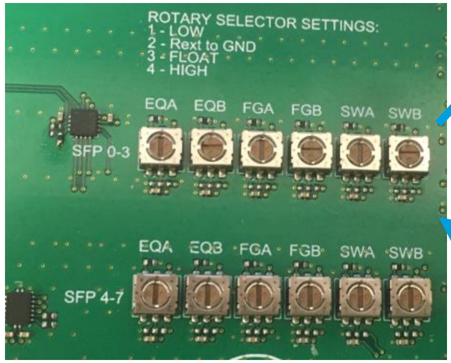
→ Licensed to I-Tech

Talk: B. Boghrati



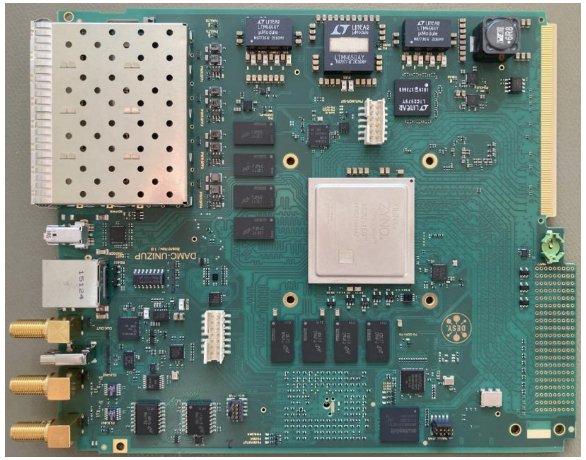


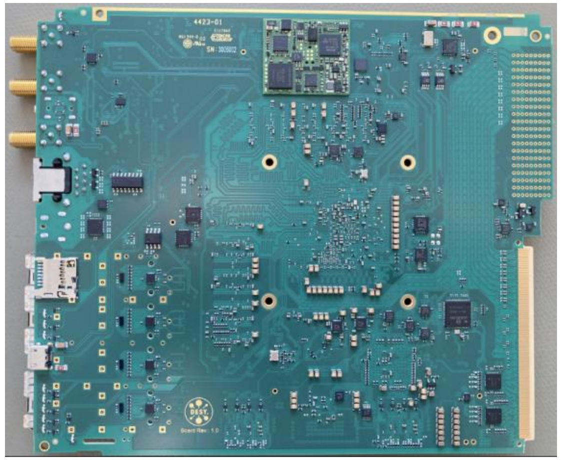
Courtesy: M.Fenner, S.Chystiakov



Channel tuning

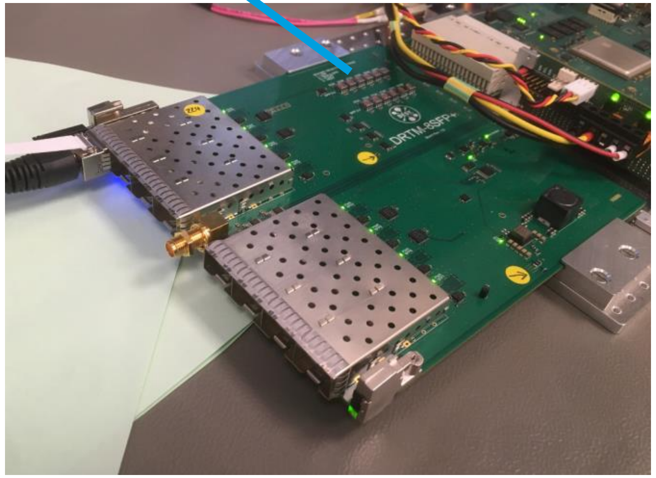
Courtesy: M.Fenner, S.Chystiakov





DRTM-8SFP+

- Fanning out the MGT channels from DAMC-UNIZUP
- Brings 1 to 8 MGTs to RTM @ 12.5 Gbps



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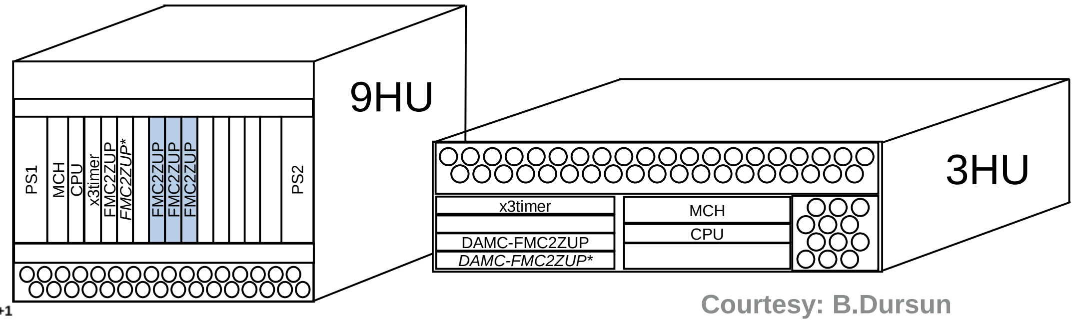
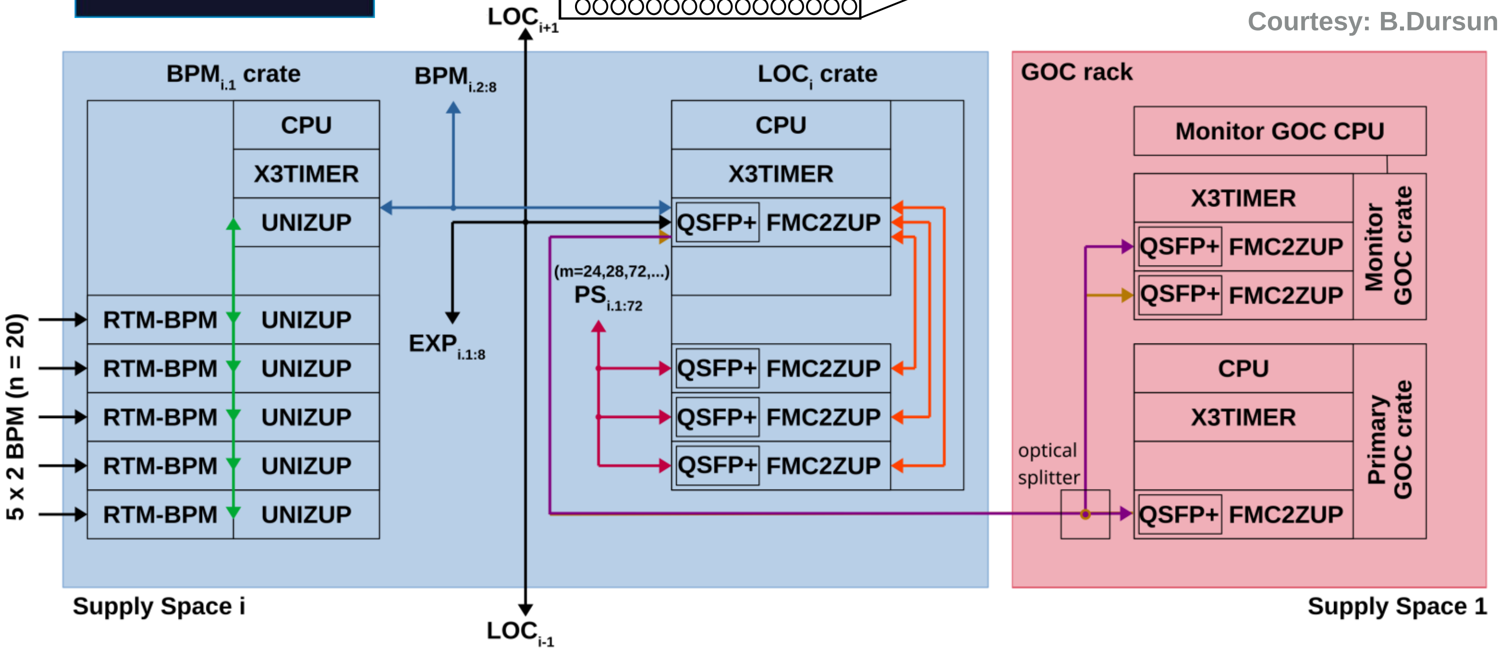


Courtesy: B.Dursun



Standard support modules/boards per crate

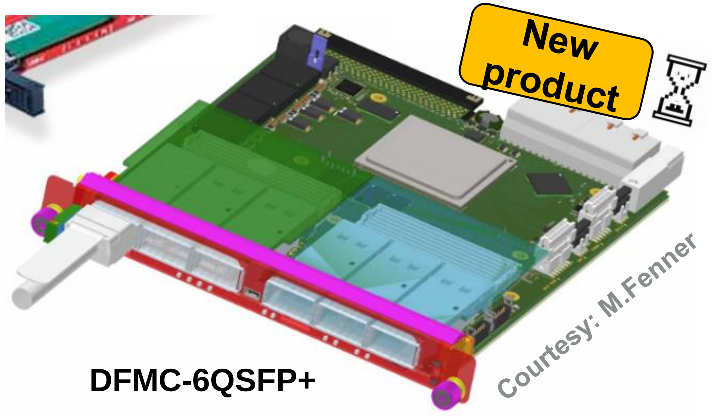
- 2x PS (redundant)
- MCH, CPU, x3timer

2 versions of AMC boards only (no options)

- DAMC-UNIZUP as BPM data collector
- DAMC-FMC2ZUP for
  - BPM data concentration, main processing
  - Communication with frequency shaping filter to magnet PS
- DFMC-6QSFP+ (24LC fiber links)

Monitor GOC crate as observer

https://www.caenels.com/product/damc-fmc2zup/



DFMC-6QSFP+

Latency budget

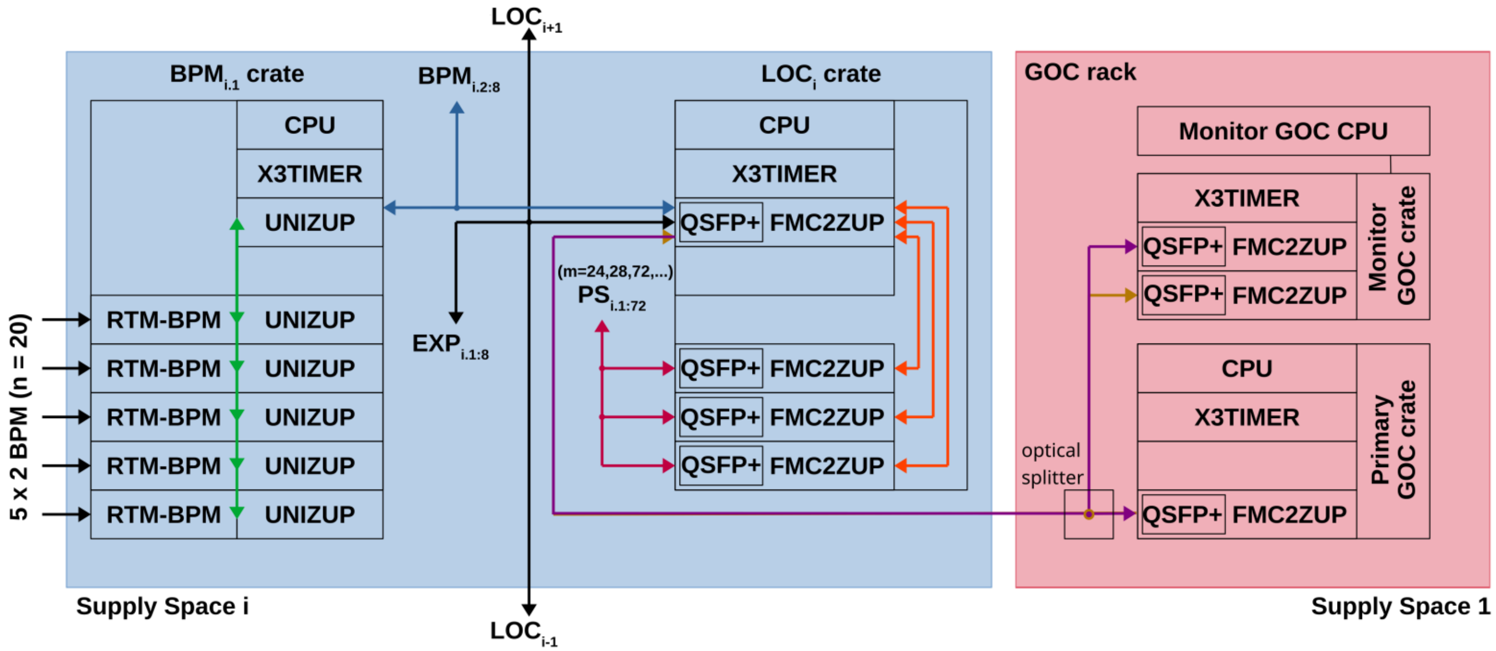
Baseline concept

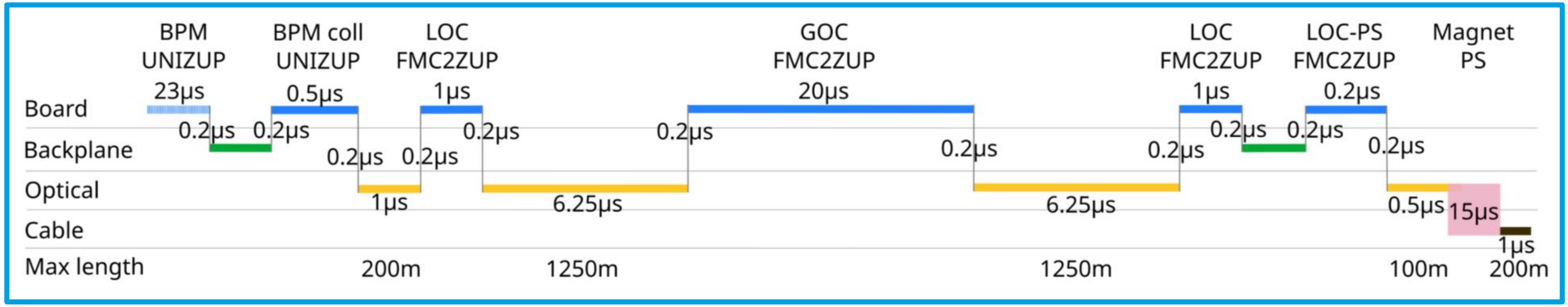
Long delays/latencies (>1µs)

- BPM electronics
- FB computation by large scale matrix multiplications
- Magnet PS
- Communication

Short delays/latencies (<1µs)

- Data serialization for 1 lane link (el. or opt.) transfer
- Data alignment
- Data filtering to equalize dynamical transfer function





→ 78µs as expected loop latency with central node

Digital signal and processing chain

Requirements for the MicroTCA components

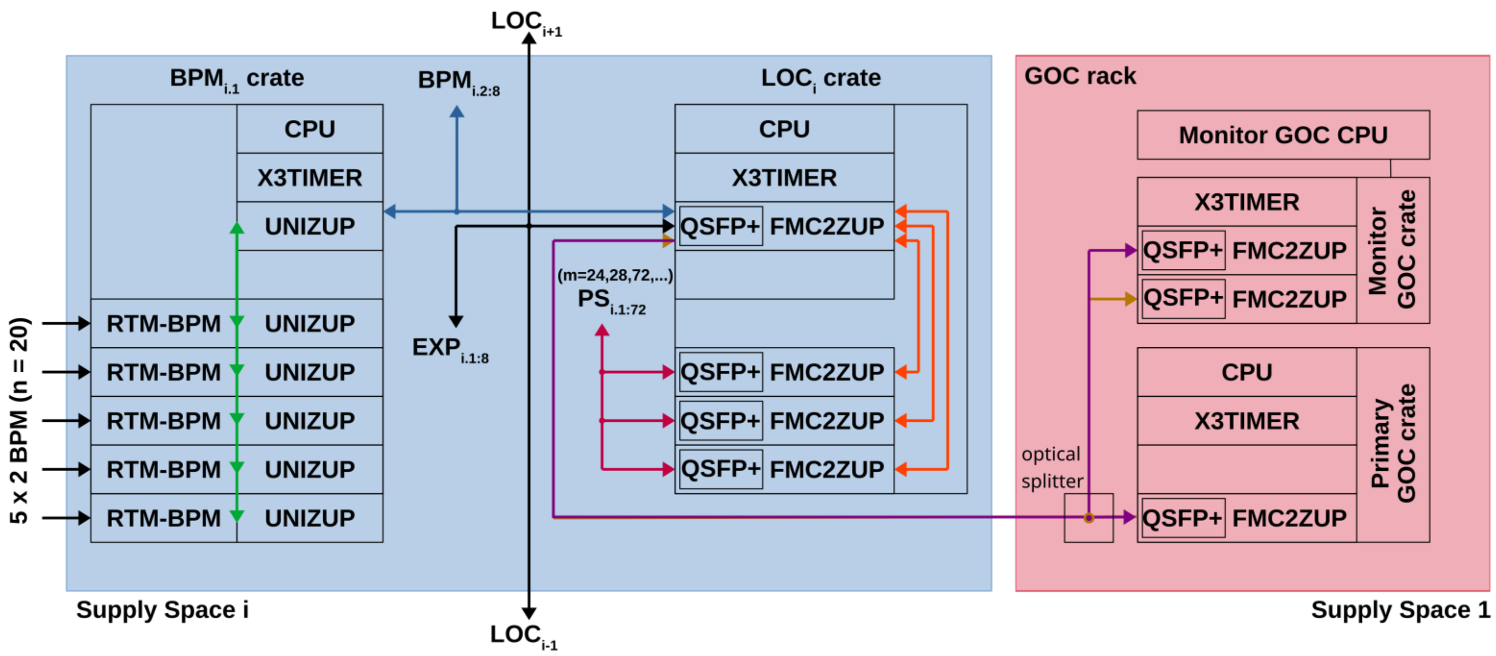
- **Software** with ChimeraTK framework
- Open source FPGA **firmware** framework
- **Hardware**
  - Operability (Low latency and parallel processing in FW)
  - Maintainability
  - Modularity / flexibility (FPGA IP libraries)
  - High data rates & long communication paths
    - QSFP+ and optical single-mode links
  - Scalability
    - Larger to smaller FOFB schemes
      - **BPM – LOC – GOC**
      - BPM – GOC
      - BPM only

ChimeraTK

FWK
FPGA firmware framework

gitlab.desy.de/fpgafw/fwk

Talk: Michael Randall



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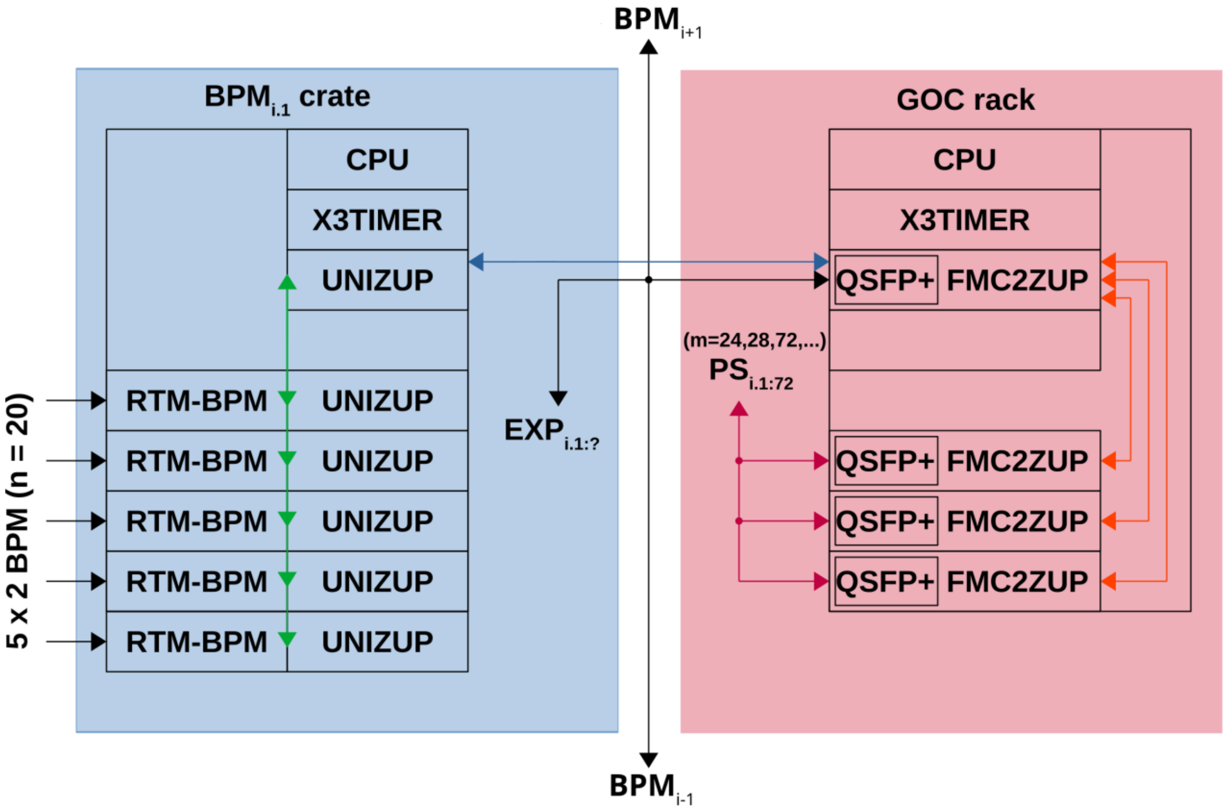
        - **(1) PS control from GOC crate**
        - (2) PS control from BPM crate
      - BPM only

gitlab.desy.de/fpgafw/fwk

Talk: Michael Randall



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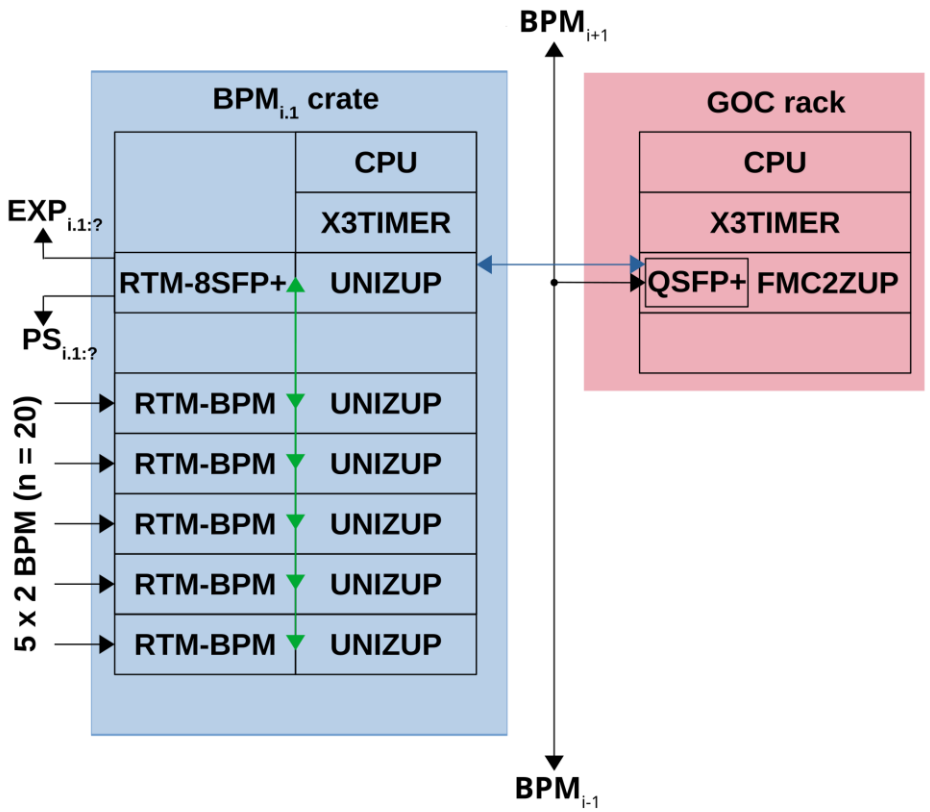

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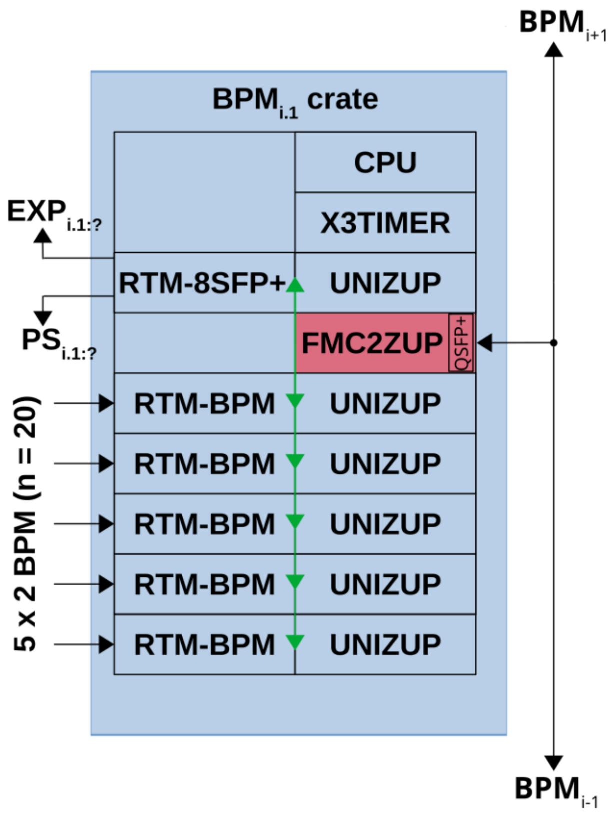
ChimeraTK

FWK FPGA firmware framework

gitlab.desy.de/fpgafw/fwk

Talk: Michael Randall



FOFB system

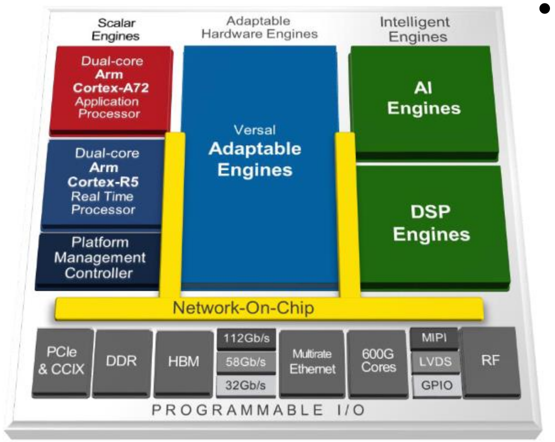
Outlook

Fast orbit feedback developments

- **Large scale GOC processing**
  - Twice ***large scale matrix multiplication*** with 1580 x 560 elements
  - ***Fast fault detection*** of non-functioning correctors and their exclusion from ORM

    → Local effect otherwise global error

- **Versal chip**
  - Programmable logic for fine-grained parallel processing, sensor fusion, …
  - Low latency DSPs, AIs, …
  - Terabit network-on-chip
  - …

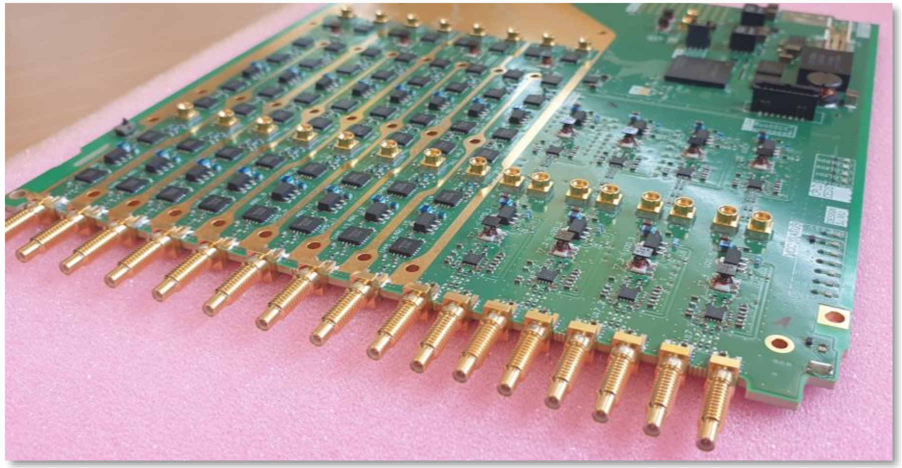


https://www.xilinx.com/publications/events/developer-forum/2018-frankfurt/introducing-the-versal-architecture.pdf

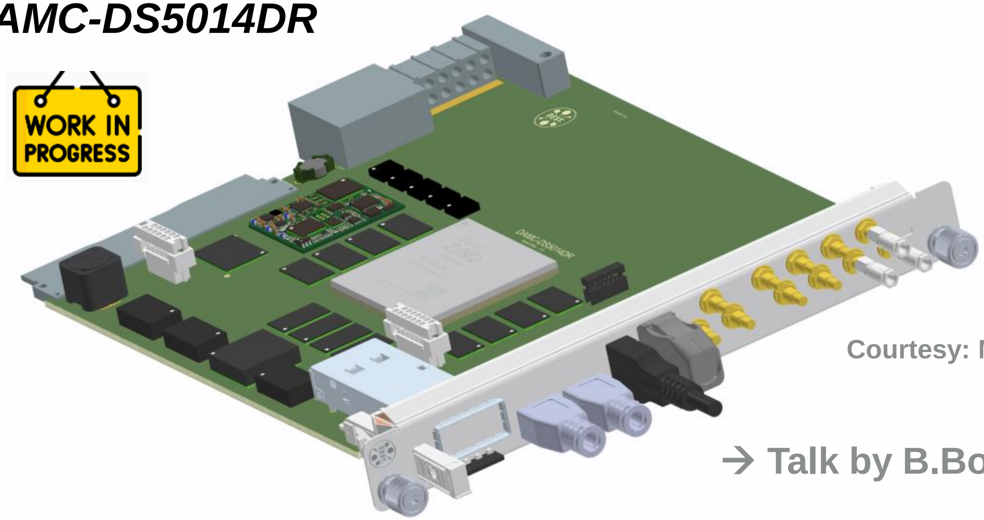
Multi-bunch feedback developments

- ***DRTM-MBFB-FE*** ✓

Courtesy: S.Jablonski



- ***DAMC-DS5014DR***



Courtesy: M.Fenner

→ Talk by B.Bograthi

Thank you.

For the materials provided:

- Adeel Amjad
- Behzad Boghrati
- Stanislav Chystiakov
- Burak Dursun
- Michael Fenner
- Szymon Jablonski
- Sajjad Hussain Mirza

& those who were forgotten here...

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