RFSoC-Base LLRF Development for CSNS-II LINAC

Zhexin Xie, CSNS LINAC RF GROUP

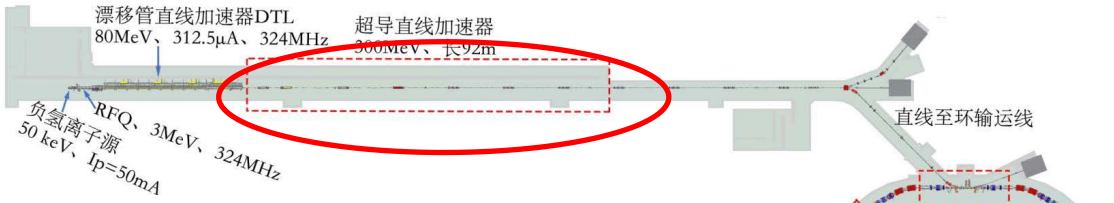
2025 MicroTCA/ATCA International Workshop for Large Scientific Facility Control

Chongqing

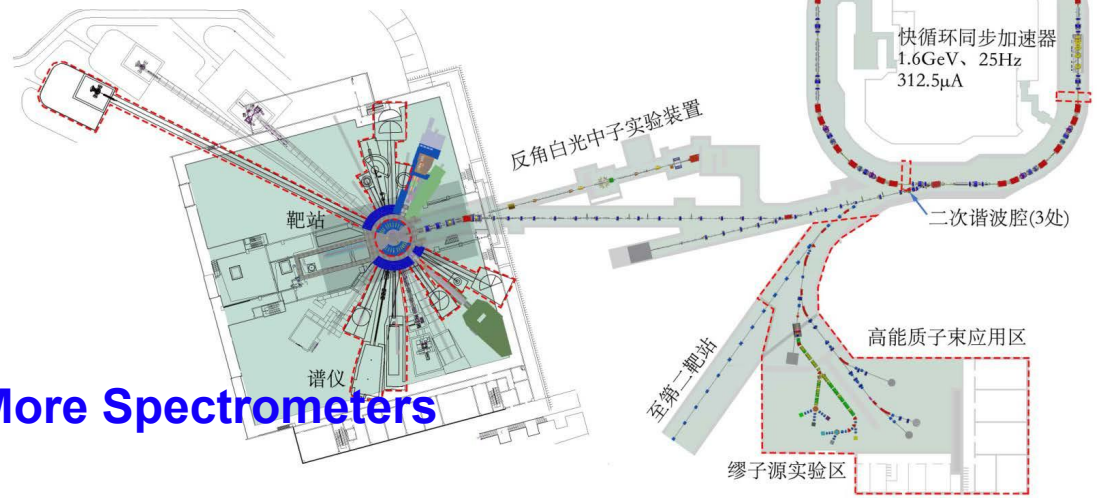
CSNS-II Overview

- Construction Time:2023.12 ~ 2029.3
- A SRF section is to be added to increase energy from 80 to 300MeV.

Linac Energy:80MeV→300MeV



Target Power:100→500kW



More Spectrometers

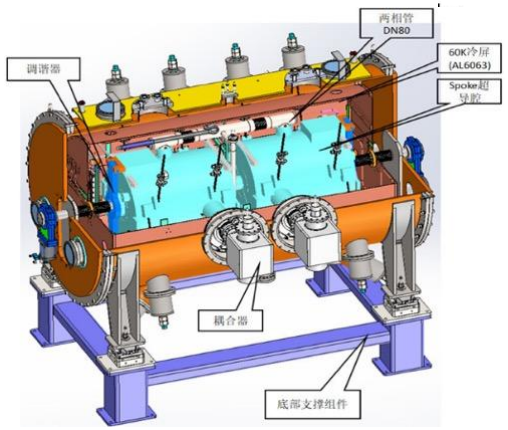
Layout of CSNS

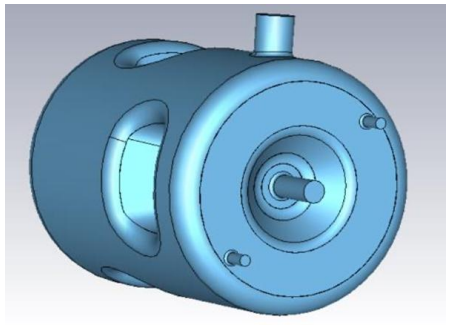
CSNS	Phase I	Phase II
Beam power on target(kW)	100	500
Linac energy (MeV)	80	300
Extraction beam energy (GeV)	1.6	1.6
Average beam current (μA)	62.5	312.5
Linac Peak beam Current(mA)	15	40
Repetition(Hz)	25	25
Linac Beam Len(μs)	500	~500

SRF Section Accelerator

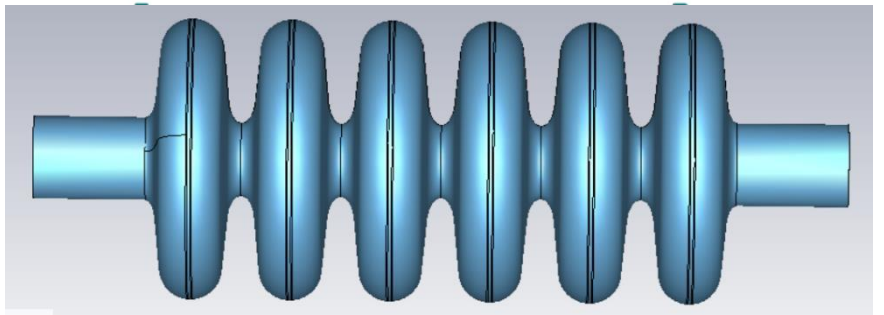
- **SRF cavity is processing and testing.**

Items	SPOKE	SPOKE (Improved)	ELLIPTICAL
Freq(MHz)	324	324	648
Gradient(Mv/m)	7.3	9	14
Length(m)	0.694	0.694	0.86
R/Q（Ω）	410	401	309
QL	2.3e5	2.3e5	9.6e5
LFD Hz/(MV/m)²	-10.7	-4.56	-1.5
LFD@ Max Gradient	530	369	250
f_{3db}	1408	1408	674
df/dp(Hz/mbar)	0.773	38	6.3





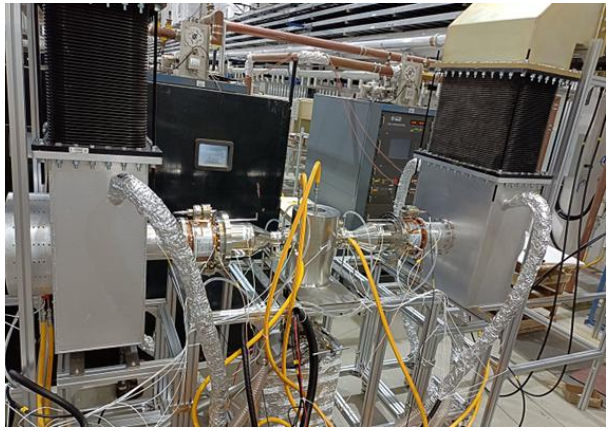
324MHz Double-Spoke Cavity X 20



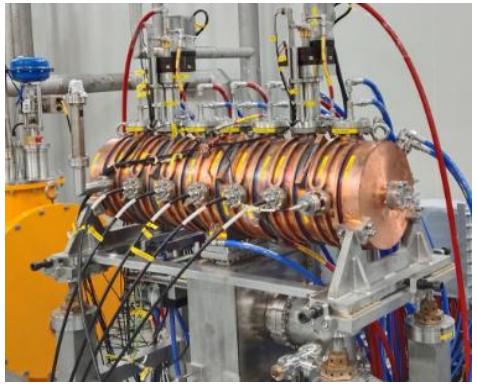
648MHz Elliptical Cavity X 24

Some projects

Some projects completed or are currently underway ,most used mTCA



324MHz coupler aging



648MHz debuncher LLRF

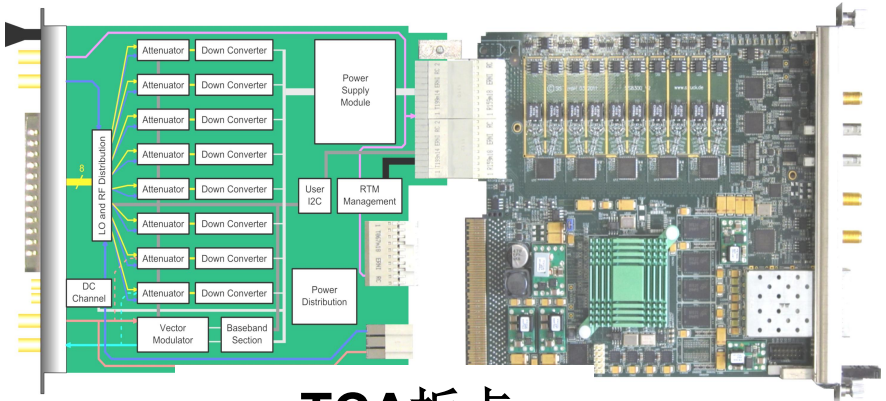
648MHz Klytron LLRF

C-Band Klytron

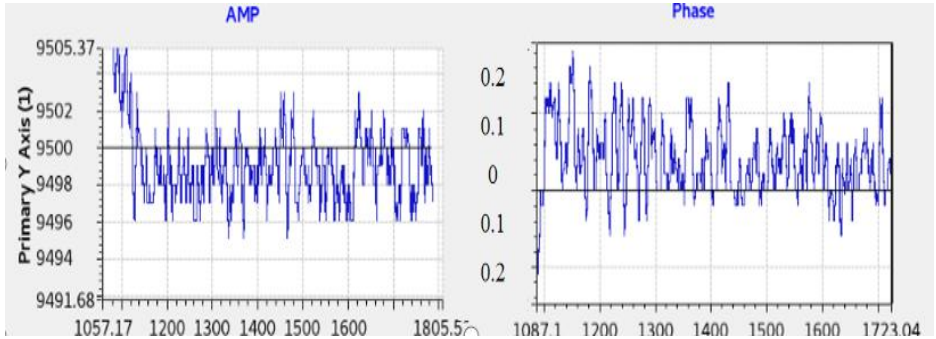
Spoke Horizontal Test

Spoke Horizontal Test /2023 mtca

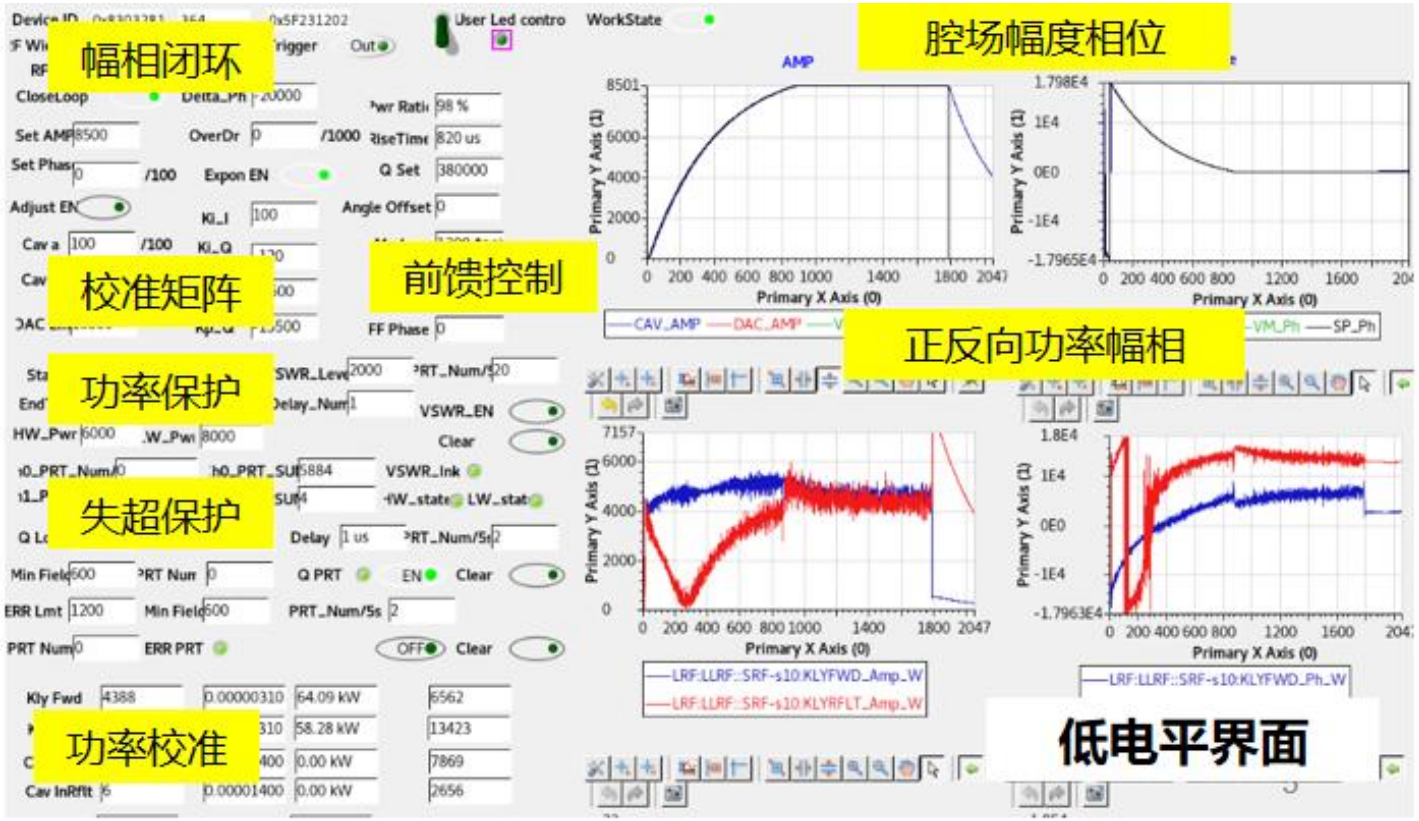
- Amp and ph stability is :±0.1%， ±0.1° 。



mTCA板卡

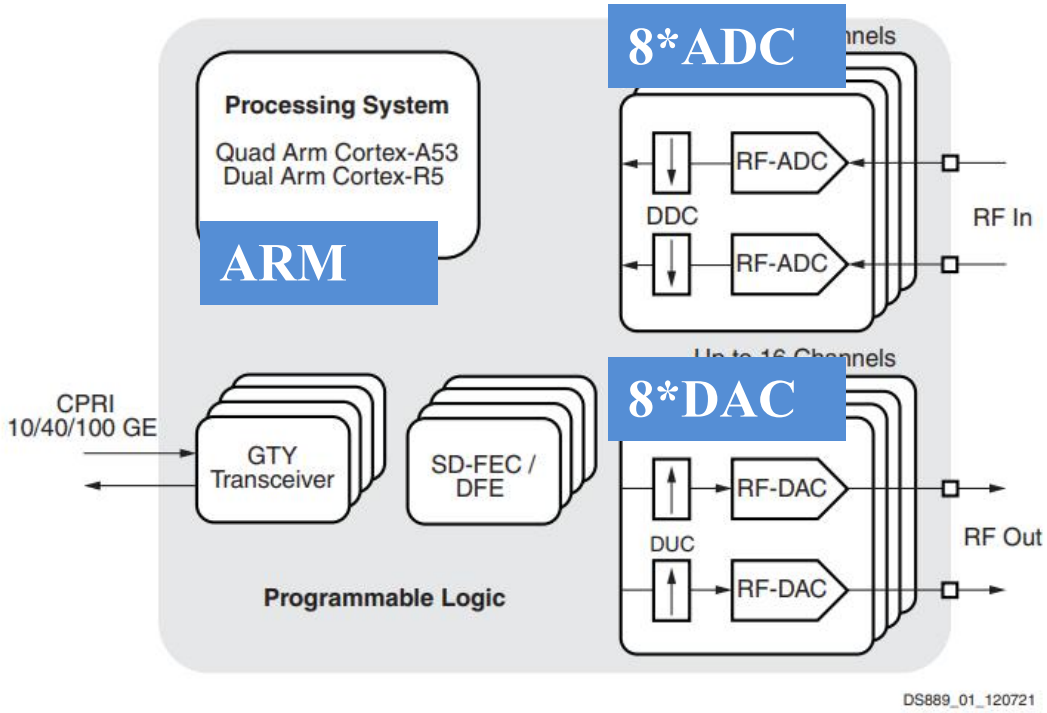


Amp/Ph stability : ±0.1%,±0.1°



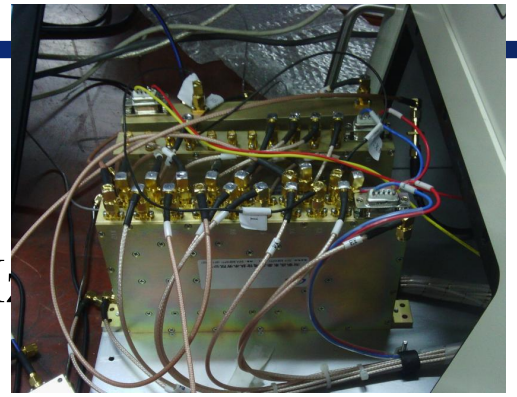
RFSoC(RF System on Chip)

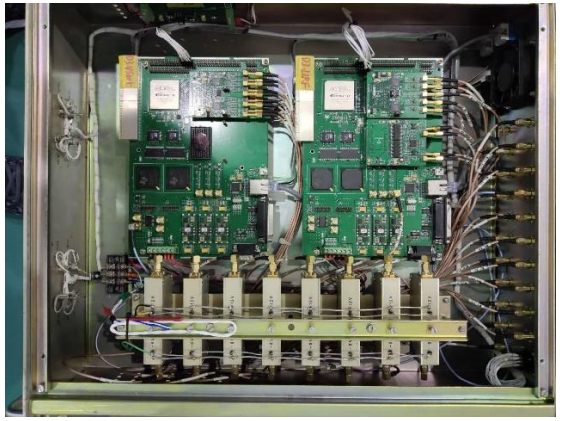
- Low latency, high speed,
- high integration, few components, easy to maintain
- The main clock frequency can reaches over 300MH



8*RFADC，8*RFDAC，6GHz sample rate，4-core ARM, abundant FPGA resources

CSNS-I LLRF





3.5cmx3.5cm

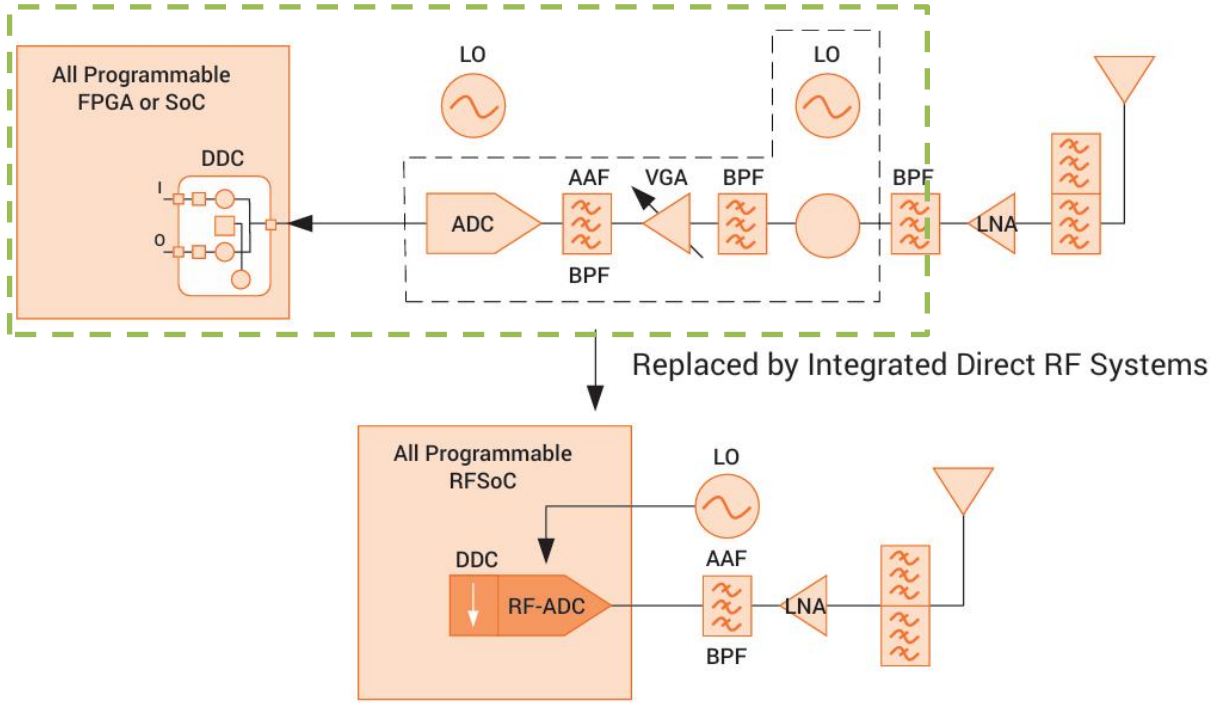
RFSoC Military applications

RFSoC is widely used in military applications

RFSoC for Radar and Electronic Warfare

RFSOC Technology – What's the big deal?

High IF Superheterodyne Receiver to a Direct RF-Sampling Receiver



All-Programmable, all connected

The **Zynq UltraScale+ RFSoC** from Xilinx eliminates the limitations of antennae bandwidth and the need for cumbersome external devices altogether by connecting data from the RF signal chain to FPGA accelerated hardware and software logic.

It enables direct conversion RF data without an intermediary.

As one of the first design houses in the world with access to this technology, DornerWorks can help you integrate that capability into your own system.

RFSoC technology is ideal for:

- 5G baseband wireless communications
- Millimeter wave mobile backhaul
- Cable Remote-PHY
- Milcom / airborne radio
- High performance RF applications requiring minimal ramp-up time and strict security

Innovation potential of the RFSoC

The Zynq UltraScale+ RFSoC has tremendous potential for applications in aerospace and the military, as well as consumer-focused wireless networks.

It leverages FPGA programmable logic to enable powerful and portable, low power RF signal processing. DornerWorks engineers are already experimenting with tools like Matlab, Simulink, and C/C++ to create HDL and VHDL models.

RFSoC design capabilities

- Programmable sine generator
  - 6 Gs/s to DAC
- Mix
- Capture 500 ms/s raw data
- Port VxWorks 7 to RFSoC
- ADC data to Digital Signal Processing
  - FIR filter
  - 2D FFT

https://dornerworks.com/wp-content/uploads/2020/08/DornerWorks-RFSoC-Design-Services.pdf

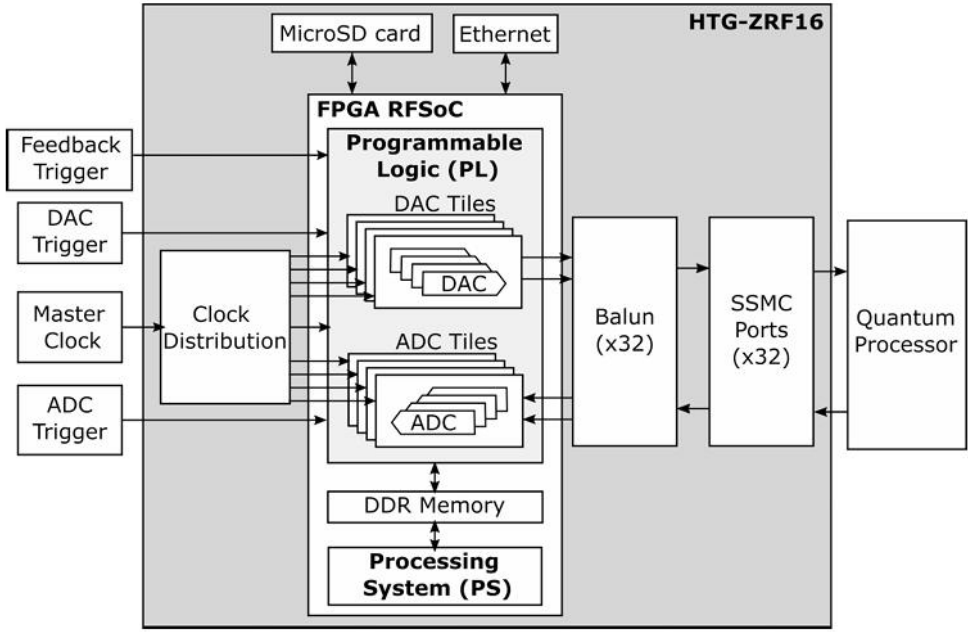
RFSoC Used in superconductig quantum computers

ICARUS-Q: A scalable radio-frequency system-on-a-chip based control system for superconducting quantum computers

Kun Hee Park,[1] Yung Szen Yap,[2,1,*] Yuanzheng Paul Tan,[3,1] Christoph Hufnagel,[1] Long Hoang Nguyen,[3] Karn Hwa Lau,[4] Patrick Bore,[1] Stavros Efthymiou,[5] Stefano Carrazza,[6,7,5] Rangga P. Budoyo,[1] and Rainer Dumke[1,3,†]

[1] *Centre for Quantum Technologies, National University of Singapore, 3 Science Drive 2, Singapore 117543, Singa*
[2] *Faculty of Science and Centre for Sustainable Nanomaterials (CSNano), Universiti Teknologi Malaysia, 81310 UTM Johor Bahru, Johor, Malaysia*
[3] *Division of Physics and Applied Physics, School of Physical and Mathematical Sciences, Nanyang Technological University, 21 Nanyang Link, Singapore 637371, Singapore*
[4] *Advinno Technologies Pte. Ltd., 22, Sin Ming Lane, #05-75 Midview City 573969, Singapore*
[5] *Quantum Research Centre, Technology Innovation Institute, Accelerator 2 building, on Plot M12, PO Box 9639, Masdar City, Abu Dhabi, UAE*
[6] *TIF Lab, Dipartimento di Fisica, Università degli Studi di Milano and INFN Sezione di Milano, via Celoria 16, 20133, Milan, Italy*
[7] *Theoretical Physics Department, CERN, Esplanade des Particules 1, 1211 Meyrin, Switzerland*

We present a control and measurement setup for superconducting qubits based on Xilinx 16-channel radio frequency system on chip (RFSoC) device. The proposed setup consists of four parts: multiple RFSoC boards, a setup to synchronise every digital to analog converter (DAC), and analog to digital converter (ADC) channel across multiple boards, a low-noise direct current (DC) supply for tuning the qubit frequency and cloud access for remotely performing experiments. We also design the setup to be free of physical mixers. The RFSoC boards directly generate microwave pulses using sixteen DAC channels up to the third Nyquist zone which are directly sampled by its eight ADC channels between the fifth and the ninth zones.



https://ui.adsabs.harvard.edu/abs/2022RScI...93j4704P/abstract

RFSOC used in BPMs

Conclusions…

I would like to say "none really: this was meant this user group, and maybe a collaboration?"

But looks weird a presentation without conclusions, so:

- **RF-SoC is a very promising technology**
- **The RF-SoC will be the core of the HL-LHC IR BPM system**
  - It is estimated that for this relatively complex system we will not go beyond 50% of the available resources in the FPGA logic
- **There are many resources online to get up to speed with designing for RF-SoC, still is a quite complex flow**

CERN

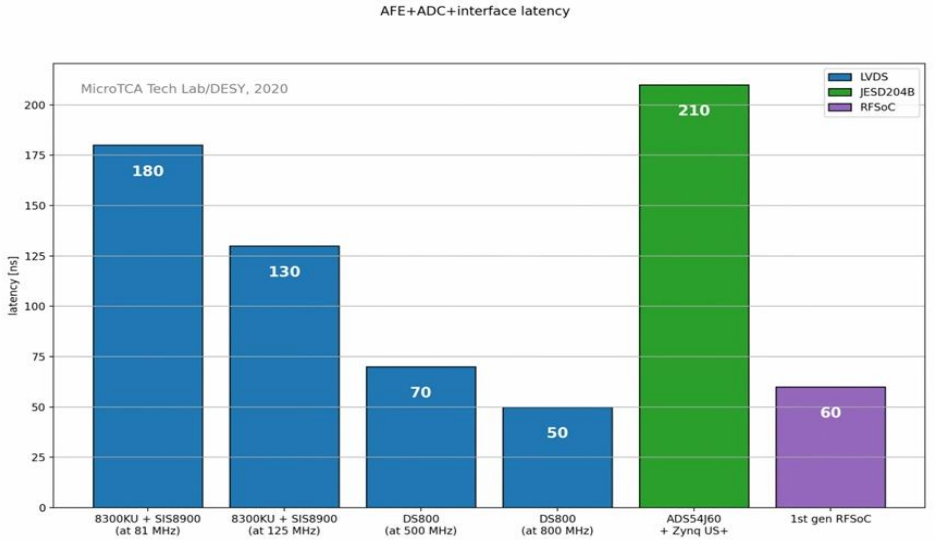
RF System-on-Chip use in the CERN Beam Instrumentation group

Andrea Boccardi, **slides from Irene Degl'Innocenti's presentation to the CERN 3rd SoC workshop** – CERN SY-BI-BP

TWEPP 2023 - FPGA user group

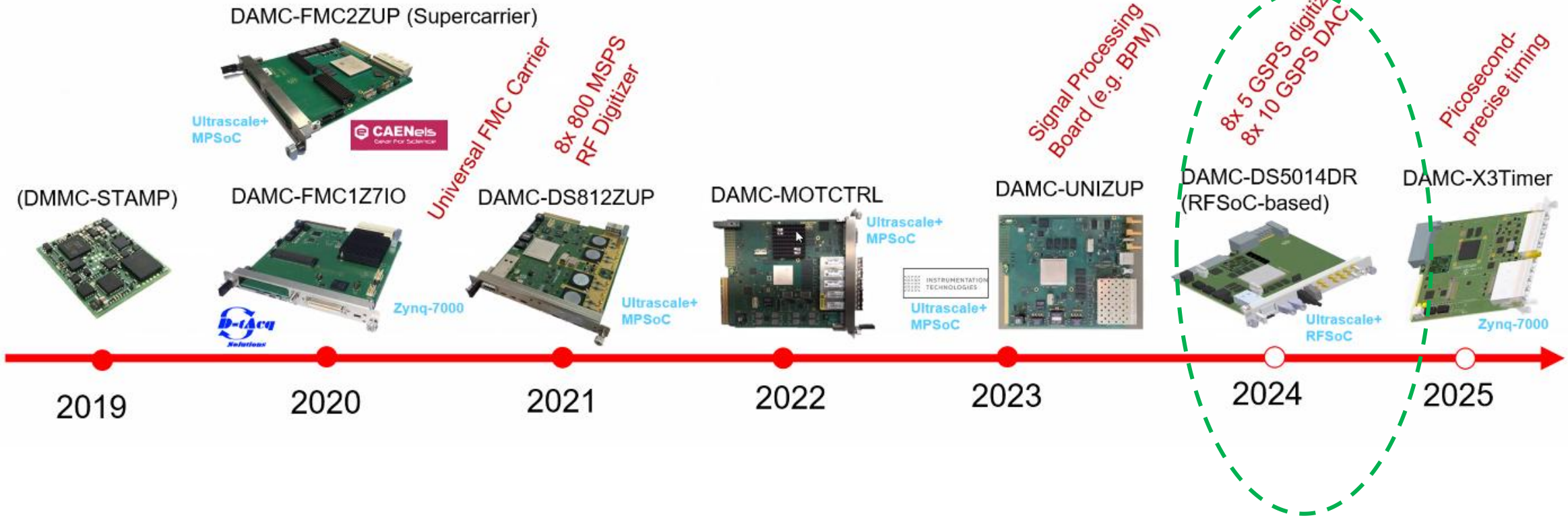
https://indico.cern.ch/event/1255624/contributions/5602029/attachments/2724818/4735110/TWEPP_RFSoC.pdf

RFSoC based mTCA



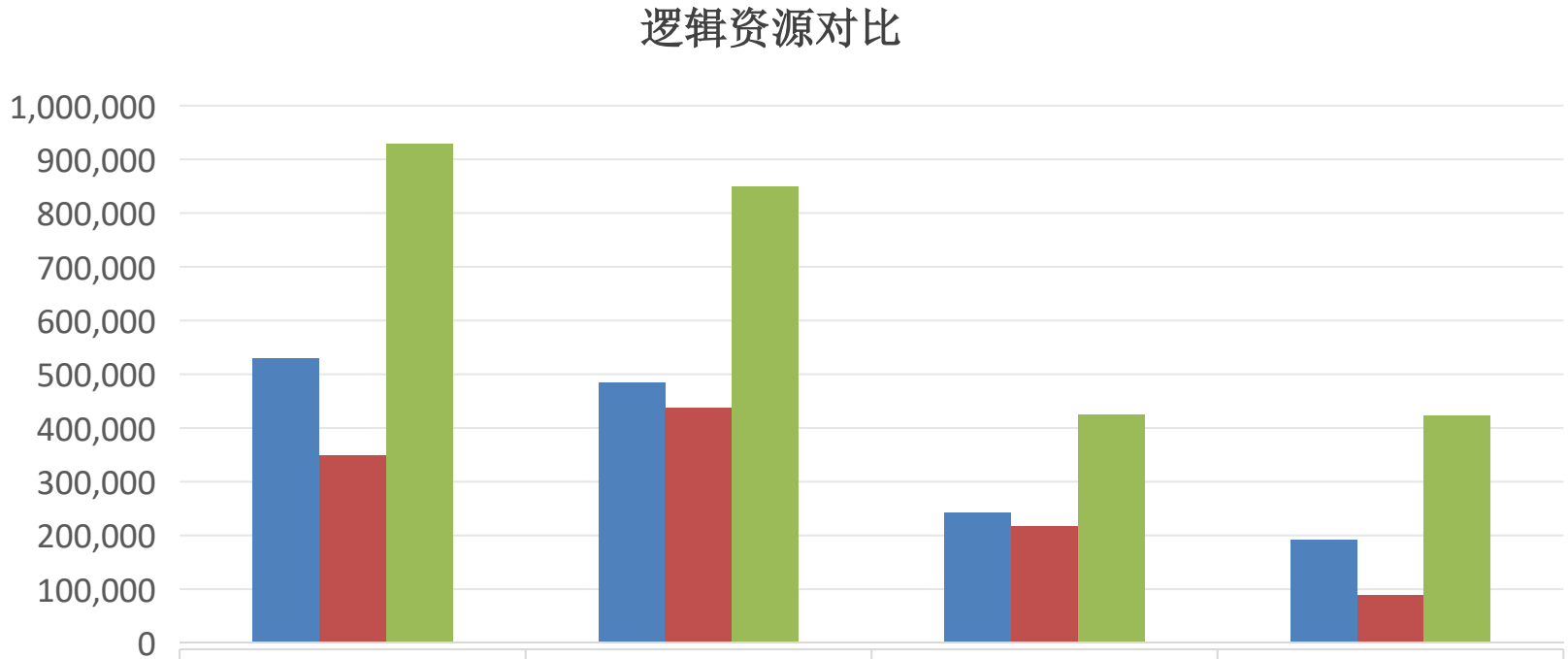
All SoC developments of the

Boards are all based on DMMC-STAMP



Logical Resource Comparison

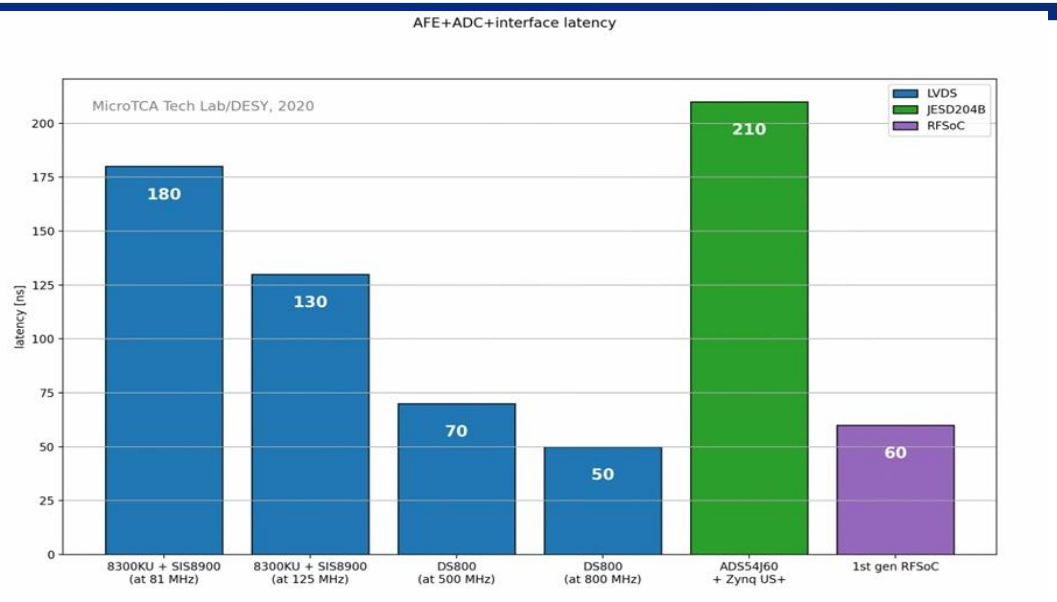
- FPGA resources are about twice that of conventional FPGA chips

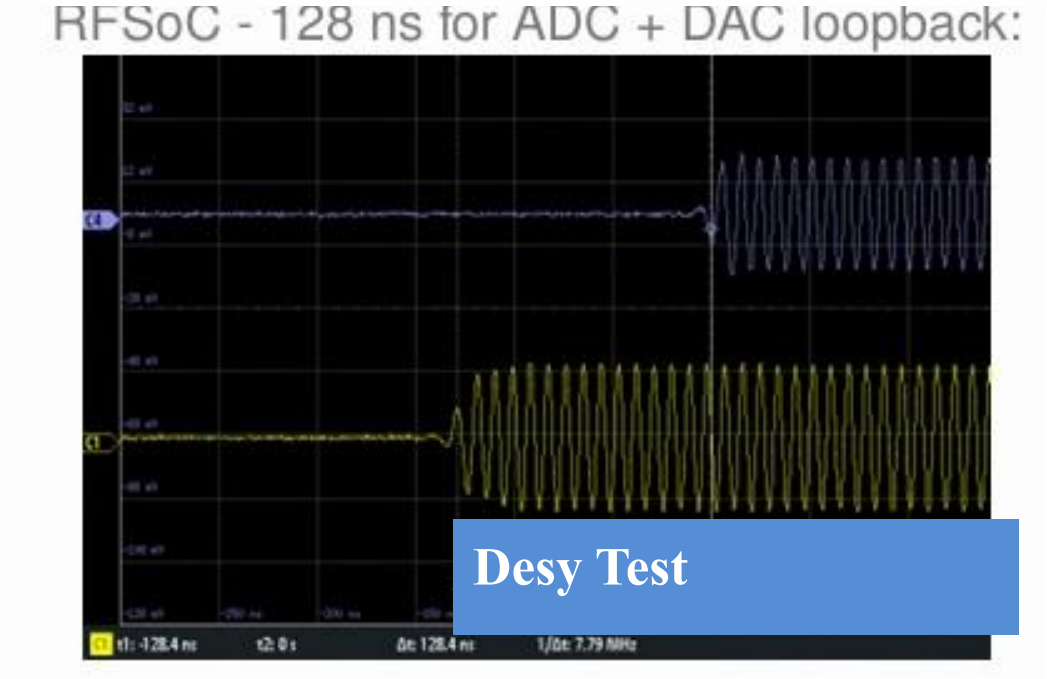


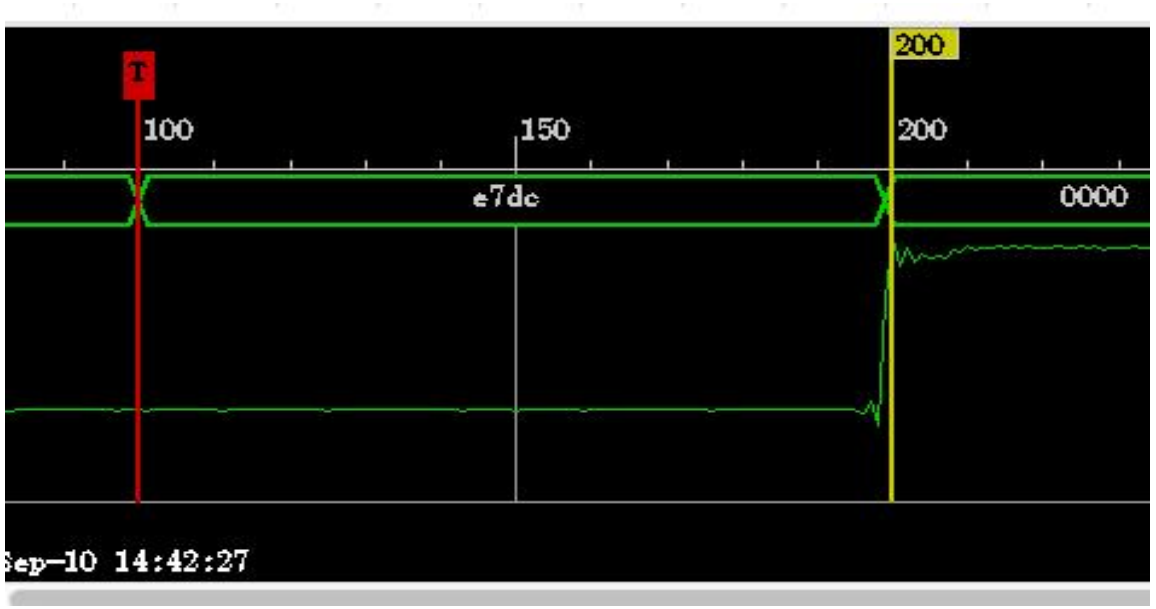
	System Logic Cells	CLB Flip-Flops	CLB LUT	DSP(*100)
8300KU	530,000	484000	242000	192000
ZYNQ-7000	350,000	437000	218000	90000
RFSOC-47DR	930,000	850000	425000	422700

注：DSP资源需要除以100才是真实值

RFSoC ADC+DAC LOOPBACK latence







- ✓ about 200ns for loopback
- ✓ Normal cir delay maybe about 1us

Comparison with 8300 board specifications

- Due to the wide sampling range of RF ADC and the need to cover the entire Nyquist sampling noise in SNR, it is not suitable for comparison. Generally, NSD (Noise Spectral Density) is used for comparison.

Board and signal		SNR(dBc)	SFDR(dBc)	NSD(dBFS/Hz)
SIS8300	ADC-20MHz	76	86	-154
	DAC-20MHz	74	64	-152
RF SOC	ADC-240MHz	59	86	-152
	ADC-900MHz	58	79	-151
	DAC-900MHz	-	81	-

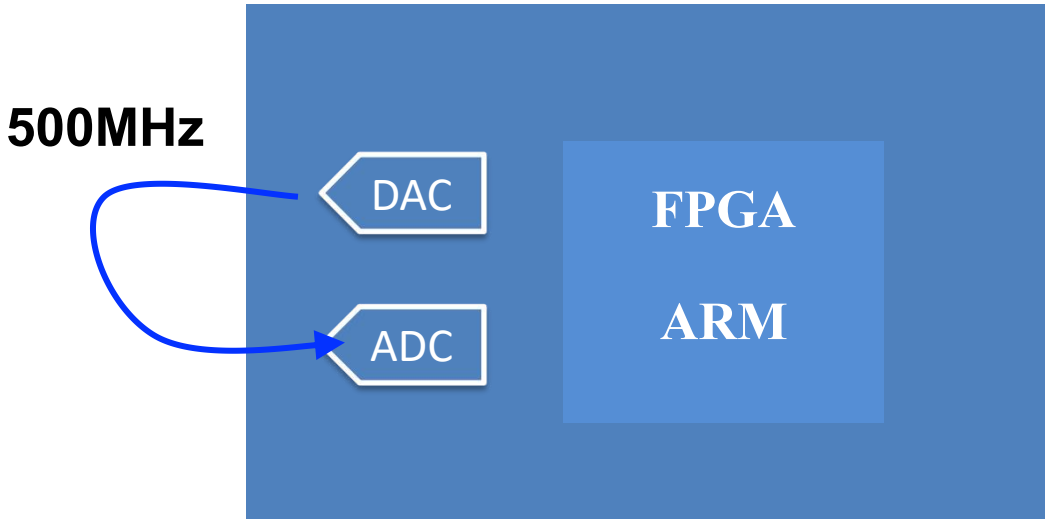
$$SNR_{(dB)} = 10\log_{10}\left(\frac{P_{fundamental\ signal}}{P_{noise\ (over\ Nyquist\ BW)}}\right)$$

$$NSD_{(dBFS/Hz)} = -SNR_{measured(dBFS)} - 10\log_{10}\left(\frac{fs}{2}\right)_{(Hz)}$$

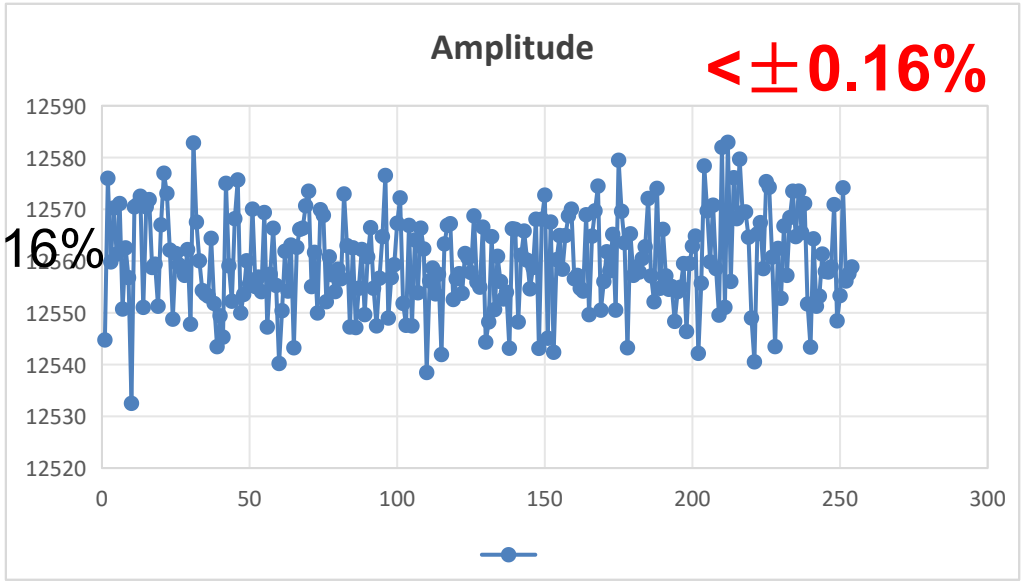
RFSoC and KU board NSD are close

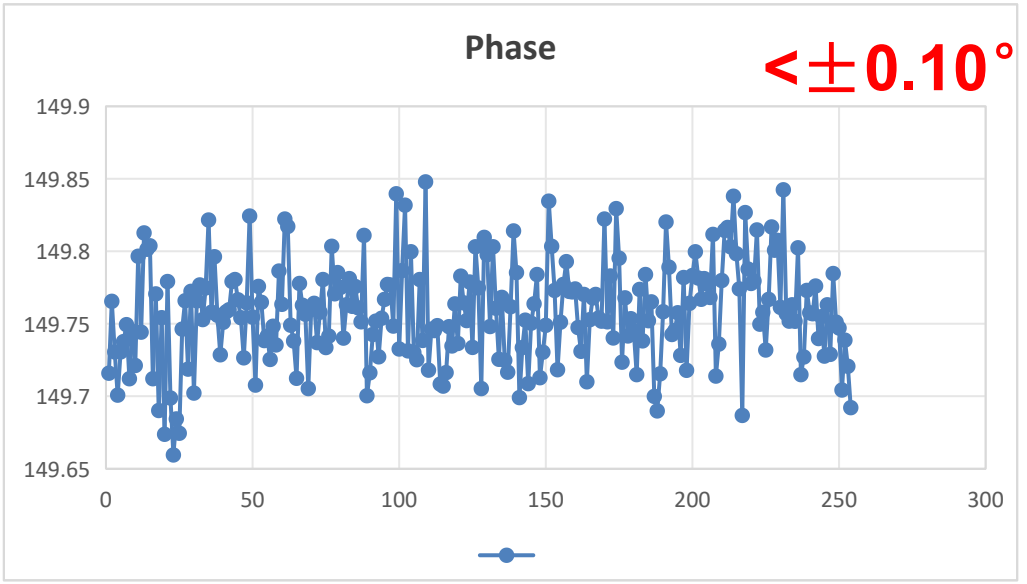
ADC/DAC Loop Test

- Test conditions:
  - The center frequency is 500MHz.
  - The amplitude and phase are less than ± 0.16% and ± 0.1 ° , respectively.
  - Meet the requirements of Phase II

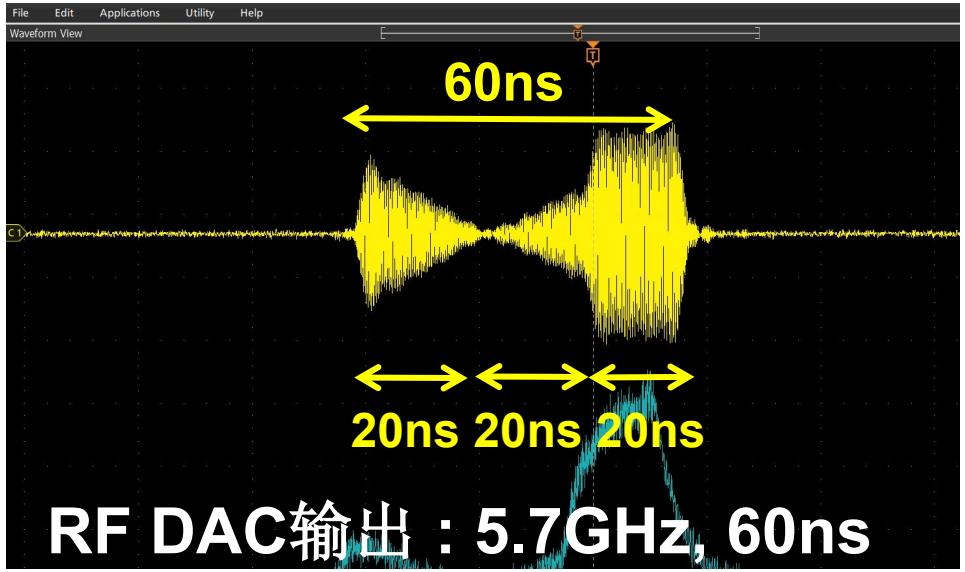


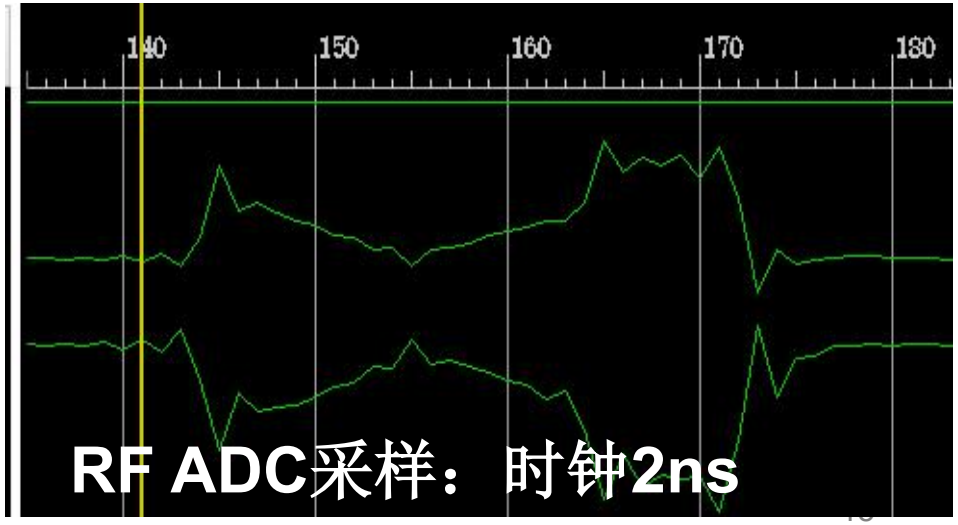
RFSoC Loopback test



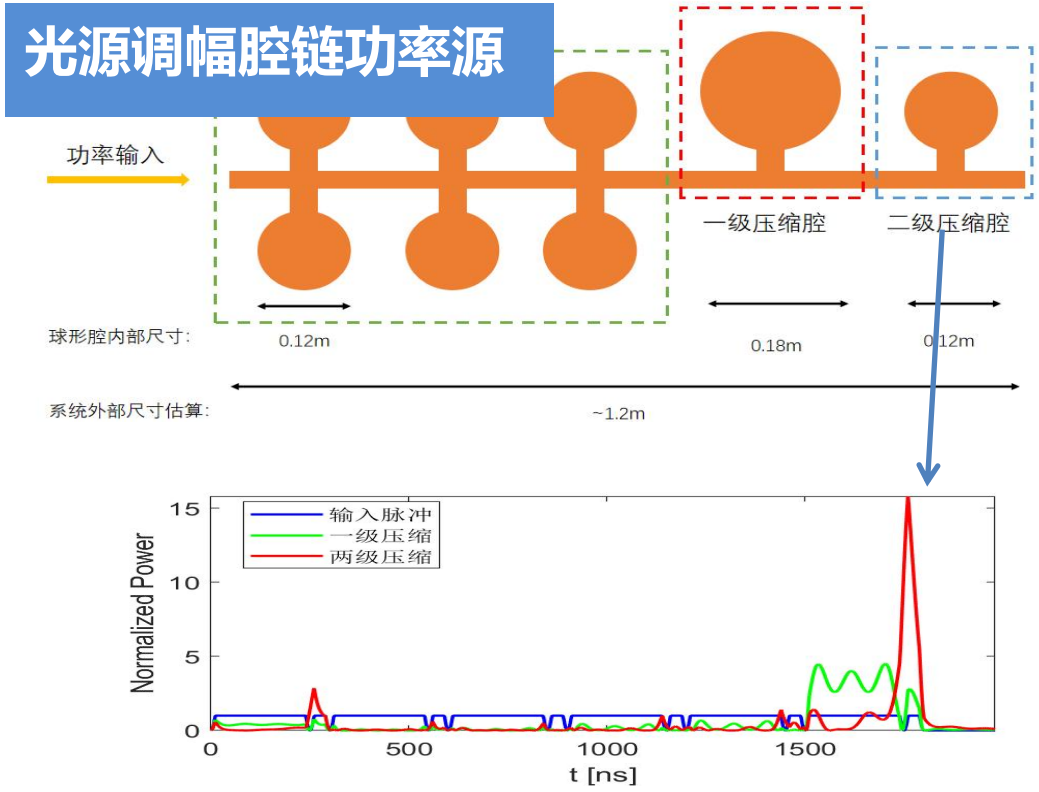


RFSoC Short pulse sampling



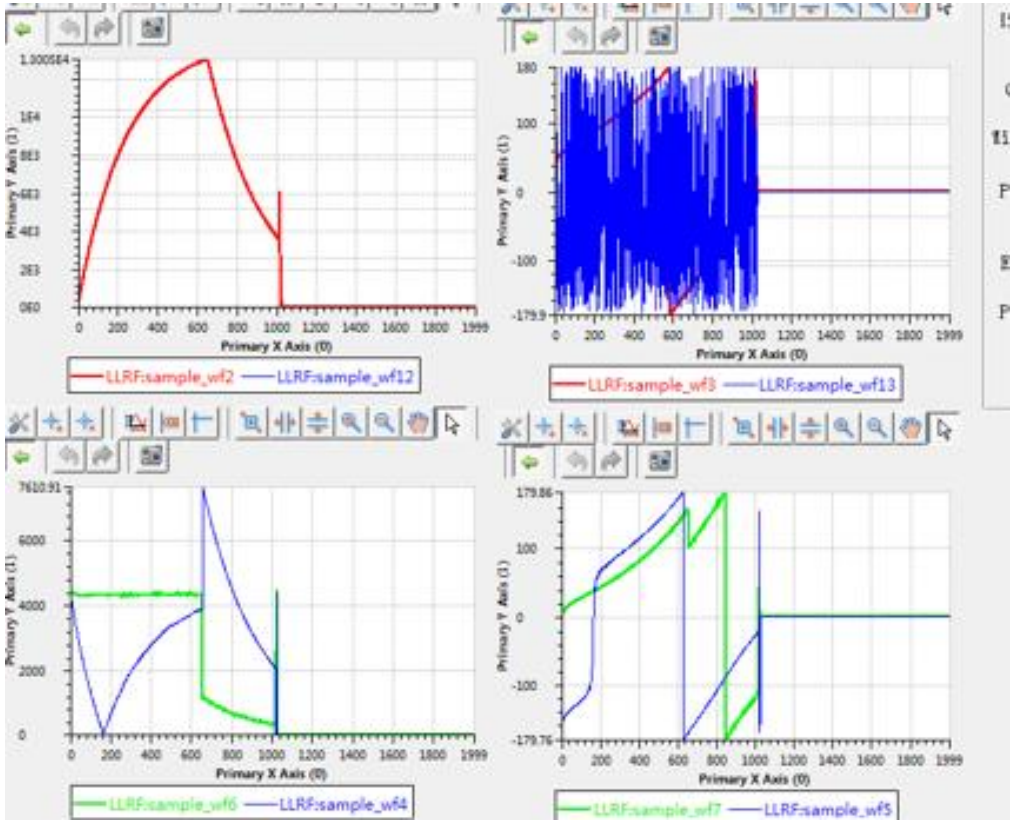


Short pulse are widely using in S/C BAND RF power source. Some may less than 50ns.

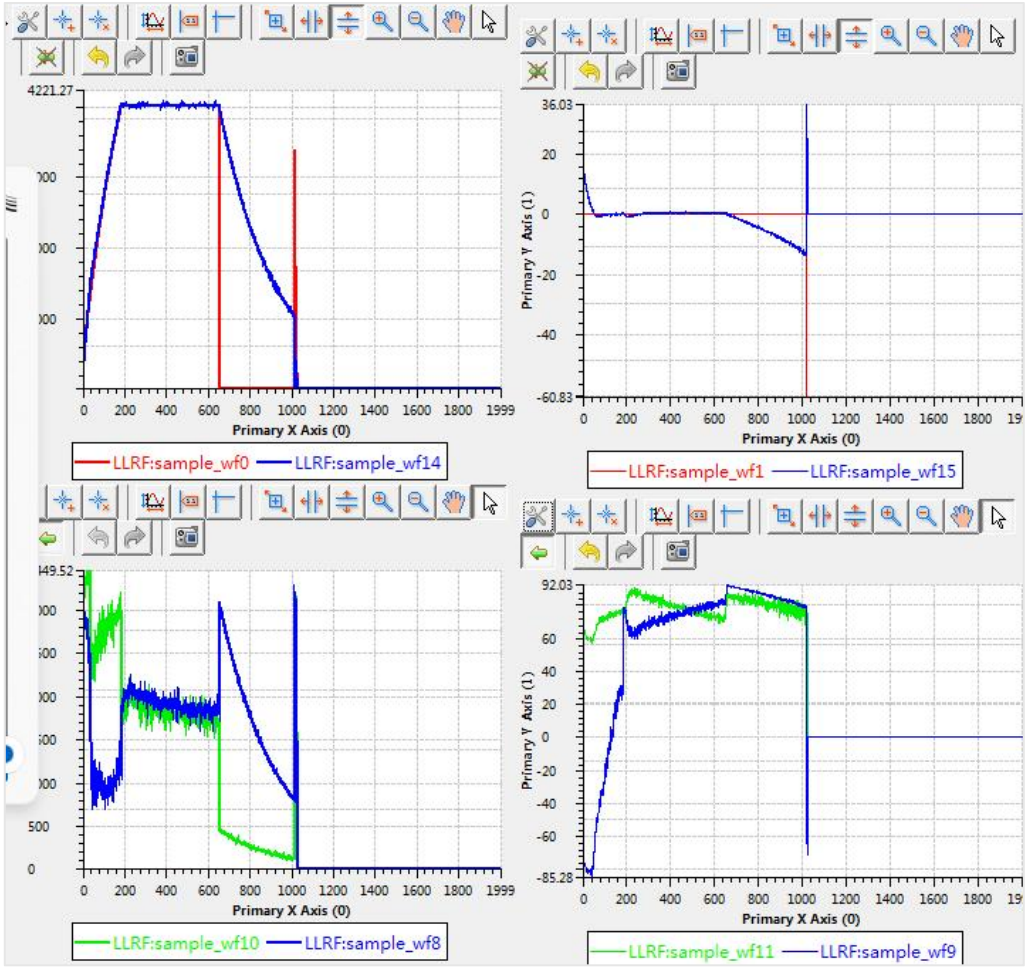


Second compress, 50ns

Horizontal Test using RFSOC/2025-8



Self-excite LOOP test



AMP/PH CLOSE LOOP TEST

Conclusion

- Studies on the performance metrics and applications of RFSoC have been carried out.
- Successful horizontal testing of superconducting cavities has been realized.
- More research will be conducted in the future,long-term stability,etc.

Thank you!