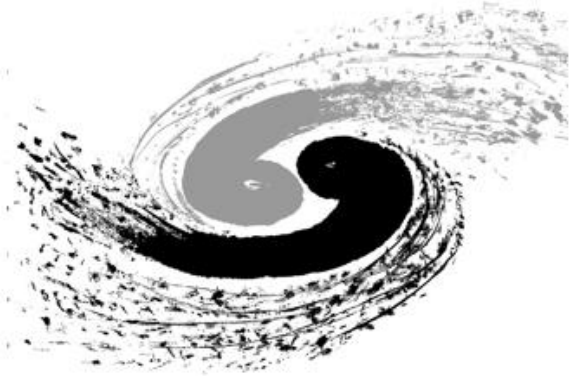
Development progress of LO&CLK distribution RTM board

GAO Wenbin（高文斌）, GAN Nan（甘楠）, MA Xinpeng（马新朋）,
MU Yajie（牟雅洁）,PENG Yongyi（彭永宜）, LI Jingyi（李京祎）



LINAC Group, Accelerator Center
Institute of High Energy Physics, CAS
2025-9-15

Outline

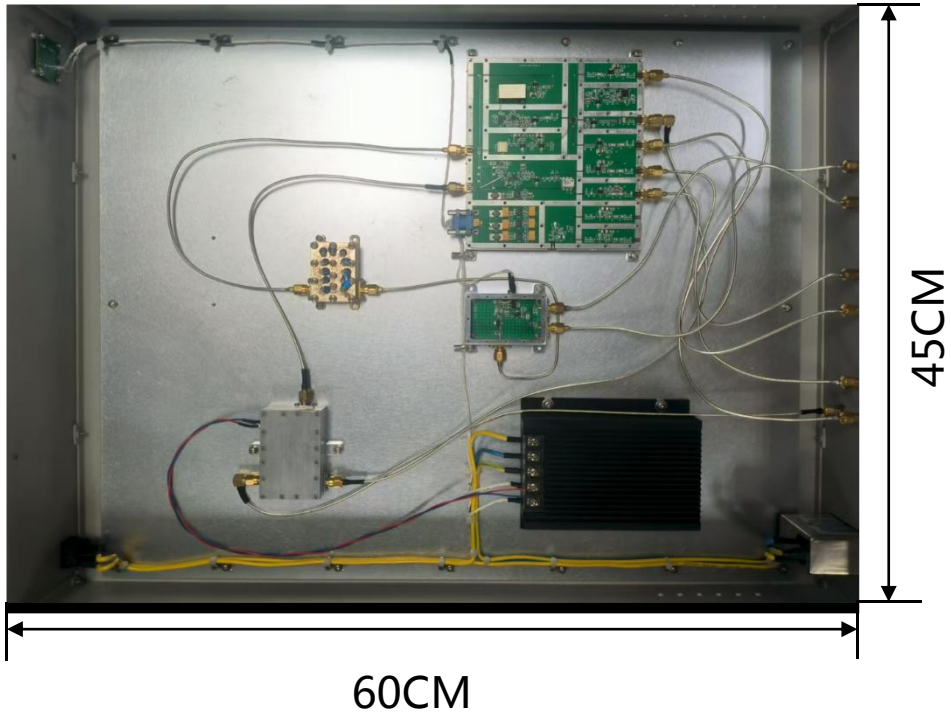
- Motivation
- Design, progress and status
- Future plans

Motivation

- at IHEP, several types accelerators, different frequencies, BEPCII: 2856MHz / 571.2MHz / 142.8MHz, HEPS: 2998.8MHz / 499.8MHz / 166.6MHz, CEPC 9cell SC/NC: 1.3GHz / 650MHz / 2860MHz / 5720MHz ..... many different LLRF
- LO/CLK and RF front-end are different for these projects, should be modular and least change among develop and maintainence

Motivation

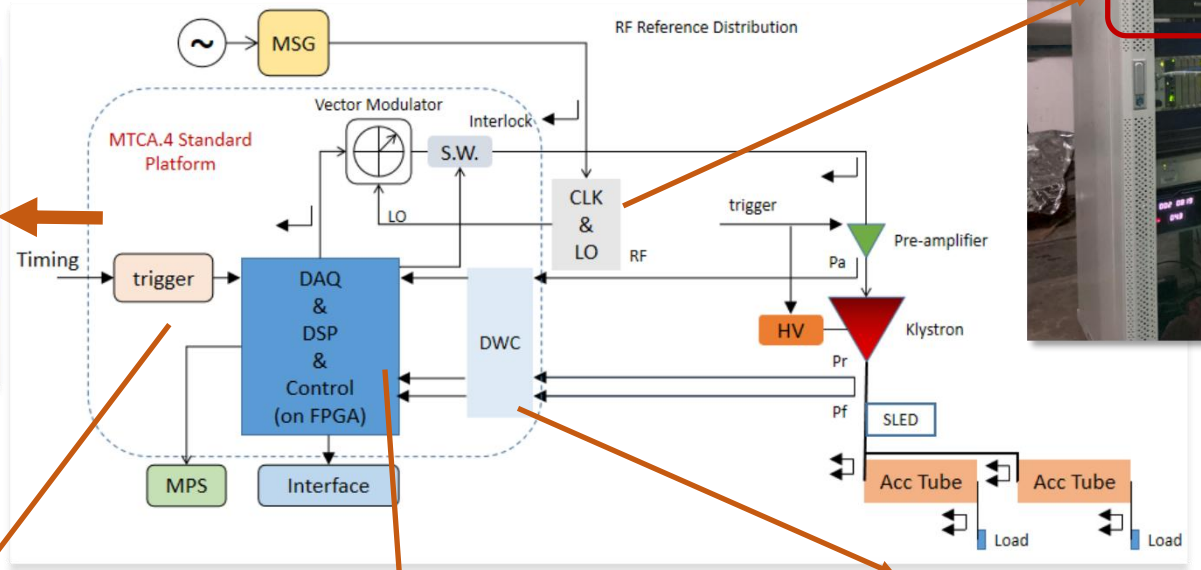
- Now LO&CLK modules used are standalone ‘box’ with limited temperature stability and not fully monitored and managable
- Change of LO/CLK due to temp/humi not easy fully monitored and calibrated even using “reference tracking”
- LO&CLK shall be absolutely stable

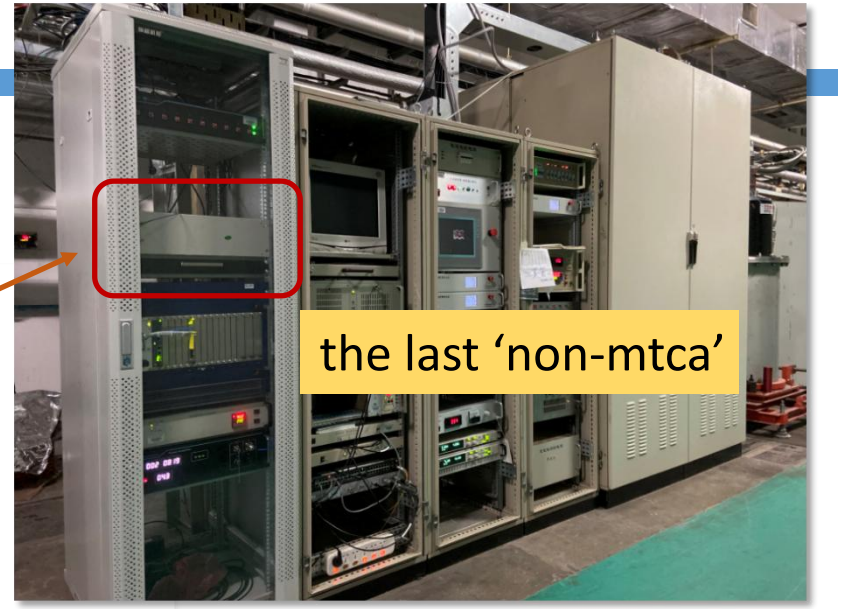


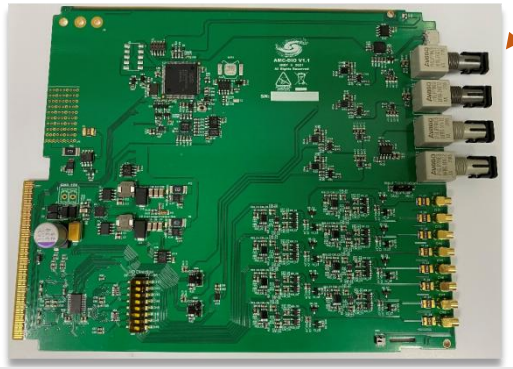
Motivation

- Besides, our MTCA hardware: .

HEPS chassis (3U/2U/9U)







In-house made Trig/DIO

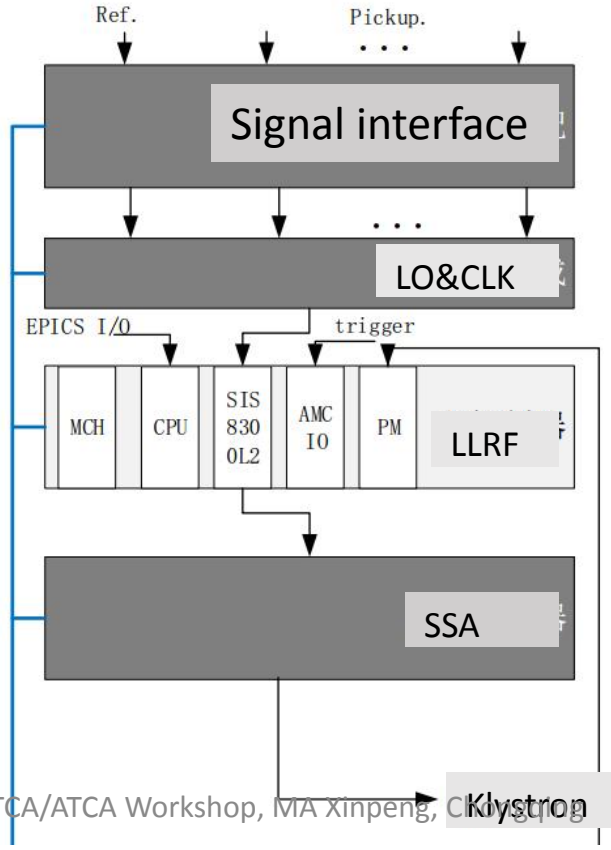
DAQ controller

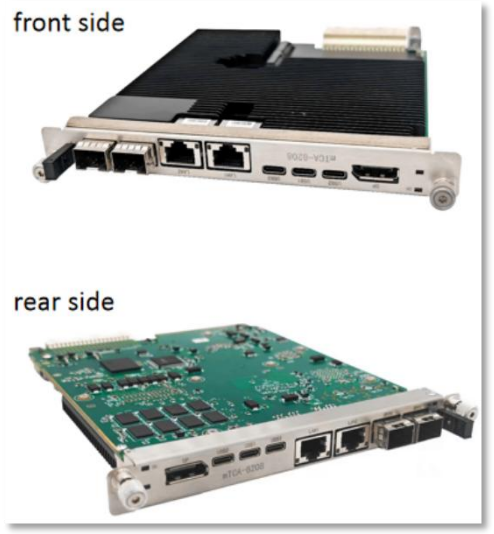
In-house DWC 2998.8MHz

In-house DS 166.6/499.8MHz

Motivation

- our most cases are compact application in small chassis
- one MCH/CPU/PM, 4~6 AMC/RTM boards are sufficient including digital boards, so only 4 LO&CLK are required
- work with our new downconvert RTMs and 2U chassis etc.

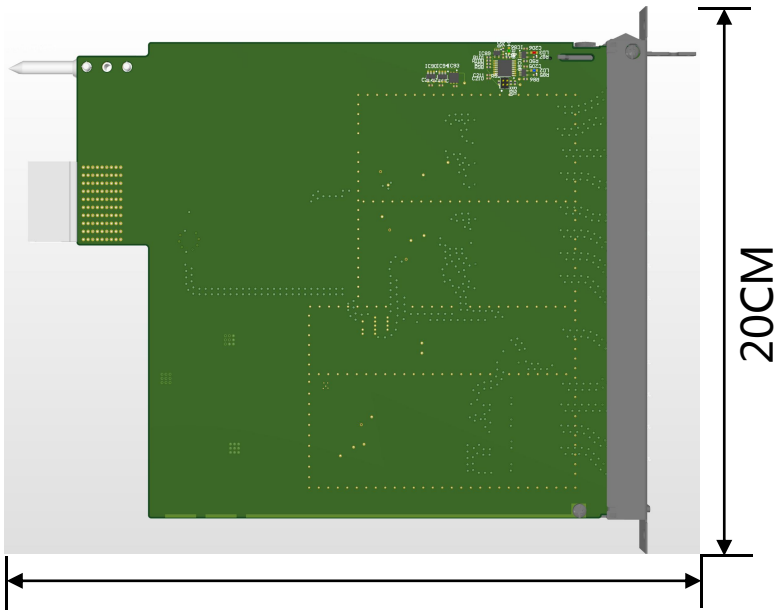




Design, progress and status

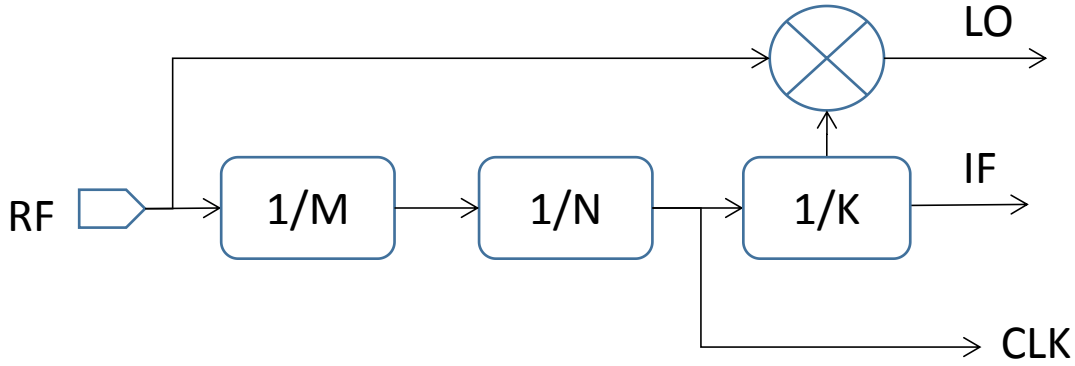
Design

- Purpose:
- develop one LO&CLK generation and distribution RTM board, compatiple with existed DWC-RTM and 2U/3U chassis
- 1 RF Reference input
- Generate 3 types frequencies, each type distribute out 4 channels, for maximum 4 DWC applications



Design

- LLRF frequencies choice(LO/CLK/IF):
- I/Q sampling is enough for most cases, as phase relation is easy to restore
- all the IF/CLK ratio is tried to be the same in design period so that the firmware and software could be remain the same
- So only LO/CLK-RTM board need modified, DAQ-AMC/DWC-RTM barely change - over lifetime



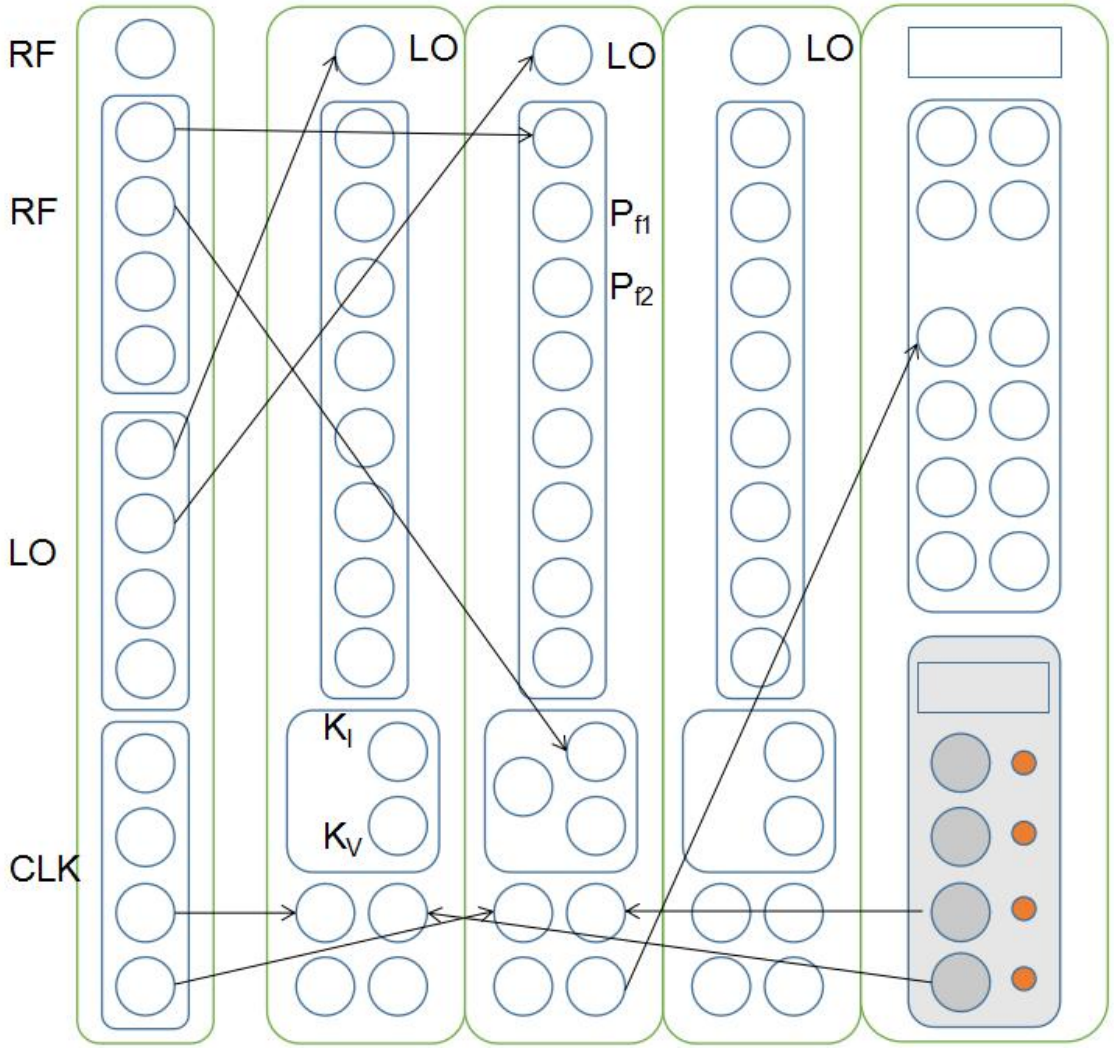
Singals/MHz	M=2 N=14 K=4	M=2 N=15 K=4	M=1 N=13 K=4	M=1/2 N=13 K=4
RF	2998.8	2856	1300	650
LO=RF-IF	2972.025	2832.2	1275	625
CLK	107.1	95.2	100	100
IF	26.775	23.8	25	25
IF/CLK	1/4	1/4	1/4	1/4

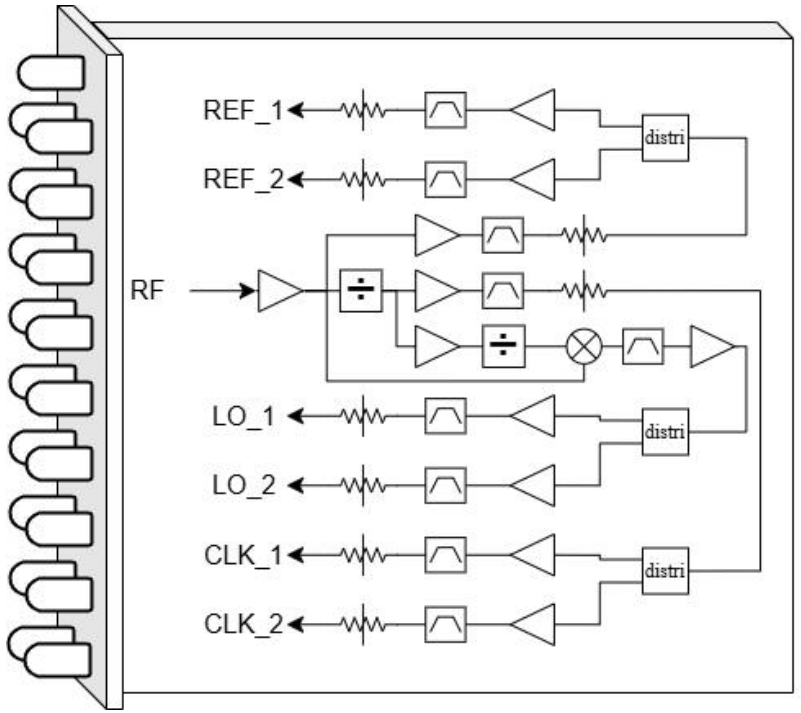
Design

- Main Spec :
- Ref RF frequency：2856MHz
- CLK frequency：95.2MHz
- LO frequency：2879.8MHz
- input signal level：-10~10dBm
- output signal level：>13dBm

- Compatible with MicroTCA.4 RTM, supported by MMC protocal with an AMC
- Provide singal power, board status info by I2C bus
- Prototype is 2856MHz, CLK can be suitable for most ADC, IF/CLK = 1/4 for I/Q sampling

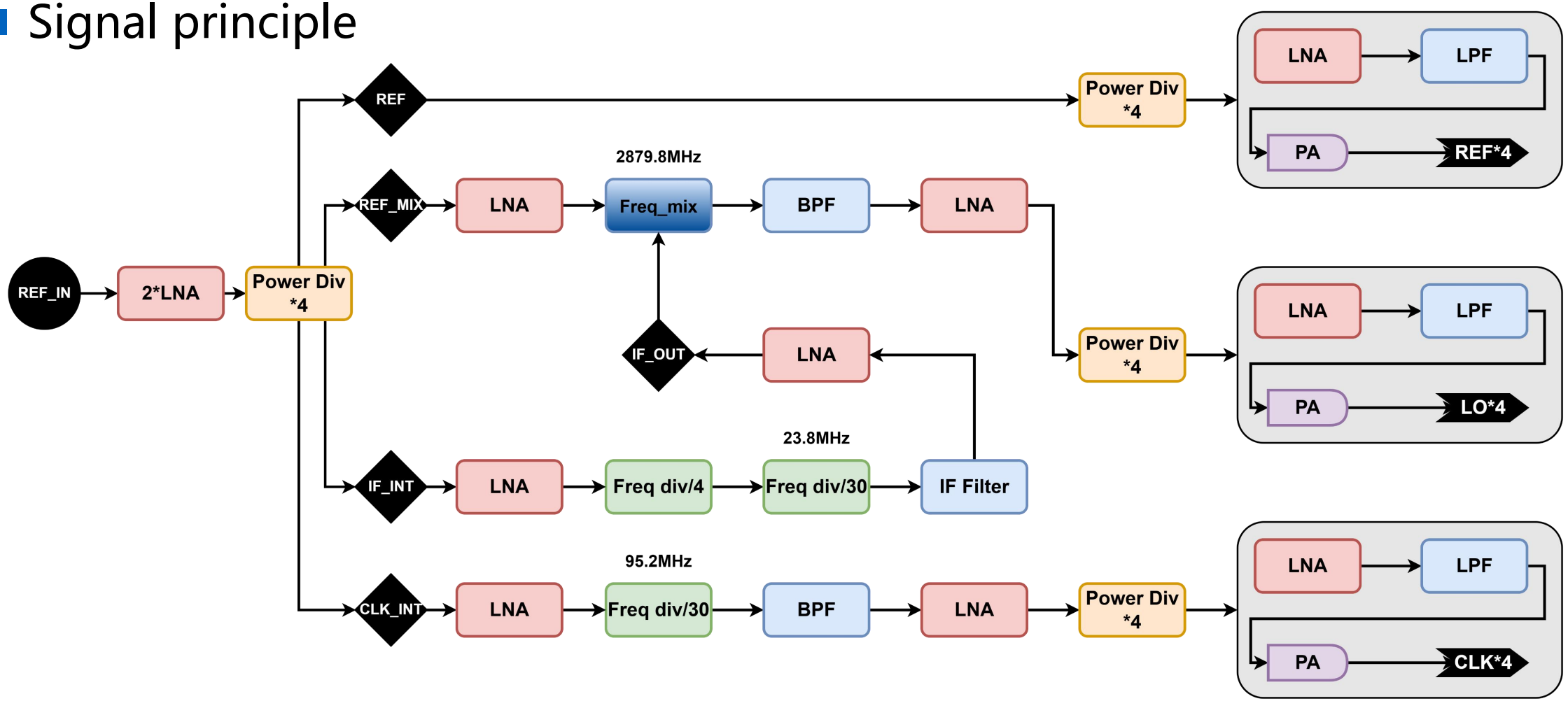
Design


RF
RF
LO
CLK
LO
LO
LO
P_{f1}
P_{f2}
K_I
K_V


REF_1
REF_2
RF
LO_1
LO_2
CLK_1
CLK_2
distri
distri
distri

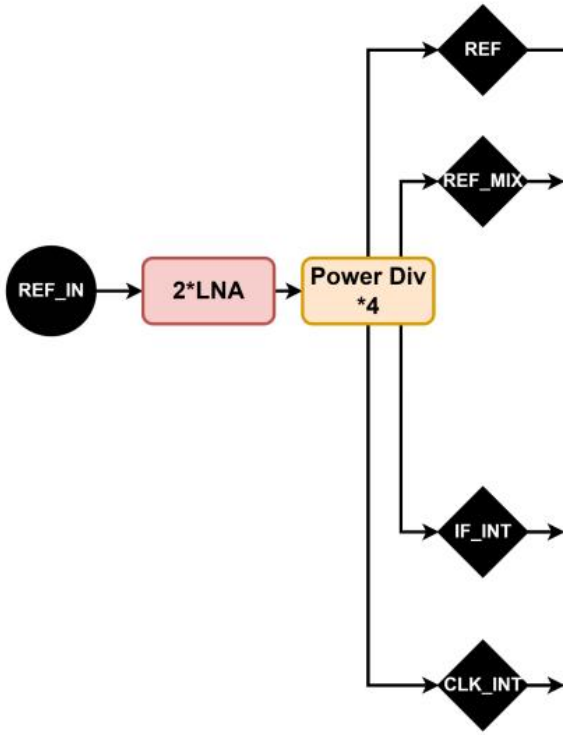
Progress

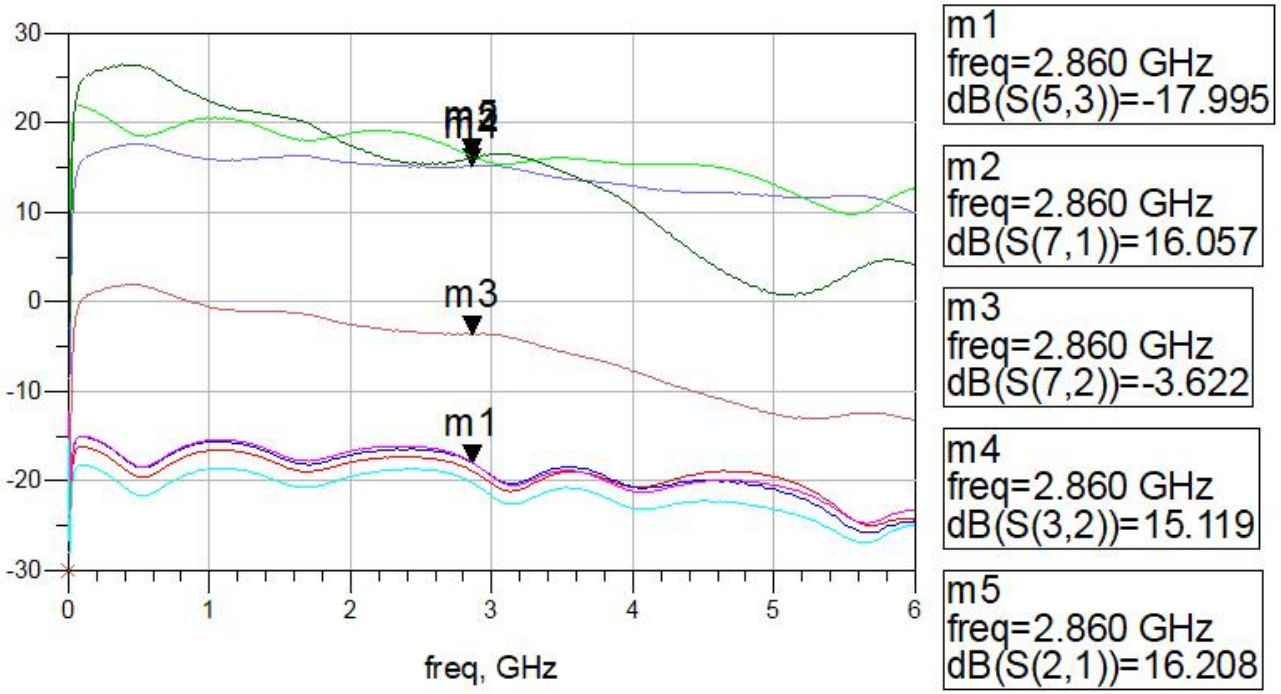
- Signal principle



Progress

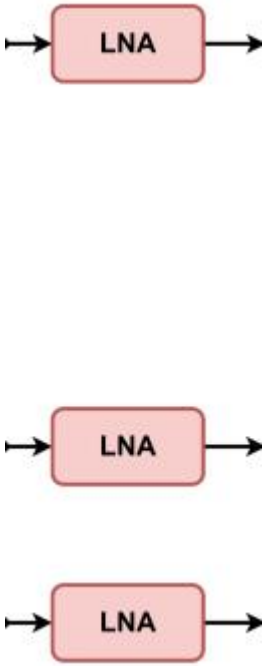
- Pre-amplifier and divider part S parameter simulation
- calculate and evaluate the required power output for each path - ✔

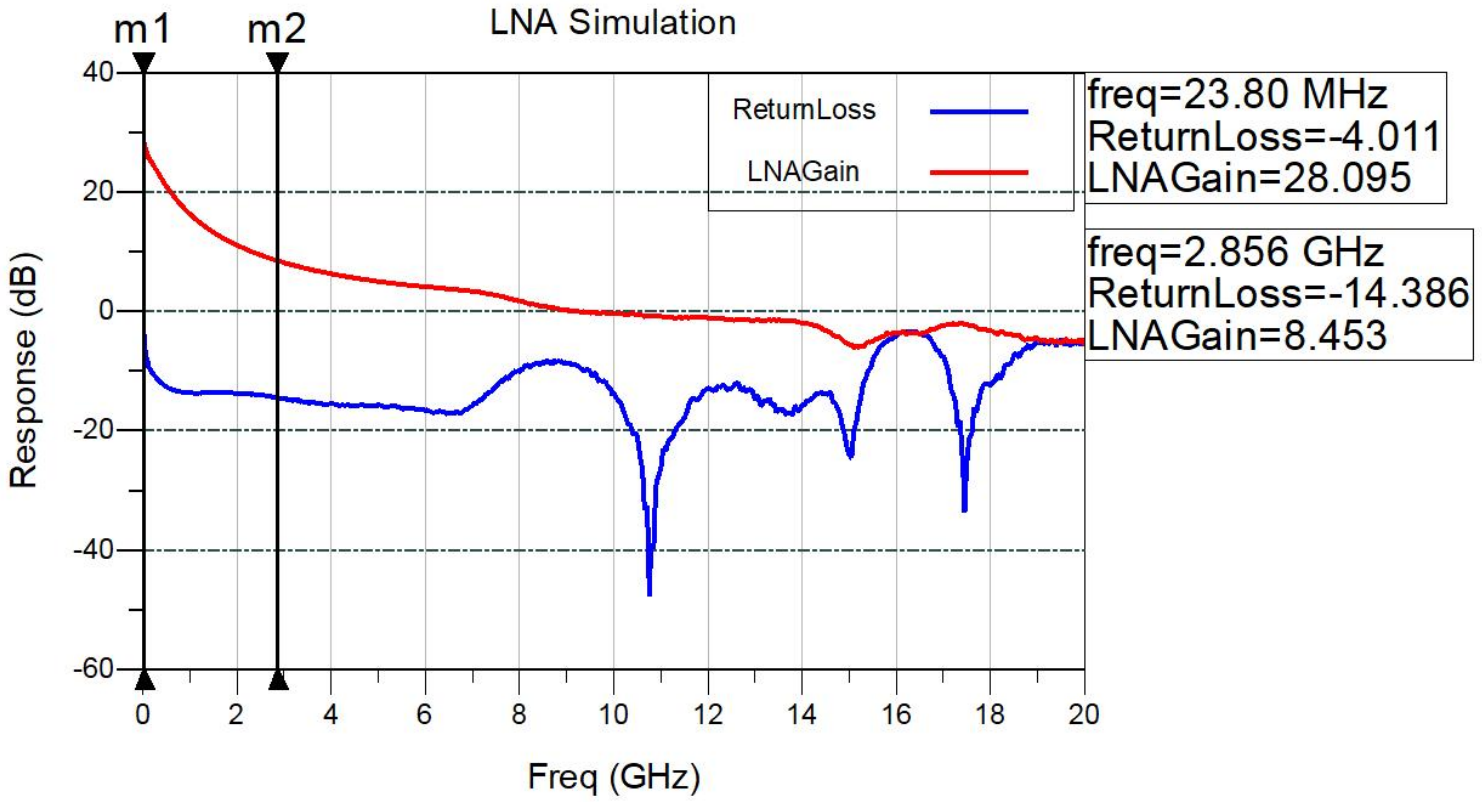




Progress

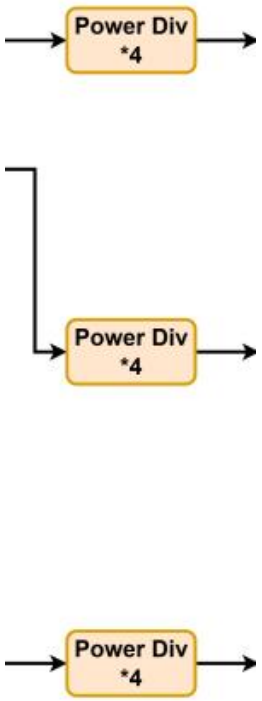
- Low noise amplifier S parameter simulation
- Simulate the LNA/attenuator to evaluate the signal power along - ✔



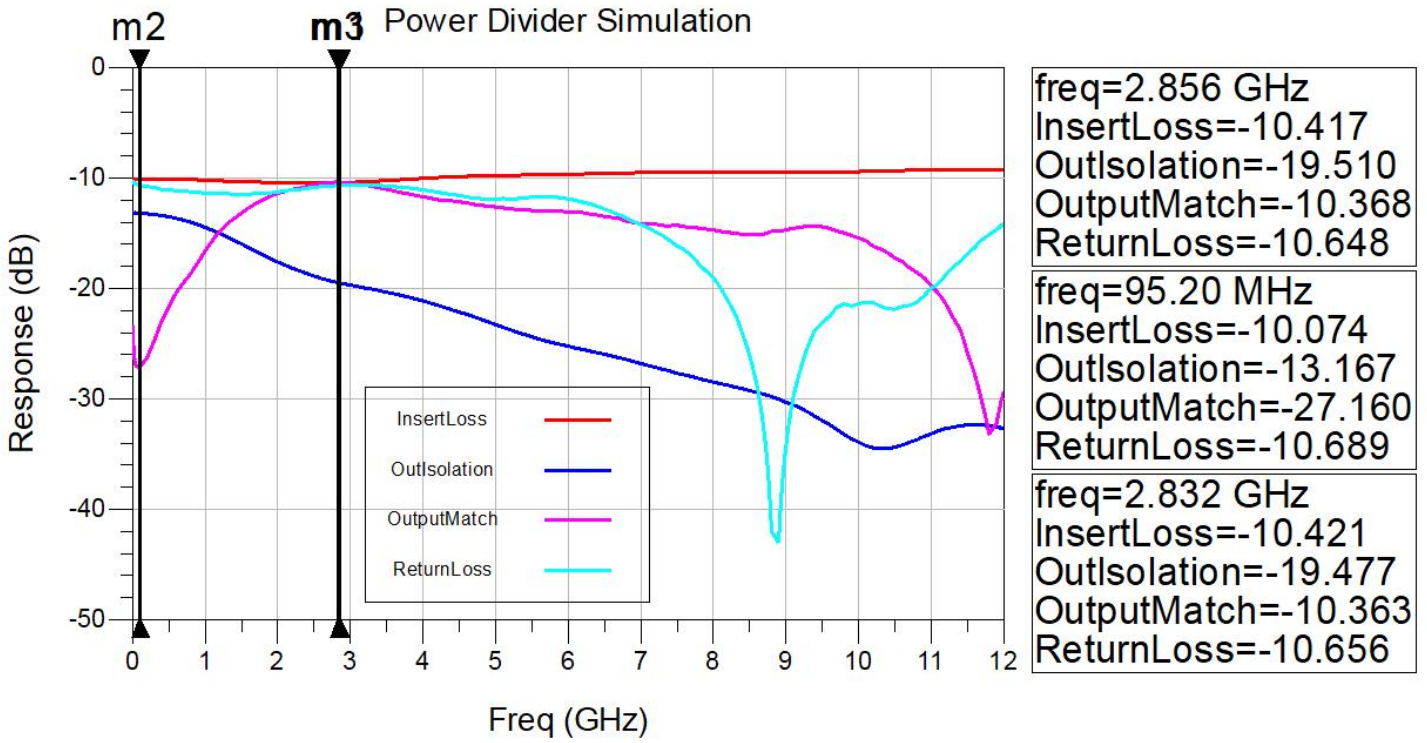


Progress

- Power divider
  S parameter simulation

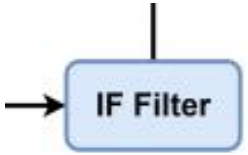


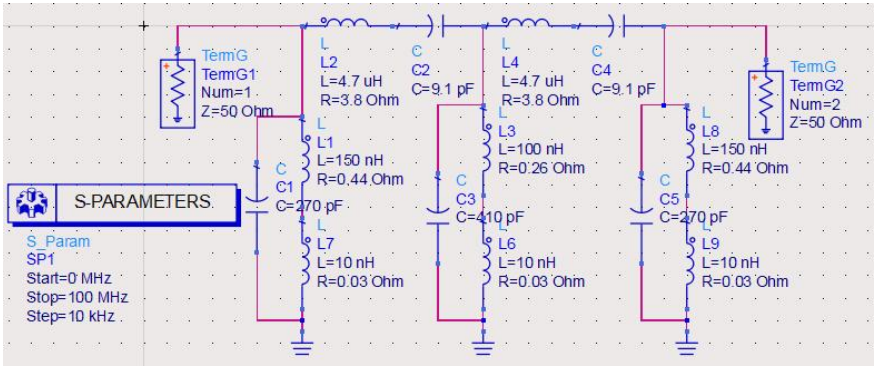
- Simulate the power divider - ✔



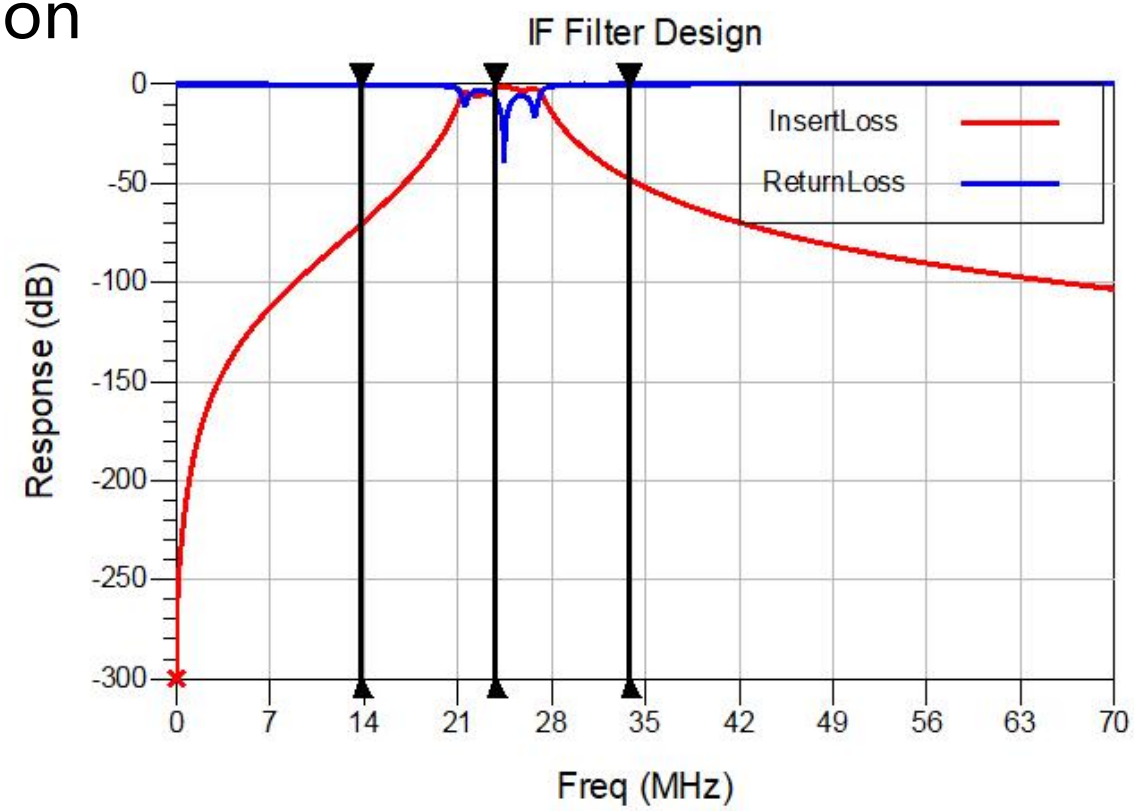
Progress

- IF Band pass filter (23.8MHz, LC type), S parameter simulation





- Simulate the BPF - ✔



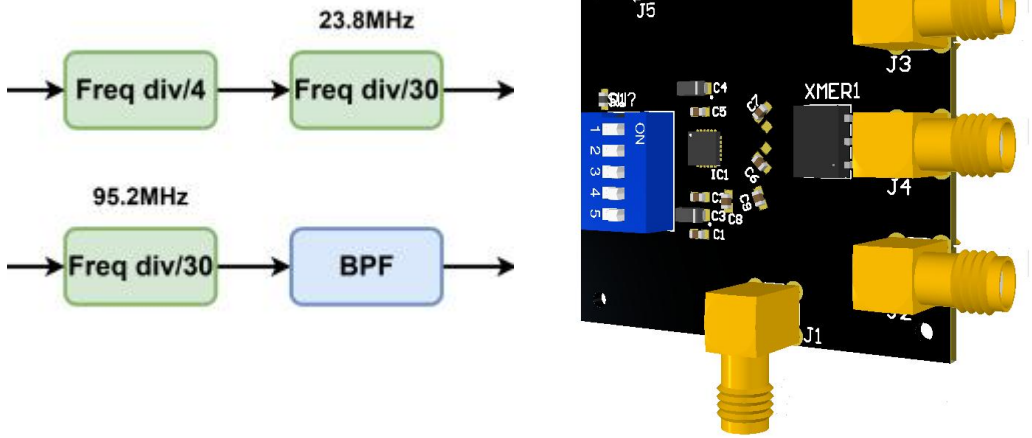
freq=23.80 MHz
InsertLoss=-2.493
ReturnLoss=-7.067

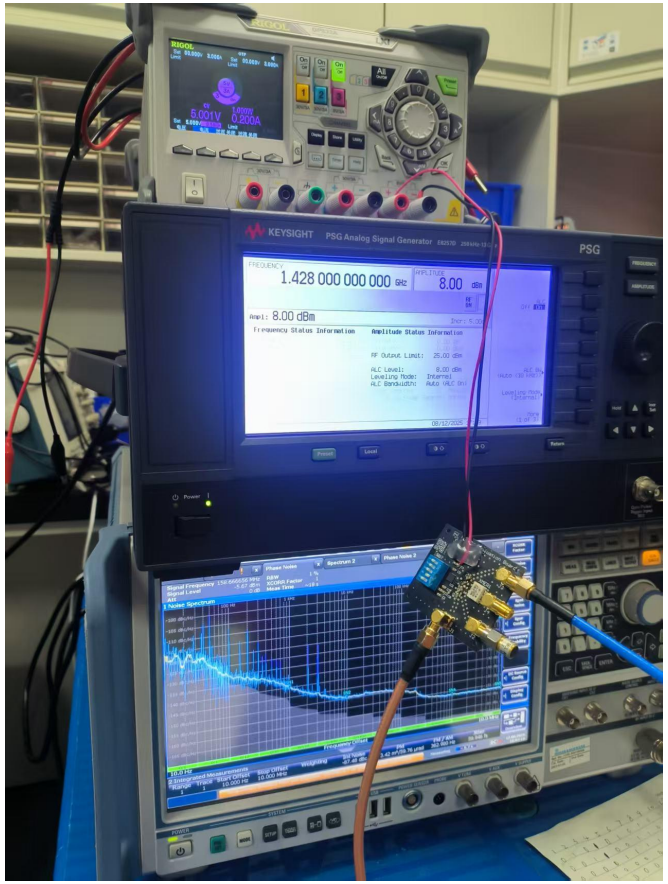
freq=13.80 MHz
InsertLoss=-70.640
ReturnLoss=-0.320

freq=33.80 MHz
InsertLoss=-47.963
ReturnLoss=-0.140

Progress

- Frequency divider evaluation
- still under test with harmonic filter, divide number, insertion loss …





输入：1428MHz 8dBm　　源噪声：27.547fs	
分频率	相位噪声/fs（10Hz~10MHz）
1	/
2	37.085
3	43.231
4	47.855
5	53.808
6	56.834
7	60.648
8	63.367
9	69.961
10	70.631
11	74.743
12	75.288
13	79.035
14	84.016
15	90.584
16	89.887
17	97.655
18	99.426
19	106.568
20	111.124
21	114.601
22	122.368
23	203.117
24	178.569
25	177.339
26	181.47
27	178.267
28	179.904
29	198.727
30	193.528
31	197.484
32	209.469

Progress

- Evaluate several used low noise amplifier (LNA)
- Mostly use PGA103 from Mini-circuit ✔

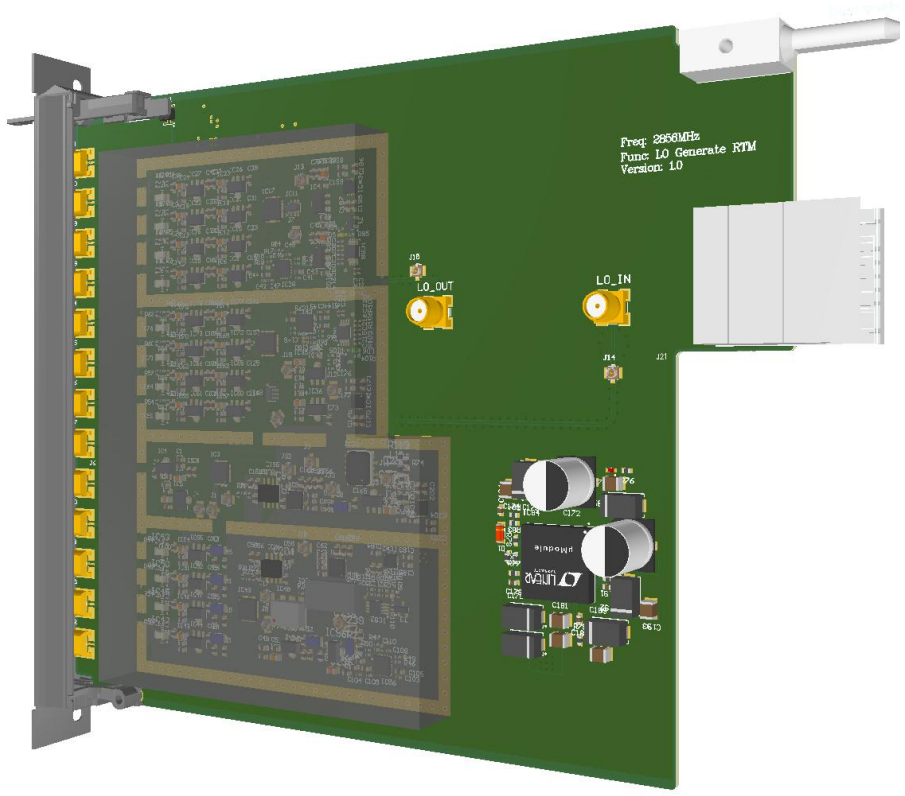
Chip	Freq/MHz	Gain/dB	jitter/fs/ /10Hz-10MHz	Vendor
SPF5122Z	166.6	24	40	Qorvo
	499.8	30	20	
SPF5189Z	166.6	25	34	Qorvo
	499.8	19	35	
	2998.8	5	18	
ZX60-P103LN+	166.6	15	34	Mini-circuit
	499.8	11	22	

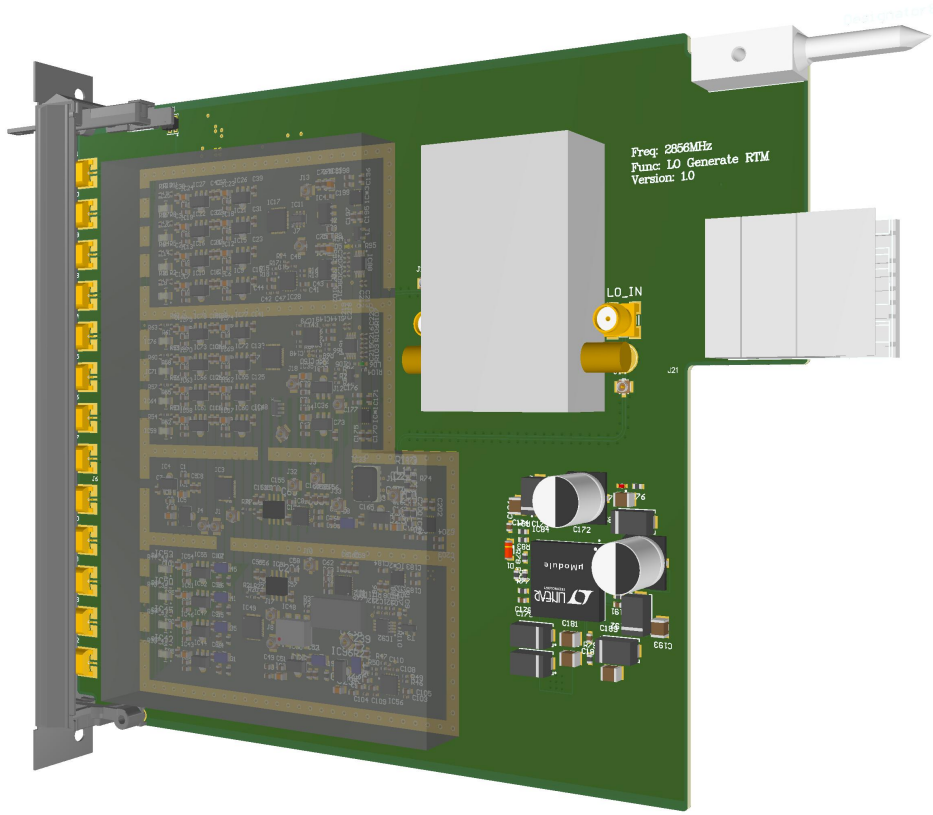
e.g. 499.8MHz jitter 10Hz-10M/1M/100kHz: 21.4/20.2/16.4fs

Status

PCB 3D

- principle design
- key chip Select
- schematic draw
- layout
- matching
- EMI shielding
- power supply tree
- connectors
- MMC





Next steps

- 2025Sep. PCB in production
- then test, debug, basic function verification
- 2025Q4. version 2 design starts, add temperature control, reoptimization
- 2026Q1. upgraded PCB in production
- 2026Q2. board complete, starts to install on test facility

Future plans

- Make more efforts on the firmware and software of new MTCA boards
- Extend to broader band and other frequencies
- Build an open webpage about basic introduction and knowledge

Thank you for your attention!