Development and New Progress of a Universal Signal Processing Platform for Beam Diagnostics and Control

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On behalf of collaboration team

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USTC

IMP

IHEP

SARI

Outline

Motivation

NSRL 中国科学技术大学 国家同步辐射实验室 NATIONAL SYNCHROTRON RADIATION LABORATORY

Intelligent Light sources

➢ **Expected Goals：**

Integrated with big data + AI technologies, to achieve the following operational objectives:

- **Automatic optimization** of accelerator facility parameters**, one-click operation**, early fault warning, and **predictive maintenance**
- Efficient **automatic analysis** of experimental data, **data fusion** of different experimental methods, and data analysis compensation based on changes in accelerator beam parameters

➢ **Current Status**

- AI technologies have begun to be applied in accelerator measurement & control and experimental data analysis, but their **application scope is limited**.
- The accelerator and experimental stations have stored massive amounts of **historical data** based on their respective data collection and storage systems, yet the **utilization efficiency is very low**.
- The facility has a high level of overall informatization, but its **intelligent level remains quite low**, and many new AI technologies have not been fully utilized.

Motivation

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Intelligent Light sources

➢ Main Technical Bottlenecks

- From the perspective of the facility as a whole, there are **various types of data acquisition equipment**, and the data lacks unified standards and formats.
- **Data synchronization** is achieved through the soft time scale of the NTP server. For high-speed data, the synchronization accuracy is **insufficient**, and the consistency of the dataset is compromised.
- Most of the existing historical databases store slow-speed data while discarding transient high-speed data, resulting in a **data pool that is sufficient in breadth but insufficient in depth**.
- AI technology requires high data integrity and consistency. Under the existing framework, a large number of experts and human resources are needed to **clean and label the original data**.

➢ Solutions:

Develop an Integrated Beam Measurement and Control General Signal Processing Platform with Hard Time Scale Function

- All data acquisition for the accelerator and experimental stations shall be completed under this platform.
- A real-time dataset for large-scale facilities shall be formed, which requires no further preprocessing**, can be directly used online by AI**, and ensures data integrity and consistency.

Motivation

Current status of the signal processing platform for BI and control

Over the world:

- The digital beam signal processor, a core device required by all accelerator facilities, adopts a general signal processing platform to meet the needs of multiple facilities, which is currently a common choice among major laboratories.
- uTCA @ DESY (EXFEL/ESS/FLASH), User defined platform @ PSI (SwissFEL/SLS), ATCA @ SLAC (LCLS-II/SPEAR), etc, …

In China:

- Multiple research institutions are engaged in the development of digital beam signal processing platforms, having **developed multiple versions of dedicated electronic equipment that have been put into engineering applications in batches**. However, **multiple small-sized teams are simultaneously conducting nearly identical hardware and software development work**. Due to the lack of unified standards, **hardware and software cannot be shared among different research institutions**, which also hinders technical exchanges.
- Currently, the mainstream signal processors still use the **AD/DA chips that were relatively mainstream 10 years ago**, leaving significant room for upgrading and optimization. It is feasible to develop a next-generation general beam measurement and control processing platform with **bunch-by-bunch diagnosis** and feedback capabilities.
- The measurement and control equipment used in experimental stations is still dominated by commercial products. Nevertheless, existing technologies already support the **integration of some detectors into the system** via self-developed data acquisition modules, while the remaining detectors can be connected through data interfaces such as GIGE.

Outline

Project objectives

Define and develop an open-source standardized hardware/software (open-source within the Chinese Accelerator Alliance):

- Hardware framework design of the general signal processing platform for beam measurement and control (including design principles, overall structure, electrical schematics, PCB layouts, bill of materials, etc.);
- Hardware design of IO modules capable of basic measurement and control functions (including function descriptions, electrical schematics, PCB layouts, bill of materials, etc.);
- Linux operating system driver support software and EPICS support software packages corresponding to the aforementioned core processing modules and IO modules;
- The combination of a signal processing motherboard and different IO function boards can cover over 90% of the applications in large scientific facilities.

Develop and verify prototype devices through beam experiments:

- Prototype of the general beam measurement and control signal processing platform (including a general processor motherboard, IO daughter boards with different functions, and several signal conditioning front-end modules).

Build a shared resource research team:

- A unified domestic R&D team for measurement and control applications (software/hardware) in large scientific facilities (co-owned by multiple institutions and shared across different projects).

Project objectives

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Cultivate high-quality partners in the industry:

- Cultivate a group of domestic high-tech companies (3-5) focusing on the field of accelerator diagnostics and control.

Localization of key core equipment:

- Localization at the device and board levels (core chips such as FPGAs, high-speed ADCs, and high-speed DACs are imported), ensuring all technical indicators meet standards and reach the international advanced level;
- Localization at the chip level, with all components (including core high-end chips) adopting domestic products.

Reduce equipment costs in the construction and operation and maintenance of subsequent facilities:

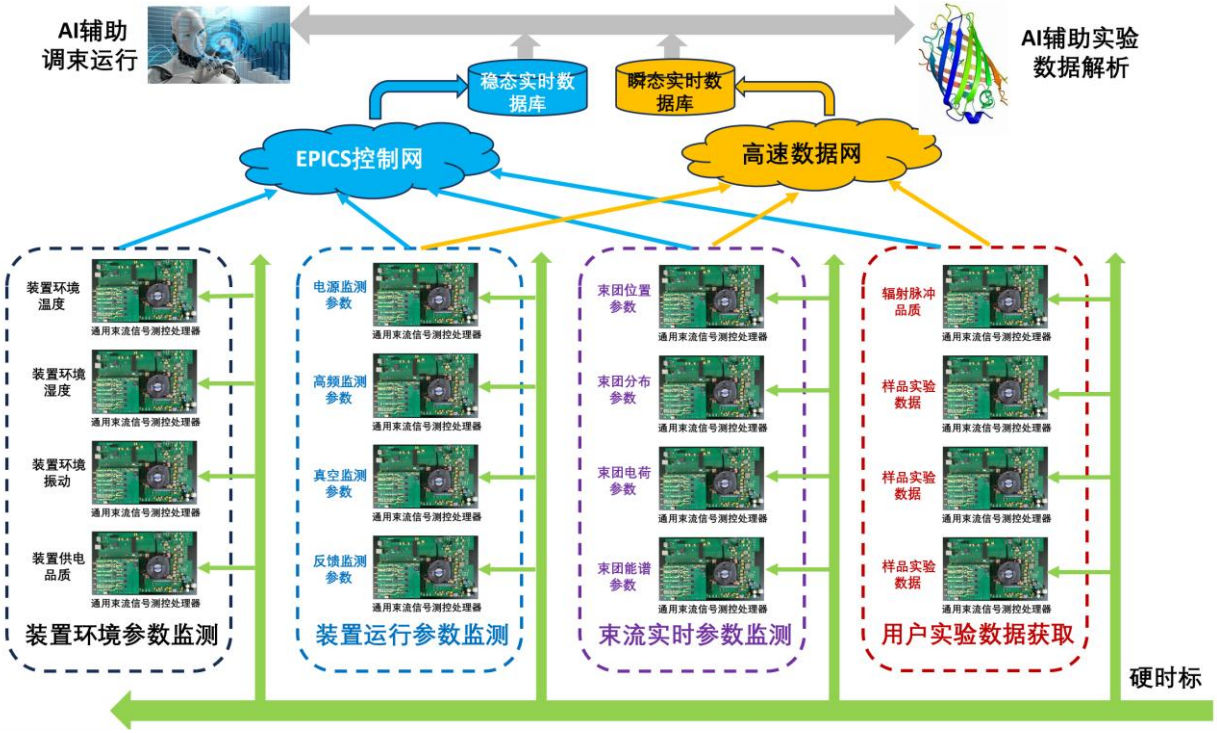
- A conservative estimate shows that the demand for general diagnostics and control platforms will exceed 3,000 sets;
- Under the condition of equivalent technical indicators, the procurement cost (including hardware and software) is reduced by more than one-third.

Outline

Research plan

- Build a standardized DAQ (Data Acquisition) system for light sources based on the integrated general signal processing platform for beam diagnostics and control.
- A real-time dataset of light sources with guaranteed integrity and consistency.
- AI calls data from the standardized real-time data warehouse online to complete tasks of assisting facility operation and auxiliary experimental data analysis.
- The application of the latest AI technologies is supported by data guarantees.

Intelligent Light Source DAQ

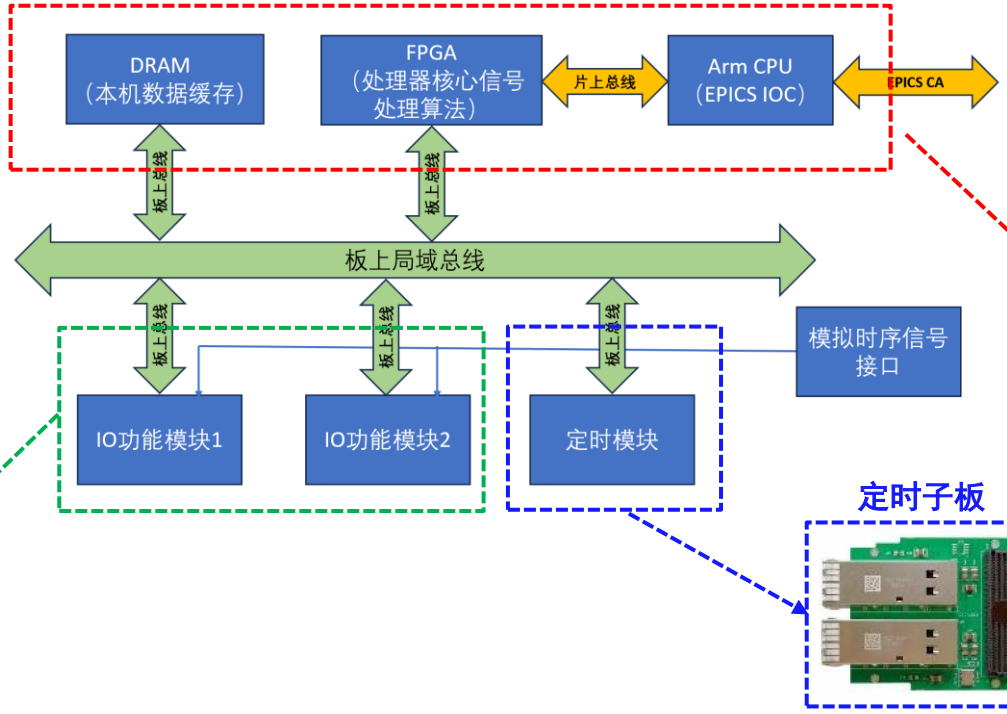


Research plan

Processor Platform Structure:

Digital Signal Processing (DSP) Motherboard + Dedicated Timing Daughterboard + 2* IO Function Daughterboards：

- Digital Signal Processing (DSP) Motherboard: A high-performance FPGA module with a built-in ARM CPU, featuring one FMC (FPGA Mezzanine Card) slot dedicated to timing and two universal FMC slots for IO.
- Timing Slot: Supports WR (White Rabbit) or EV (Event) timing systems respectively, providing real-time hard time stamping and radio frequency (RF) reference signals.
- Universal IO Slots: Combinations of different IO daughterboards enable coverage of over 90% of applications.



数字信号处理母板

IO功能子板

定时子板

Research plan

IO Modules design: by combining any two of the following 12 different types of IO modules, the measurement and control application requirements of over 90% of the facilities can be covered.

SN	IO module name	functionality	applications
IOM01	RF signal direct sampling module	Direct acquisition of RF signal baseband, under-sampling of band pass C-Band signals	BYB diagnostics in the ring, beam loss monitor, CBPM, MBFB, LLRF, etc.
IOM02	IF signal sampling module	Direct baseband acquisition of intermediate frequency (IF) signals, Under-sampling of bandpass 500MHz Signals	TBT diagnostics in the ring, beam loss monitor, CBPM, MBFB, LLRF, etc.
IOM03	High resolution ADC	High resolution voltage and current signal	DCCT, XBPM, etc.
IOM04	Multi channels ADC	Multi channels slow voltage and current	Array detector, multiwire profile
IOM05	RF direct sampling DAC	Arbitrary waveform generator	MBFB, LLRF, AWG, etc.
IOM06	IF DAC	Arbitrary waveform generator	MBFB, LLRF, AWG, etc.
IOM07	Multi-channel DIO	Monitoring and control of switch state, digital pulse counting, etc.	MPS, device control
IOM08	Industrial camera Interface	General-purpose image data acquisition	Profile for beam or laser
IOM09	Area detector Interface	End station user detector data acquisition	Customized detector data access, TS
IOM10	GIGE data exchange	Multi-processor data aggregation	FOFB
IOM11	WR timing module	Receiving WR timing signals	Add time stamp for local processor
IOM12	Event timing module	Receiving Event timing signals	Add time stamp for local processor

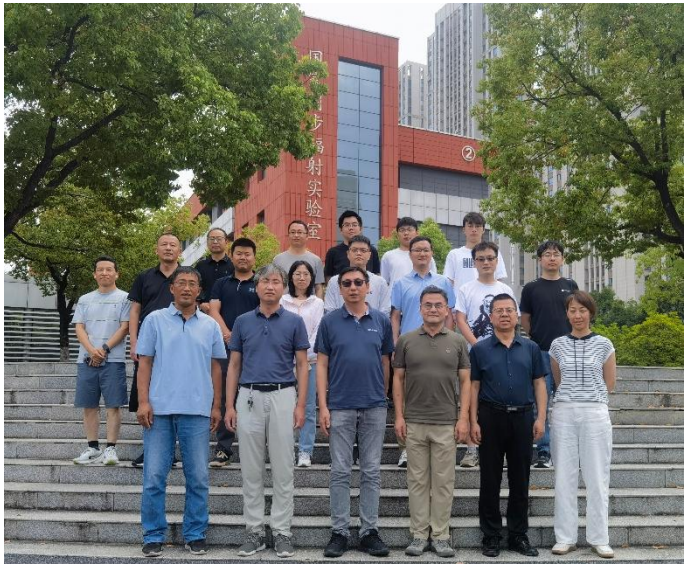
Research plan

Typical application demo: the eight most typical applications in accelerator control, beam measurement, and feedback can be realized through the combination of two IO modules.

SN	Applications	Functionality	IO module combination
APP01	DBPM for electron ring	turn-by-turn and closed orbit measurement of the beam's transverse position	**IF ADC** BPM Signal Processing Algorithm for Electron Rings
APP02	DBPM for hadron ring	turn-by-turn and closed orbit measurement of the beam's transverse position	**IF ADC** **BPM Signal Processing Algorithm for Hadron Rings**
APP03	BYB DBPM for electron ring	Bunch-by-Bunch 3D position measurement	**RF ADC + RF ADC** BYB 3D position Algorithm for Electron Rings
APP04	BYB charge and current	Bunch-by-Bunch charge and lifetime measurement	**RF ADC + High resolution ADC** BYB charge and lifetime Algorithm for Electron Rings
APP05	MBFB for electron ring	Beam Instability Suppression	**RF ADC + RF DAC** **Digital filtering and phase shift**
APP06	Beam profile monitor	Image acquisition and processing of screen monitor or other optical signals	**Industrial camera Interface** **Image acquisition and Gaussian fitting**
APP07	Fast MPS controller	Summarization of fast interlock signals	**Multi channel DIO + Multi channel ADC** **Interlock logic**
APP08	Timing Master and Slave	Generate and distribute timing signals required by the entire facility	**WR timing or Event timing** **Timing signal encoding and decoding**

Outline

Research team



总体架构设计团队

姓名	单位	科研/工程岗位	技术专长
冷用斌	中国科技大学，教授	NSRL副主任（分管信息部）/HALF测控分管副总工程师	储存环及FEL诊断技术，诊断新方法
赵雷	中国科技大学，教授	快电子学实验室负责人	高速数据采集处理技术
武军霞	近代物理研究所，研究员	束测负责人	束流诊断及反馈技术
岳军会	高能物理研究所，研究员	HEPS束控部副主任	束流诊断及逐束团反馈技术
阎映炳	上海高研院，研究员	束测控制部负责人/SHINE通用技术分总体负责人	加速器控制及定时技术

算法及软件开发团队

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杨永良	近代物理研究所，副研究员	HIAF 同步环束测负责人	加速器控制技术，EPICS资深工程师
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李志学	近代物理研究所，工程师	束测、机器保护电子学研发负责人	电子学硬件设计
魏书军	高能物理研究所，研究员	HEPS快轨道反馈系统负责人	束流信号处理技术
杜垚垚	高能物理研究所，高级工程师	数字BPM电子学负责人	电路开发，信号处理算法研究
刘智	高能物理研究所，工程师	逐束团流强测量、束损电子学负责人	定时及控制技术，EPICS工程师
赖龙伟	上海高研院，研究员	束测组副负责人/SHINE束测电子学负责人	束流诊断及反馈技术
周逸媚	上海高研院，助理研究员	逐束团3D位置电子学/SHINE BPM电子学软件负责人	束流信号处理技术，EPICS工程师
陈广花	上海高研院，副研究员	控制组副负责人/SHINE总控集成系统负责人	设备控制及定时技术，EPICS工程师

USTC + IMP + IHEP + SARI

Total 16 staffs, more than 10 post-docs and students

Research schedule

The development cycle is from June 2024 to June 2027, totaling 36 months.

December 2024 — December 2025 (Structural Design and Process Scheme Review)

Complete the structural design of the open-source software and hardware framework, define the technical specifications of the processor motherboard and all functional sub-boards. On this basis, confirm the equipment processing unit through inquiry, and complete the design and review of all circuit boards.

January 2025 — December 2026 (Hardware Processing and Software Development)

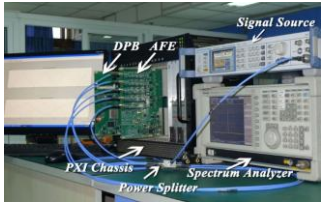
Complete the processing and laboratory debugging of the processor motherboard and all functional sub-boards, develop and test the corresponding Linux driver programs, develop and test the EPICS support software package, and discuss and confirm the beam experiment plan.

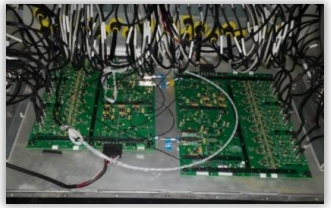
January 2026 — December 2027 (Application Verification and Acceptance Summary)

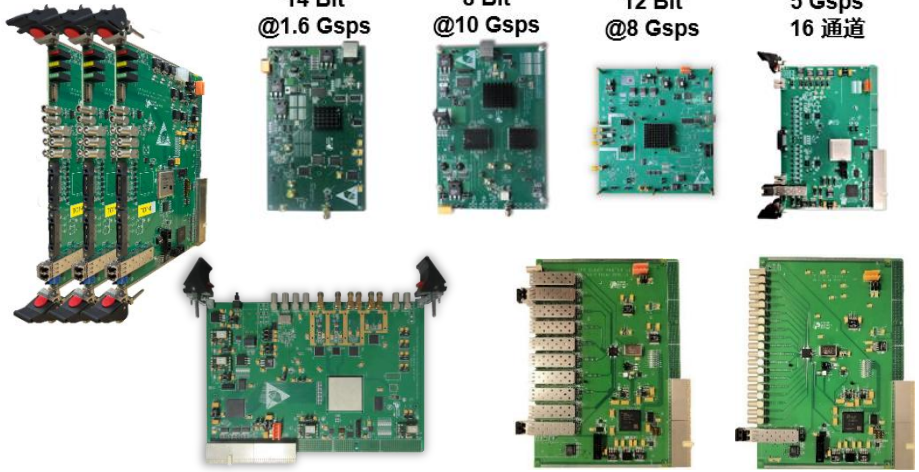
Complete the laboratory performance test of all prototype equipment, build the accelerator measurement and control application platform as planned, complete the beam experiment test of the application platform, compile the test report and summary report, and organize the work test and acceptance.

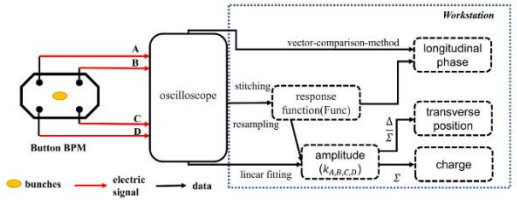
Research foundation: USTC

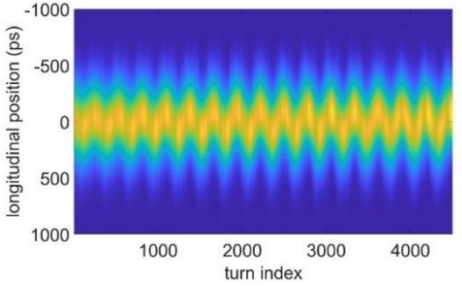
- Relying on the HALF (Hefei Advanced Light Source) pre-research project, we have developed and completed the DBPM electronics prototype.
- Based on the Hefei Synchrotron Radiation Facility (HLS) and the Shanghai Synchrotron Radiation Facility (SSRF), we have conducted systematic research on multi-parameter bunch-by-bunch diagnostic technology and developed a variety of bunch-by-bunch information extraction algorithms.





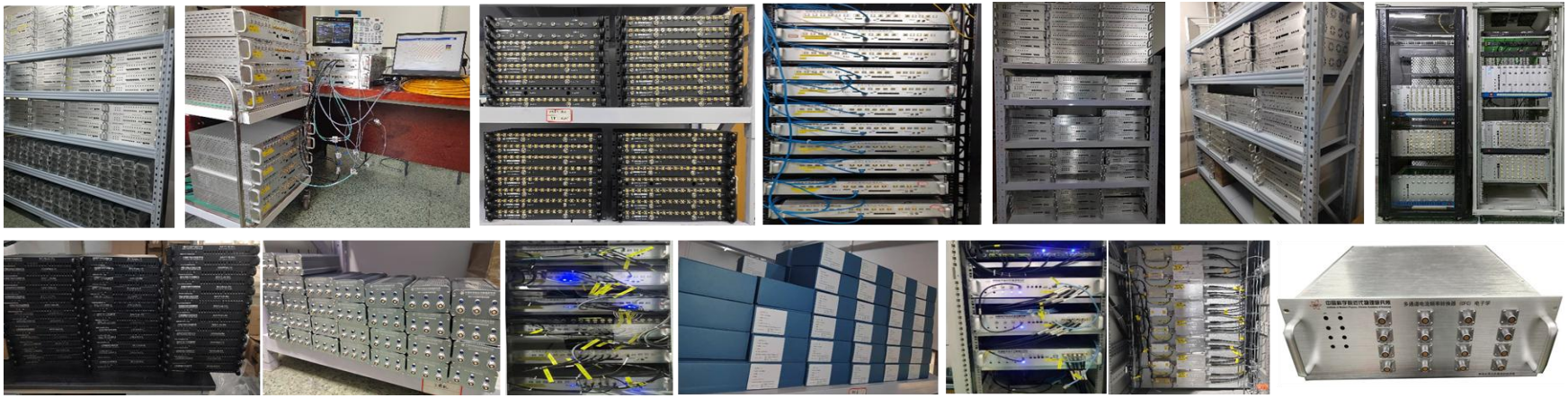






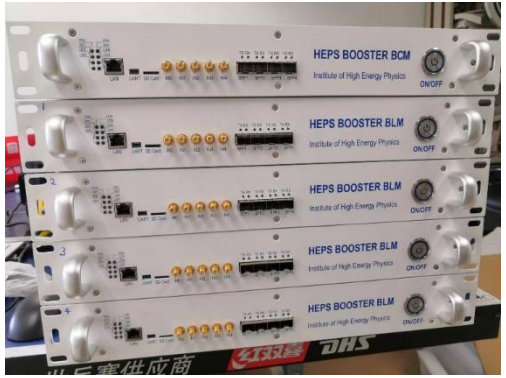
Research foundation: IMP

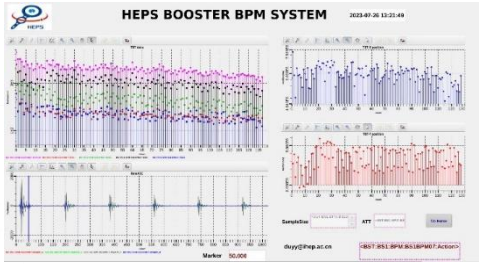
- To meet the needs of engineering construction such as HIAF and the upgrade of HIRFL facility, we will build a high-end customized electronic hardware and software R&D platform, break through the core technologies of heavy ion beam measurement electronics, realize domestic substitution, get rid of dependence on imports, and independently develop the entire line of beam measurement electronics for HIRFL and PREF.



Research foundation: IHEP

- In response to the requirements of HEPS, the Institute of High Energy Physics has, after years of research and development and multiple version iterations, successfully developed single-pass BPM electronics and storage ring BPM electronics. Their measured indicators are comparable to foreign commercial products, realizing domestic substitution. Over a hundred sets have been deployed in BEPCII and HEPS, and they have also been adopted by relevant institutions such as the Ninth Academy and the China Institute of Atomic Energy.
- Bunch-by-bunch measurement electronics have been developed and applied to position measurement, current measurement, beam loss measurement, and feedback systems, among others.





Research foundation: SARI

- To address the needs of engineering construction projects such as SXFEL, DCLS, and SHINE, as well as the upgrade and renovation of SSRF, a full range of domestic hardware platforms for beam measurement and timing has been built.
- Rich experience has been accumulated in the design, development, debugging, and operation of hardware, algorithms, and software for beam signal processors used in linear accelerators and circular accelerators.
- The timing system for the SXFEL beamline stations has operated stably for three years; the self-developed domestic timing hardware for SHINE has achieved synchronous phase locking with the accelerator clock for the first time.

第一代
电子学平台

采样率125MHz，带宽650MHz

第二代
电子学平台

采样率125MHz，带宽650MHz

采样率1GHz，带宽2GHz

采样率2.6GHz，带宽9GHz

Outline

Hardware progress: DSP motherboard

- Zynq UltraScale+ MPSoC: EG

	ZU1EG	ZU2EG	ZU3EG	ZU3TEG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32 KB/32 KB L1 Cache, 1 MB L2 Cache												
Real-Time Processing Unit	Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32 KB/32 KB L1 Cache, and TCM												
Embedded and External Memory	256 KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC												
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters												
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII												
Graphic Processing Unit	Arm Mali-400 MP2; 64 KB L2 Cache												
System Logic Cells	81,900	103,320	154,350	157,500	192,150	256,200	469,446	504,000	599,550	653,100	746,550	926,194	1,143,450
CLB Flip-Flops	74,880	94,464	141,120	144,000	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	37,440	47,232	70,560	72,000	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
Block RAM Blocks	108	150	216	144	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	0	48	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	0	14.0	13.5	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	3	1	4	4	4	8	4	8	4	11	11
Max. HP I/O(1)	156	156	156	52	156	156	208	416	208	416	208	572	572
Max. HD I/O(2)	24	96	96	72	96	96	120	48	120	96	120	96	96
System Monitor	1	2	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver(3)	0	0	0	8	16	16	24	24	24	32	24	44	44
GTY Transceivers	–	–	–	–	–	–	–	–	–	16	–	28	28

Hardware progress: DSP motherboard

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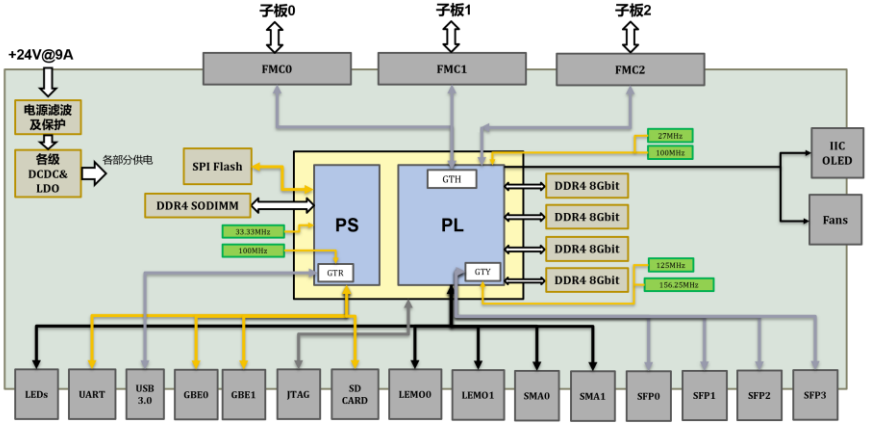
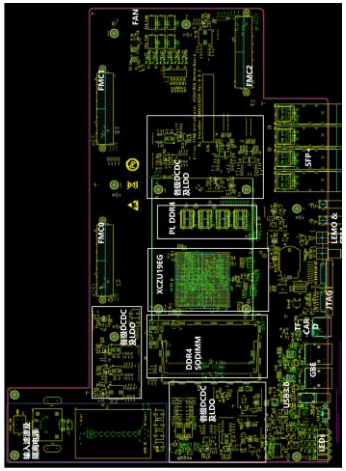
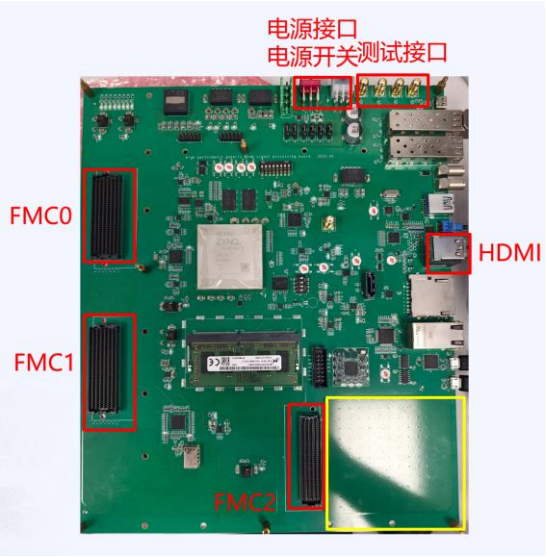
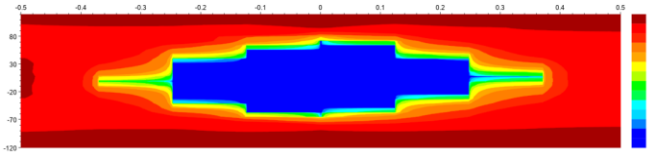


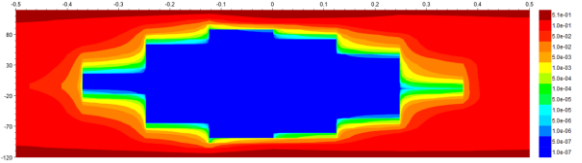




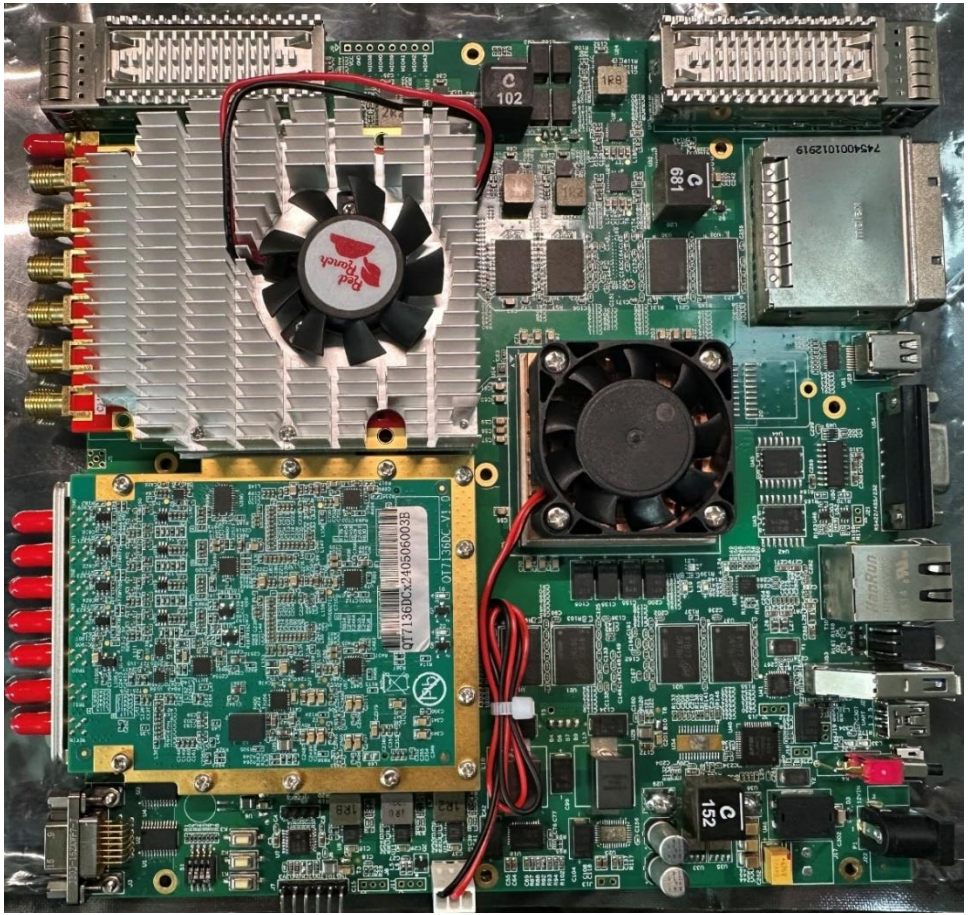
FMC interface test: 12.5Gbps



SFP interface test: 10Gbps



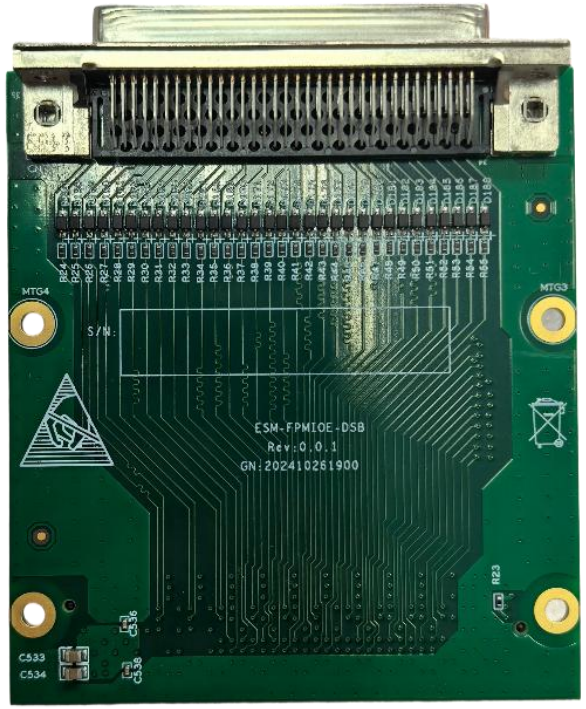
Hardware progress: DSP motherboard



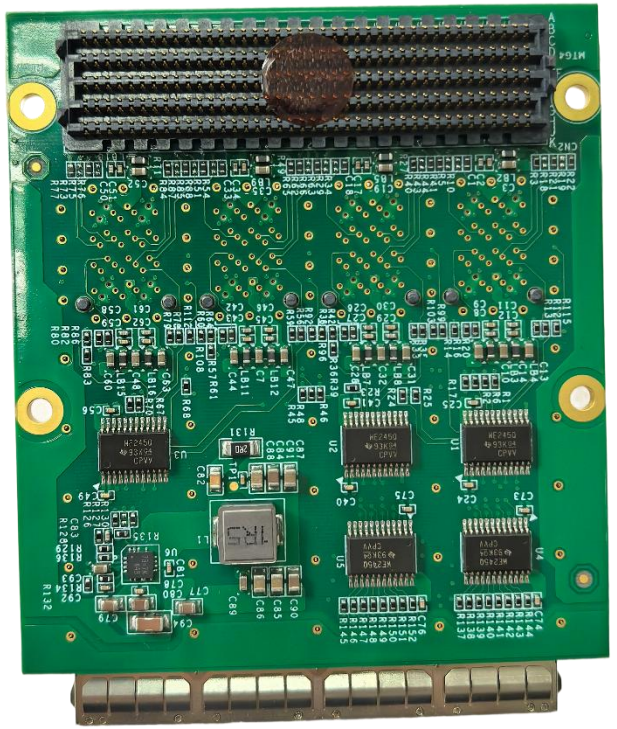
Commercial evaluation board

Used to do FMC IO cards test and software development

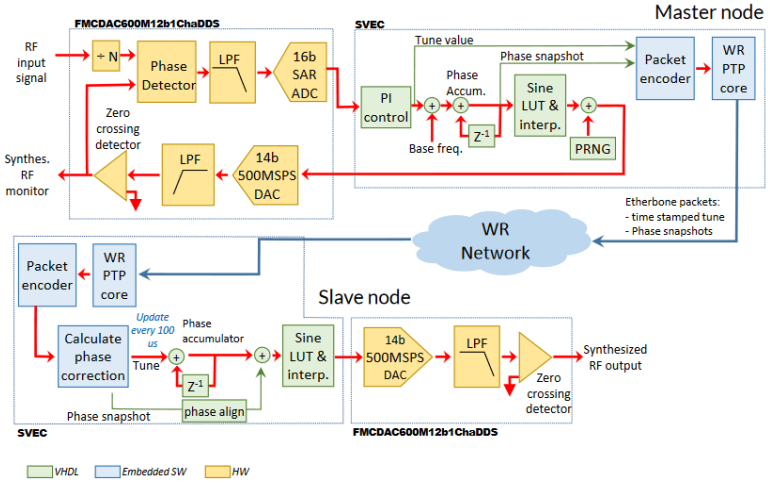
Hardware progress: IO module (DIO)

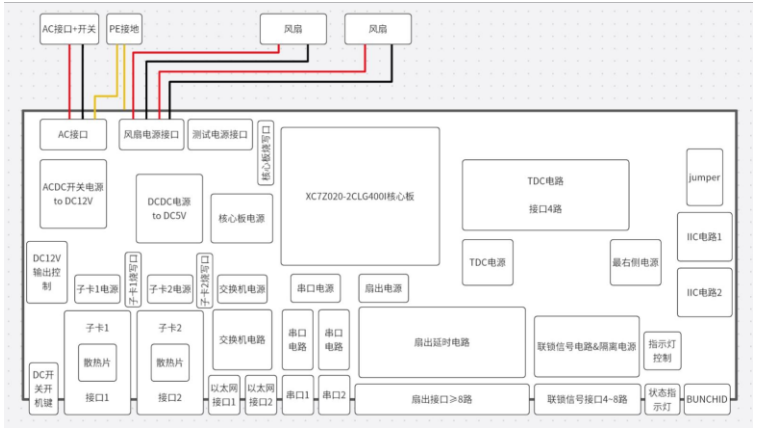


Hardware progress: IO module (GIGE)



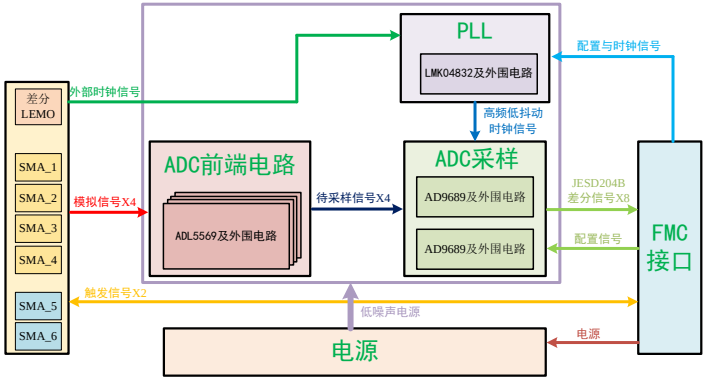
Hardware progress: IO module (WR)

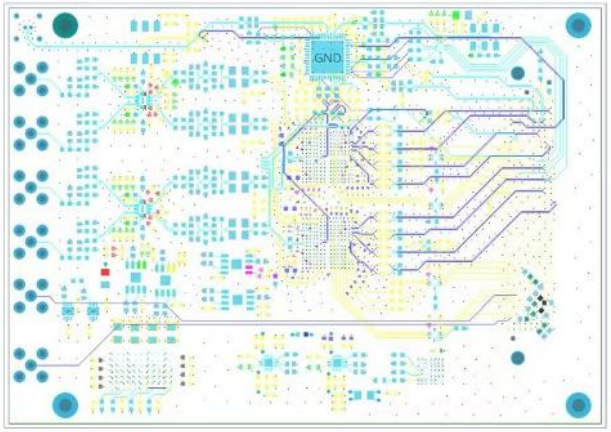


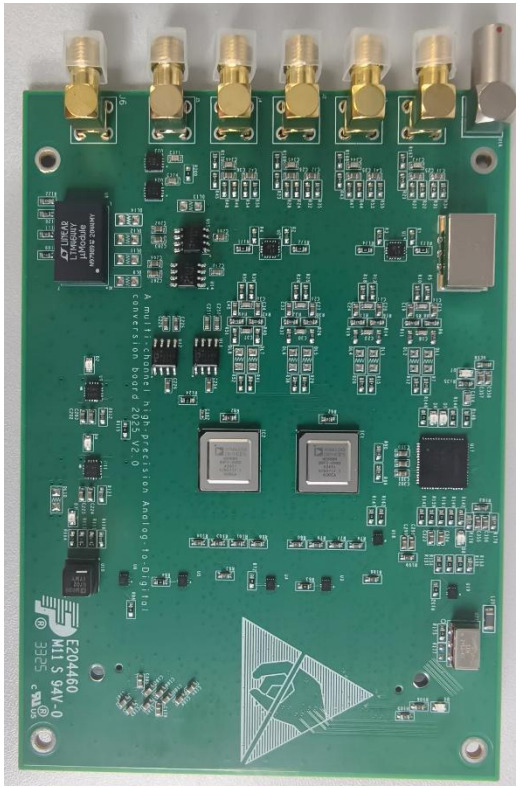


Hardware progress: IO module (RF ADC)

Sampling rate up to 2 GHz, 14 bits

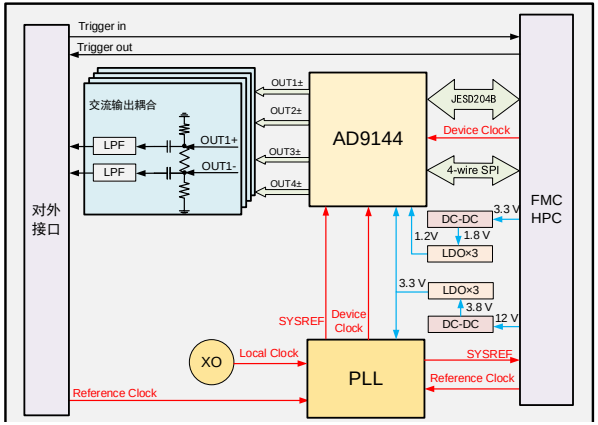


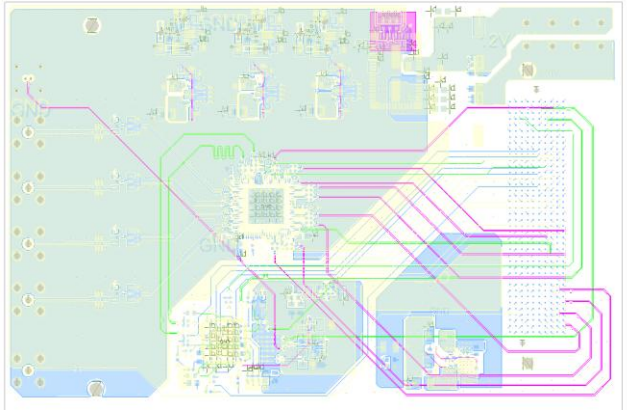


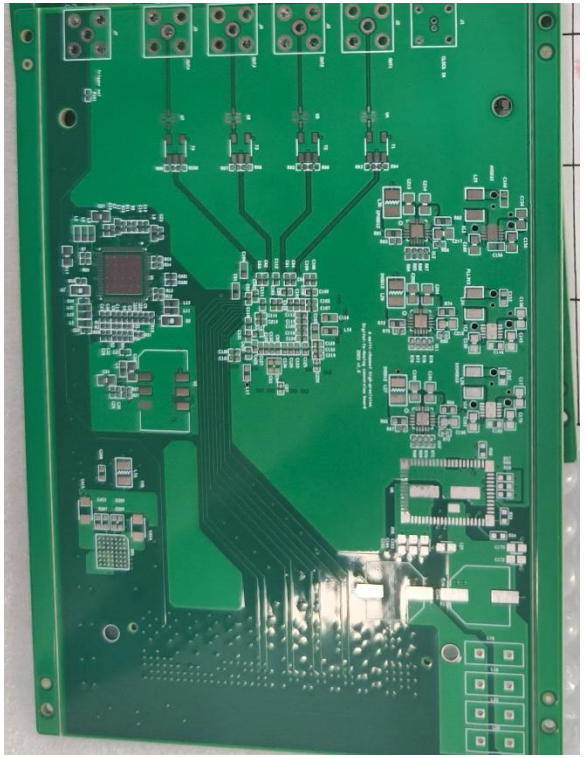


Hardware progress: IO module (RF DAC)

Digitizing rate up to 2.8 GHz, 16 bits

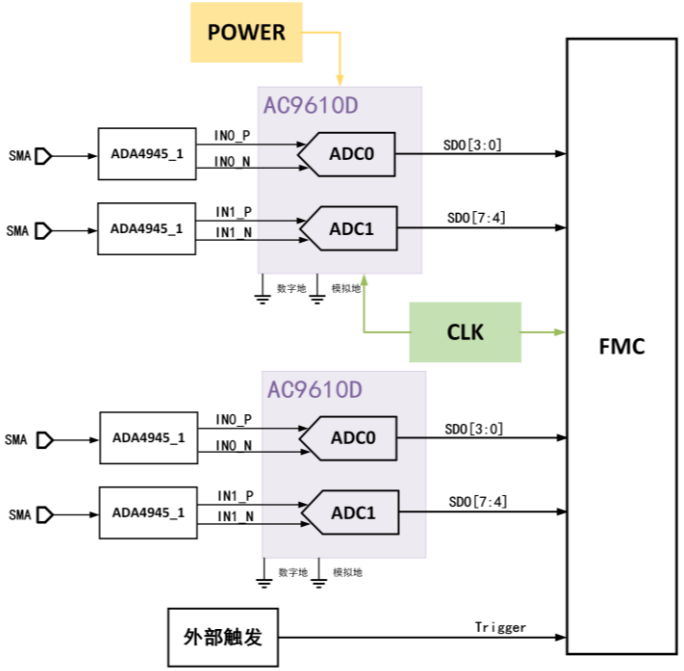


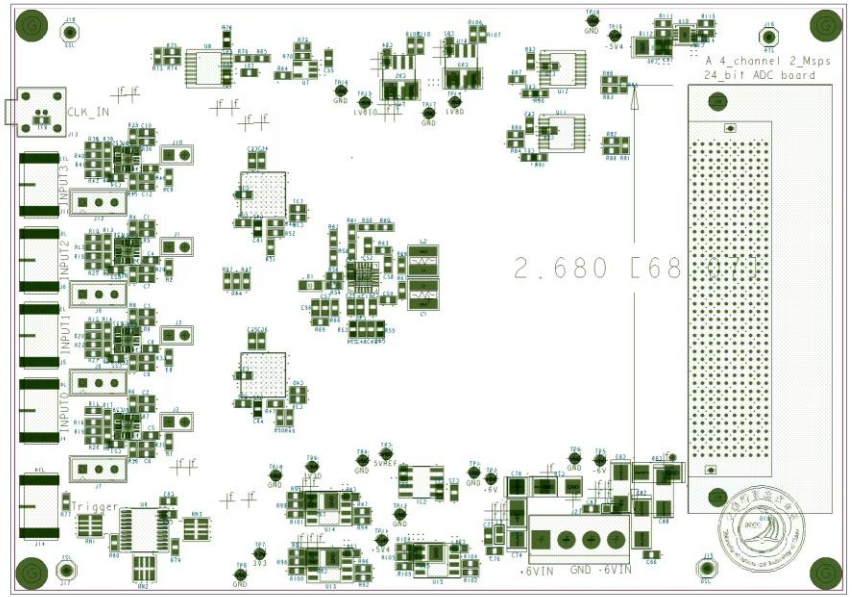




Hardware progress: IO module (HR ADC)

Sampling rate up to 2 MHz, 24 bits

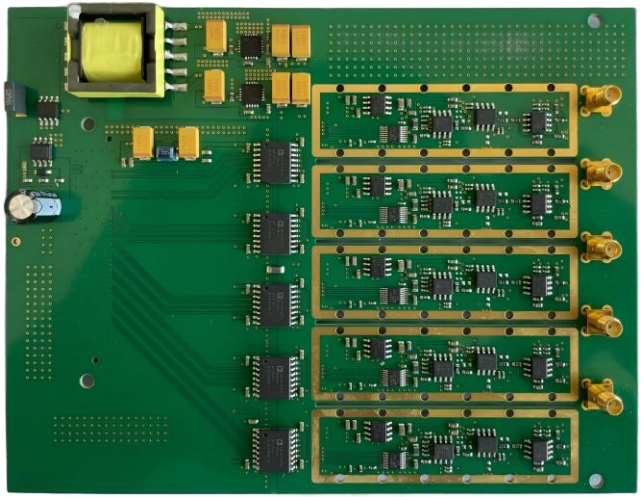


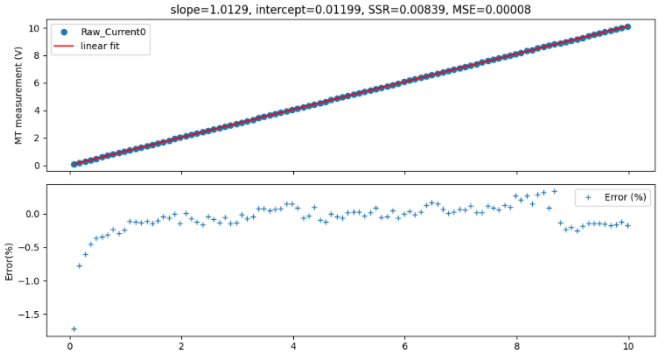


Hardware progress: IO module (HR ADC)

高精度模拟信号采样模块设计参数

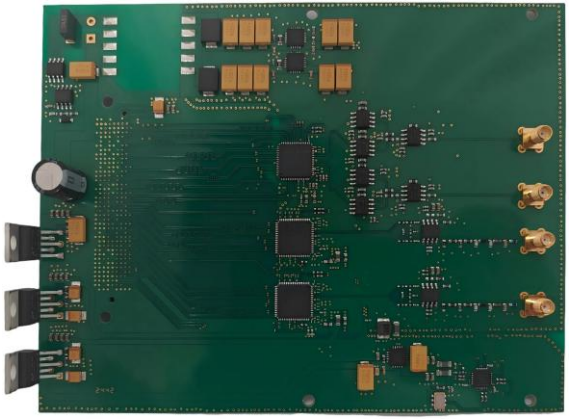
参数	设计指标
通道数	5/10
输入电压范围	±10 V
最大采样率	1 Msps/CH
数据分辨位数	24 bits
全范围线性误差	±1.5%（100 mV~10 V）
系统带宽	2 kHz / 10 kHz / 20 kHz
本底噪声	≤±100 uV @ BW=2 kHz
分辨率精度	10 ppm @ 2 kHz
长期稳定性（开路）	≤±50 μV/℃
长期稳定性（输入5 V）	＜±1% @168 h
通道间隔离度@1 kHz	≥90 dB





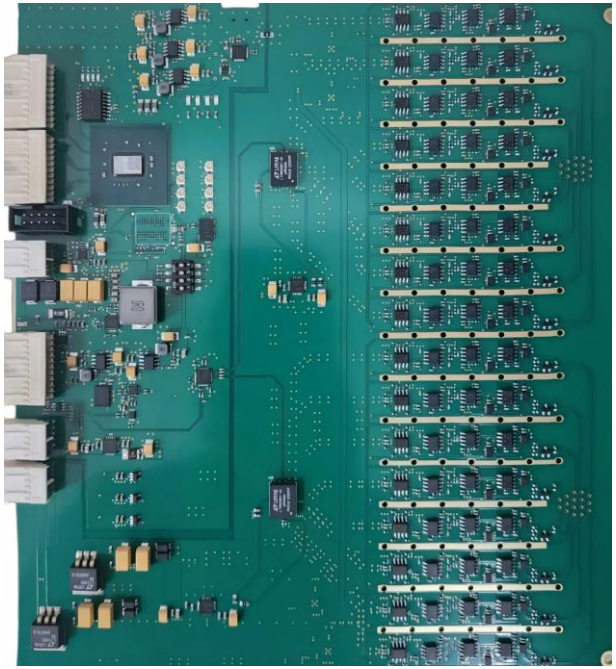
Hardware progress: IO module (IF DAC)

参数c	设计指标
中速AD通道	2
中速DA通道	2/4
ADC输入信号范围	13 dBm_{max}
ADC采样率	250 Msps
ADC分辨位数	16 bits
DAC输出范围	＞ 10 dBm
DAC采样率	250 Msps/125 Msps
DAC分辨位数	16 bits
电子学输出带宽	100 kHz-10 MHz
ADC输入本底噪声	＜-50 dBm
DAC输出信噪比	＞60 dB
通道间隔离度	≥90 dB



Hardware progress: IO module (MC ADC)

参数	设计指标
通道数	64/128
输入信号类型	电流、电压
测量电流范围	2 pA ~ 2 μA
线性度误差 （全范围）	≤ ± 10 %
通道间一致性误差	≤ ± 5%
噪声	＜5 pA
长期稳定性	优于5%
通道间隔离度	≥100 dB



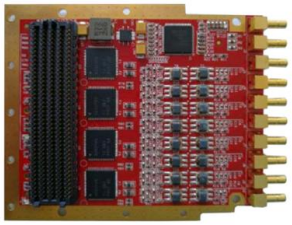
Mature commercial products: Qingyi Tech

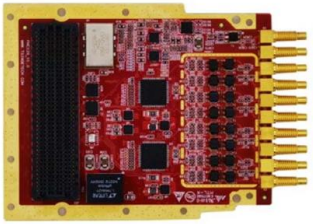

FMC120


FMC121


FMC122

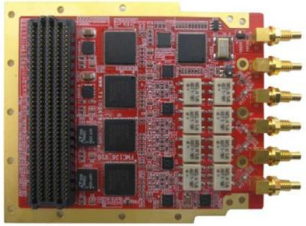

FMC123

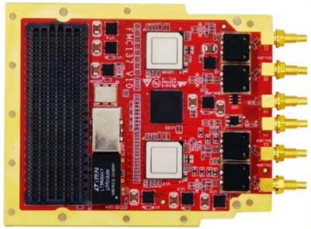

FMC128


FMC129


FMC131


FMC134


FMC136


FMC137


FMC139


FMC140


FMC141

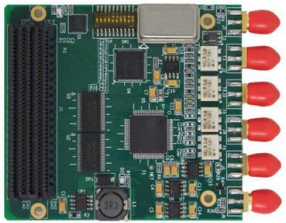

FMC142


FMC147


FMC148


FMC150

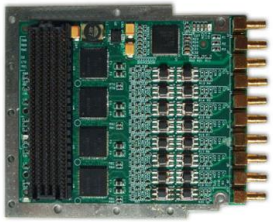
Mature commercial products: Tisu Tech



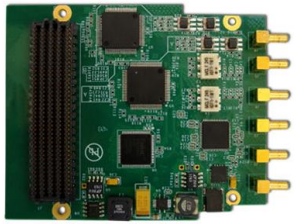
FMC125

FMC145

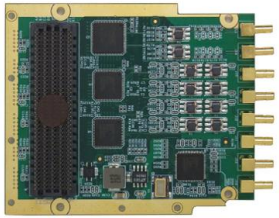
FMC141



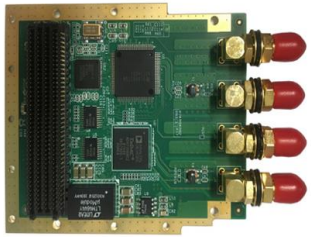
FMC144



FMC160

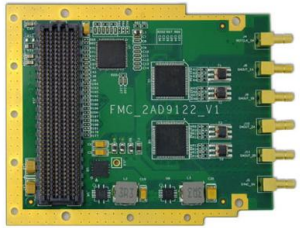


FMC209



FMC210

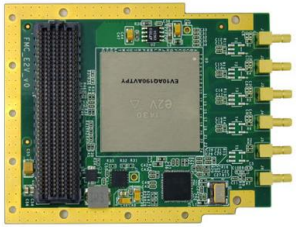
FMC181



FMC228

FMC229

FMC303



FMC147

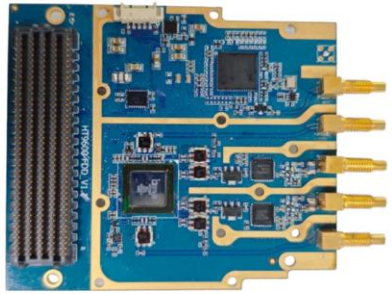
FMC123

FMCJ452

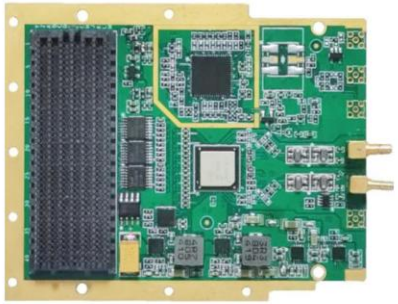
Mature commercial products: Henan Juxun

JX-FMC-ADS54J60&AD9172-ADDA01

JX-FMC-AD9467&AD9122-ADDA01



JX-FMC-ADRV9009-ADDA01



JX-FMC+-AD5200-AD01

JX-FMC-AD9689-AD01

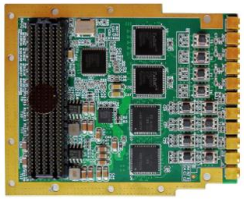
JX-FMC-AD9172-DA02

Mature commercial products: Kunchi Tech


QT7336DC


QT7350DC


QT7331


QT7351


QT7350


QT7332


QT7125+


QT7150


QT7135


QT7136DC

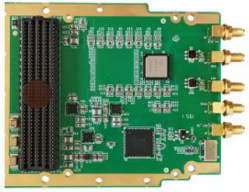

QT7131U


QT7152


QT7131+


QT7126

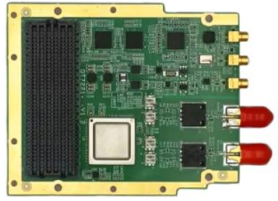

QT7231


QT7228


QT7227


QT7251


QT7225


QT7221+

Mature commercial products: Nanjing Anpu

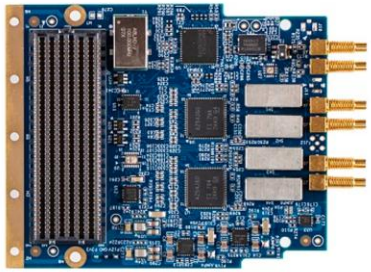
M34880

M34671

M34771

M18800

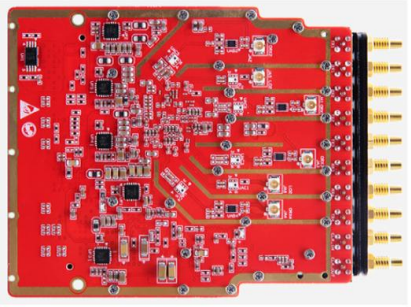
M11550



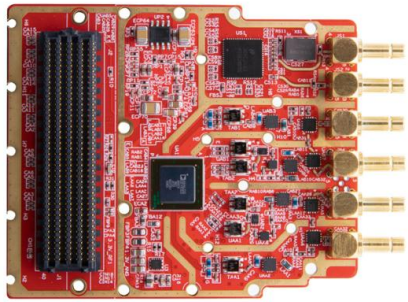
M14811

M22821

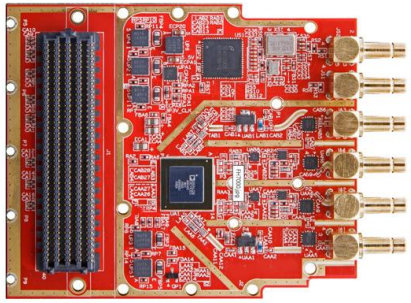
Mature commercial products: Shanghai Xinyi



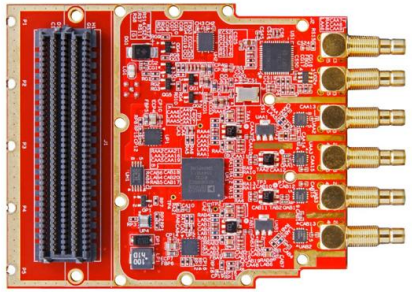
FH9600



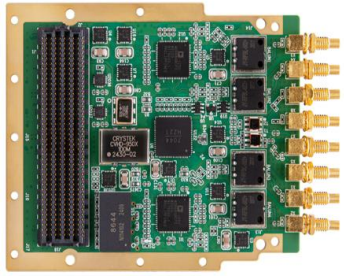
FH9000



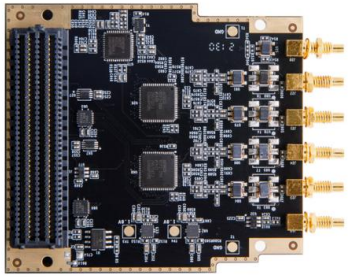
FH7000



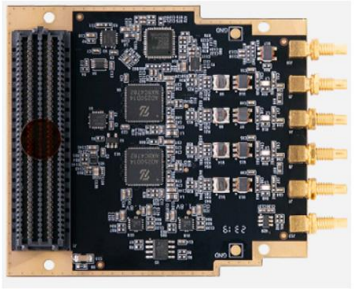
FL6000



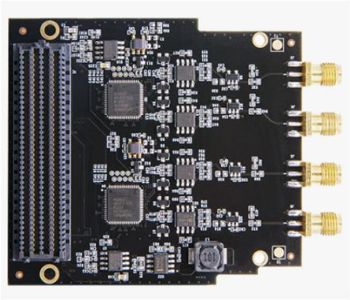
FH9680



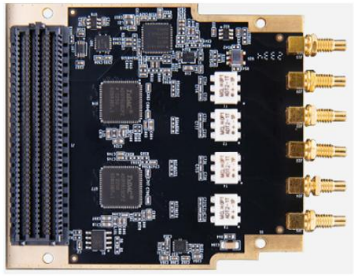
FL9613



FL2514



FL9627



FL9781

Outline

Summary

- To strengthen technical exchange and cooperation among different domestic research institutions, the Chinese Academy of Sciences has launched the Universal Signal Processing Platform Open-Source Project for Beam Diagnostics and Control.

- The joint research team from USTC, IMP, IHEP, and SARI has now completed the overall framework design of the platform and the primary hardware board designs, and has begun fabricating the equipment.

- All software and hardware development, along with beam-involved application demonstrations, will be completed by the end of 2026.

- The research outcomes will be directly applied to the construction of the HALF and SHINE, as well as the upgrades and retrofitting of other facilities.

Thanks for your attention