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Universal Dual-channel FMC Carrier Board based on mTCA.4

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1. Background

- **Requirement:** Currently, the fast interlock protection systems for devices in HEPS and BII, as well as the drivers for motors and piezoelectric ceramics used in tuning, are still housed in traditional chassis. These devices feature numerous interfaces, lengthy wiring, large size and weight, and the dispersed nature of individual devices further reduces system integration.
- **Objective:** To develop a universal digital FMC carrier board based on the mTCA.4 standard, which allows for the selection of different FMC mezzanine cards according to various scenario requirements. This approach will enhance system integration and facilitate functional implementation across different scenarios.
- **Application Scenarios:**
  - Frequency control for motors and piezoelectric ceramics in cavity tuning
  - Hardware platform for multi-channel digital pulse delay generators
  - Fast interlock protection system for devices based on universal interfaces

2.1.1 Component Selection（ZYNQ UltraScale+）

Selection Principles：

1.Prioritize ZYNQ UltraScale+ series chips with a larger number of **configurable I/O ports** to ensure the versatility and applicability of the FMC carrier board.

2.Consider **cost-effectiveness and availability** in the Chinese market.

3.Ensure package **portability** for potential design adjustments.

AMD Zynq™ UltraScale+™ MPSoCs

			ZU1	ZU2	ZU3	ZU3T	ZU4	ZU5	ZU6	ZU7	ZU9	ZU11	ZU15	ZU17	ZU19
Pkg Footprint[2,3]	Dimensions (mm)	Ball Pitch (mm)	PS I/Os[1], 3.3V HD I/O, 1.8V HP I/Os PS-GTR 6 Gb/s, GTH 16.3 Gb/s, GTY 32.75 Gb/s												
A494	9.5x15	0.5	170, 24, 58 4, 0, 0												
A530	9.5x16	0.5		170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A484	19x19	0.8	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A625	21x21	0.8	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0										
C784[4]	23x23	0.8	214, 24, 156, 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 72, 52 4, 4, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
D784[4,5]	23x23	0.8				214, 72, 52 4, 8, 0									
E784[4,5]	23x23	0.8					214, 72, 58 4, 8, 0	214, 72, 58 4, 8, 0							
B900	31x31	1.0					214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0					
C900	31x31	1.0							214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		
B1156	35x35	1.0							214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		
C1156	35x35	1.0								214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0			
B1517	40x40	1.0										214, 72, 416 4, 16, 0		214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
F1517	40x40	1.0								214, 48, 416 4, 24, 0		214, 48, 416 4, 32, 0			
C1760	42.5x42.5	1.0										214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16
D1760	42.5x42.5	1.0												214, 48, 260 4, 44, 28	214, 48, 260 4, 44, 28
E1924	45x45	1.0												214, 96, 572 4, 44, 0	214, 96, 572 4, 44, 0

2.1.2 Component Selection （MMC）

	N.A.T	CERN	DMMC-STAMP	Samway	MMC in this paper
MCU	AVRxmega128	ATmega128	Atmel SAM	Kinetis K10	LPC176X
MicroTCA.0	Y	Y	Y	Y	Y
MicroTCA.4	Y	Y	Y	Y	Y
Schematic reference	Y	Y	N	Y	Y
Layout reference	N	N	N	N	Y
Firmware source	Y	Y	Y	Y	Y
Mezzanine format	N	Y	Y	N	N

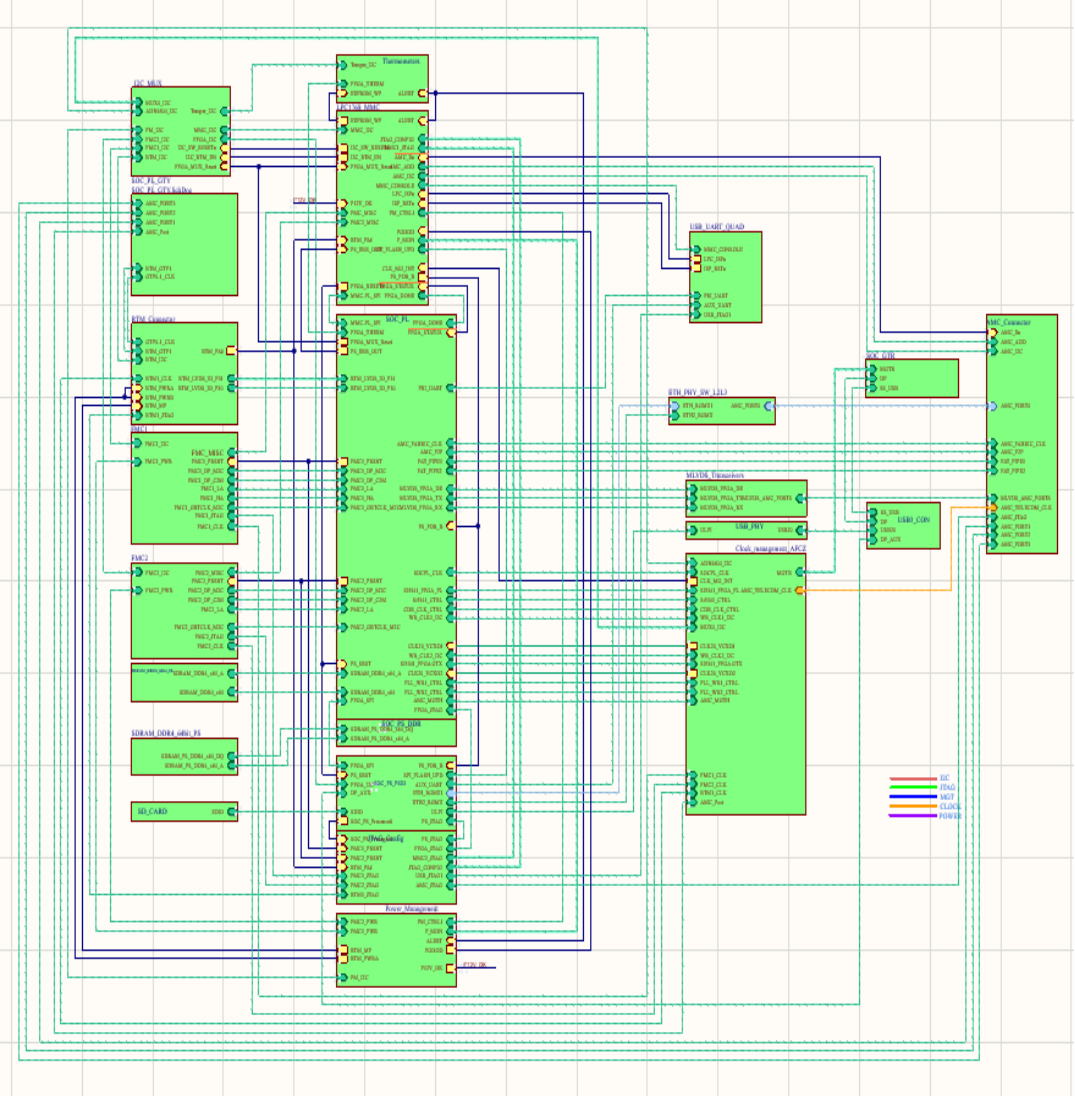
Selection Principles

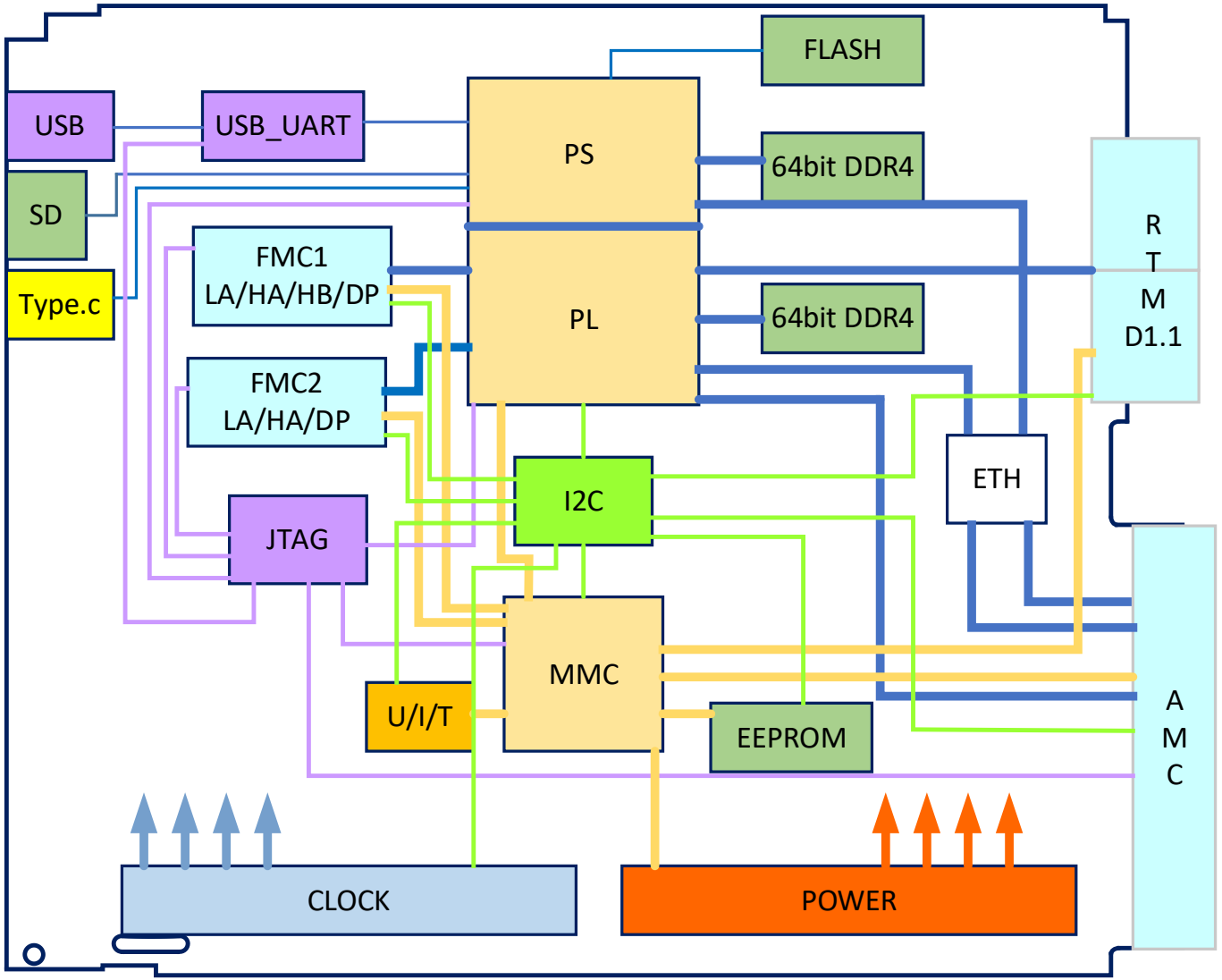
1.Prioritize MMCs with **open-source firmware, and available reference schematics** and layouts to save development time.

2.Consider **cost and market availability** in China.

3.Leverage the laboratory’s previous research and development **experience**.

3.1 Overall Structure



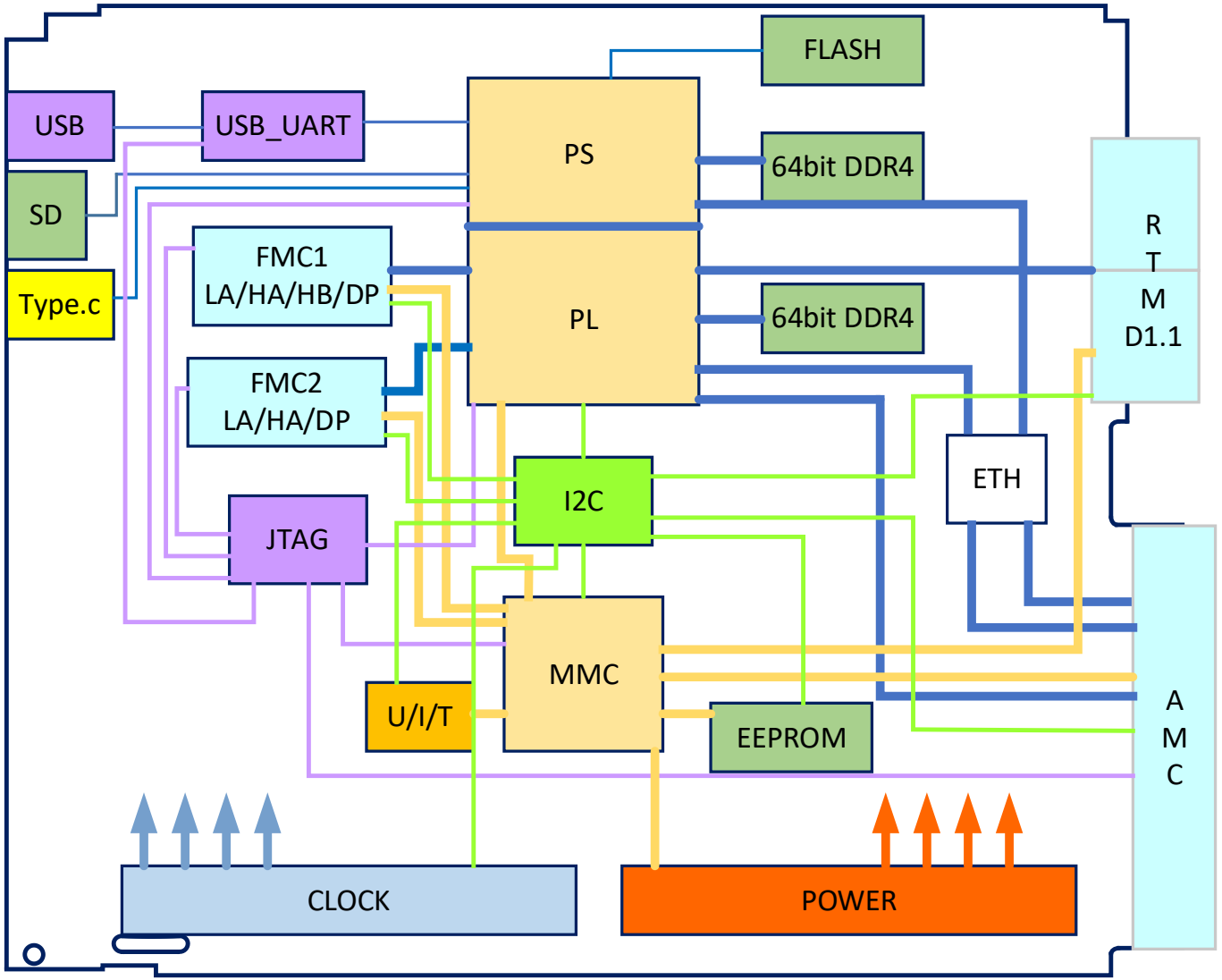


3.1 Overall Structure

- The FMC carrier board consists of the following core components:

- **ZYNQ UltraScale+ MPSoC** (main processing unit)
- MMC (module management and monitoring)
- I2C (inter-integrated circuit communication bus)
- JTAG (debugging interface)
- Clock management module
- Power supply module
- Dual FMC interfaces (FMC1, FMC2)
- RTM (Rear Transition Module) interface
- AMC (Advanced Mezzanine Card) interface
- Ethernet port (Gigabit Ethernet)
- USB-UART (serial communication interface)
- DDR4 memory (for data storage and processing)

etc.



3.1 Overall Structure

Key technical parameters:

•Main chip: Xilinx Zynq Ultrascale+ MPSoC (Model: **XCZU19EG-2FFVC1760**)

•FMC interfaces:

- FMC1: All LA HA , HB and DP pins connected (68,48,44;10)
- FMC2: LA, HA, and DP pins connected(68,48;10)

•PCIe support: PCIe Gen.3 x4 (expandable to Gen.3x8 if conditions permit)

•Gigabit Ethernet ports:

- Port 0: Connected to the Processing System (PS) of ZYNQ
- Port 1: Connected to the Programmable Logic (PL) of ZYNQ

•DDR4 memory:

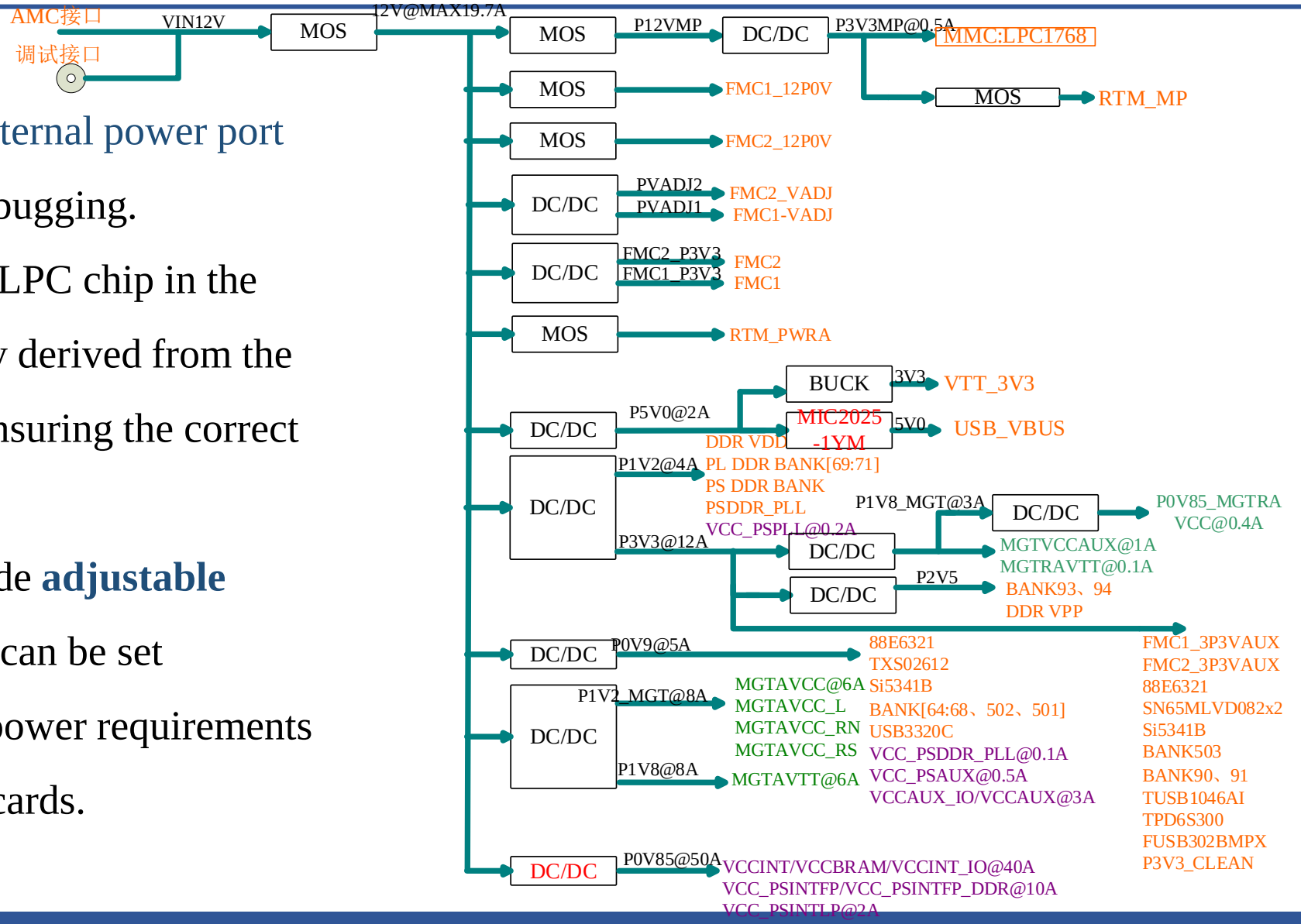
- 4 GB DDR4 (2400 MT/s) connected to PS
- 4 GB DDR4 (2400 MT/s) connected to PL

•RTM connectivity: Compliant with DESY RTM Class D1.1 (42 LVDS I/O signals, 2 high-speed links)

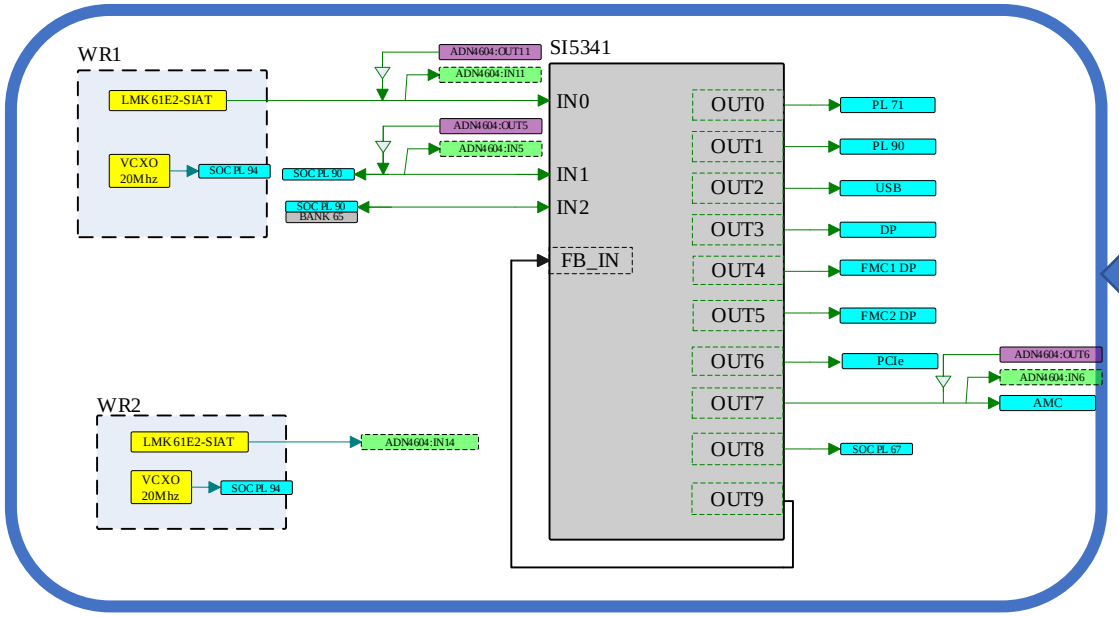
•Additional interfaces: SD-Card slot, White Rabbit (high-precision time synchronization) support

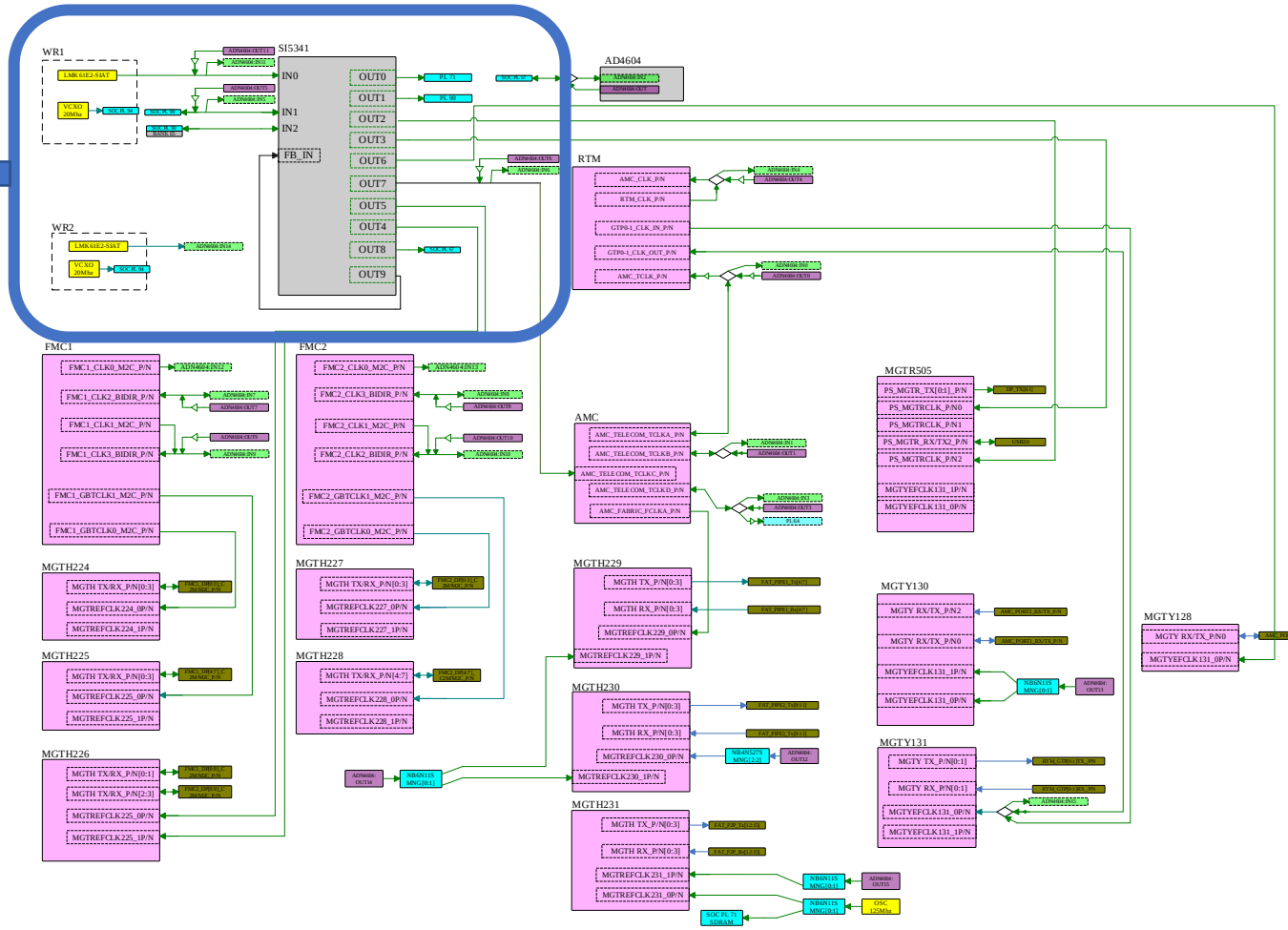
3.3 Power Supply Module

- Equipped with a 12V external power port to enable **off-chassis** debugging.
- The 3.3V power for the LPC chip in the MMC module is directly derived from the P12V_MP power rail, ensuring the correct power-on sequence.
- FMC1 and FMC2 provide **adjustable voltage outputs**, which can be set according to the actual power requirements of the FMC mezzanine cards.



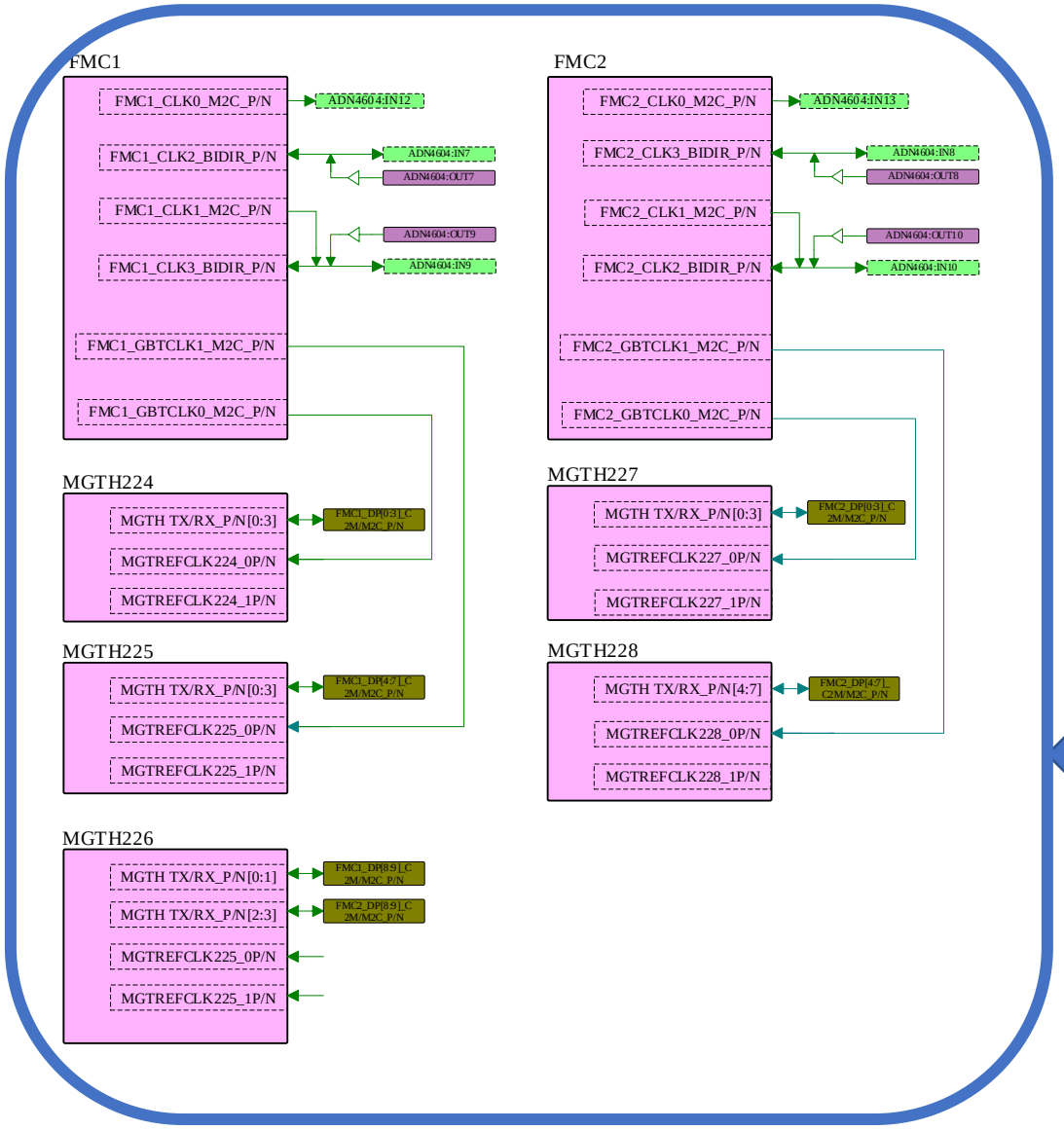
3.4.1 Clock Management Module



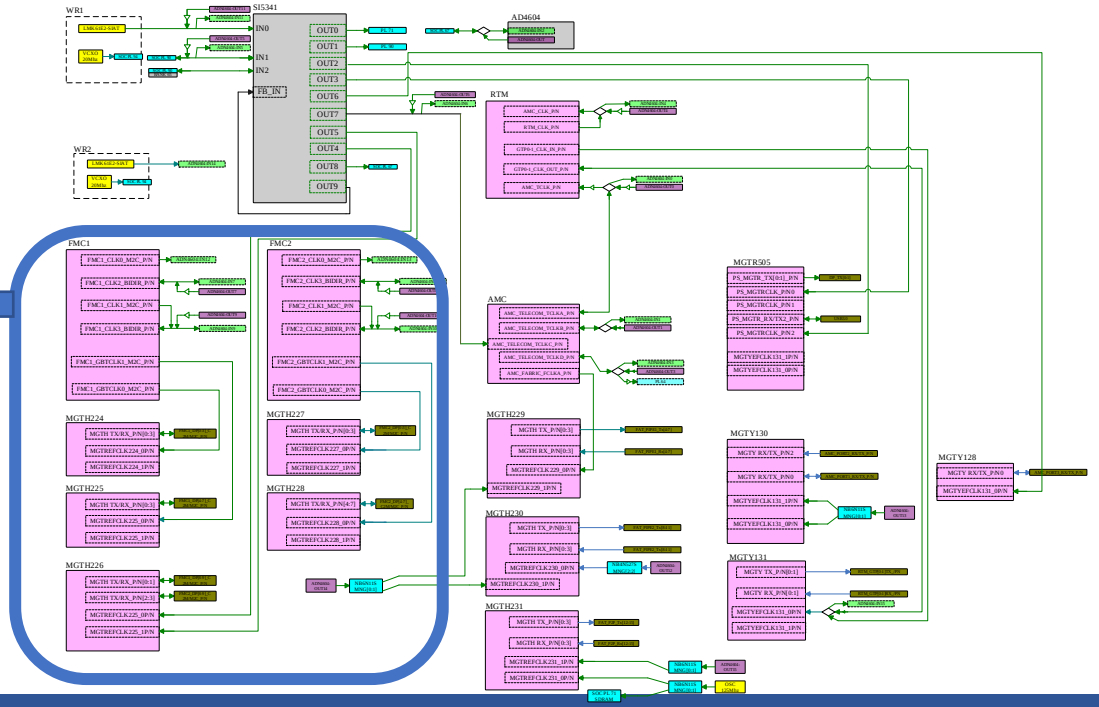


- **Clock sources:** Internal voltage-controlled crystal oscillator (VCXO) or external clock input.
- **Clock generation:** **Si5341** clock generator is used to output clocks with different frequency multiplication and division ratios.
- **Clock distribution:** The **ADN4604** clock buffer distributes clocks to the banks where each transceiver is located, covering

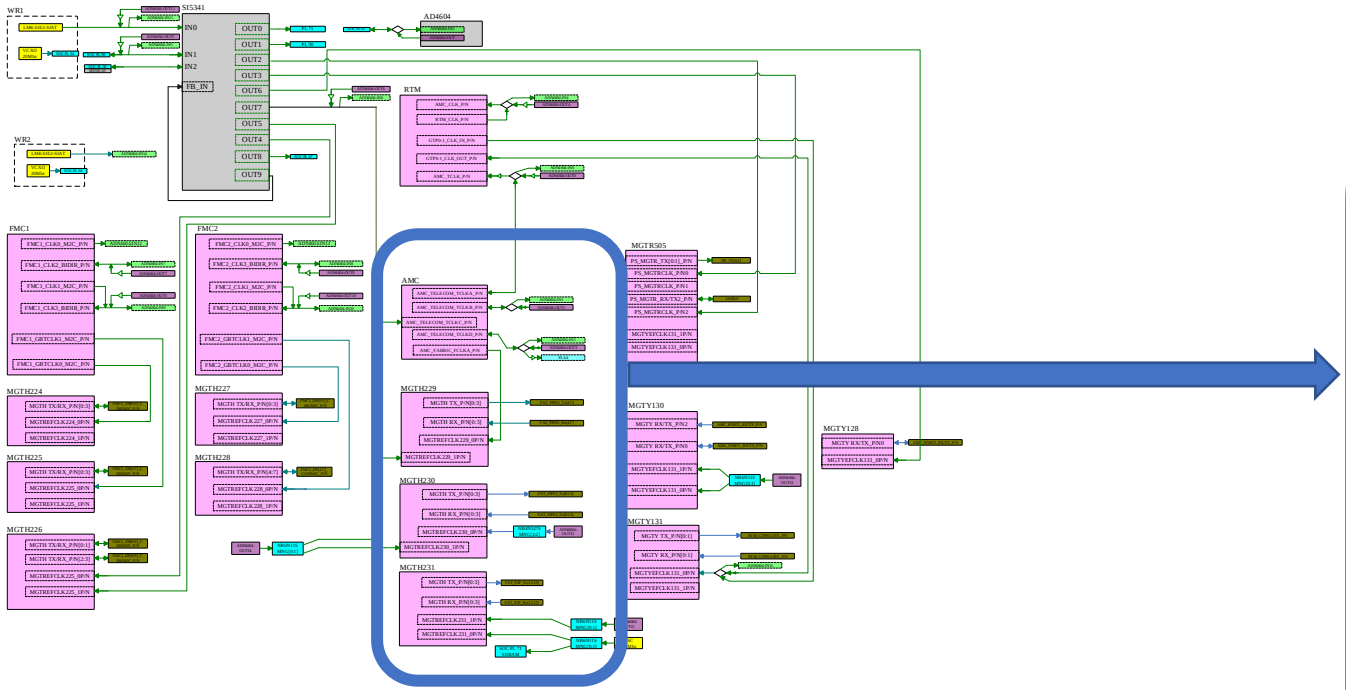
3.4.2 Clock Management Module

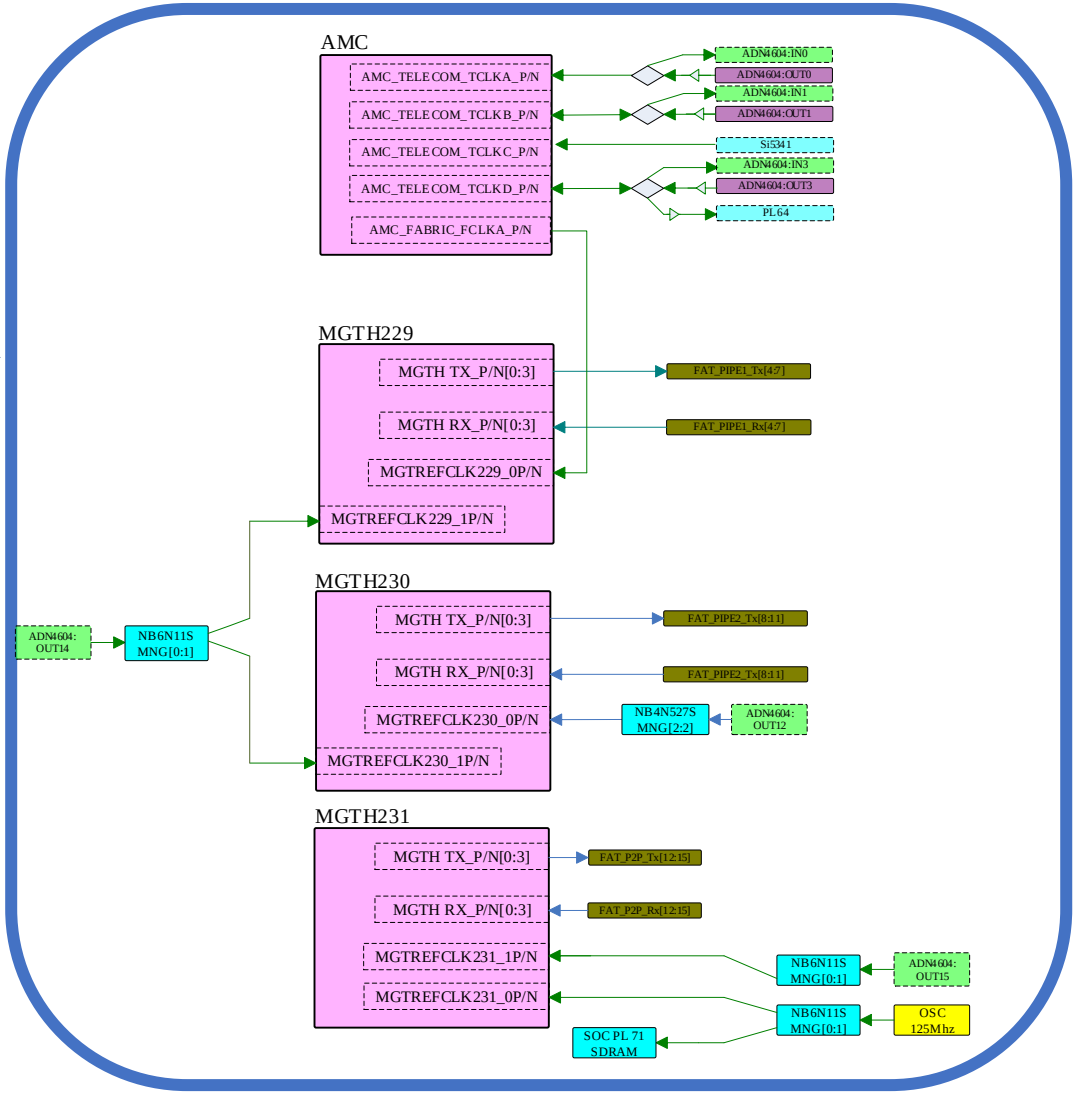


- A total of 20 transceivers from 2 High-Performance Connectors (HPCs) are connected to 5 GTH banks in the PL of ZYNQ.
- Two GBTCLK (Gigabit Transceiver Clock) signals from each HPC are connected to two GTH banks in the PL. The clock for the last GTH bank is provided by the Si5341



3.4.3 Clock Management Module





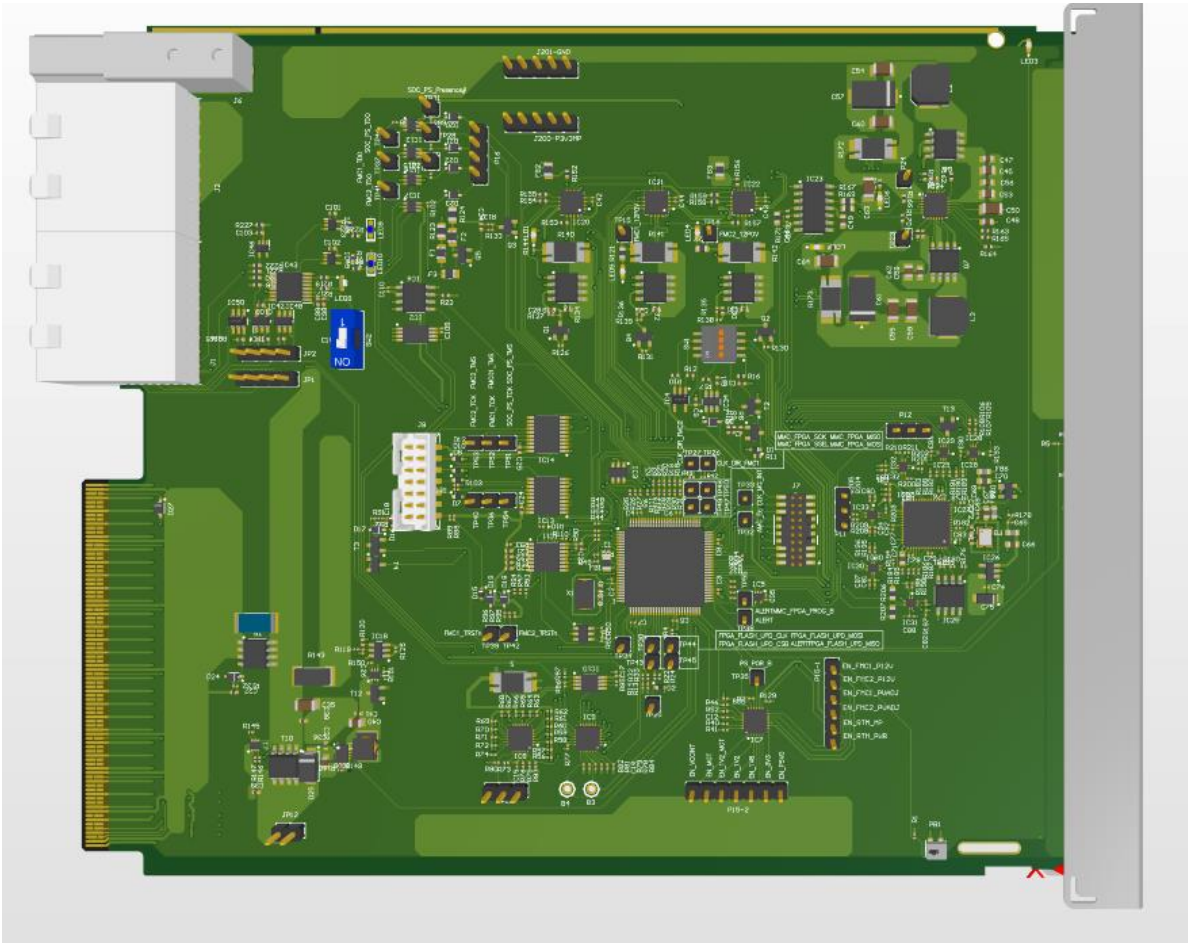
- Supports PCIe Gen.3x4 (expandable to Gen.3x8 if conditions allow).
- When only Ports 4-7 of PCIe are used, Ports 8-15 can be utilized as point-to-point Multi-Gigabit Transceiver (MGT) interfaces.
- In addition to the clock provided by the ADN4604, a separate crystal oscillator is equipped as a backup clock source.

4.1 Project Progress（MMC…）

- The board fabrication is divided into two phases:

  MMC module first, then full AMC board.

- **Phase 1: MMC Module Testing**
- Retain core modules: MMC, EEPROM, JTAG, power supply, current monitoring, and partial pins of the AMC backplane and RTM.
- verify the following functions:
  - ◆ I2C communication function of the MMC module
  - ◆ Power-on program execution
  - ◆ Current monitoring
  - ◆ Power supply connection with the AMC backplane
  - ◆ JTAG debugging function



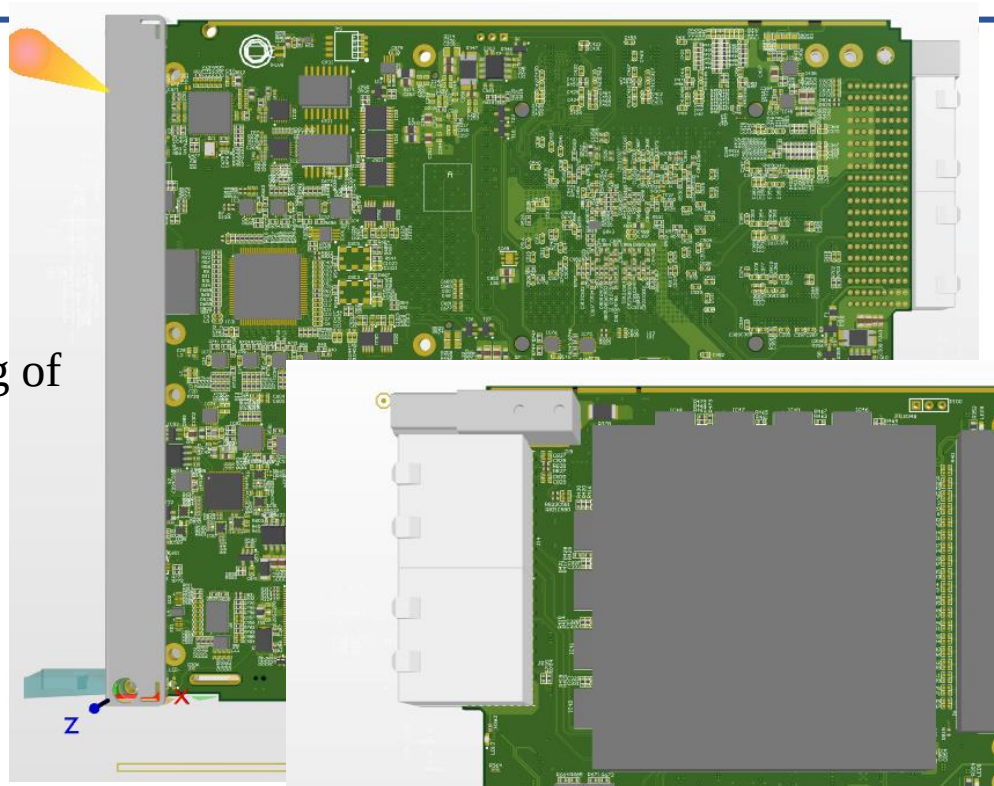
4.2 Project Progress（AMC）

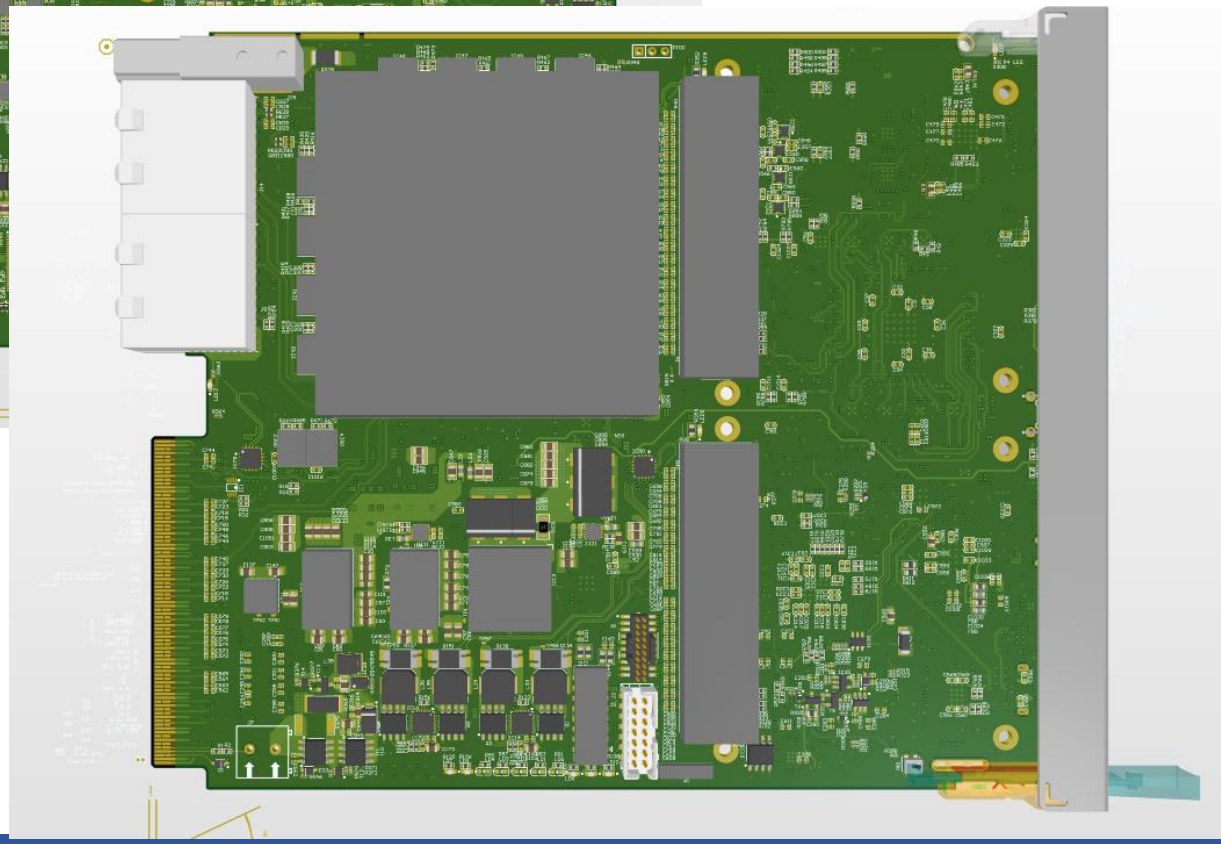
Phase 2: Full Board Fabrication

- After verifying and optimizing the MMC module functions, proceed with the fabrication of the full carrier board.
- This phased approach ensures separate debugging of the MMC chip and ZYNQ chip, streamlining the development logic.

Current Progress:

- The final layout of the MMC module has been completed; production will start after final verification.[mmc]
- Completed board thickness calculation and impedance matching analysis.
- Completed the preliminary layout design of the AMC module.






THANKS