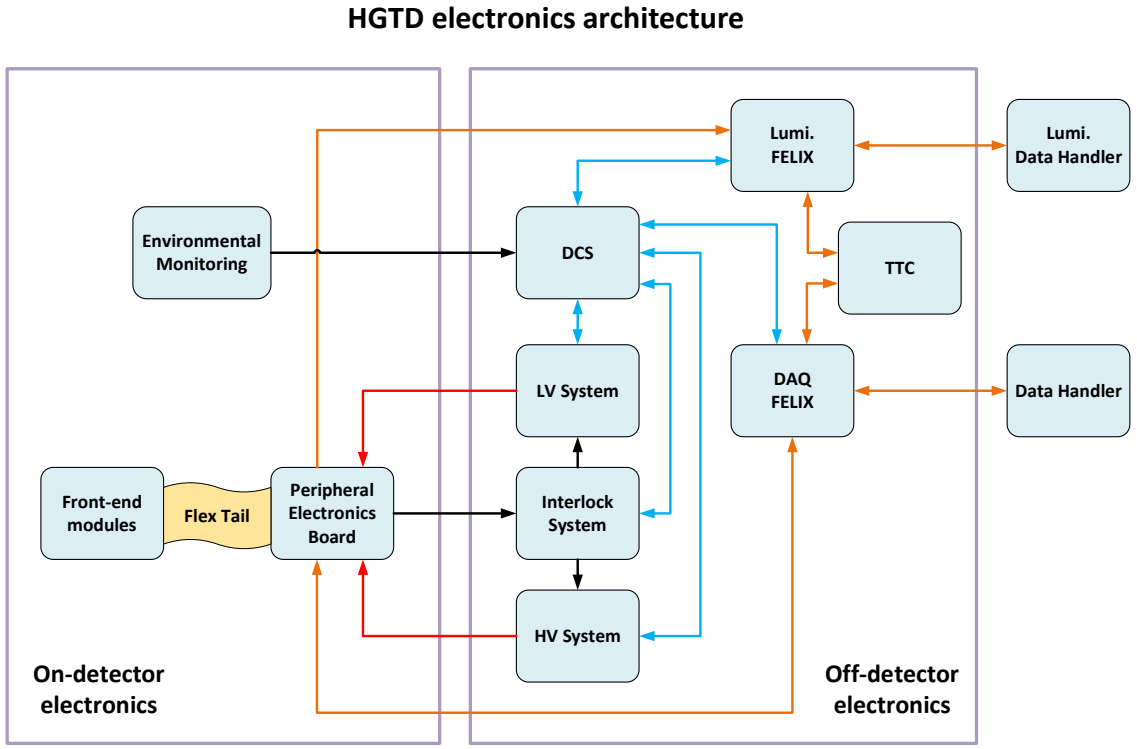
Status of HGTD Electronics

Jie Zhang on behalf of the HGTD Electronics Team

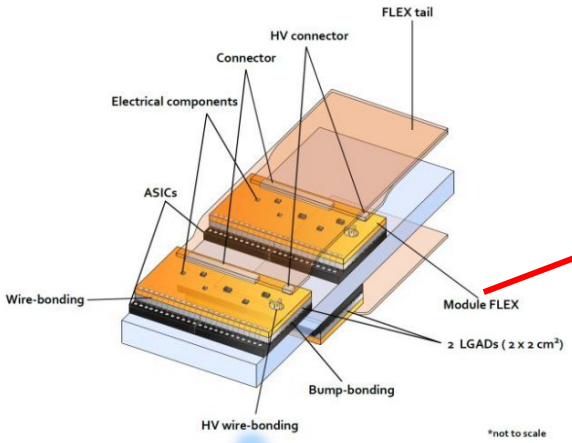
June 7th, 2025

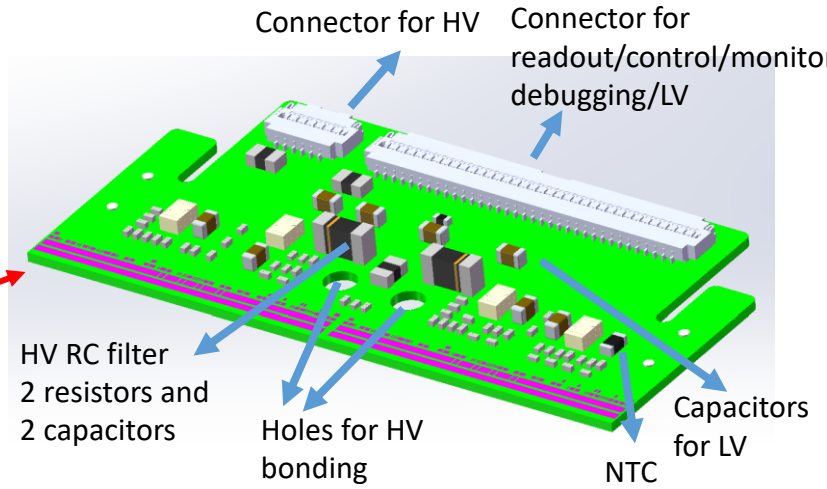
Overview of HGTD readout electronics

- On-detector
  - Front-end Modules
    - Flex PCB: Designed and produced by **IHEP (100%)**
  - Flex tail cables
    - Designed by Mainz
    - Produced by **Shandong University**, Mainz, JSI
  - Peripheral Electronics Boards (PEB)
    - Designed by IHEP, NJU (Nanjing University) and Morocco group
    - Produced by **NJU (50%)** and **IHEP (50%)**
- Off-detector
  - High Voltage Power Supply
    - **IHEP** and **Shandong University**

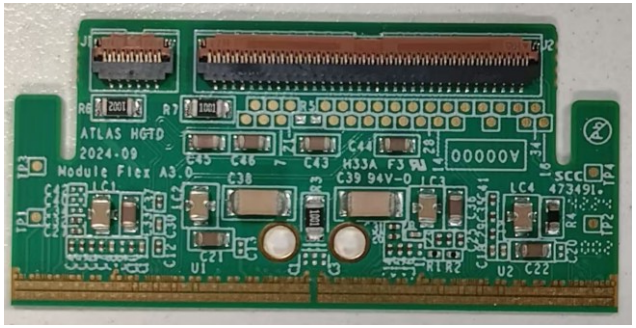


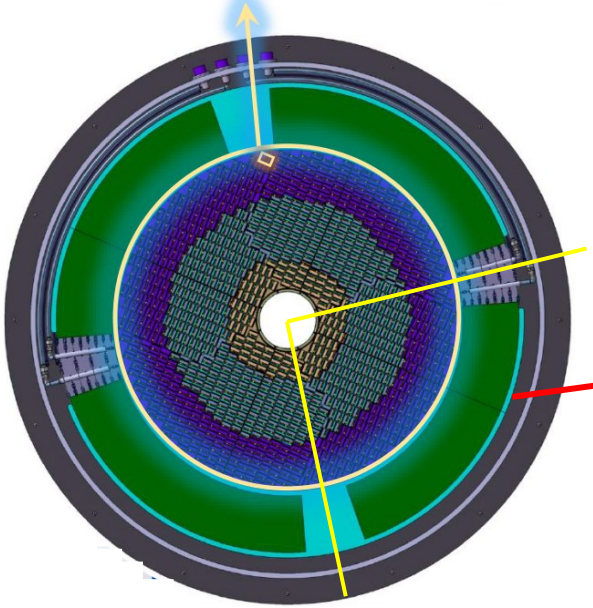
On-detector Readout Electronics – Scope

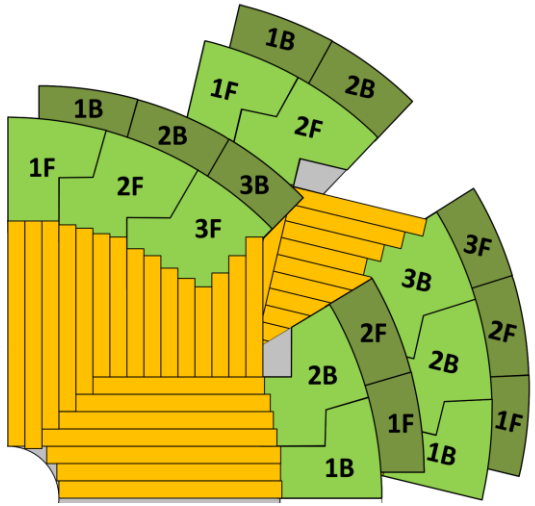




- The **front-end modules** are connected via **flex tails**, arranged in rows







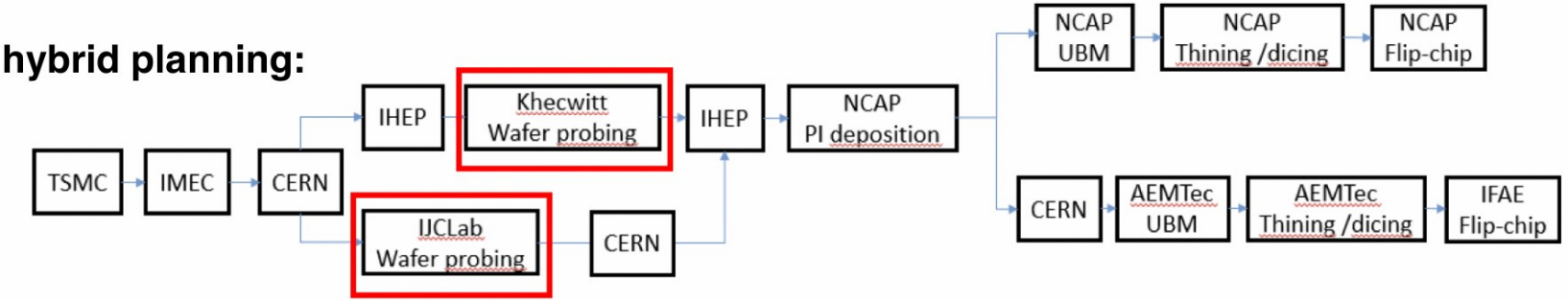
One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- **PEB** @ 660 < r < 920 mm
- Six types of PEB to be designed (front and back side)
  - Board 1F, 2F, 1B and 2B can be used both on front and back
    - According to the optimization of mirror structure for module layout
  - Each board covers three or more readout rows in order to have a similar number of modules

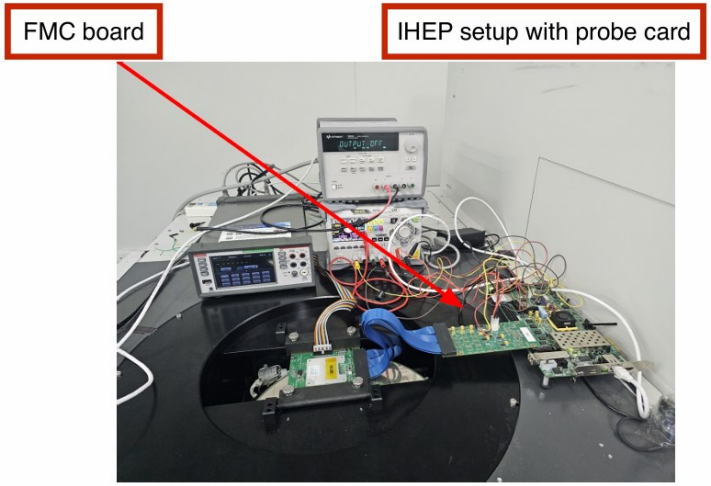
ALTIROC-A Status

- Pre-production ASIC: HGTD-ALTIROC-A
  - Minor modifications in ALTIROC-A compared to ALTIROC-3
- Pre-production quantity ~5% → ~800 good ASICs: 10 wafers w/ yield
- TID (irradiation) testing showed variations in TOA LSB which can be solved with external resistors for Vctrl
  - Changes to the module flex which were adopted to reduce impact

ASIC to hybrid planning:



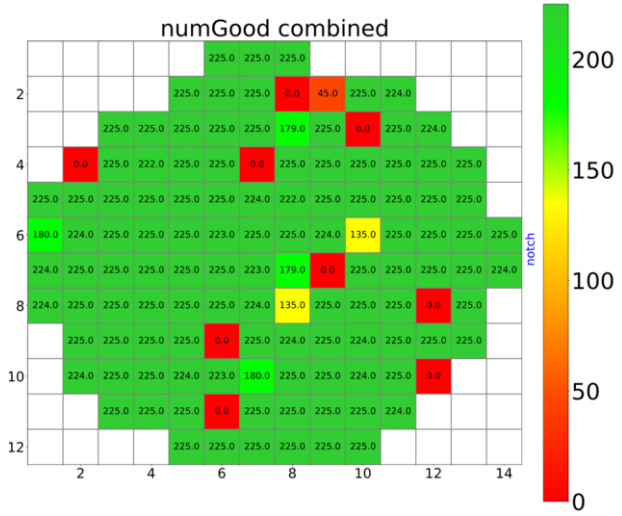
- Pre-production wafer probing at IHEP and IJCLab
  - Good progress in the last few weeks, now IHEP and IJCLab have each wafers probed
  - Remains the critical schedule driver of the project
  - Finalization of testing procedure and calibration



Status of ASIC pre-production wafer probing

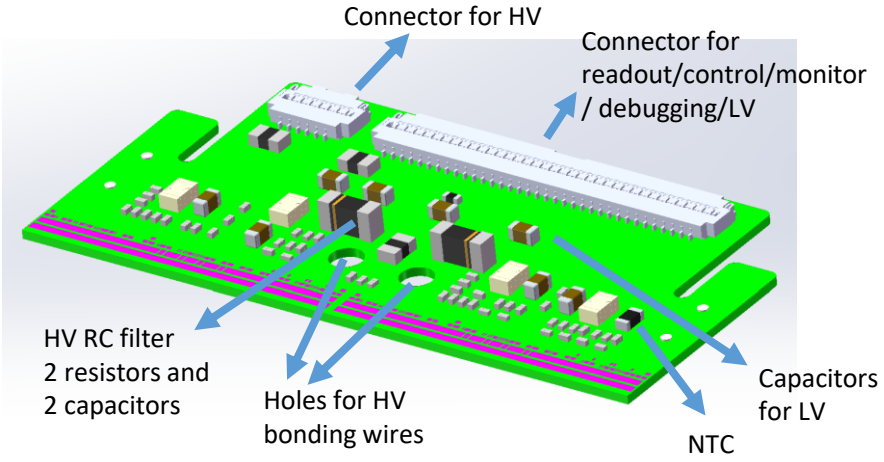
- 5 full wafers probed at IHEP with preliminary yield ~ 80.5 % (assumed in BoE)
  - Re-testing needed on noisy pixels
  - Critical item requiring immediate attention: finalize the testing scripts for all testing criteria and analysis of pre-production wafers

Site	Wafer ID	Test ASICs	Good ASICs	Yields	Potential Good ASICs	Best estimate yields	Comment
IHEP	Wafer001	124	-	-	-	-	Engineering run for setup
	Wafer002	124	80	64.5%	15	76.6%	
	Wafer003	124	89	71.8%	12	81.5%	
	Wafer004	124	57	46%	47	83.9%	no re-test yet
	Wafer005	124	70	56.5%	26	77.4%	
	Wafer006	124	88	71%	15	83.1%	



Wafer006 Results

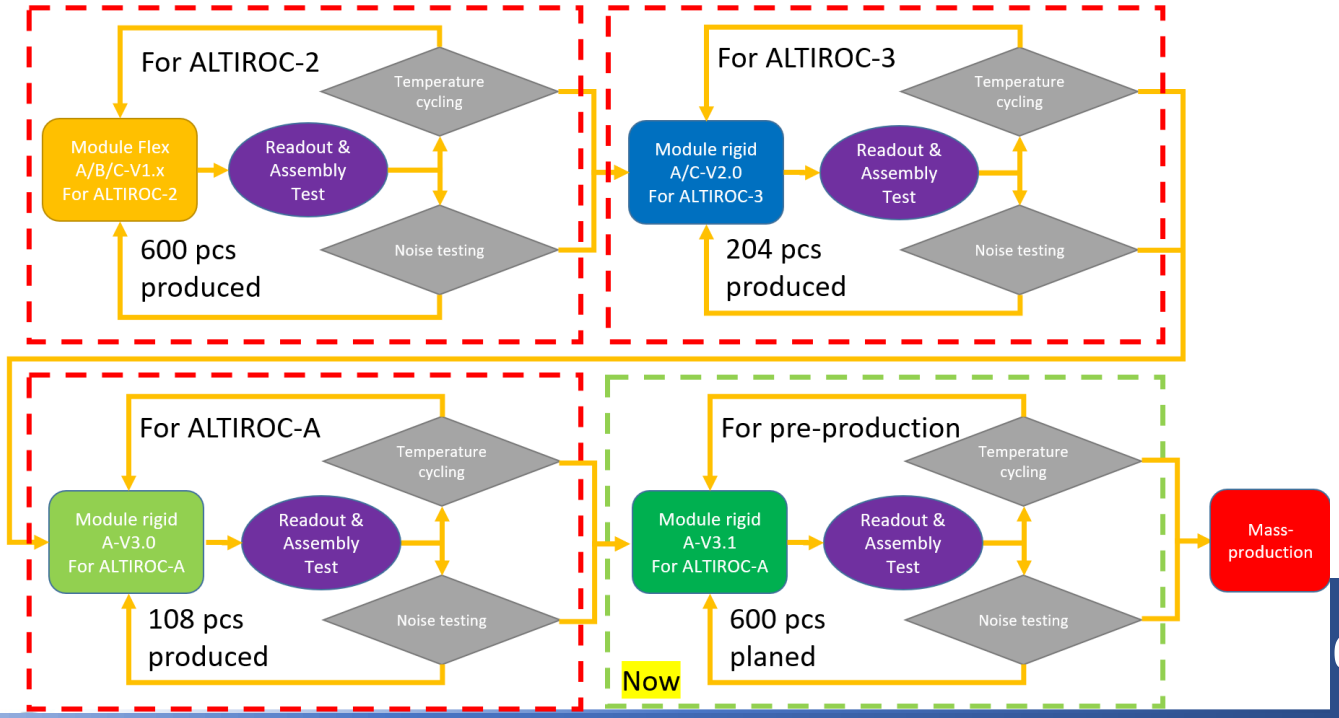
Status of module flex



Design and verification

- Finished the selection and evaluation of components
- Early prototype has been successfully produced, key parameters have met the HGTD requirements
- Sent the early prototypes to every assemble site

- From V3.0 to V3.1
  1. Add external R & C for Vctrls
  2. Add conncetion between “window2p” and "ext_disc_p" for the External Time Base scan (ETBscan) of TDC calibration
  3. Move HV caps & holes to right side by 760um

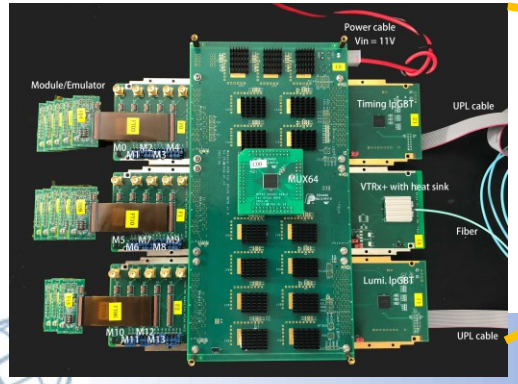


PEB Status

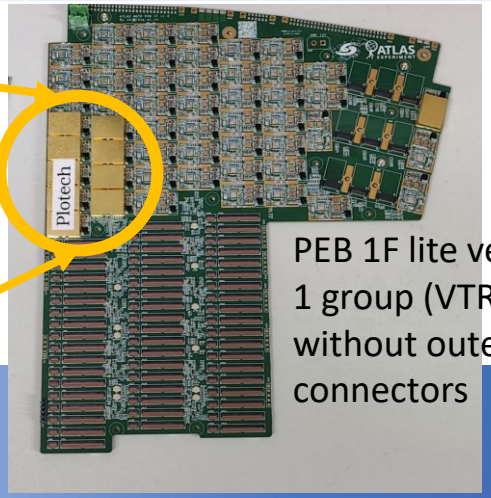
- Modular PEB
  - Start from individual test boards (Front-end module (ALTIROC), MUX64, bPOL12V, lpGBT and VTRx+)
  - To allow testing in the lab as a standalone board to verify functionality and performance separately
  - Function and performance are validated by collaborators
- PEB 1F
  - Most complex PCB in 6 types of PEB, up to 22-layer PCB
  - Process the maximum number of lpGBT, up to 12 pcs

Site	CERN	IHEP	NJU	Nikhef/Radboud	KTH	Clermont
Modular PEB	-	-	1	1	1	1
PEB 1F (lite version)	1	1	1	-	-	-
PEB 1F	2	-				
Tasks	Demonstrator, Beam test, & System integration	QA/QC, Reliability test	Training	TDAQ	Lumi.	Timing

Modular PEB is 1/9 group of PEB 1F



Modular PEB



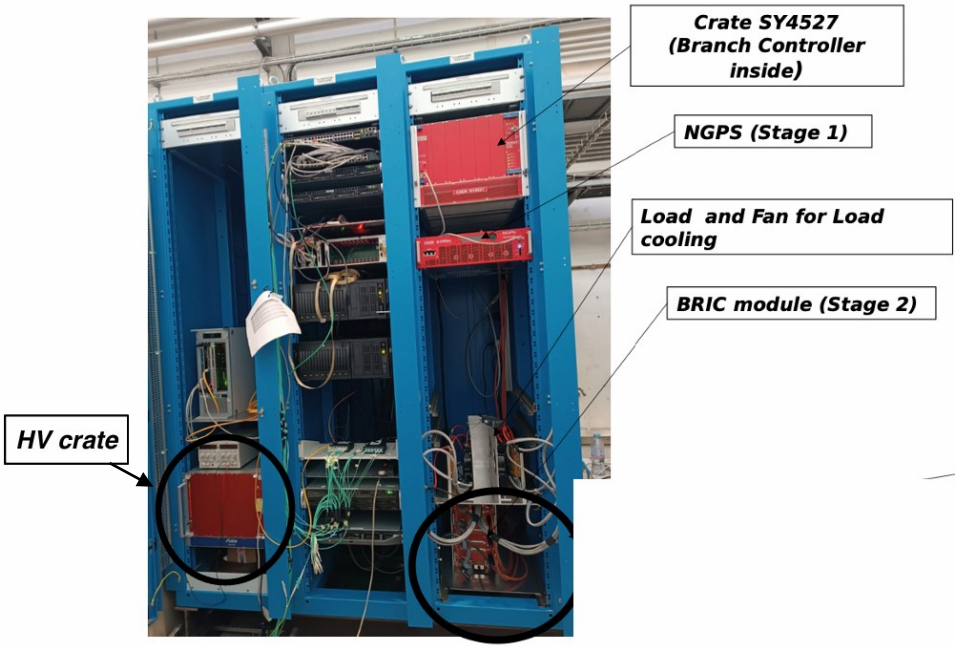
PEB 1F lite version
1 group (VTRx+ 2 lpGBT)
without outer ring
connectors

PEB 1F

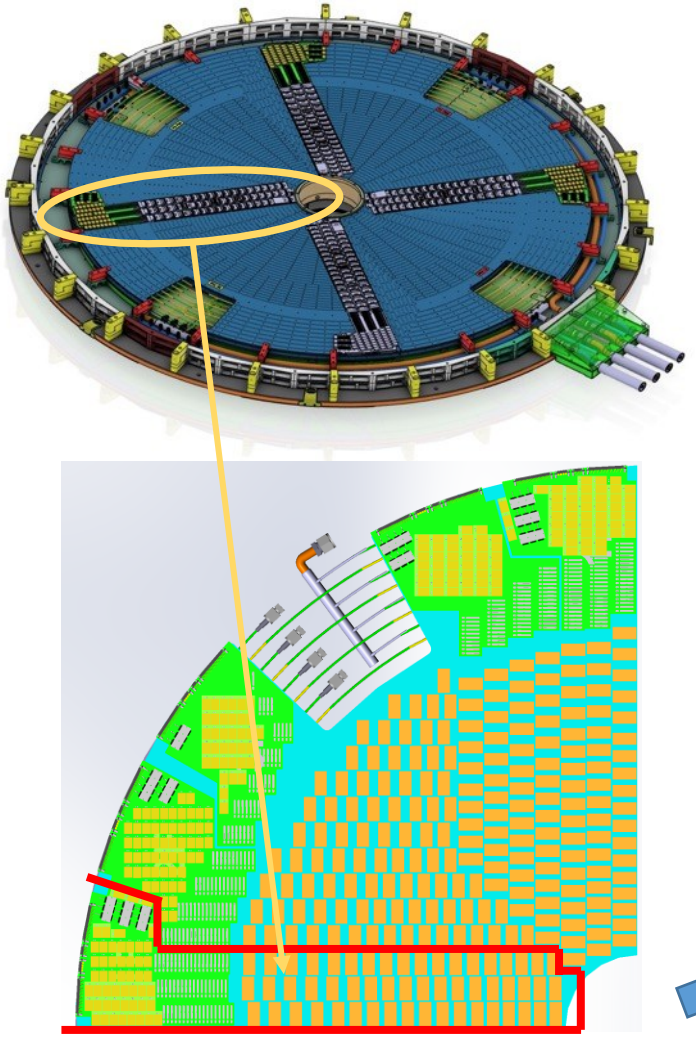
Off-detector Electronics

- Interlock crate: LISSY being tested with PEB/HV/LV at CERN in last month
- LV and HV in pre-production phase with full testing criteria being defined
  - Both LV and HV pre-production elements being tested prior to integration with demonstrator
  - LV: Power supplies similar to NSW ones Second irradiation test of BRIC modules (stage 2) on-going at CHARM

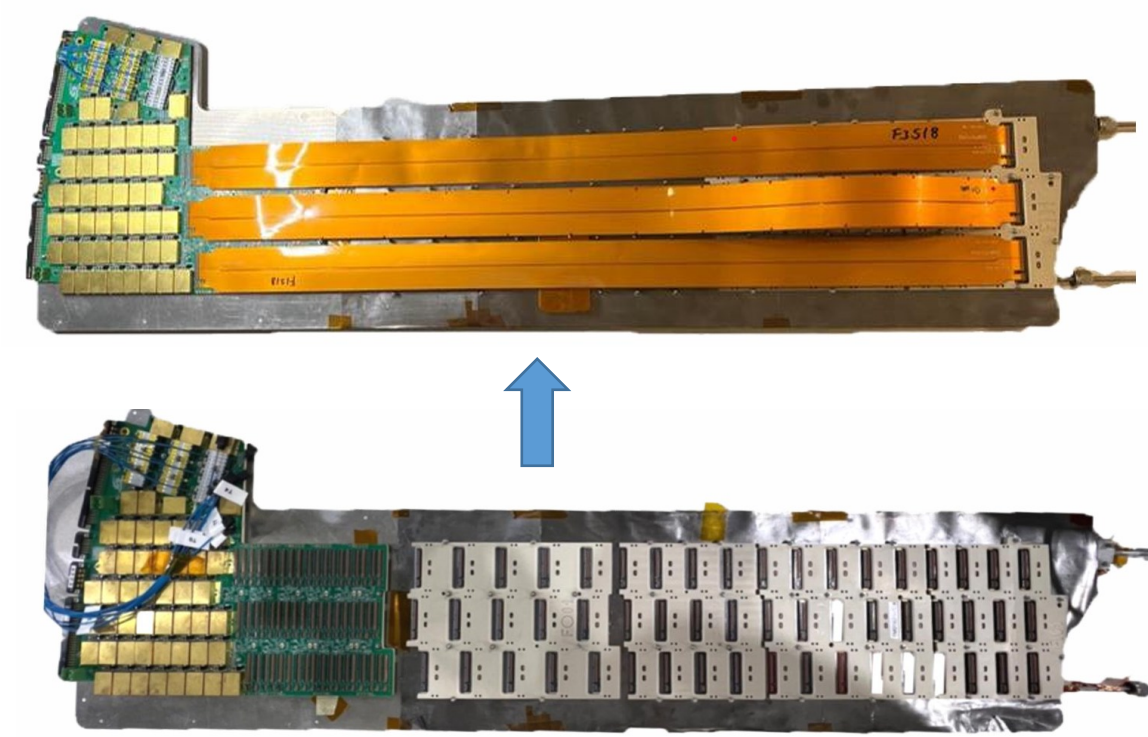
HV module, **Individual Floating Channels**



In-detector Connections in HGTD

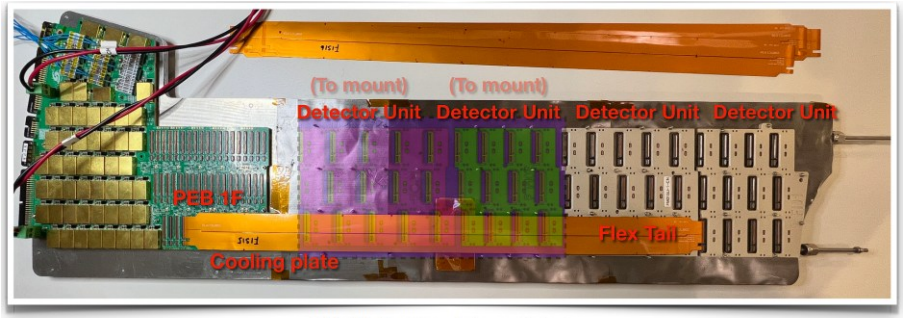


- Flex-tails use to connect the front-end modules and PEB
  - Up to 19-layer stack-up flexes in one row
  - Lengths range from about 5 cm to 70 cm
  - Full detector: 62 different lengths



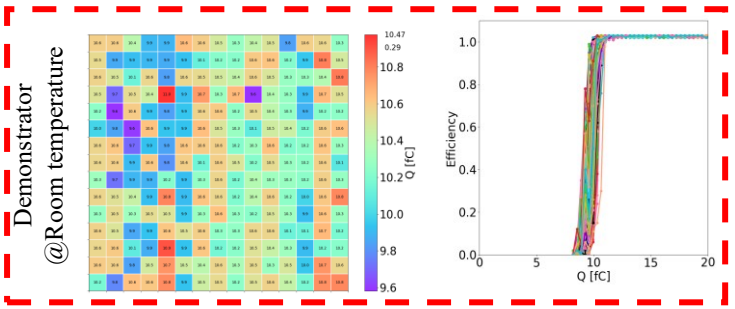
Tests in Demonstrator System

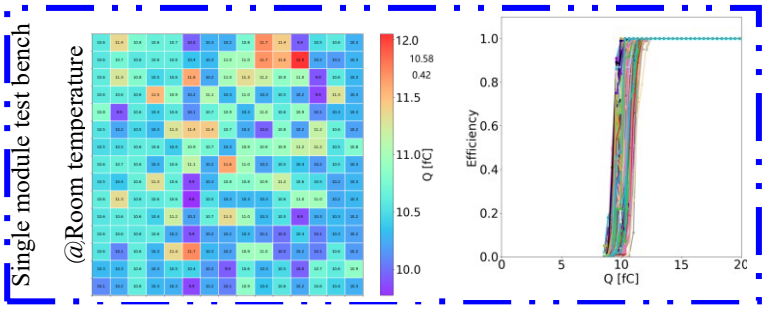
- FEB 1F prototype undergoes an integration test.
  - Including 54 real modules (about 0.7% of the full system), as well as the associated components (interlock, DCS, TDAQ, cooling system, support unit, cabling, etc.) are assembled and tested.

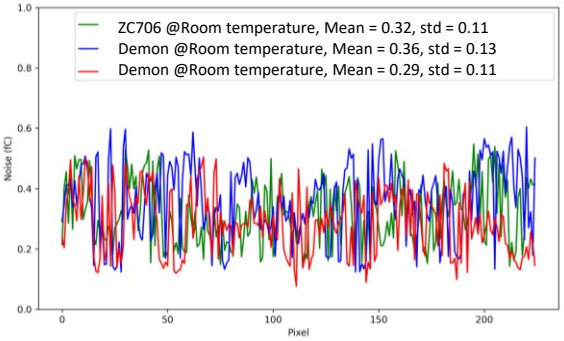


HV, LV, Cooling plate prototype
Electronics : PEB 1F + flex tails + 54 modules mounted on 4 support units (detector unit)

Demonstrator at CERN,
Vessel with Faraday cage, using the small CO_2 plant







- Noise levels were measured with 42 modules in room/cold T, and no major problem was found

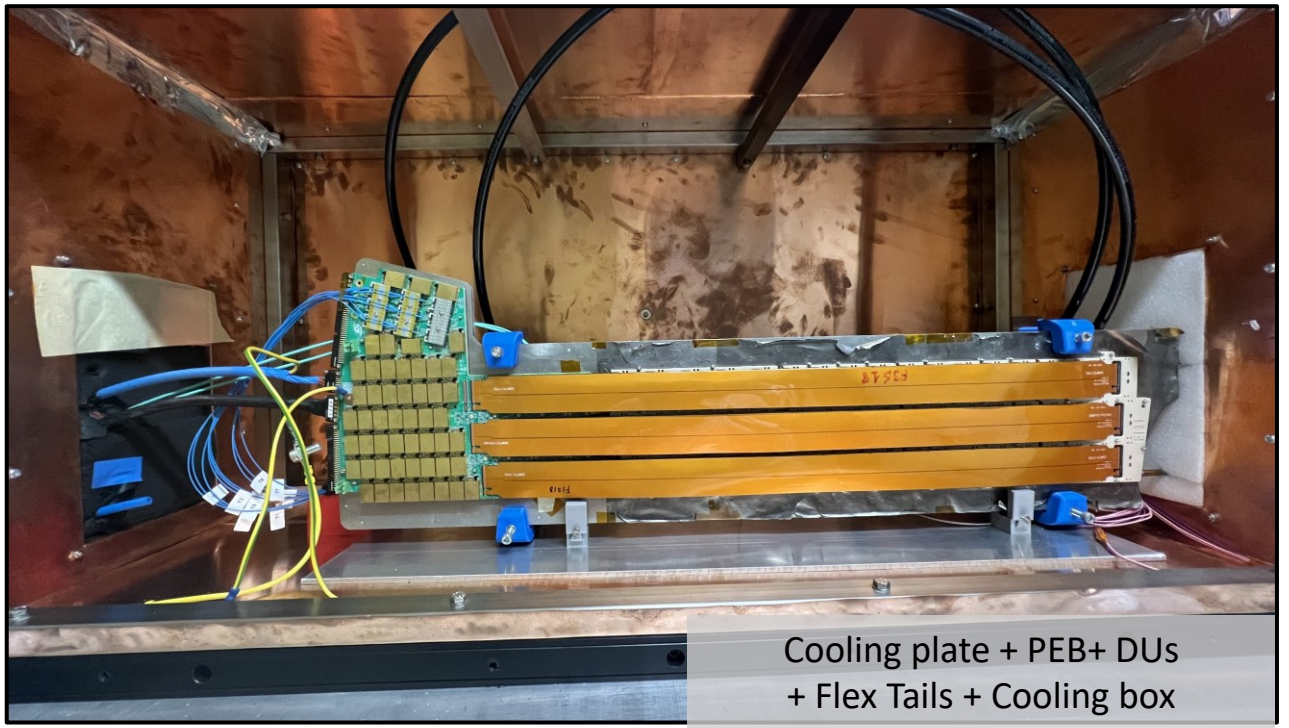
Demonstrator Setup at CERN

Measurements at high speed (1280 Mb/s)

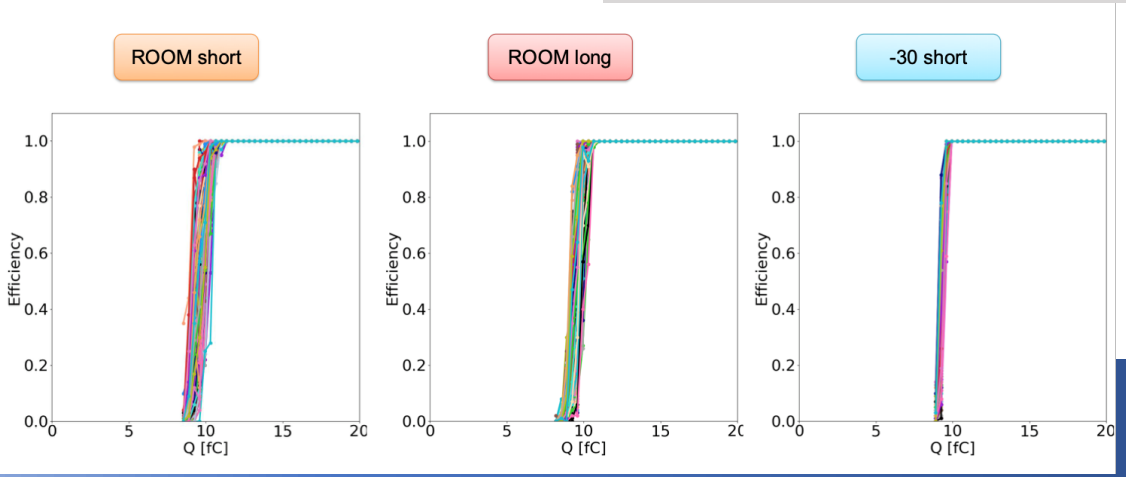
- The PEB receives timing data (TOA&TOT) @ 1280, 640 or 320 Mb/s depending on the module position in radius
- Read out 4 ALTIROC3 modules per row at 1280 Mb/s

Transmission quality:
charge scan for module R3M8

- During a charge scan with a threshold at ~ 9.6 fC, charges > 9.6 fC should have 100 % efficiency.
- If the plot shows effeciency 100% for those charges, it means that no data are lost and no communication error occured

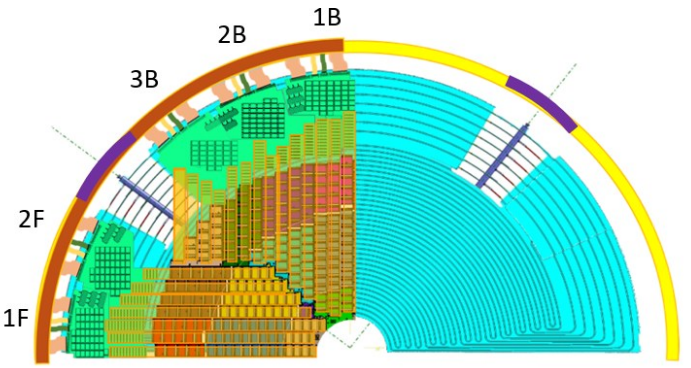


Cooling plate + PEB+ DUs + Flex Tails + Cooling box



Milestone Update and Plan

- Module Integration including the module flex
  - Successfully passed Final Design Review (FDR) in November 2024
  - Under pre-production after changes with external resistors for Vctrl
- Periphery Electronics Board (PEB)
  - Achieved conditional FDR approval on May 16, 2025
  - Currently addressing specified conditions for full approval
- ASIC Development
  - Production Readiness Review (PRR) scheduled for June 26, 2025
- High Voltage System
  - Under pre-production
  - PRR currently projected for February 2026

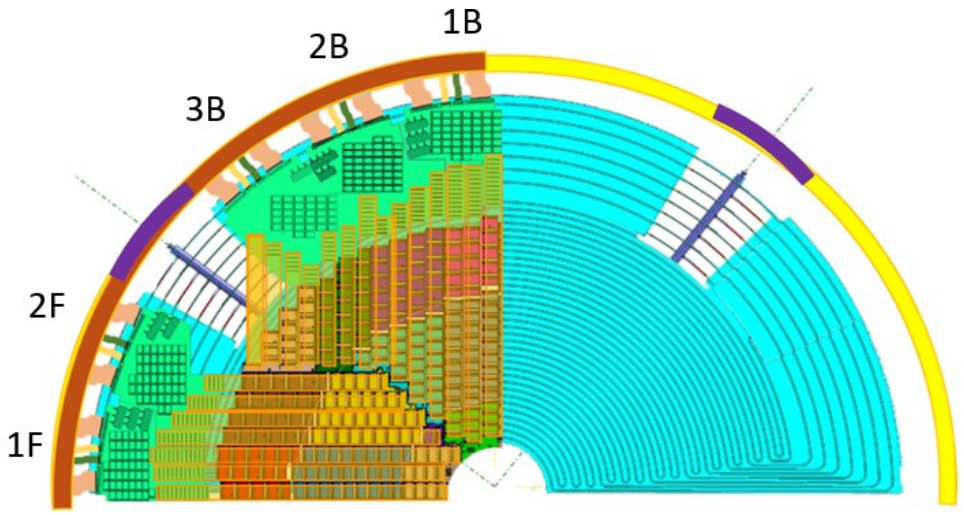


Back side	Front side
• 5 pre-prod PEB (1F,2F,3B,2B,1B) • 24 pre-prod DU - 251 modules • 5 set pre-prod pigtails • 5 pre-prod outering sectors with connectors (remaining pieces blind)	• 24 pre-prod SU

Item	Year	2024				2025				2026			
	Quarter	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
ASIC		FDR					PRR						
PEB							FDR				PRR		
HV			FDR							PRR			
Module Flex					FDR				PRR				

Now

HGTD Module 0 in 2026



Back side	Front side
• 5 pre-prod PEB (1F,2F,3B,2B,1B) • 24 pre-prod DU - 251 modules • 5 set pre-prod pigtails • 5 pre-prod outering sectors with connectors (remaining pieces blind)	• 24 pre-prod SU

- Definition:
  - Assembly and test ~ 3% of HGTD pre-production modules and their associated electronics inside the final design hermetic vessel at the CO_2 operational temperature T=-40℃
  - To be noted that in order to cool down ~ 3% of HGTD modules and the associated electronics we need essentially 50% of the mechanics and cooling to be ready (1 fully working vessel)
- Scope:
  - Validation of the integration and test of the pre-production parts (~ 3% of the HGTD active components)
  - Check and train the assembly/integration procedures
  - Check the G&S scheme
  - Also integrate Interlock, DCS and DAQ

PEB PRR is linked to Module 0

PEB Issues

- Components procurement
  - HV and LV connectors, Sao Paulo, quotation received, but quoted price is **twice over our budget**
  - Interlock and grounding connectors, **NOT in the BoE and MoU**, quotation received
  - Flex tail connectors, Sao Paulo, not started, could be shared with the module flex
  - IpGBT, CERN, delivered for pre-production
  - VTRX+ optical transceivers, Casablanca, Kenitra, MASclR, Oujda, Rabat,Nikhef, Niimegen, Stockholm KTH, delivered for pre-production, placed order for mass-production
  - Monitor MUX, Nanjing University and IHEP, delivered and passed QA/QC for pre-production and mass-production
  - DC/DC converters(including capacitors, resistors, inductors, custom shielding casings **with stamping process** and bPOL12v), CERN, Not started
  - Machining (VTRx+ clip, custom heatsink and custom cooling support), **NOT in the BoE and MoU**, Not started
- QA/QC and Reliability test
  - IHEP, Nanjing University, will be done at IHEP, **need more testing engineers**

Conclusions and Outlook

Key points:

- ASIC wafer probing progressing after months of delay, finalize all tests and verify good contact at IJCLab, TID testing complete - PRR scheduled at end of June
- Combined Module FDR passed in November 2024, module flex pre-production has started
- PEB FDR passed in May 2025, moving towards to pre-production
- HV under pre-production

THANKS TO YOUR ATTENTION

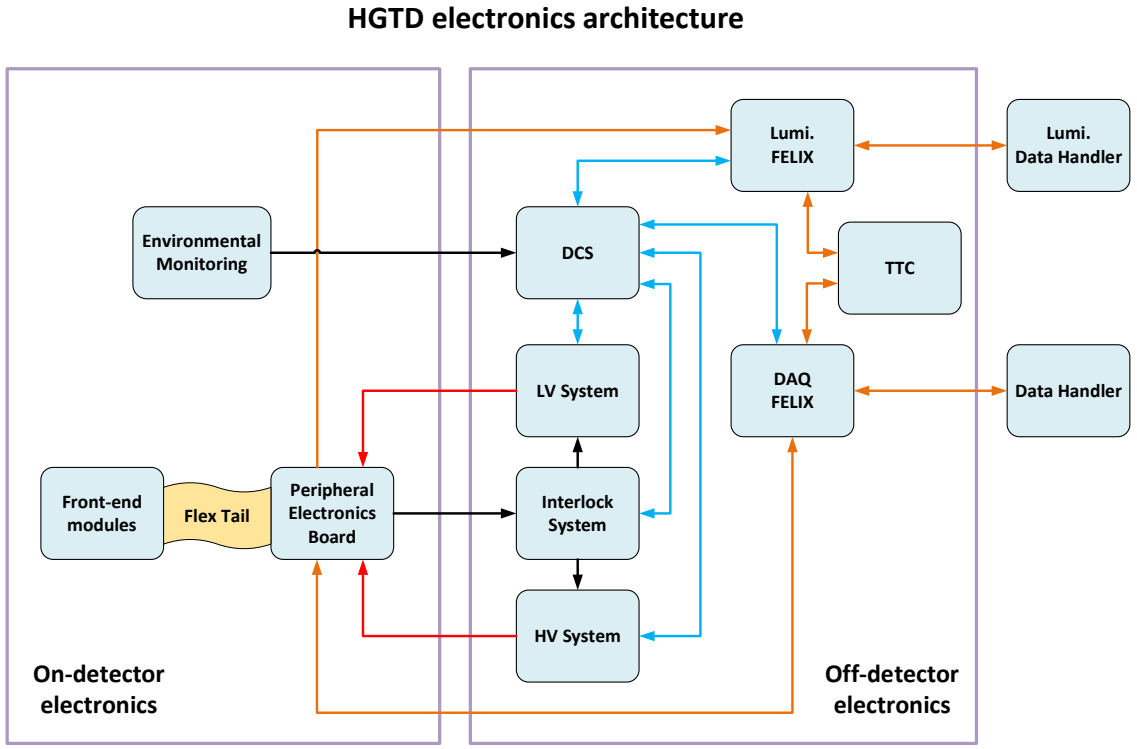
Backup

Overview of HGTD readout electronics

- On-detector Electronics
  - Front-end modules
  - Flex tail cables
  - Peripheral Electronics Boards (PEB)

Basic functions of front-end module

- Pileup rejection
  - Time resolution at the start (end): 30 (50) ps per track / 35 (70) ps per hit
- Luminosity measurement
  - Count number of hits at 40 MHz (bunch-by-bunch)
  - Goal for HL-LHC: 1% luminosity uncertainty

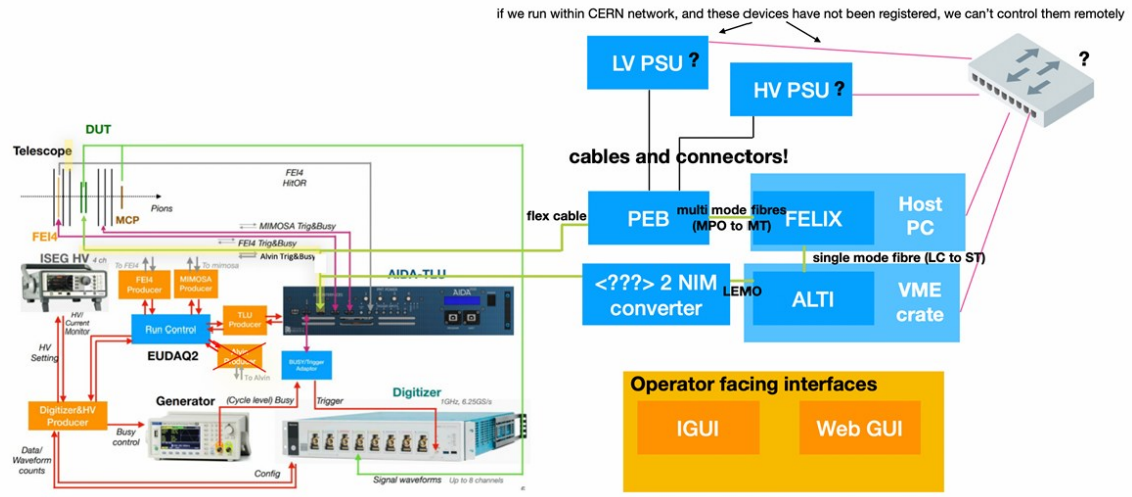


Basic functions of PEB

- Control, monitoring & data aggregation and transmission
- Power-supply distribution: LV & HV
- Thermistor connection between the front-end modules and the interlock system

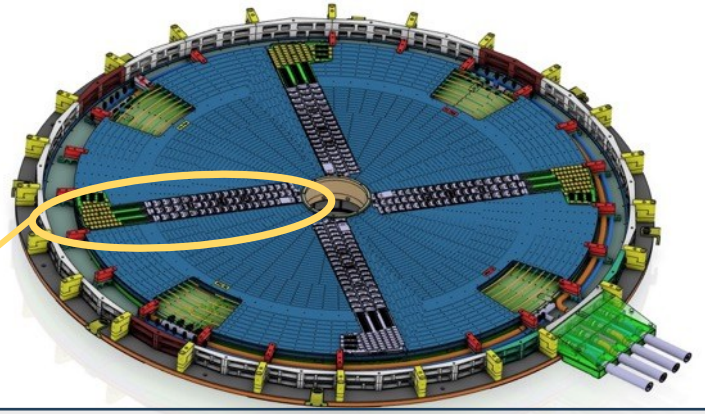
Upcoming test beams

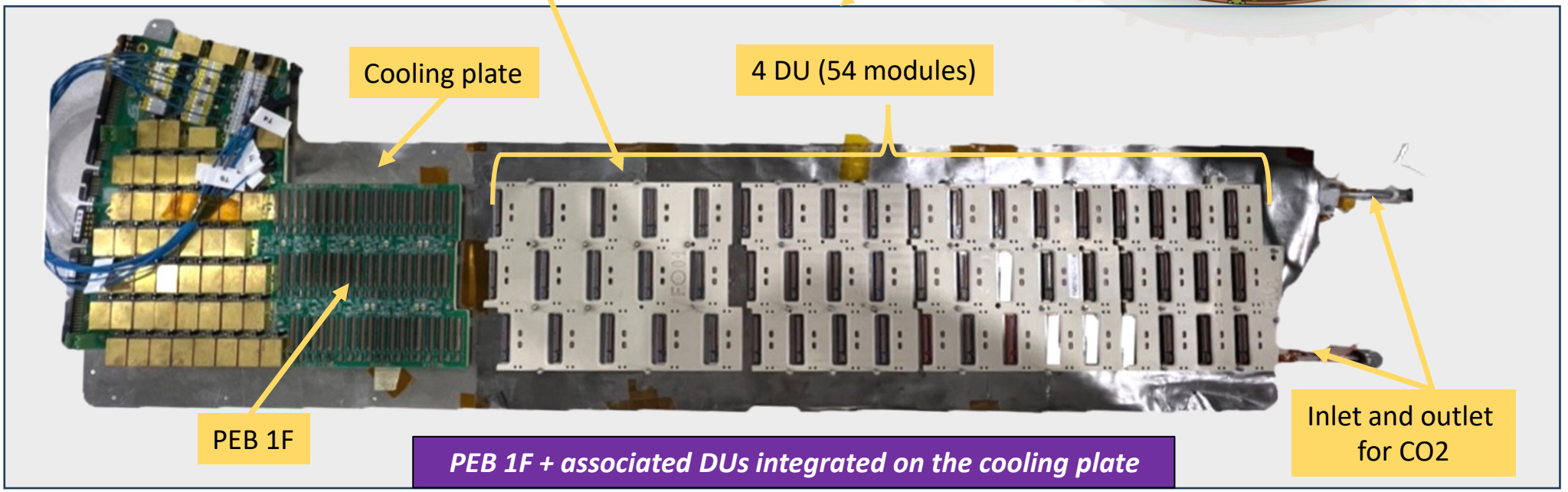
- Two upcoming test beams: June 4 - 18th and Oct 1 - 15th at SPS
- Planning an additional test beam at DESY: pre-prod modules and prod sensors
- Goal of SPS test beams to study full DAQ readout with PEB, multi-module readout and time resolution calibration methods
  - Will use hgtd-felix-sw and FELIX-star
  - TLU (Trigger Logic Unit) → LTI (Local Trigger Interface) → FELIX (Front End Link eXchange)



Demonstrator assembly at CERN

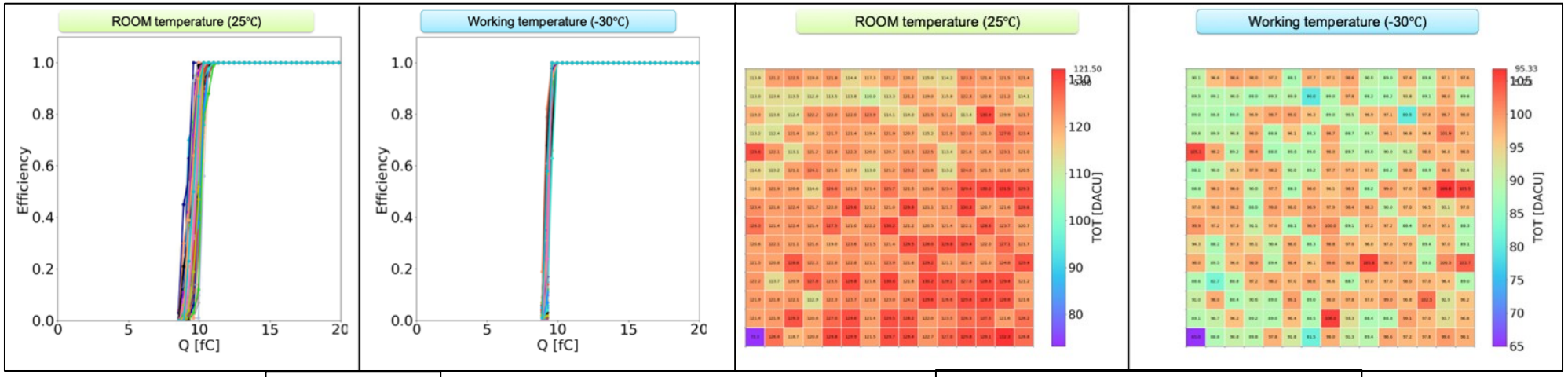
High thermal conductivity graphite sheet (PGS 70 μm):
- enhance thermal contact between ASIC & cooling plate
- compensate non-perfect planarity at the ASIC <-> cooling plate interface





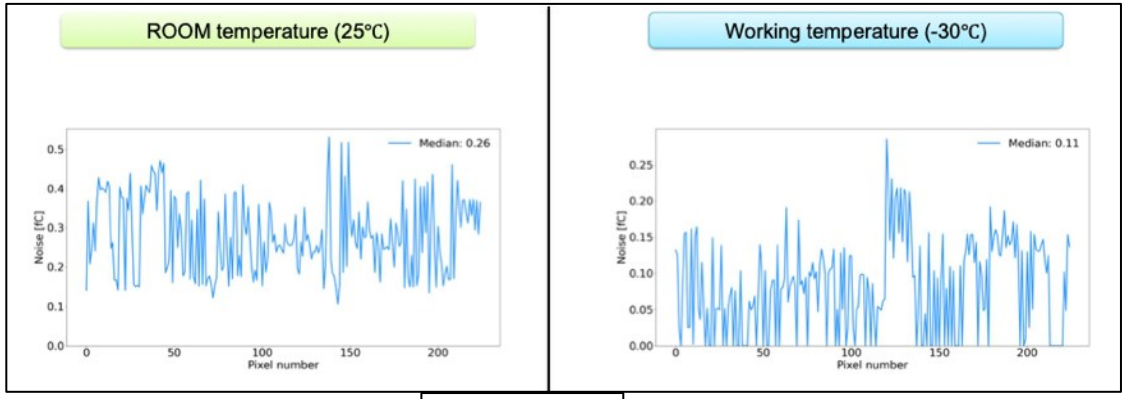
PEB 1F + associated DUs integrated on the cooling plate

Measurements 27 ALTIROC3 modules at T_{room} and T=-30℃ and 320 Mb/s with Demonstrator



Charge scan

TOT scan (bump connection test)

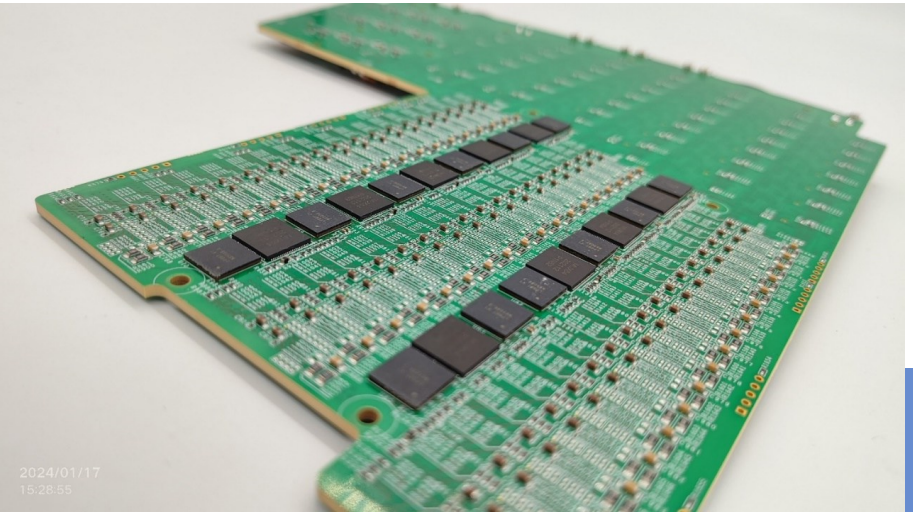


Noise scan

The 27 ALTIROC3 modules behave as expected both at T_{room} and T=-30℃

lpGBT v1 issues and HGTD-lpGBT status & plan

- Two separate issues, that may affect correct operation of a fraction of systems, have been discovered in 2024:
  - Stuck at power-up
    - Small fraction of chips may be completely unresponsive after power-up in some conditions, no communication possible, external reset is ineffective
    - Power cycle might restore functionality, but success of this is not guaranteed
  - Equalizer attenuation
    - Small fraction of lpGBT chips paired with VTRx+ modules may show correctable or non-correctable downlink data errors
    - Impacts systems even when equalizer functionality is not explicitly used
- HGTD have used 24 chips for prototype, the two problems mentioned here have **not** been found.
  - The sample of statistics is too small.
  - Usage details:
    - Power by bpol12v (12V->1.25V), rising time is 200 us, shared by two or three lpGBTs and VTRx+.
    - Power by bpol12v (12V->2.55V), rising time is 200 us, VTRx+.
    - One lpGBT acts as master (10 Gbps, FEC5, Transceiver, recovered clock from the data stream, boot from ROM), one or two lpGBTs acts as slave (10 Gbps, FEC5, Simplex TX, external 40 MHz reference clock from master, boot from ROM)
    - Operate at -35◦C $\pm$ 5◦C (CO_2 cooling)

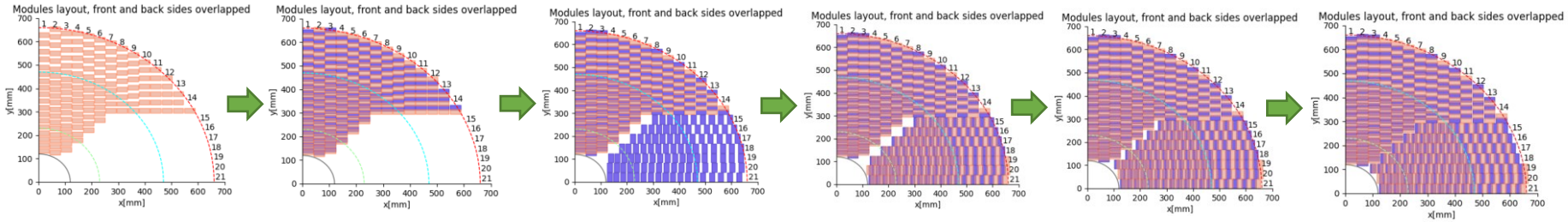


New HGTD-lpGBT plan

- Use the lpGBTv2 for pre-production (125 chips, middle 2025)
  - To avoid re-packaging, 184 lpGBTv2 (in one tray) have be picked up by Stefan on March 7, 2025
- Use the lpGBTv2 for mass-production (1988 chips, early 2026)

WBS 8.2.2: Peripheral Electronics Board – Technical Progress and Status

- Module layout adjustment to reduce PEB types from 10 to 6
  - 1F, 2F, 2B and 1B are re-used at both side
  - Reduce the risk of the new design
    - The PCB placement and routing of 1F and 1B, 2F and 2B, have something in common, but readout speed of modules near boundaries are different. This need new channel arrangement for lpGBT
  - Save costs
    - The PCB NRE (Non Recurring Engineering) Cost for rigid-flex is 8~10 times to the price per unit
  - Reduce the risk on the project schedule
    - Design, production and testing
    - Each type of PEB will have different testing setup and software
- Mirror Structure
  - Python3 script is developed according to the constraints from TDR
  - Workflow - 6 steps to generate module layout

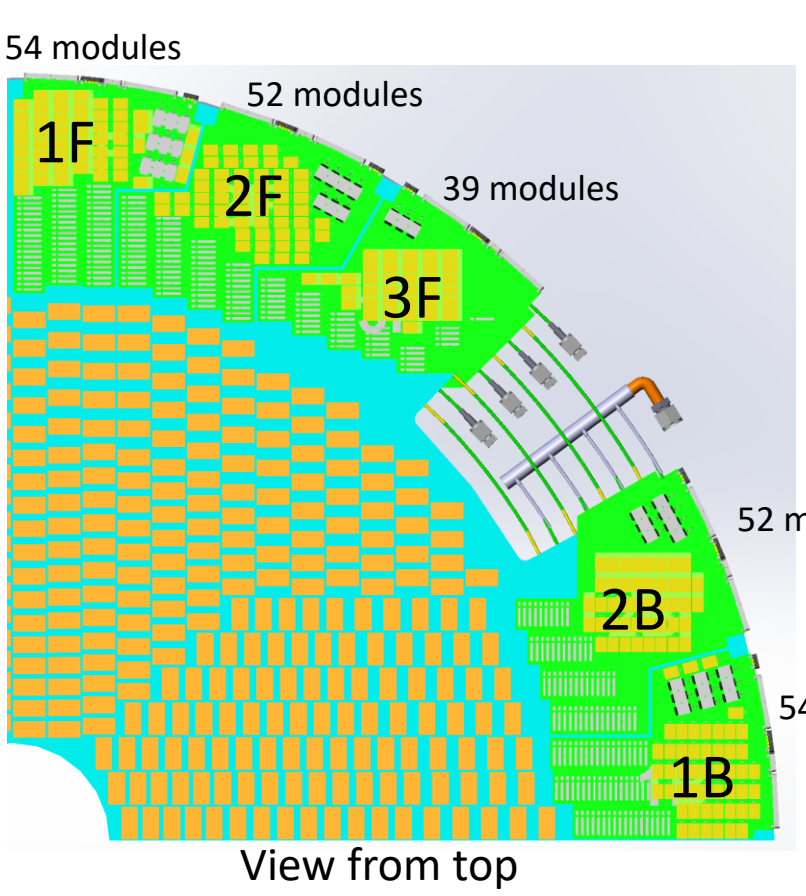


- The new layout is evaluated by mechanical design and physical simulation

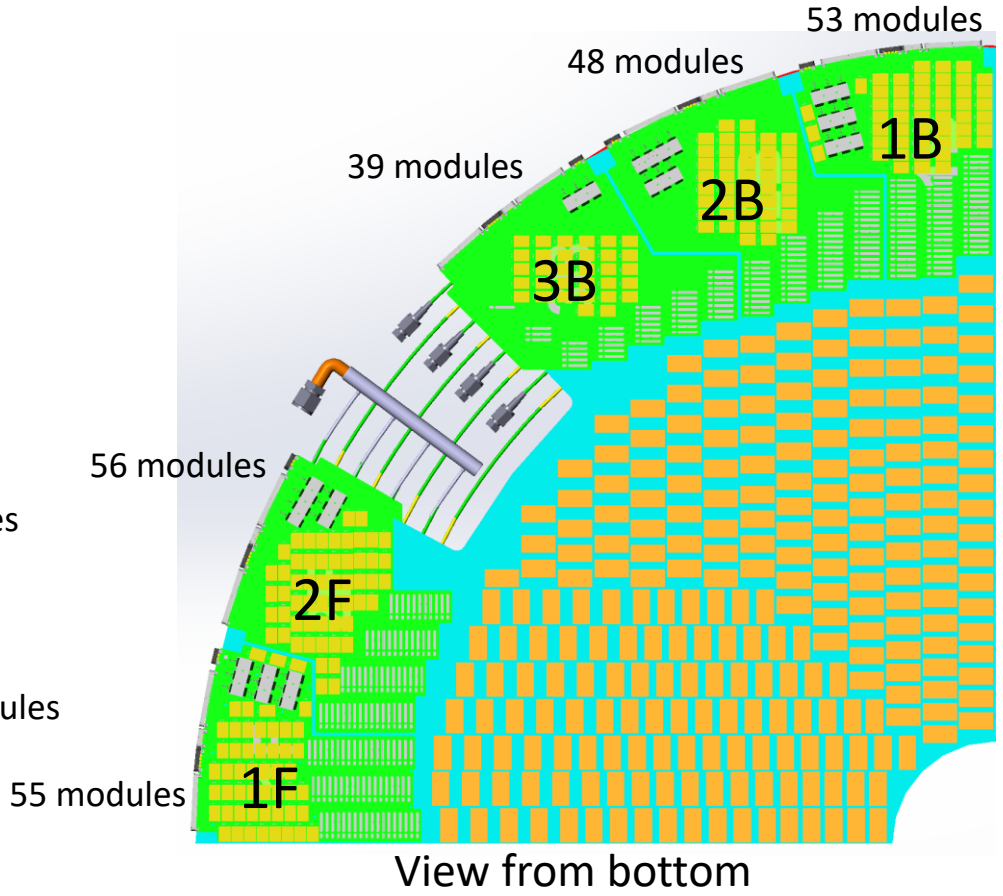
WBS 8.2.2: Peripheral Electronics Board – Scope

Number of modules attached to the different PEBs at the front and back sides

PEB	Front side	Back side
1F	54 modules	55 modules
2F	52 modules	56 modules
3F	39 modules	-
3B	-	39 modules
2B	52 modules	48 modules
1B	54 modules	53 modules



View from top



View from bottom

One quadrant of the HGTD front and back side

WBS 8.2.2: Peripheral Electronics Board – list of items

Main chips

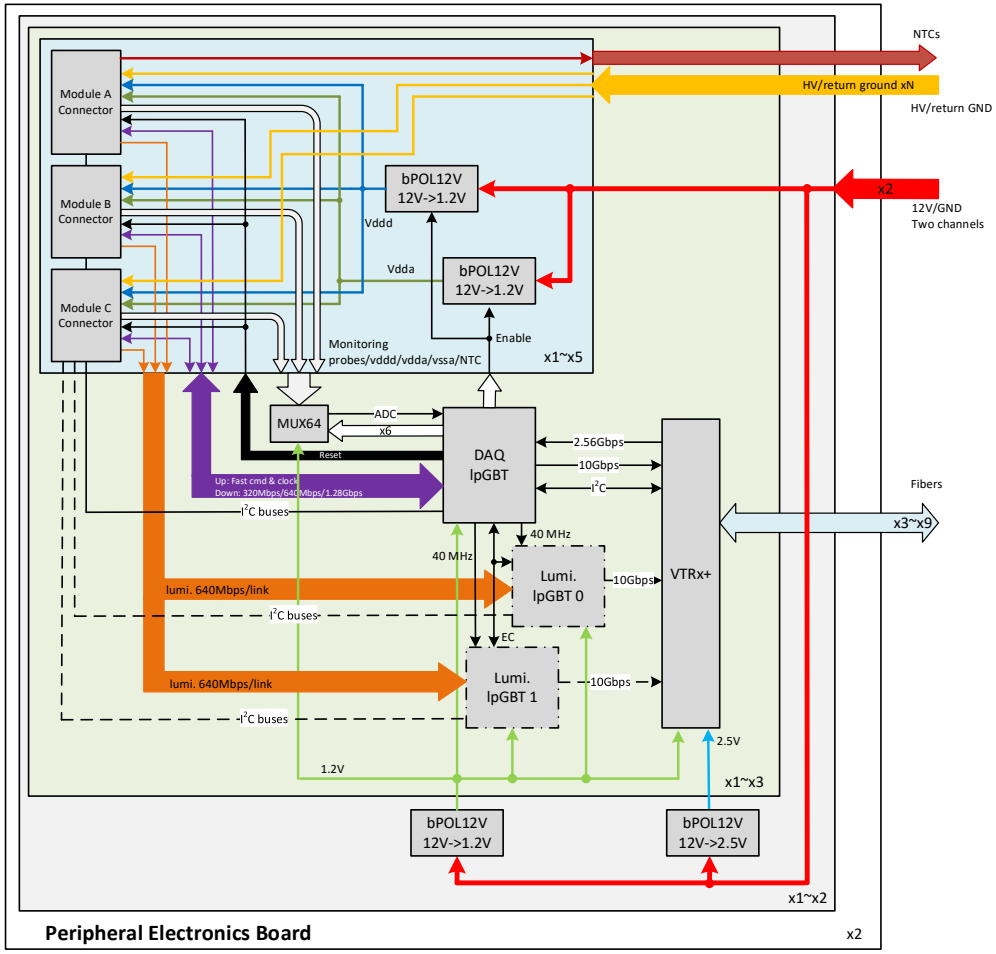
- **8.2.2.6 Monitor MUX**
  - A 64:1 multiplexer is developed by SMU to handle all voltages to be measured. Each multiplexer, which can switch the received voltages from up to 12 modules, is controlled by 6 I/O lines from one lpGBT.

From HGTD

- **8.2.2.7 DC/DC converter**
  - The peripheral electronics will contain DC-DC converters supplying the 1.2V and 2.5V required by the ALTIROC ASICs, the lpGBT ASICs and the Versatile Link.
- **8.2.2.4 lpGBT**
  - The Low Power Giga Bit Transceiver (lpGBT) is developed by CERN for the LHC upgrades. It is a radiation tolerant ASIC that can be used to implement multipurpose high speed bidirectional optical links for high-energy physics experiments.
- **8.2.2.5 VTRX+ optical transceiver**
  - The VTRX+ optical transceivers, development within the Versatile Link plus project at CERN, handle four fibers for transmission and one for receiving.

From CERN

Conceptual design of PEB



- Two LV channels
  - Each up to 12A @ 12V
- Up to 3 modules share two bPOL12v
  - One for analog power, the other for digital power
- One TDAQ lpGBT and 1~2 luminosity lpGBTs share one VTRx+
- Control
  - I2C of lpGBT
    - Module and VTRx+ configuration
    - I2C0 of TDAQ lpGBT is connected to the VTRx+ only
  - Output
    - Module reset
    - Module power on/off
    - MUX64 channel selection
- Monitoring
  - ADC of lpGBT
  - Module state monitoring
    - VDDA, VDDD, GNDA, PROBE0/1(internal state and temperature), NTC
  - PEB state monitoring
    - lpGBT voltage, temperature
    - VTRx+ RSSI(average optical power of the received light) and NTC
    - bPOL12v temperature
    - On board NTC
  - Input of lpGBT
    - bPOL12v power good signal

bPOL12V:
provide the 1.2V analog and digital voltages for the ALTIROCs

lpGBT:
Bi-directional slow control and monitoring communication between the FELIX and the lpGBT is done via the IC and EC channels.

Each lpGBT has a 8 channel multiplexed ADC.
With ~7 modules/lpGBT, an external 64-to-1 MUX is required: **MUX64**