Timing Pixel Detector Status

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On behalf of Timing Pixel Detector Group

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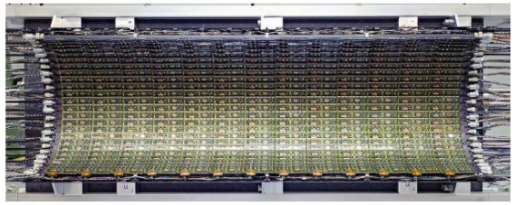
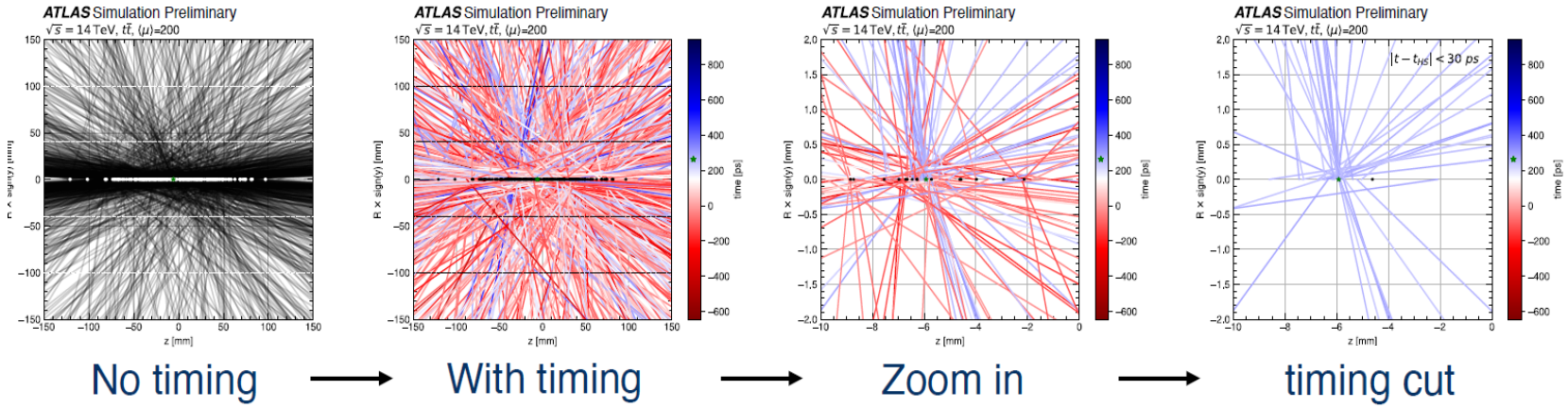
Contents

Introduction

- ATLAS experiment in HL-LHC: need to improve spatial resolution and radiation tolerance.
- HL-LHC: High Luminosity → Pile-up effects → High time precision
- Future: used for 4-D tracking, serving as a technological reserve for the next generation.

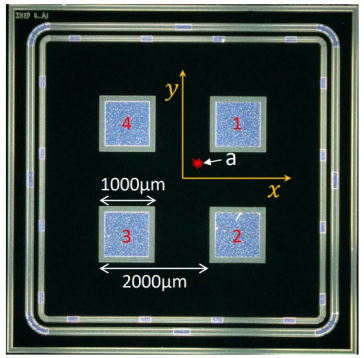


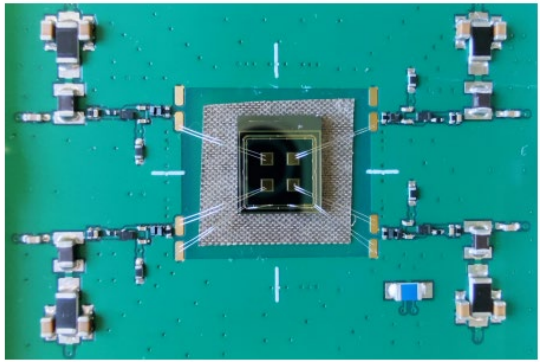


AC-LGAD R&D

➢ AC-LGAD R&D: pixelated AC-LGAD

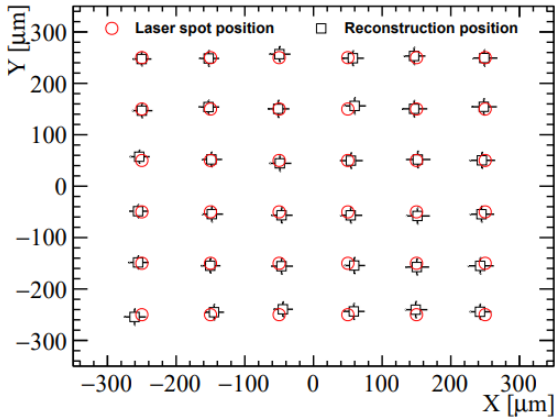
- Large pad-pitch size: 1 mm-2 mm
- To study the process parameter

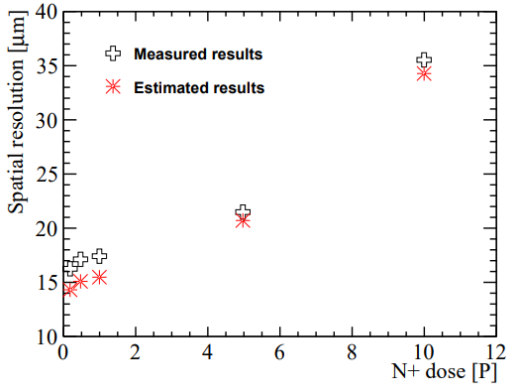




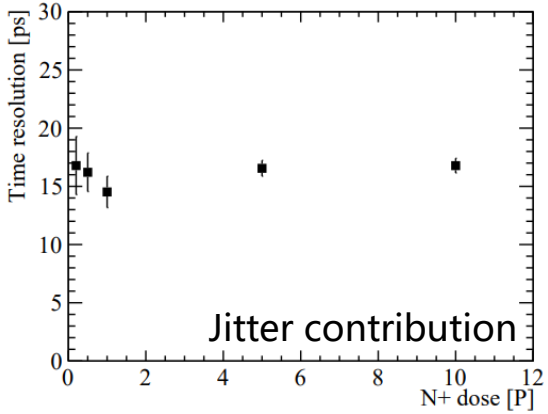
➢ Spatial resolution be better

- as decreasing the n+ dose (from 10 P to 0.2 P)





Spatial resolution: 15 μm



Timing resolution: 15-17 ps

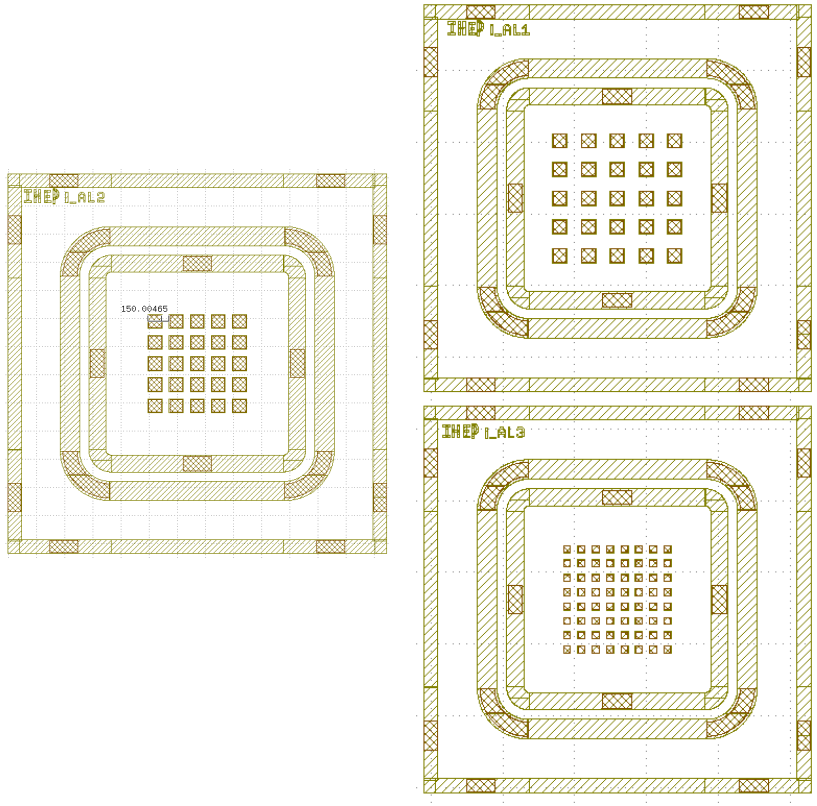
AC-LGAD new submission

- New design:

  Pixelated AC-LGAD with different pad-pitch size:

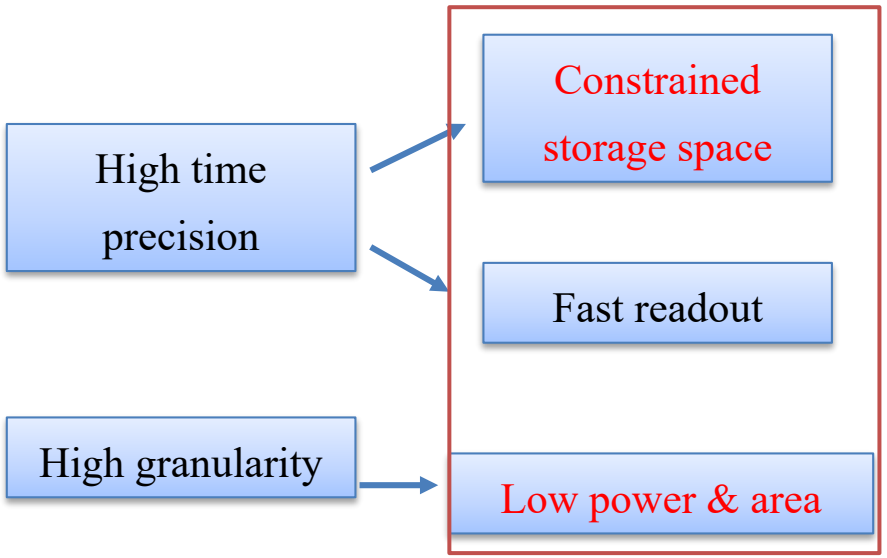
  50um-100um, 100um-150um, 100um-200um

- Submitted in March 2025
- Testing will be done after sensors be received on August 2025

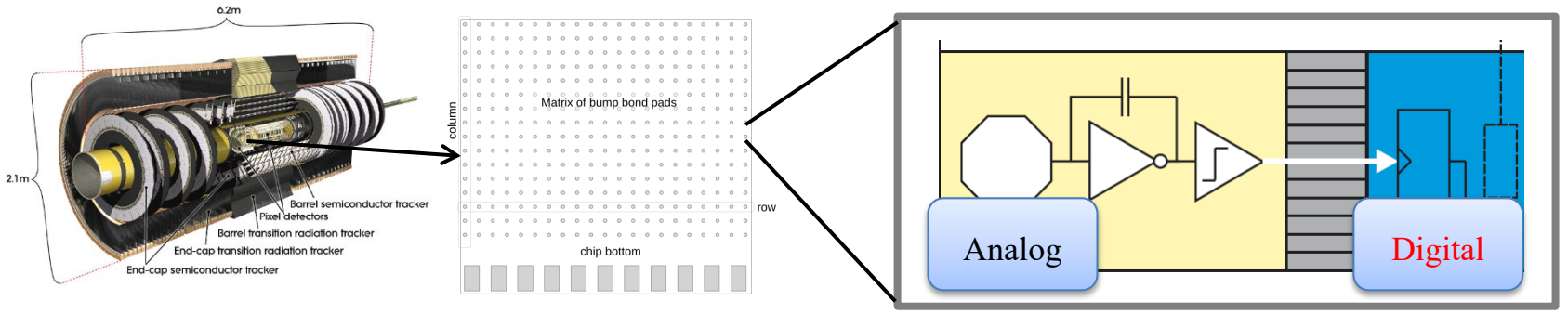


Electronics Design Targets

➢ Design challenges of digital ASIC:



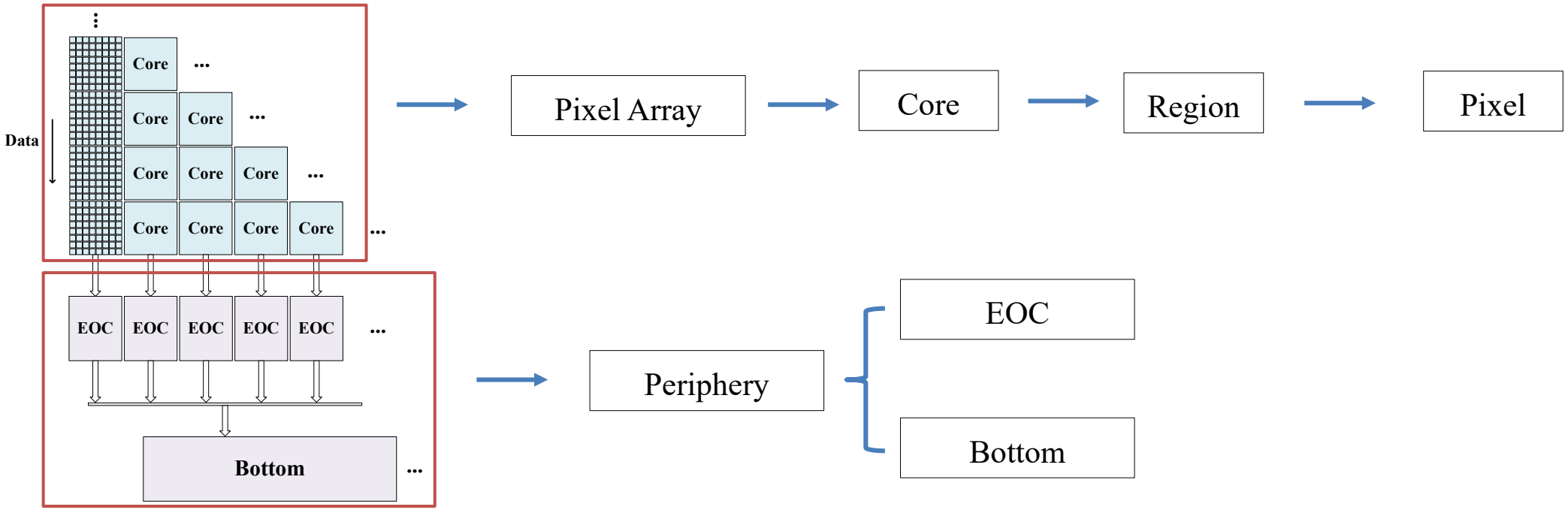
	Digital Index
ToA	<100 ps LSB @8 bits/hit
ToT	4 bits/hit
Hit rate	~75 kHz/pixel
Trigger latency	10 μs
Trigger rate	1 MHz



Overview

➢ Modules for the Readout ASIC:

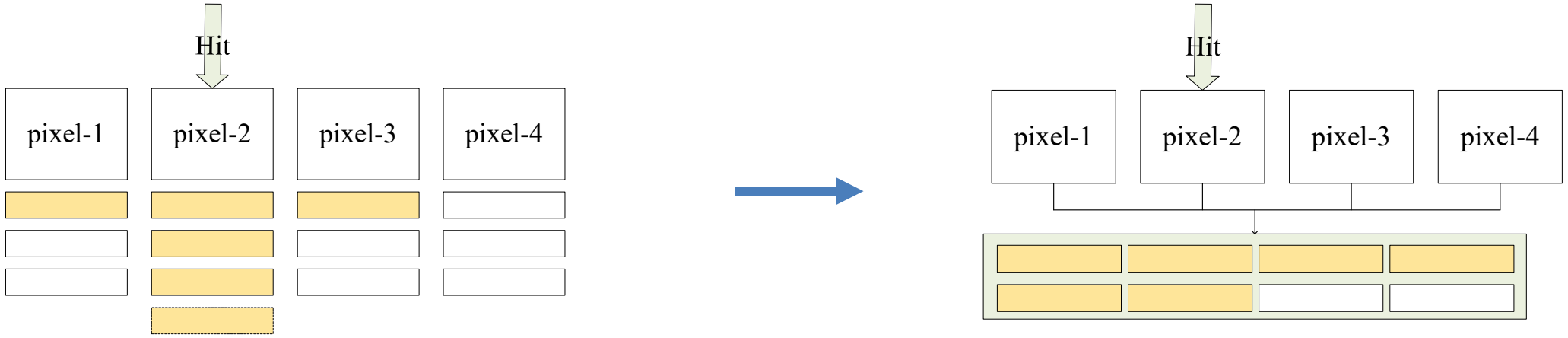
- Cores Array: 1 core includes 8×8 pixels, the cache and trigger matching of hit data
- End of Column: connects to the core array, the encoding and readout of hit data
- Chip Bottom: connects to the all columns, the concentration and output of hit data



Overview

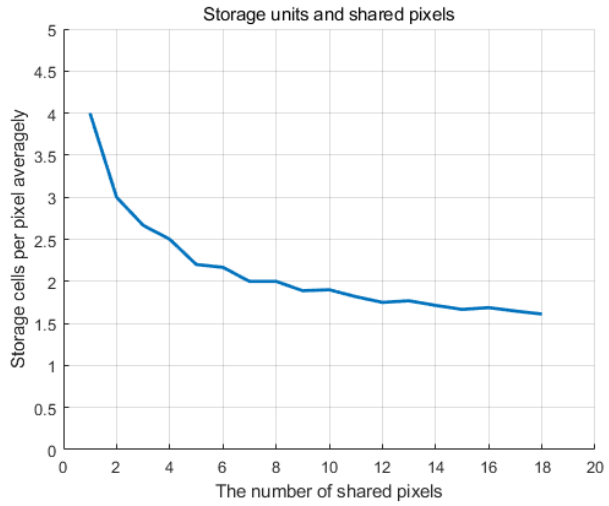
Core: shared memory

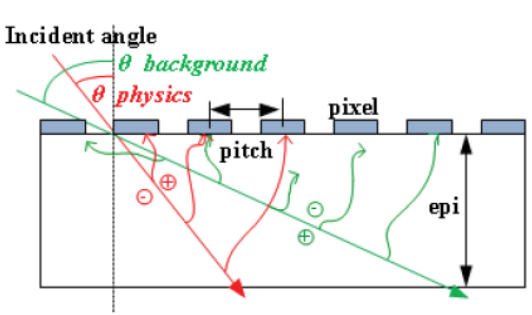
- Function: receiving and buffering data from TDC, and processing the trigger matching.
- Each core is same as others and they are connected in cascade.
- Shared memory: reduce storage space significantly

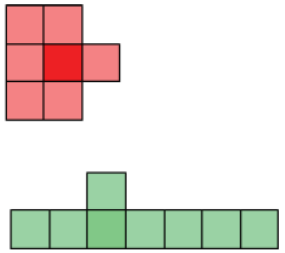


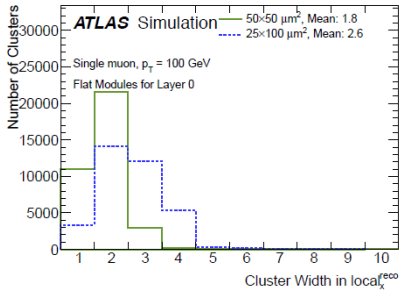
Core: shared memory

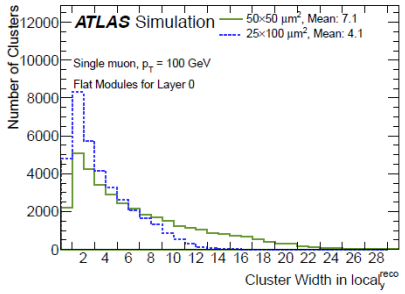
- Shared memory structure:
  - ◇Reduce storage space significantly
  - ◇Different position with different clusters
  - ◇Different interleaved grouping
    - →Eliminate the cluster in the neighboring pixels







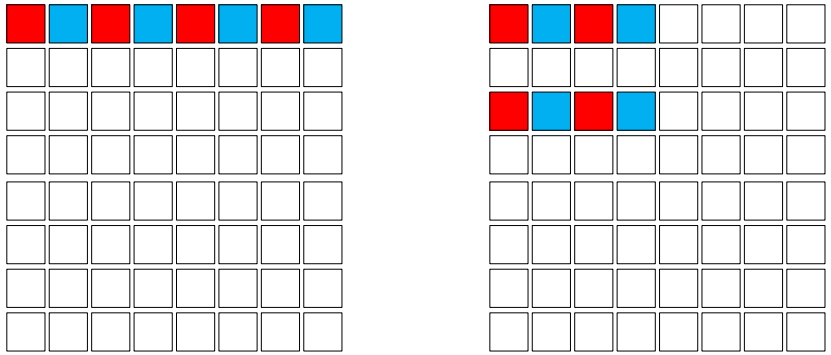




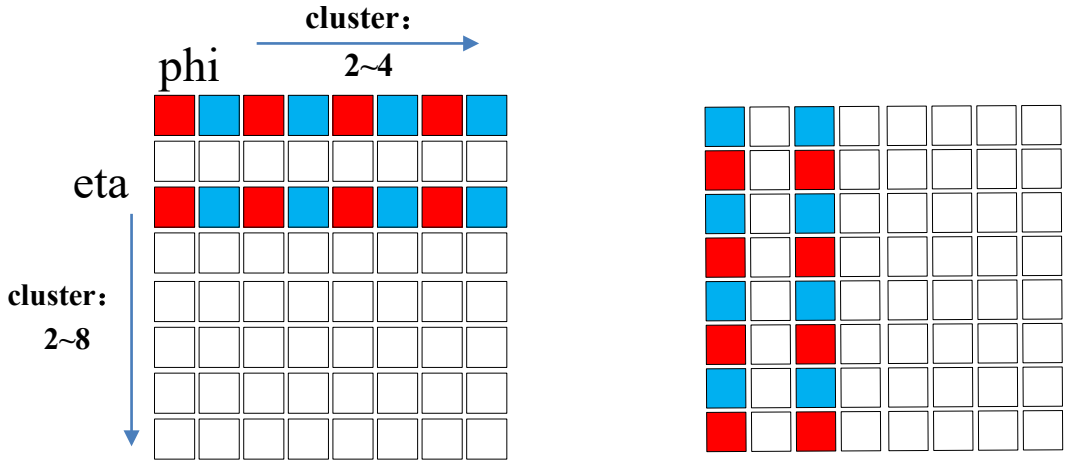
The cluster size

Core: shared memory

- According to hit data simulation, we compared different shared map (different shared pixels with different grouping in different position of the detector.)



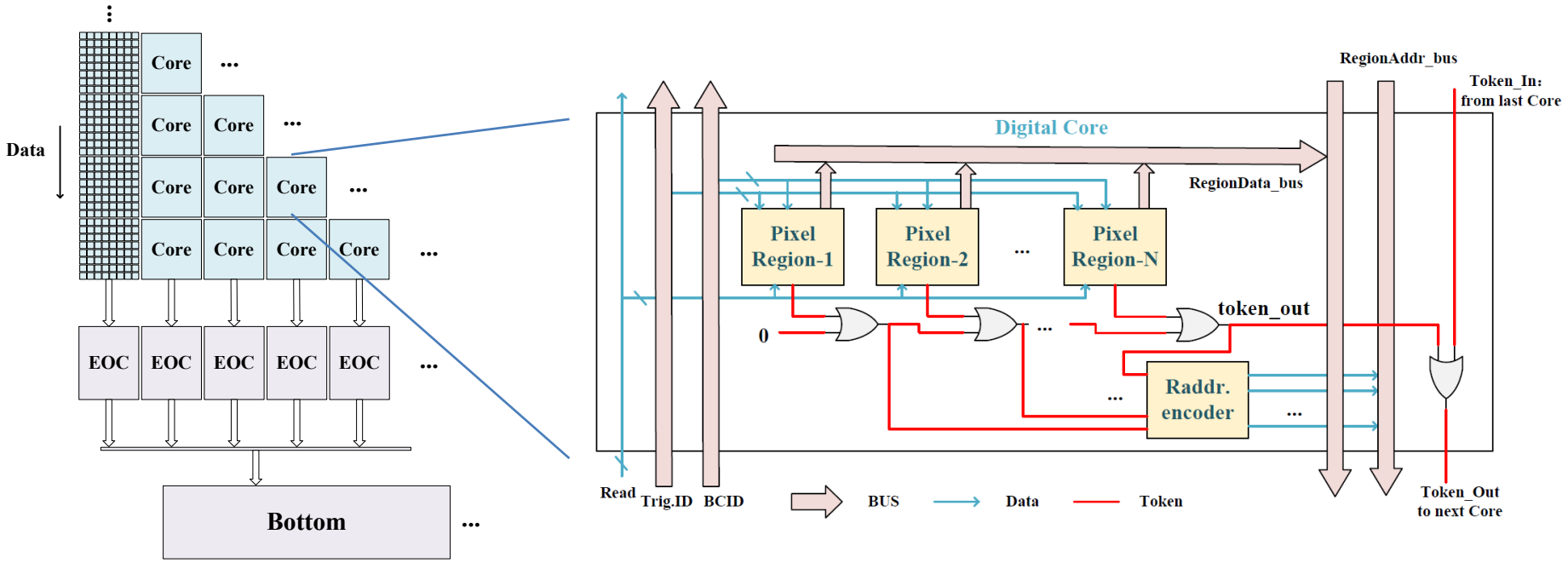
4 pixels



8 pixels

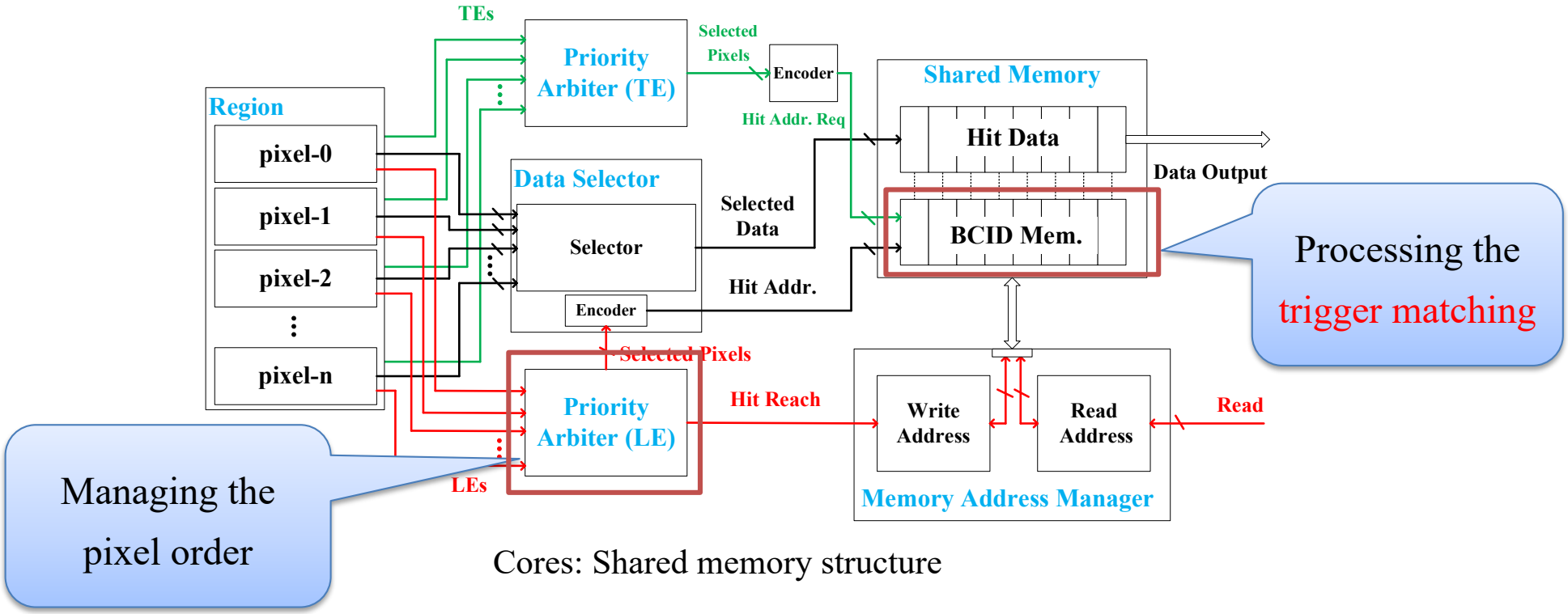
Core: core design

- All cores are connected in a chain.
- Global signals and data bus are spread by this chain in the core column
- In the core, there are several regions are connected in a chain.



Core: region design

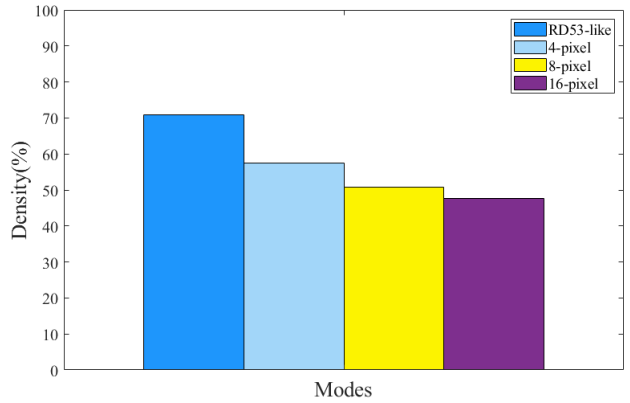
- Every region shared one memory.
- Two priority arbiter for LEs and TEs, to manage the address of memory
- Every cell in shared memory need a FSM to process trigger matching



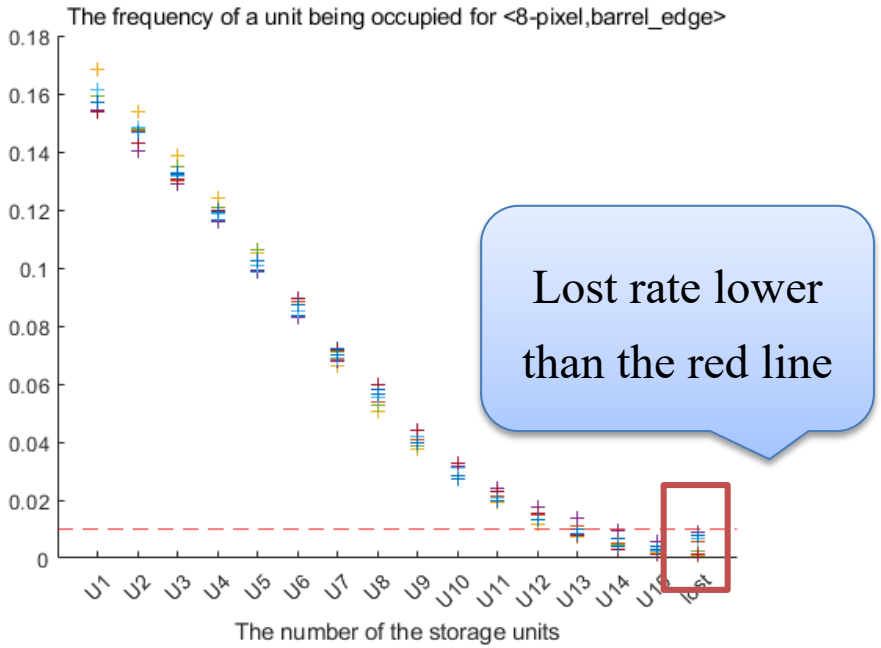
Cores: Shared memory structure

Core: simulation

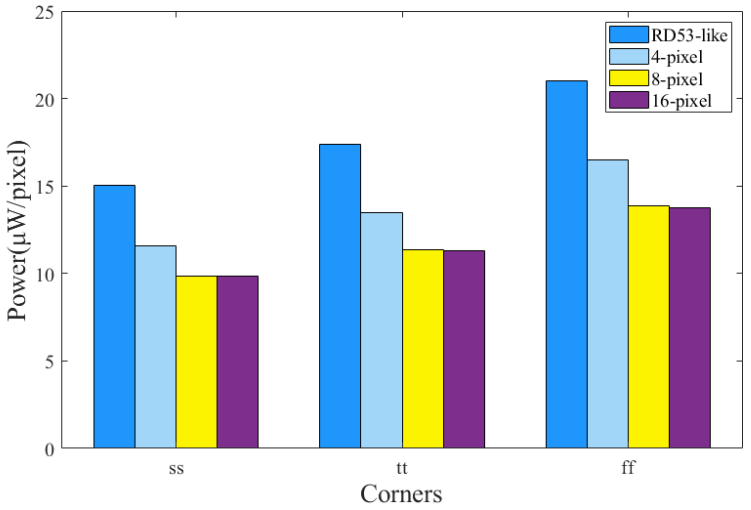
- The cores' results (in130 nm):
  - Lower density and handling high data rate
  - Lower power
- Conclusion: shared mem. can reduce power and area obviously.



The area comparison



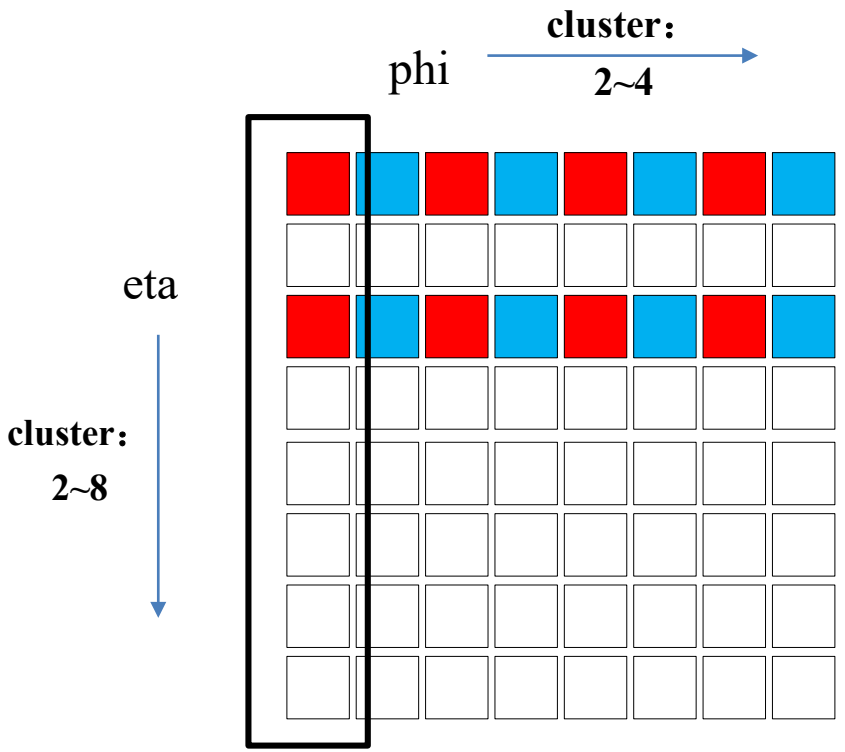
The performance of caching



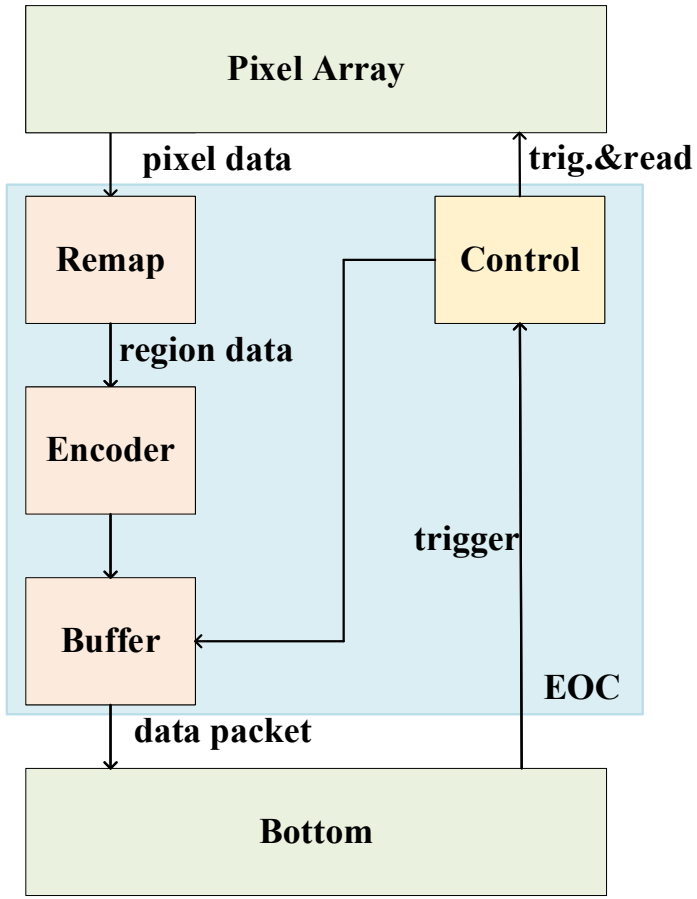
The power comparison

EOC

- EOC: controlling the readout of cores, and packaging the hit data
- Packaging the data according to physical position can reduce the data bits. It also can compressing the hit map.
- Cluster size: Packaging data along the *eta* direction is the most useful way (black box),
- Pixel data: read by shared map (not neighboring, red & blue square)
- Remapping: turning shared map into physical map (necessary).



EOC: Remapping and encoding

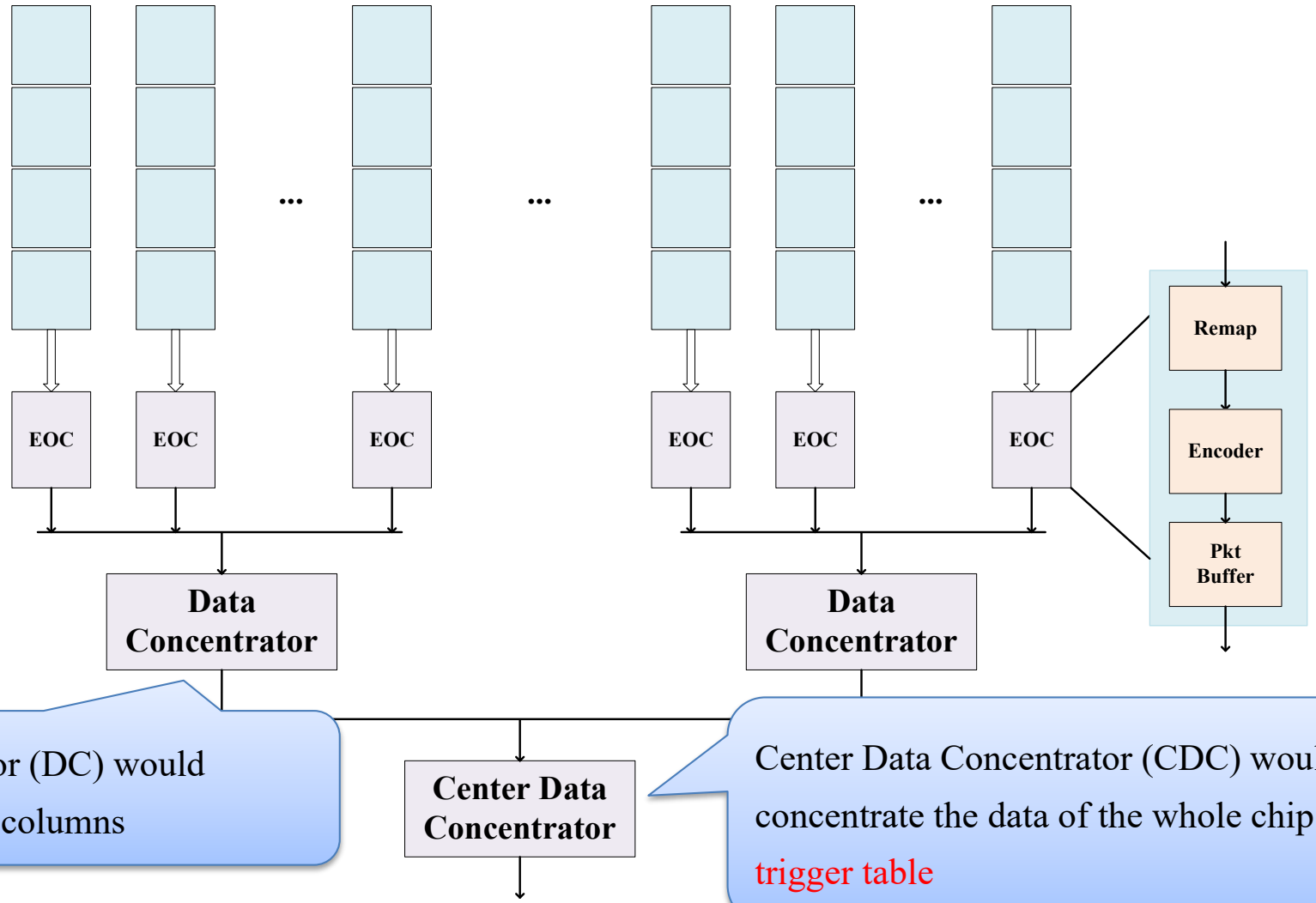


End of Column

- Encoding: when data is packed together, the hit map can be compressed.
- Hoffman: according to the frequency of hit map, the entropy is the least.

Encoding of hit map		Entropy
Bitmask		8
Binary-tree		4.74
Independent address		6.89
Multi-step Hoffman	4-6-14	4.27
	2-6-14	4.86
	3-6-14	4.10

Bottom

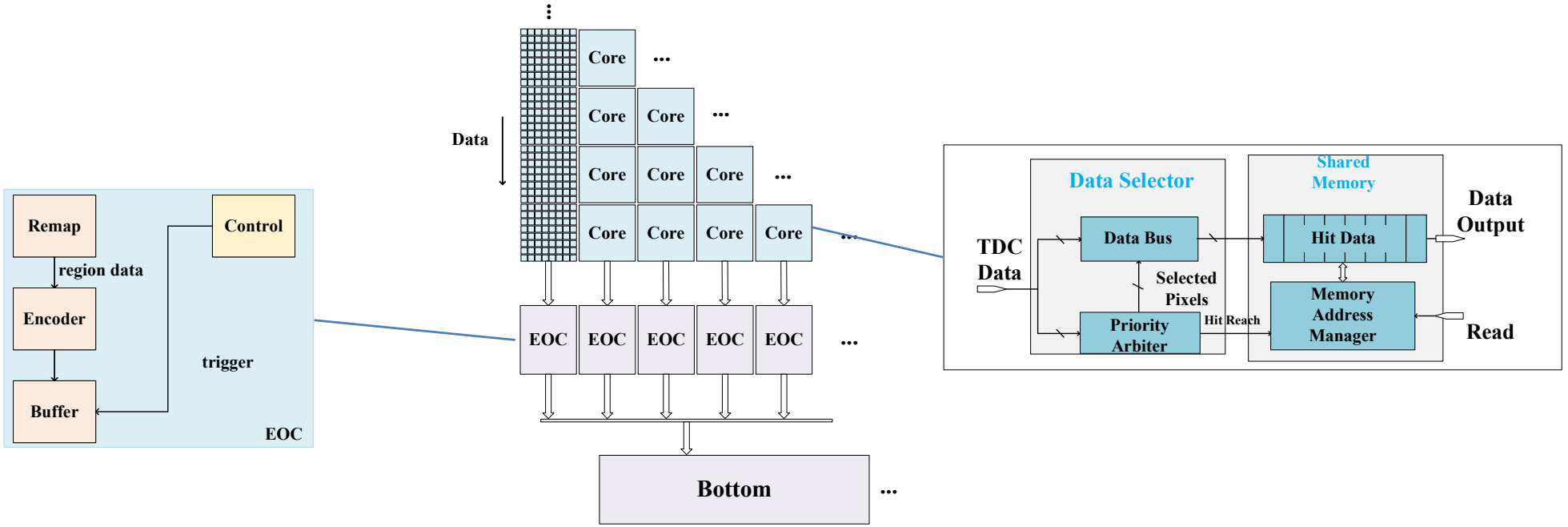


Every Data Concentrator (DC) would receive the data from 8 columns

Center Data Concentrator (CDC) would concentrate the data of the whole chip. It has a trigger table

Summary and Plan

- Sensors: AC-LGAD pixelated sensors with large pitch is tested and new submission of AC-LGAD designed with smaller pixel size is under fabrication.
- Electronics: the scheme of the chip has been designed (digital part): Pixel array, EOC, Bottom



Timetable and milestones

1、年度：2023 年 12 月—2024 年 5 月

任务：测试硅微条传感器关键性能，掌握模块生产全部流程。开展时间像素探测器文献调研，分析明确设计需求。

考核指标：通过硅微条模块站点考核。确定时间像素探测器技术路线。

成果形式：硅微条探测器国际合作组内部评审报告，时间像素探测器内部报告。

2、年度：2024 年 6 月—2024 年 11 月

任务：测试读出芯片关键性能，开始制备长硅微条模块，在卢瑟福实验室完成多桶板小系统联调测试，在 CERN 搭建桶板接收测试系统。完成时间像素探测器传感器与前端电子学整体架构设计和功能模块划分。

考核指标：研制出合格的长硅微条探测器模块，完成时间像素探测器技术设计报告。

成果形式：长硅微条探测器模块合作组内测试报告，时间像素探测器技术设计报告。

3、年度：2024 年 12 月—2025 年 5 月

任务：测试传感器、芯片在不同辐照条件下的性能表现，制备长硅微条模块。时间像素探测器完成传感器增益层设计与第一版原型验证电路功能层级设计。

考核指标：完善长硅微条探测器模块研制流程，完成时间像素传感器增益层与验证电路功能层设计验证。

成果形式：长硅微条探测器完整流程优化合作组内报告，时间像素探测器初步设计验证报告。

- 2024-11: Architecture design and functional module division ——completed
- 2025-5:
  - Gain layer of sensor ——completed
  - Functional design of the electronics ——completed
- Tape-out plan:
  - New submission of AC-LGAD is under fabrication, taped out in August this year
  - Complete the physical design of the entire chip, adding the analog part, in the second half of this year.
  - Tape out at the beginning of next year, in the 130 nm process (SMIC in China).

Thanks

Backup

课题目标、预期成果与考核指标表

课题目标[1]	预期成果			考核指标[2]				考核方式（方法）及评价手段[4]
	预期成果名称		预期成果类型	指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态	
在高颗粒度时间探测器方面，研发硅传感器、前端电子学、探测器模块组装等，研制出高时间分辨率的探测器模块与前端读出电路板，其时间分辨率好于 50 皮秒。	主要成果 1	硅径迹探测器模块	□新理论 □新原理 □新产品□新技术□新方法 □关键部件 □数据库 □软件 □应用解决方案 ■实验装置/系统□临床指南/规范□工程工艺 □标准 □论文 □发明专利 □其他	硅微条径迹探测器空间分辨率（关键核心指标）	原型模块 25 微米	预生产模块 25 微米	径迹探测器 25 微米	测试报告、同行评审。
	主要成果 2	有时间信息的硅像素探测器	□新理论 □新原理 □新产品□新技术□新方法 □关键部件 □数据库 □软件 □应用解决方案 ■实验装置/系统□临床指南/规范□工程工艺 □标准 □论文 □发明专利 □其他	硅像素探测器时间分辨率（关键核心指标）	好于 10ns	好于 1ns	好于 100ps	仿真验证和实验室测试，测试报告

科技报告考核指标	序号	报告类型[5]	数量	提交时间	公开类别及时限[6]
	1	课题年度技术进展报告	1	2024 年 12 月	公开
	2	课题中期技术进展报告	1	中期检查前	公开
	3	课题年度技术进展报告	1	2026 年 12 月	公开
	4	课题年度技术进展报告	1	2027 年 12 月	公开
	5	课题最终技术进展报告	1	2028 年 12 月	公开
其他目标与考核指标					