Develop FPGA-Based 144-Channel DAQ in RPC Phase-II Upgrade

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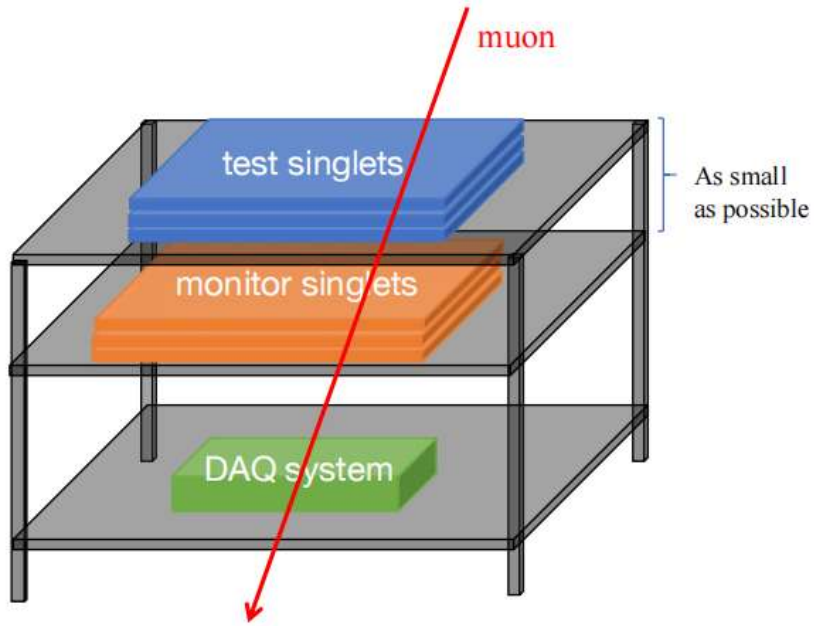
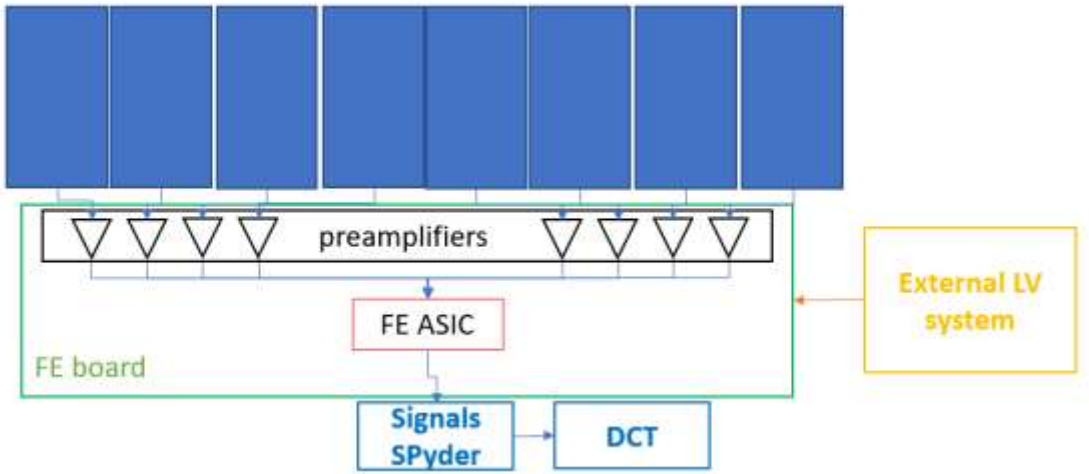
Outline

- Motivation
- FPGA-Based 144-Channel DAQ design
  - Hardware design
  - Principle diagram in FPGA
  - Software
- Performance of the TDC
  - Test with the signal generator
  - Test with RPC detector
- Summary

Motivation: Cosmic ray test in RPC production

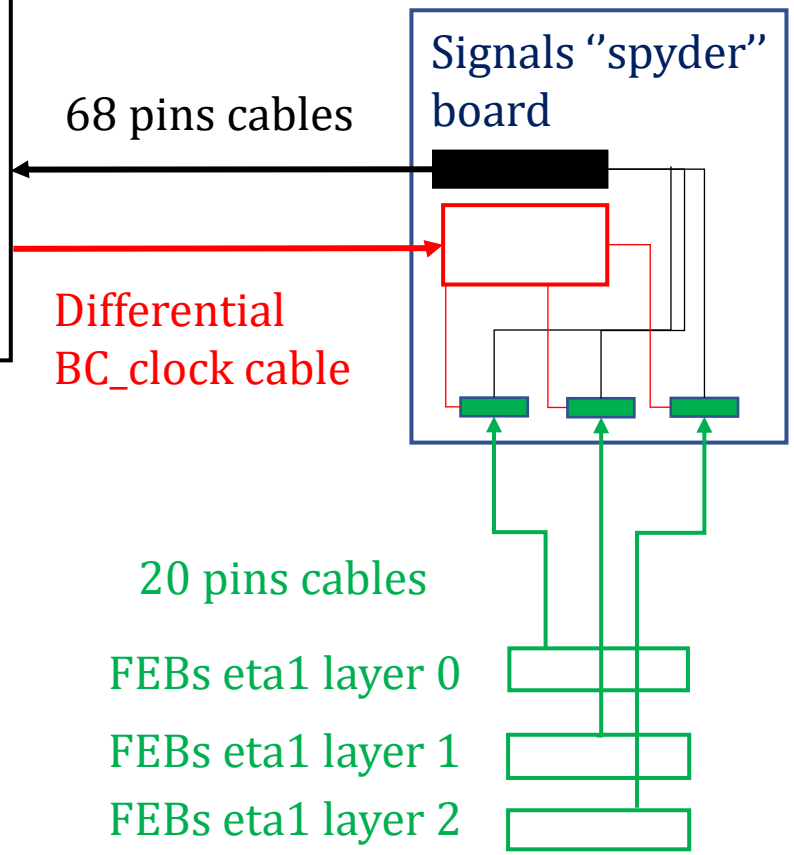
- Monitor singlets
  - used for trigger
  - 2/3 coincidence
  - the largest size of BIS singlets (Type BIS-1, 6 FE boards width)
- Test singlets
  - different types to test → Align with monitor singlets
- Advantages
  - can operate the test singlets easliy
  - monitor singlets are very close together → a better triggering rate (try to accept all hit angles)
- DAQ design goals
  - 288 channels
  - TDC function with backup chip
  - or Manchester decoder with baseline chip
  - three trigger modes: external/self/master-slave

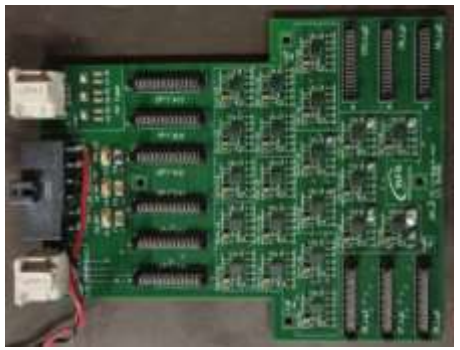




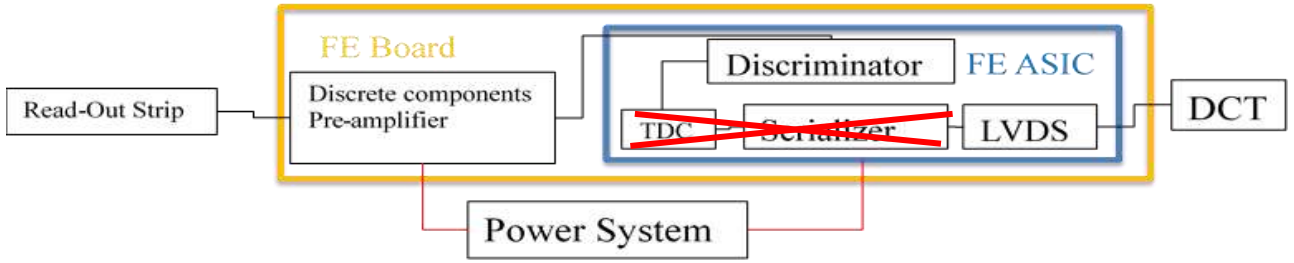
Overall signals system

DCT;
Located or directly on the chamber or maximum at 3.5m distance, depending on the ATLAS sector





Low voltage board



Signals ''spyder'' board

- The Signals ''spyder'' board is an adaptor board with 4 connectors.
- Located directly within the service boxes of the detector
- It couples in a single **68 pins** cable the signals of 3 FEBs of a readout panel column

Front-end board

- Backup solution
- 20 pins connect with spyder board
  - 16 differential output (not LVDS)
  - 1 discriminator_OR 1.3LVTTL
  - 3 GND

Low voltage board

- Power supply for FE
- Vth / Vdigital / Vamp / Vpol

DAQ hardware design

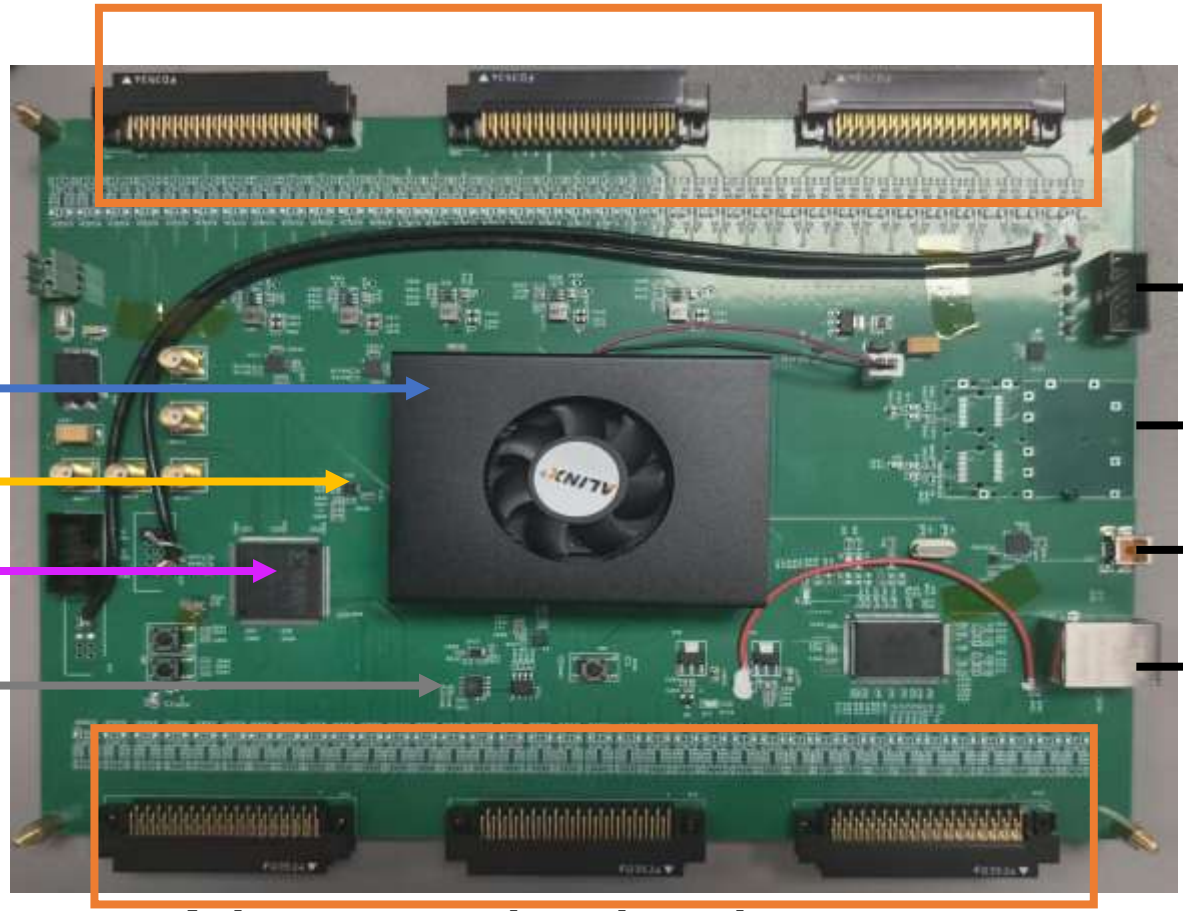
Receive data from FE board
18 FE boards = **144 channels** in total.
Integrates 144 channels **polarization circuitry**. Capable of receiving signals from **baseline or backup FE**

Xilinx KINTEX UltraScale: XCKU060
Central processing and control
Manchester decoder or TDC

Clock buffer
40 MHz LVDS clock output from FPGA.
Split into 2 channels,
then further distributed into 18 channels.

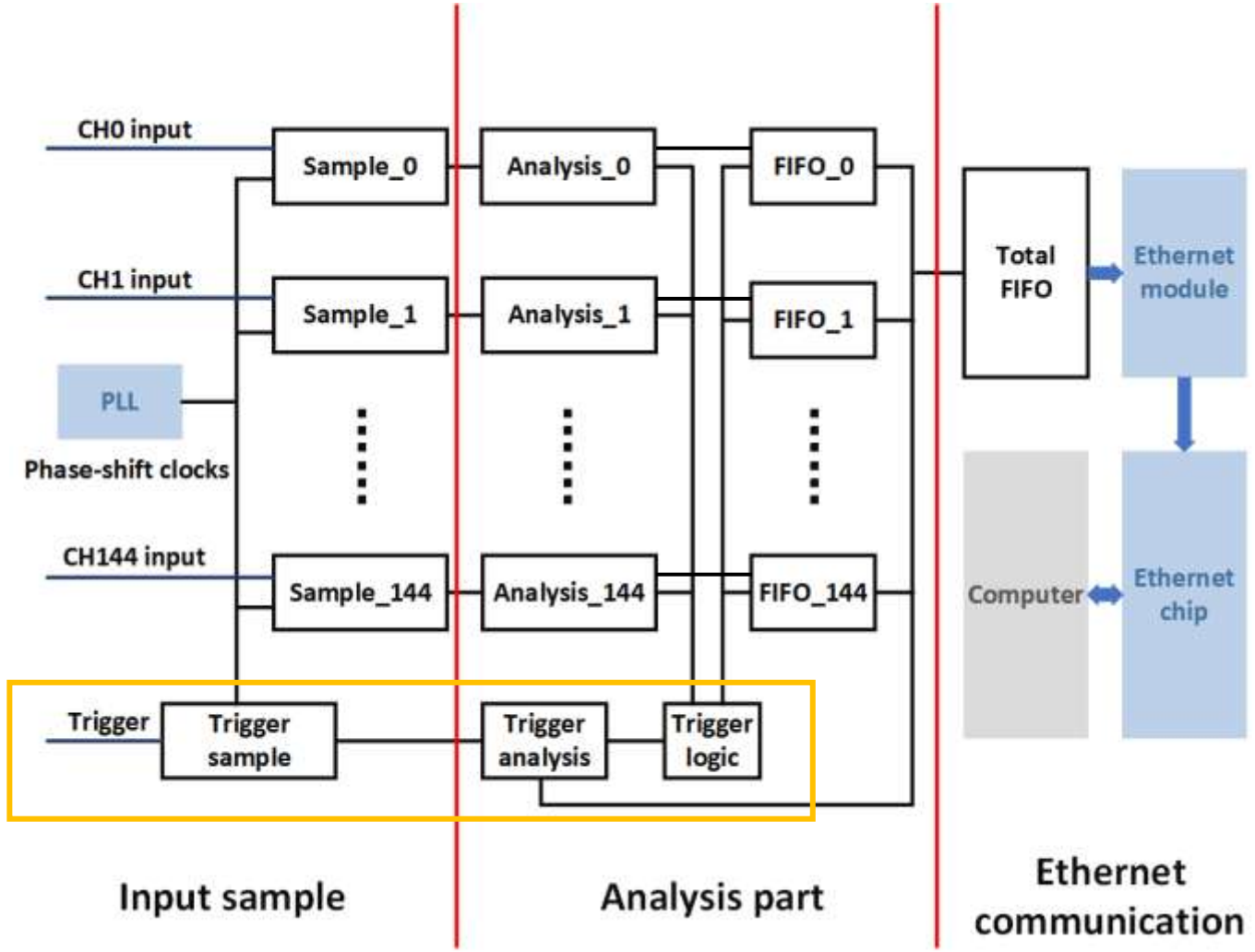
CPLD:XC95144XL
Processes 18 fast_or signals from FE board.

Other
Temperature sensor, SMA, buttons, fan, **cascading signals** between two boards, and etc.



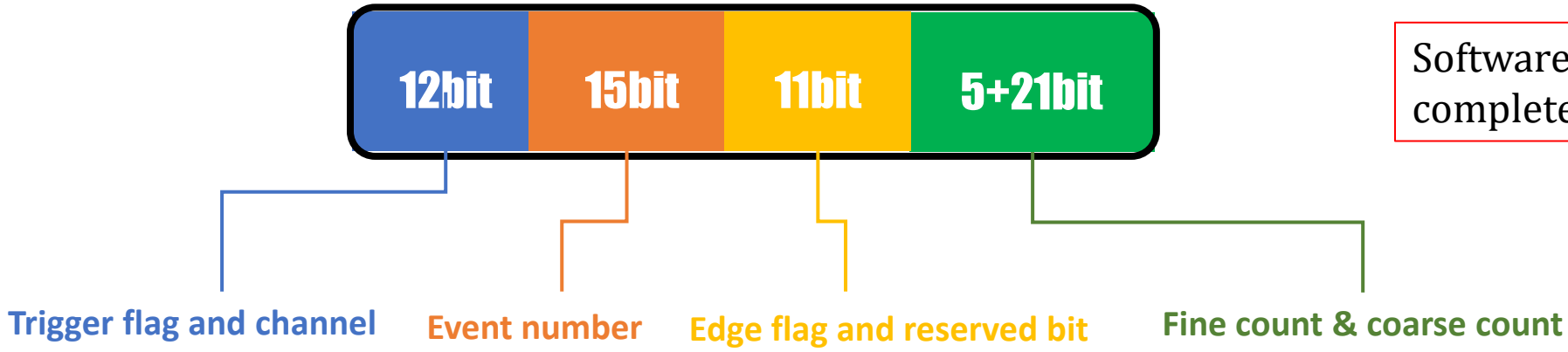
Principle diagram in FPGA

- Input sample part
  - Phase shift sampling clock: 500MHz
  - 8 bit thermometer code
- Analysis part
  - 8 bit → 3 bit fine count
  - Analyze edges → time information
- Trigger logic
  - External/self/master-slave
- Ethernet communication part
  - Transfer the data to the total FIFO
  - Gigabit Ethernet



Software design

❖Data structure: 64 bits

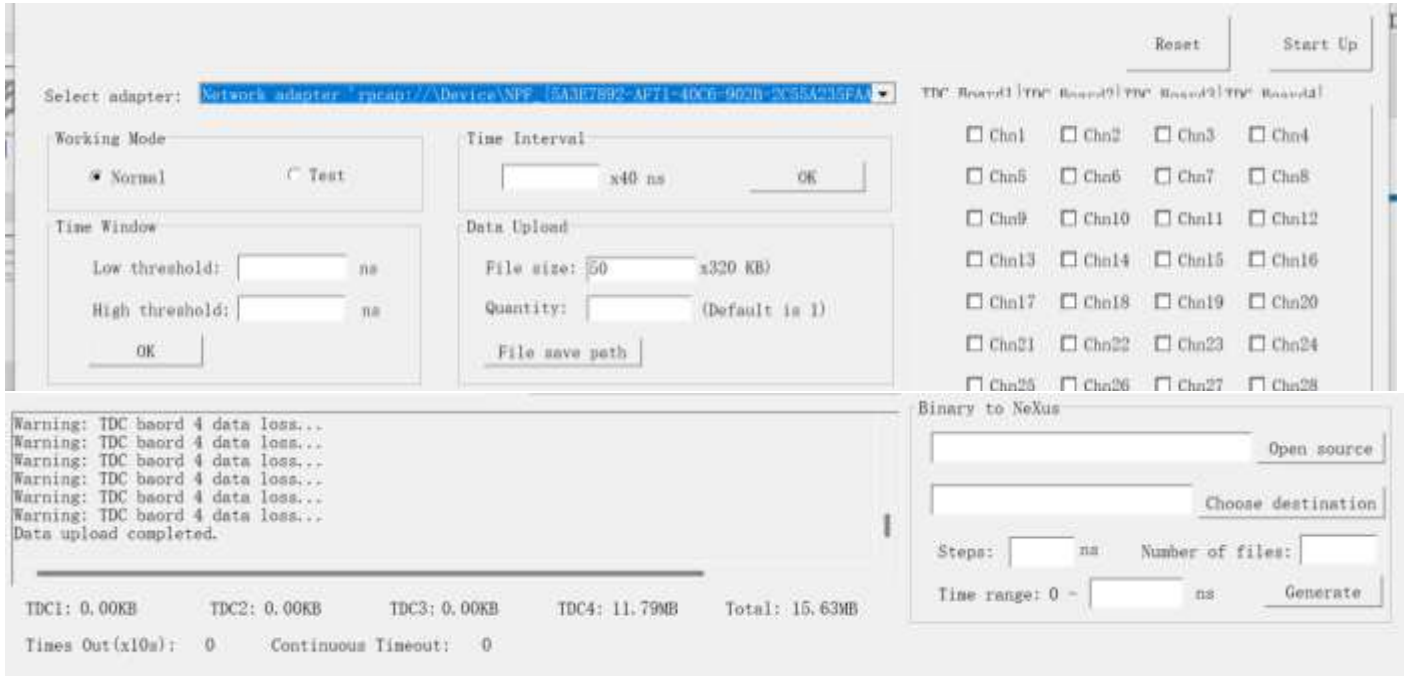


Software design needs to be completed before September.

❖Software interface

- ✓Select file save location
- ✓Save bin file
- Save root file
- Compatible with Windows and Linux

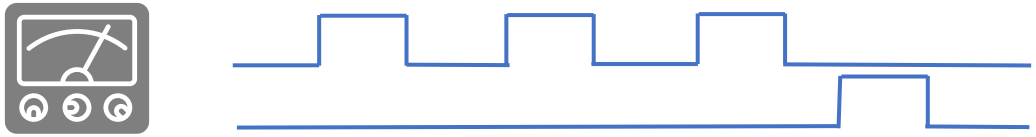
❖Online monitor



Performance: time resolution

❖Test setup

- Two pulse signals as trigger and stop



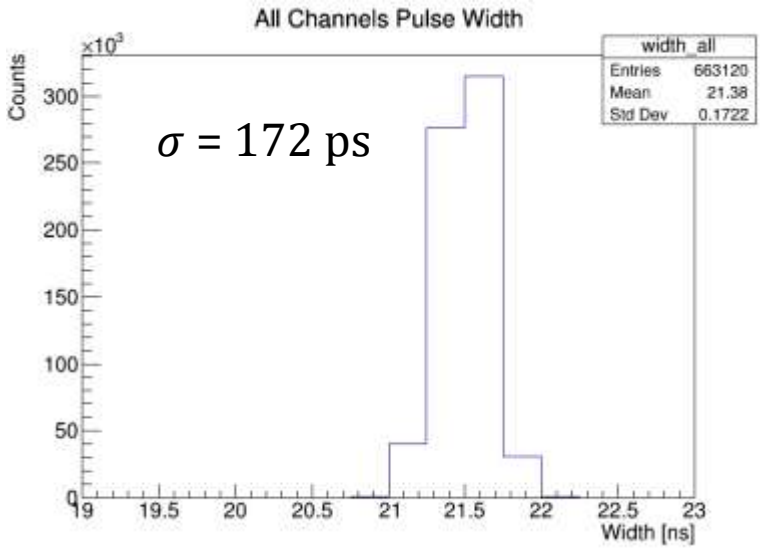
Width: 21ns
Trigger delay: 400ns

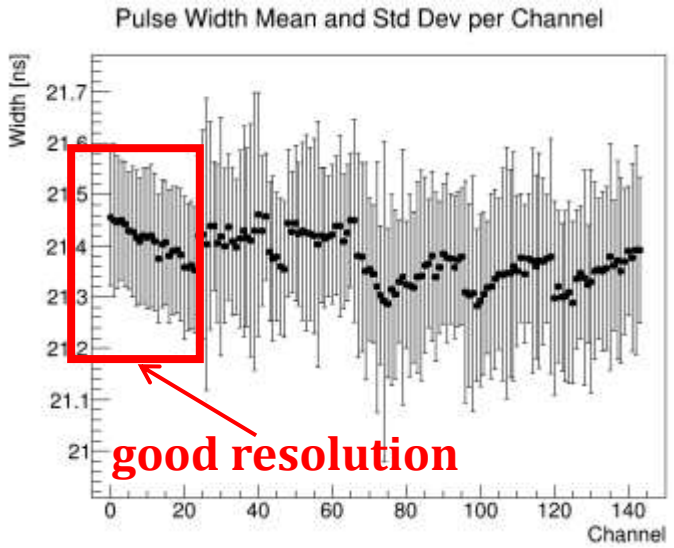
Period: 0.05ms
Period: 0.2ms

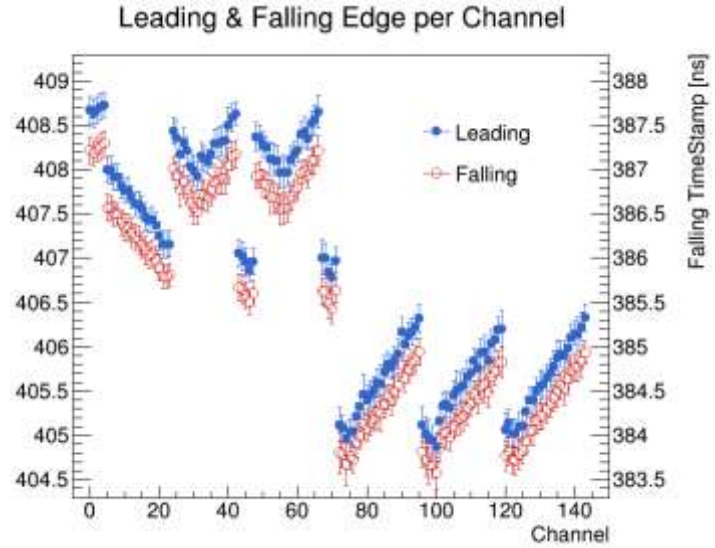
- Standard deviation is the time resolution

$$\sigma = \sqrt{\frac{LSB^2}{12} + \sigma_{time}^2 + {\sigma_C}^2 + \frac{{\sigma_L}^2}{4}}$$

❖Test results







❖Conclusion: Some channels meet the time resolution requirement, but further optimization is still needed.

Performance with RPC detector: setup

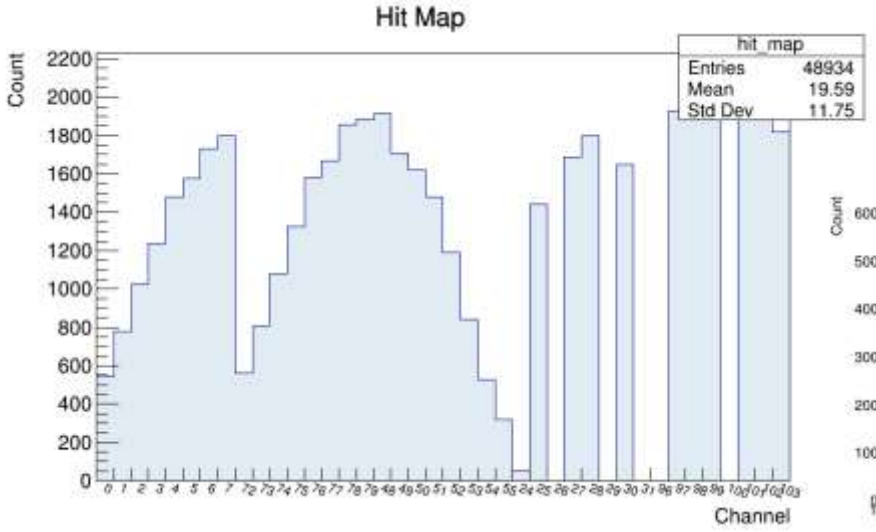
Trigger System: three scintillators operate in coincidence to generate the external trigger signal.

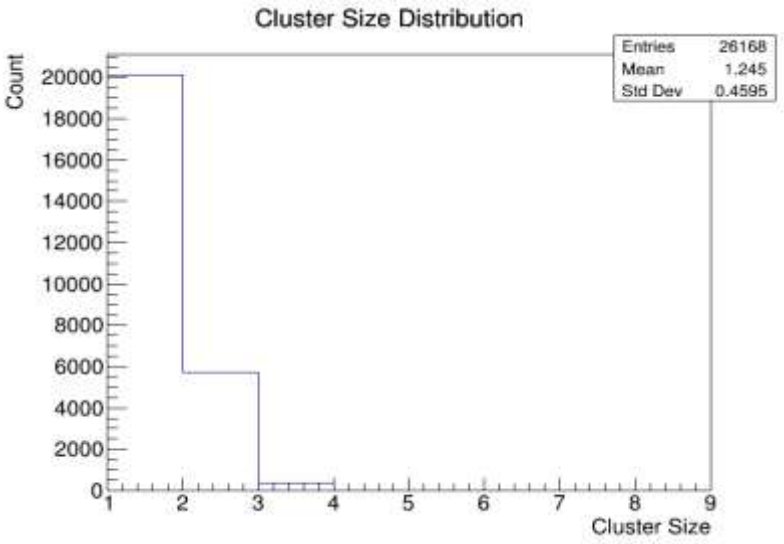
RPC Configuration utilizes two RPCs:

BIL: standard RPC

BIS: implements eta-eta readout

Results





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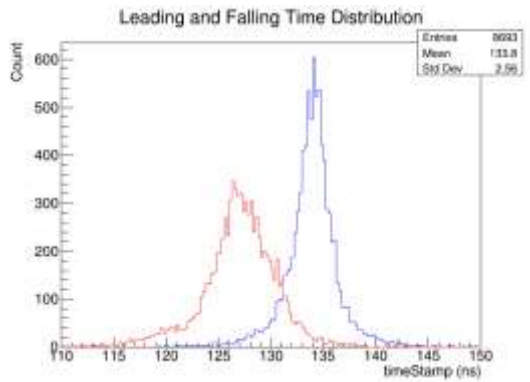
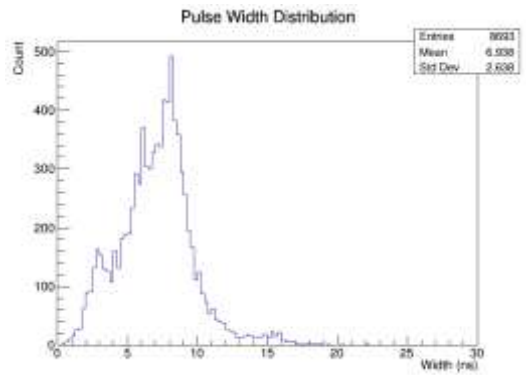
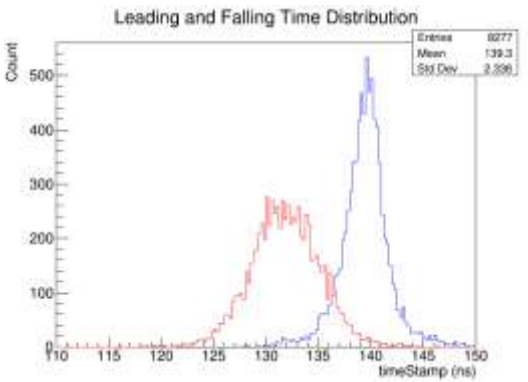
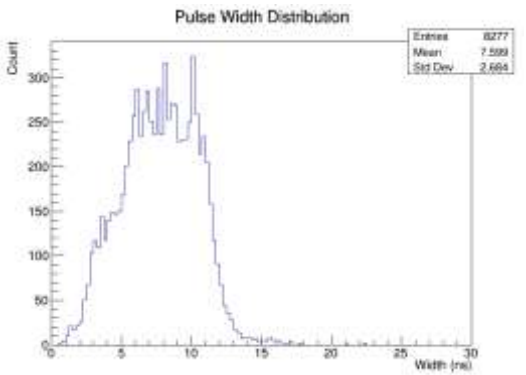


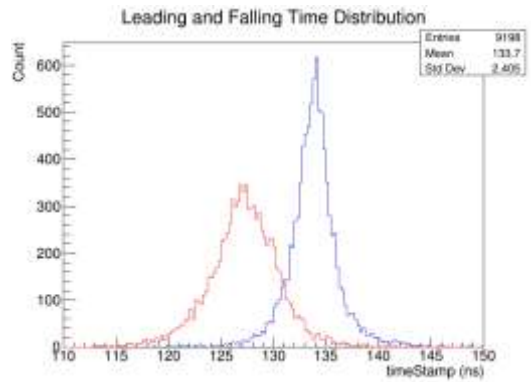


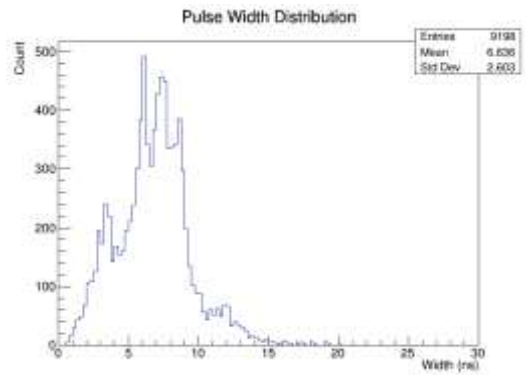
ch 48-55





ch 72-79





Conclusion: current test results are consistent with expectations, and the DAQ system can realize TDC function, data taking and transmission.

Summary and Plan

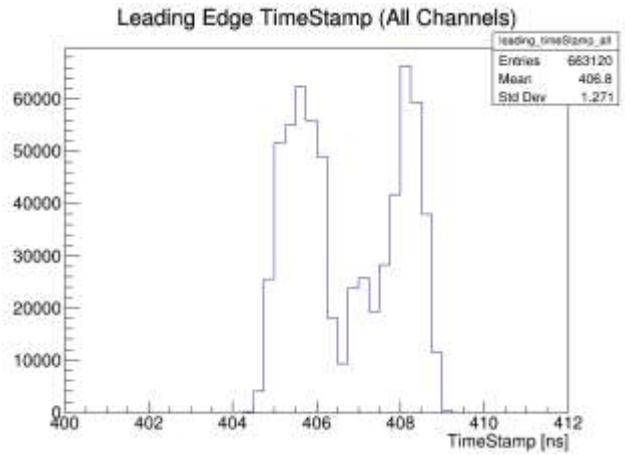
- **Hardware architecture**: passed initial validation, no critical issues observed.
- **TDC module**: key functions verified, optimization in progress.
- **Readout system**: full-chain testing pending.
- Next step:

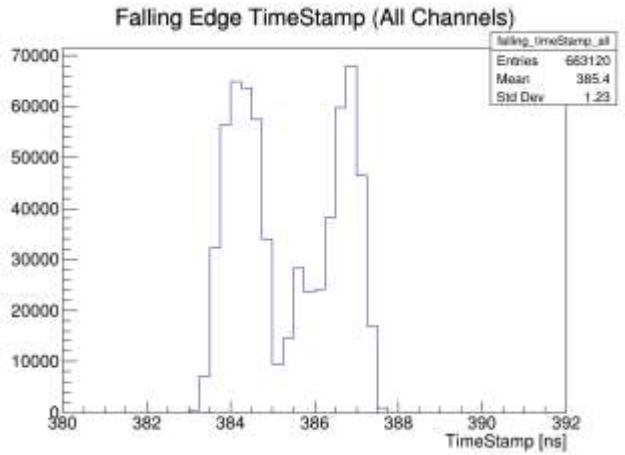
  Test with multi-DAQ boards

  Cosmic ray test in September at BB5

Back up

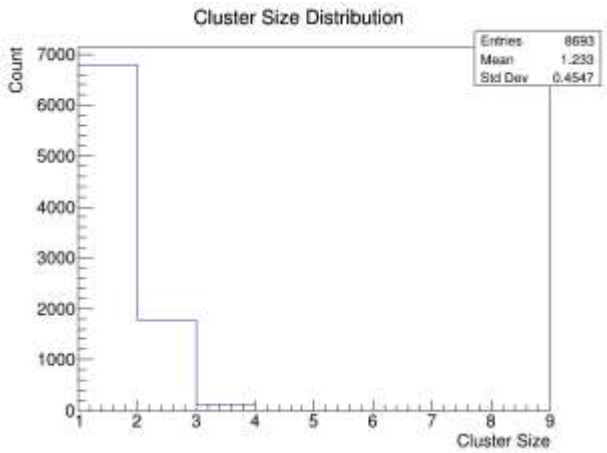
- leading and falling





Back up

- cluster size



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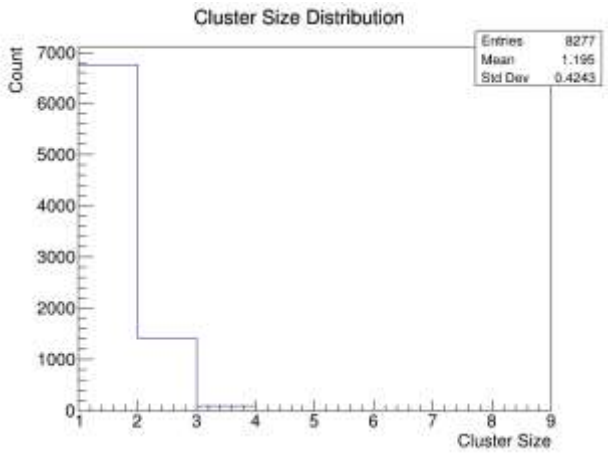

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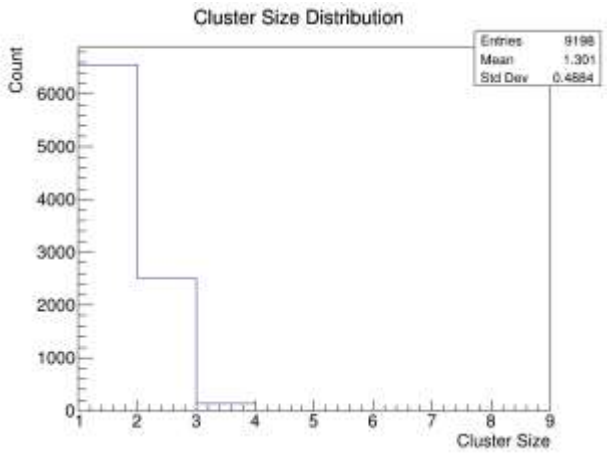

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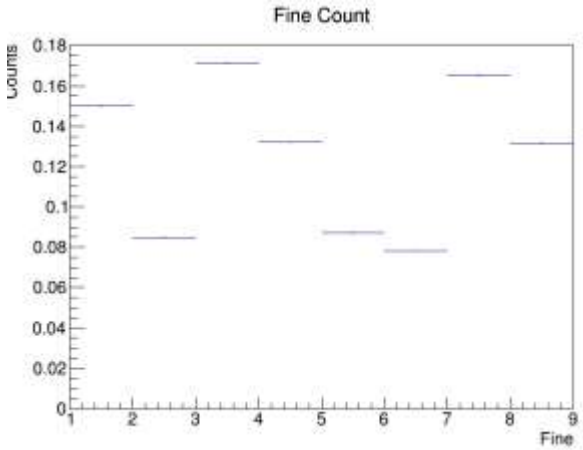
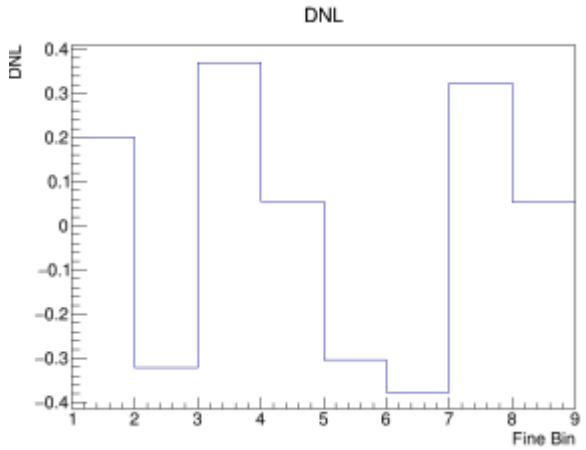
Performance with the signal generator: nonlinearity

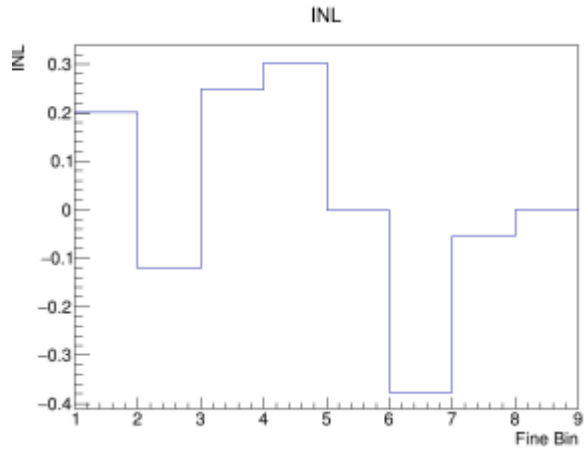
❖Test setup

The test setup used two clocks that were not completely independent. A retest is currently in progress; the previous results are shown below.

❖Test result







❖Conclusion

- Secondary contribution to σ
- Convenient method: offline modification

$$\sigma = \sqrt{\frac{LSB^2}{12} + \sigma_{time}^2 + {\sigma_C}^2 + \frac{{\sigma_L}^2}{4}}$$