Status of HGTD Peripheral Electronics Board

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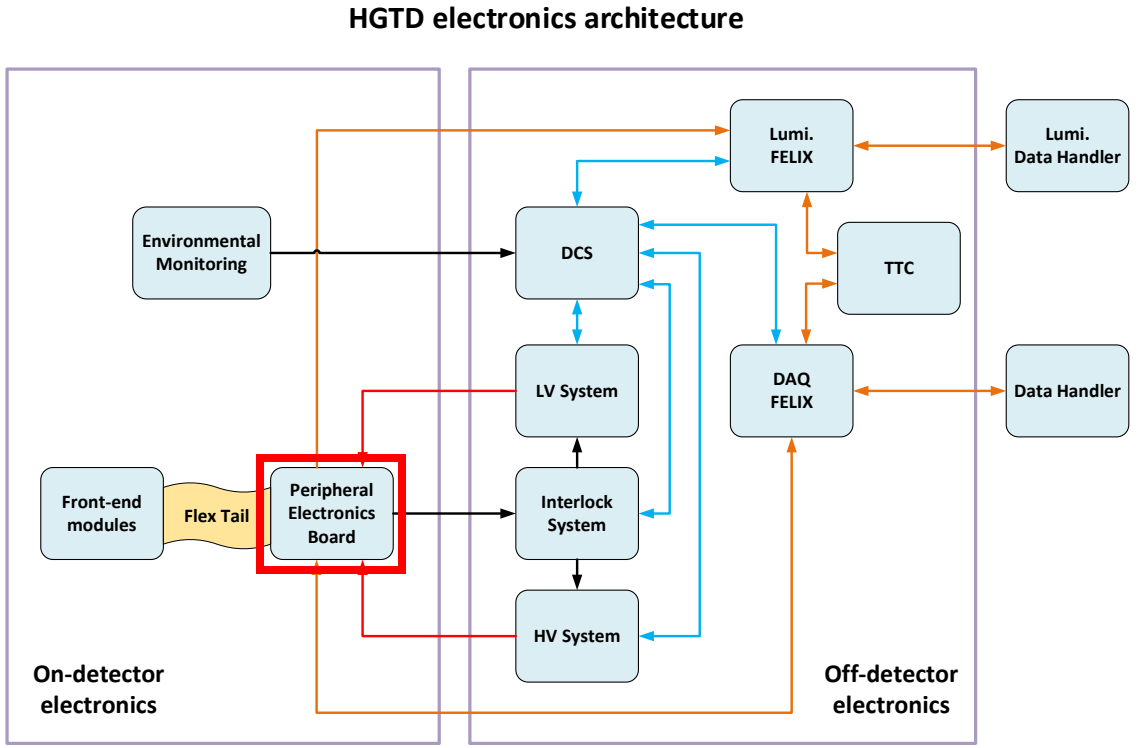
on behalf of the HGTD Electronics Team

June 7th, 2025

Overview of HGTD readout electronics

- On-detector Electronics
  - Front-end modules
  - Flex tail cables
  - Peripheral Electronics Boards (PEB)
- Off-detector
  - Data Acquisition System (DAQ)
  - Low Voltage (LV)/High Voltage (HV) system
  - Luminosity System
  - Timing, Trigger and Control (TTC)
  - Detector Control System (DCS)
  - Interlock system



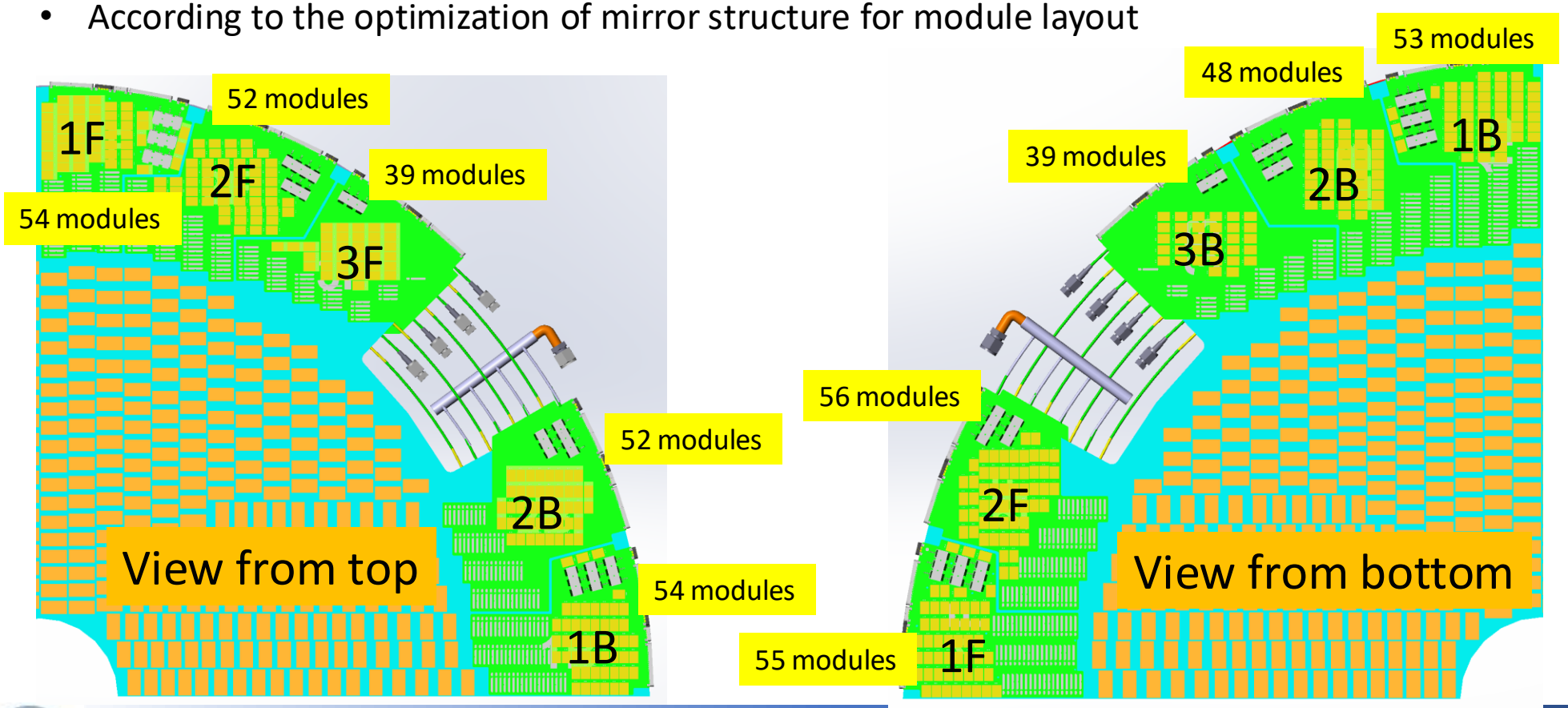
Main functions of Peripheral Electronics Board (PEB)

- Control, monitoring & data aggregation and transmission
- Power-supply distribution: LV & HV
- Thermistor connection between the front-end modules and the interlock system

Peripheral Electronics Board

Six types of PEB (front and back side)

- Board 1F, 2F, 1B and 2B can be used both on front and back
- According to the optimization of mirror structure for module layout



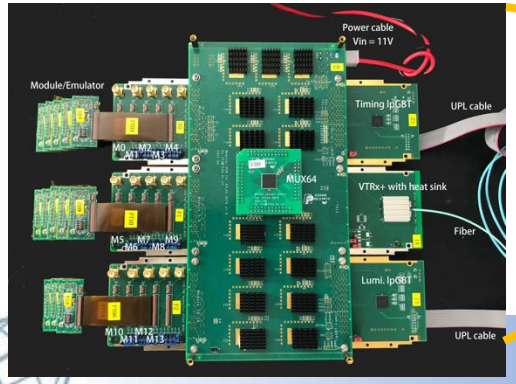
One quadrant of the HGTD front and back side

PEB R&D overview: from simple to difficult

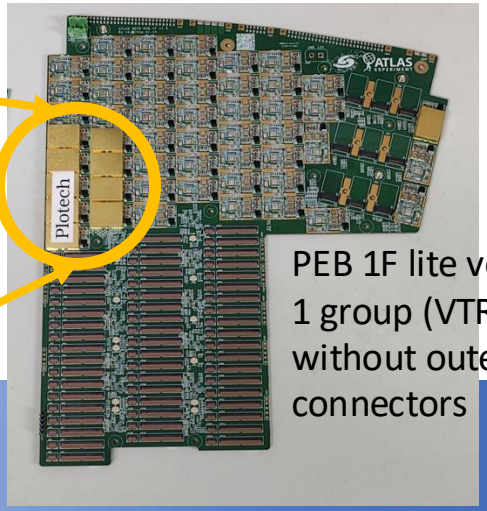
- Modular PEB: assemble of test boards for all individual key components
  - Front-end module (ALTIROC), MUX64, bPOL12V, lpGBT and VTRx+
  - Standalone board to verify functionality and performance separately
- PEB 1F (2 versions): most complex PCB in 6 types of PEB, 22-layer PCB

Site	CERN	IHEP	NJU	Nikhef/Radboud	KTH	Clermont
Modular PEB	-	-	1	1	1	1
PEB 1F	3	1	1	-	-	-
Tasks	Demonstrator, Beam test, & System integration	QA/QC, Reliability test	Training	TDAQ	Lumi.	Timing

Modular PEB is 1/9 group of PEB 1F



Modular PEB



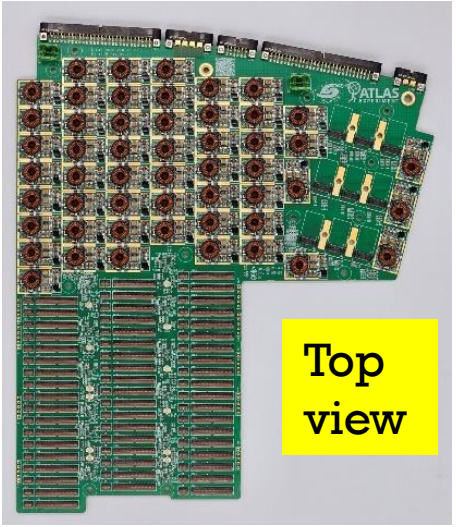
PEB 1F lite version
1 group (VTRx+ 2 lpGBT)
without outer ring
connectors

PEB 1F

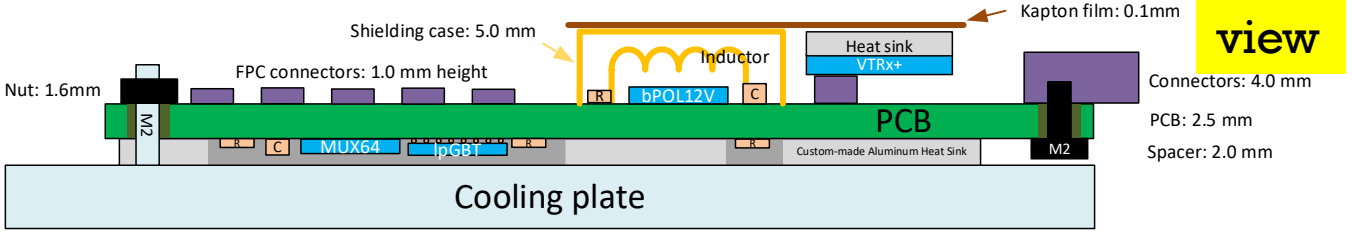
PEB R&D overview: **1F board** from difficult to simple

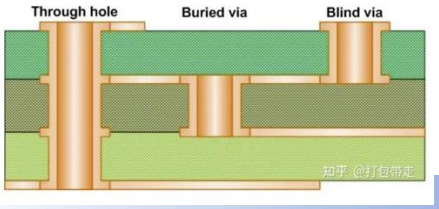
- **Total thickness: 9.7 mm**
  - Shielding case: 5.0 mm
  - PCB: 2.5 mm
  - Spacer: 2.0 mm
  - Others: 0.1~0.2 mm
- **55 FPC connectors**
  - Center to center distance: 6.5 mm
- **52 bPOL12v power blocks**
  - Size: 24 mm x 14.5 mm
  - Height above : 5 mm
  - Height under: 2 mm

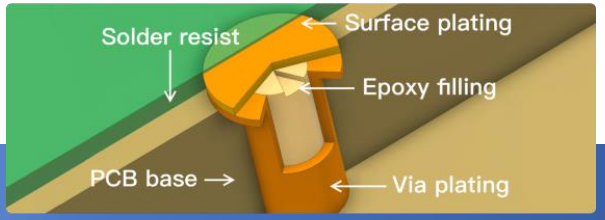
- **High speed**
  - low loss multi-layer material and Impedance control
- **Halogen free:** EM-890 or IT-170/988 or TU-883A
- **Symbols and nets:**
  - **3386 components, 12996 connections**
- **22 layers, includes:**
  - 8 layers for signals, 2 layer for HV and HV return ground
  - 4 layers for ground, 8 layers for power
- **High Density Interconnector:** Micro via
- **VIPPO/POFV:** Via-in-Pad Plated Over PCB



- **Other boards: derived from this board, sharing library files, stack-up, and design specifications**

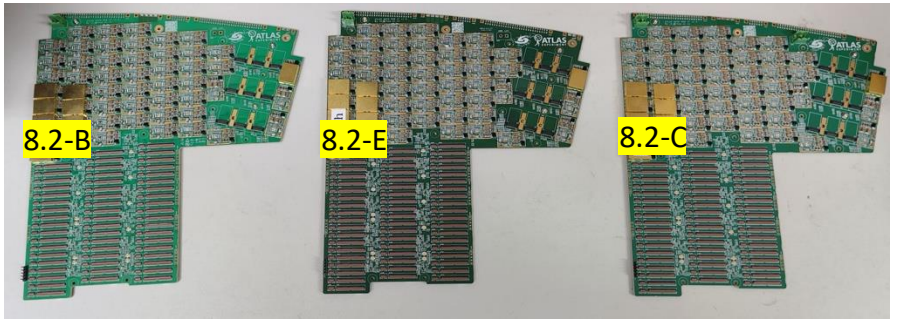


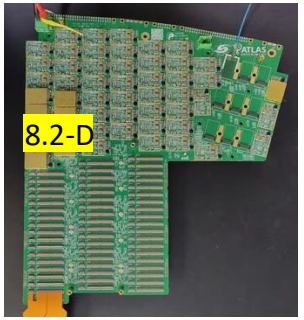




PEB 1F-Prototype Fabrication & Pre-qualification

- Qualified vendor chosen for the PCB fabrication and assembly
  - 4 companies for PEB 1F prototype fabrication



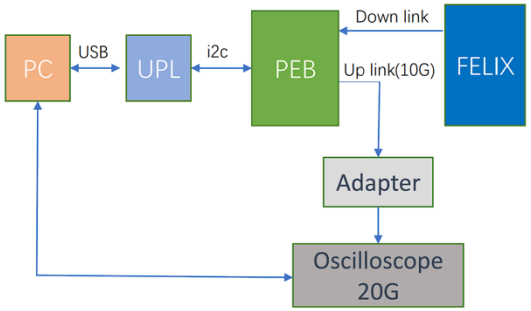


Vendor	2022 annual revenue in China (*)	PCB Material	Fabrication time	Comment	Assembly	
8.2-D	In top20	IT-170	54 days	Failed to merge the sandwich in the first batch, alignment; The second batch is OK	1 group	Finished at Nov. 29th, 2023
					-	-
8.2-C	In top100	EM-890K	89 days	Failed in the first batch; The second batch is OK	1 group	Finished at Dec. 21st, 2023
					-	-
8.2-B	In top5	EM-890K	39 days	High quality, promised fabrication time	1 group	Finished at Jan. 2nd, 2024
					Full assembly	2 pcs finished at Jan. 15th, 2024 One sent to CERN at Jan. 22th, 2024 Another sent to CERN at May. 6th, 2025
8.2-E	Taiwan	TU-883A	20 days	High quality, very fast, but need custom clarence	1 group	Finished at Dec. 27th, 2023
					-	-

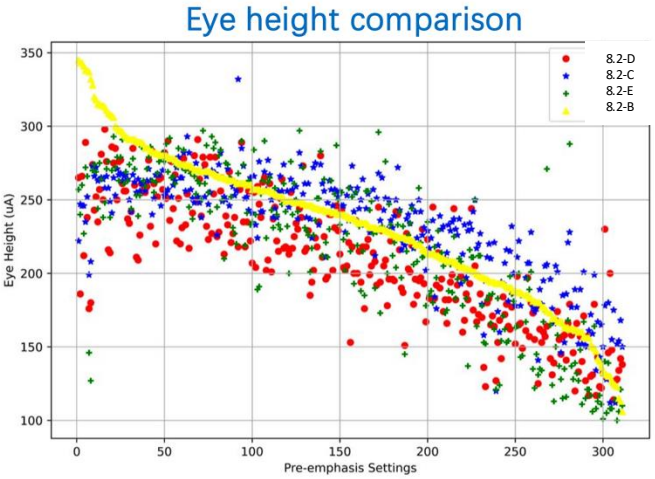
*Note: https://www.eet-china.com/mp/a133351.html

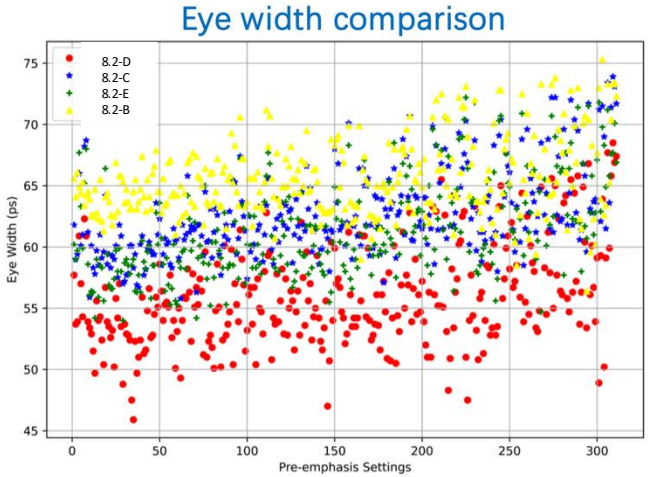
Eye Diagram: High speed test

- Setup for 10.24 Gbps
  - FELIX to provide down link data for lpGBT clock recovery
  - UPL to configure the pre-emphasis parameters of lpGBT



- Result
  - Eye height: **8.2-B, 8.2-C are better** than 8.2-D, 8.2-E
  - Eye width: **8.2-B > 8.2-C** > 8.2-E > 8.2-D
  - Consistent with the expectation based on the materials used by each vendor
- 8.2-B chosen as the **qualified vendor**
  - One of the "official" vendors for CERN
  - Also the vendor for JUNO, HEPS and COMET experiments





PEB 1F-test Matrix

Details summarized in NJU student Zhenwu Ge's PhD thesis: "Evaluation of the PEB 1F.pdf"

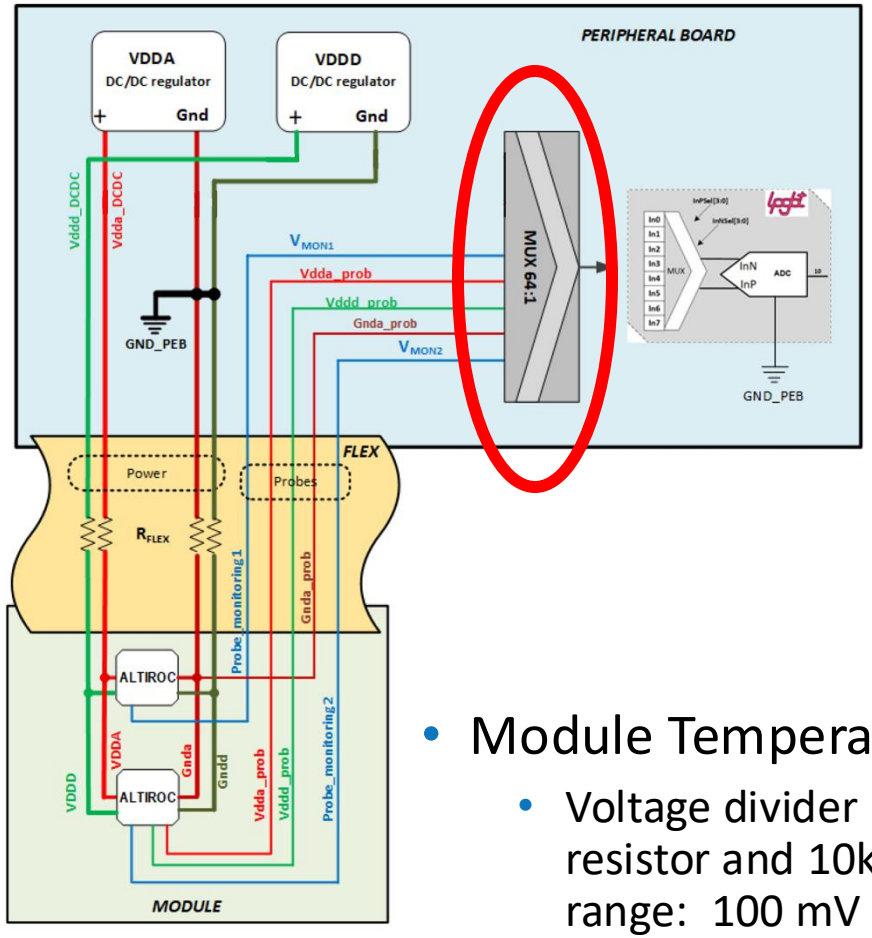
Items			Full assembly 8.2-B At IHEP	Full assembly 8.2-B At CERN	Documents
PEB self-testing	Power on/off, voltage check		Done	Done	BPol12V output values meet expectations (details in page 3)
	HV check		Done	Done	HV leakage current test, < 5 nA@1100 V
	Communication test	lpGBT & modules	Done	Done	Up/Down link bit error rate < 10^{-12} Multi modules/emulaters BERT test with PEB 1F
		lpGBT & FELIX	Done	Done	
		MUX64 and ADC	Done	Done	
	TDR (Time Domain Reflectometry)		Done	-	Compare the products of four companies through TDR testing, All meet the requirements. Choose the best one for pre-production
	Clock jitter and skew test		Done	Done	Total jitter < 10 ps (including FELIX, PEB, flex-tails and module flex), Clk and fastcmd skew < 0.5 ns for 320 MHz clock, < 0.7 ns for 640 MHz clock, satisfying ALTIROC specification Clk jitter and skew measurements for PEB 1F, Multi modules/emulaters BERT test with PEB 1F, Use PNA(Phase noise analyzer from Keysight) to measure jitter from frequency domain
	Eye-Diagram test for optical links		Done	Done	Bit error rate < 10^{-12}, PEB 1F eye diagram test for 10Gbps
Operating condition test	Full power test with thermal emulators and flex tails		Done	In progress with 54 modules	Support up to 250W, from PEB Thermal Cycle Status
	Performance test at low temperature		-	In progress	Measurements at Demonstrator, conduct performance evaluations for some of the modules.
Joint test	With front-end modules	Front-end module config	Done	Done	Multi-module config via I2C buses
		ALTIROC2	Done	Done	Testing with PEB 1F
		ALTIROC3	Done	Done	1.28Gbps readout with ALTIROC3 modules and PEB/FELIX in demonstrator
		ALTIROC-A	Done	In progress	Scripts development for AltirocA module test on PEB + FELIX, but need to adjust power output
	And with HV	Noise analysis	Done	Done	Combined test at CERN
Calibration	DSC Monitoring measurement		-	Done	All temperature data have been read out
	TDC Calibration		Done	In progress	Altiroc3 TDC calibration update, Scripts based on ALTIROC-A is currently being migrated.
Reliability test	High Temperature Operating Life (HTOL)		Done	-	
	Temperature Cycling (TC)		Done	-	-40°C to 70°C, 96 thermal cycles passed, from PEB Thermal Cycle Status

Design for all shapes

- Designs file managed by version control tool (GitLab)
  - Facilitate collaborative design and prevent design bugs
- Dimensions for all boards
  - Determined and confirmed by HGTD mechanical group
- Three sites started to design other shapes
  - **IHEP**: 1B/2F/2B; **NJU**: 1F/3F; **MASCIR**: 3B;
- Manpower status

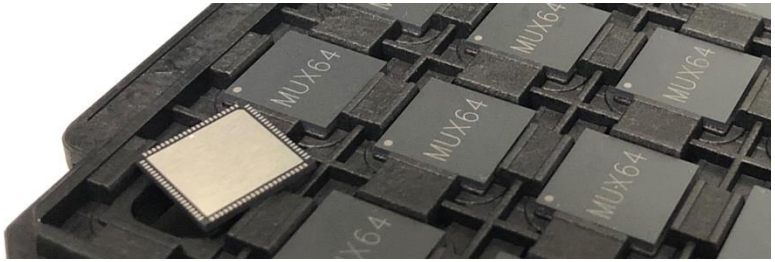
	Senior engineer	Technician	Postdoc	Student
IHEP	1 √	1 √	-	2 √
NJU	1 √	-	1 √	2 √
Morocco	1 √	-	-	-

MUX64 chips: 64-to-1 analog multiplexer ASIC



- Module Temperature
  - Voltage divider by 100 k resistor and 10k NTC, range: 100 mV to 900 mV

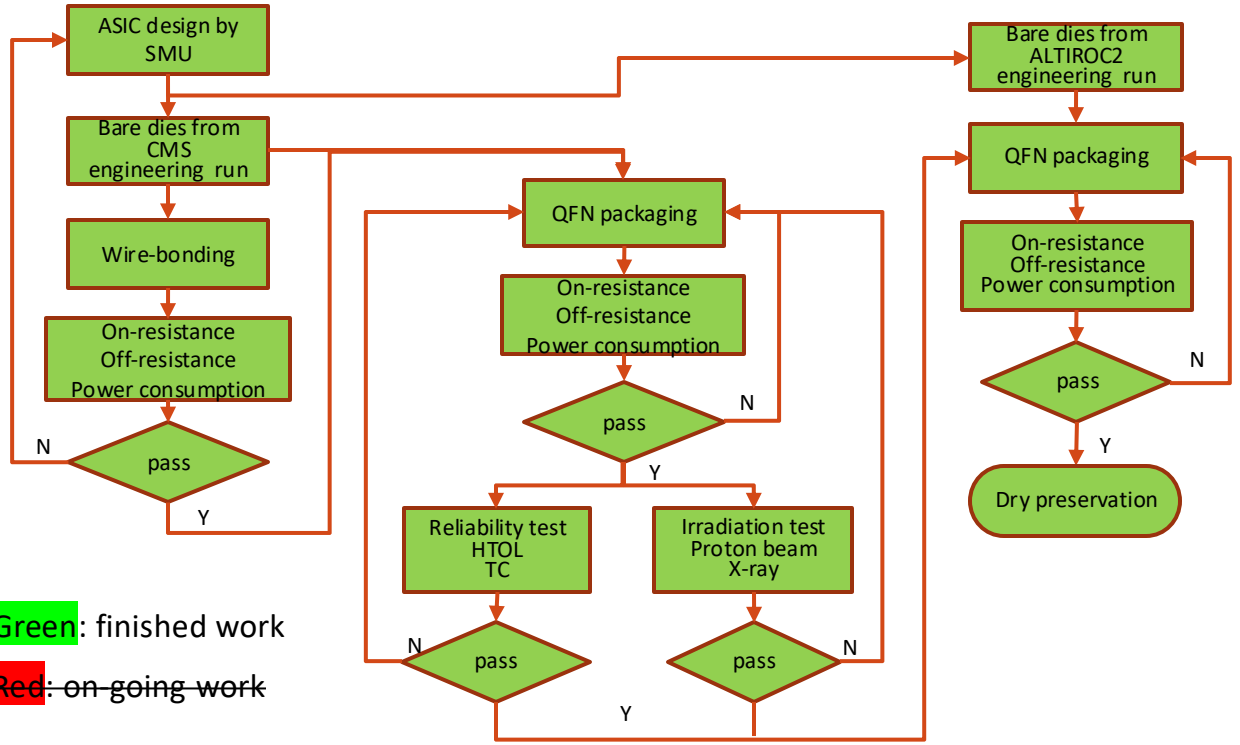
- NJU: ~ 2000 pcs packaging and QA/QC
  - Designed by SMU, taped out with ALTIROC



Monitoring front-end modules

- Power supply voltages
  - Vdda, Vddd, range: 800-850 mV
  - Gnd, range: 0 to 50mV
- ALTIROC ASICs analog outputs
  - Temperature, range: 380 - 820 mV
  - Preamplifier bias voltage, range: 650 - 950 mV
  - ...

MUX64 Production Flow

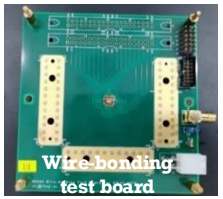


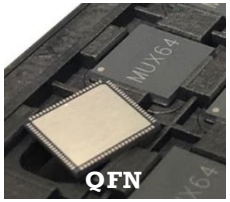
- Green: finished work
- ~~Red: on-going work~~

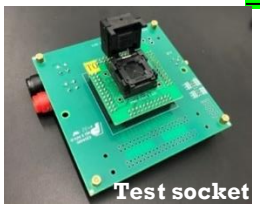
- Reliability test
  - High Temperature Operating Life (HTOL)
    - 32 samples, 85 ˚C, 16days, All pass HTOL
  - Temperature Cycle (TC)
    - 48 samples, -40 ˚C to 85 ˚C
    - 4 batches launched, more than 100 cycles per batch, pass TC
- Irradiation test
  - Proton beam
    - Beam energy: 80 MeV.
    - Spot size: 20 x 20 mm^2
    - Measured injection rate: 1.89 × 10^9 pps/cm^2
    - 2 samples, irradiation time: 9.4 days, all pass test
  - X-ray
    - Instrument model: MultiRad160
    - TID dose rate: up to 5 Gray/s, pass TID test
    - 5 samples, pass TID test

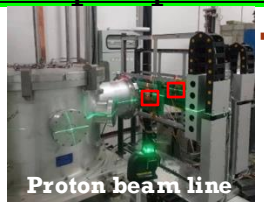
	Requirement	Tested
Si 1MeV n_{eq} fluence	2.5 x 10^{15} n_{eq}/cm^2	3.21 × 10^{15} n_{eq}/cm^2
TID	0.54 M Gy	0.75 M Gy

- 1434 pcs passed QA/QC test
  - QA/QC results:
    - Class I (good): 1434 (78.1%)
    - Class II: 292 (15.9%)
    - Class III: 47 (2.6%)
    - Class IV: 30 (1.6%)
    - Class V (Damaged): 33 (1.8%)









MUX64 in HGTD database

By Jiawei Wang (NJU)

- Test results of 1807 MUX have been uploaded
- Each chip has 65 attributes:
  - **Max resistance of 64 channels** :ch0_ohm_max … ch63_ohm_max.
  - **Inspection** :class one, class two … class five (one = best, five = worst).

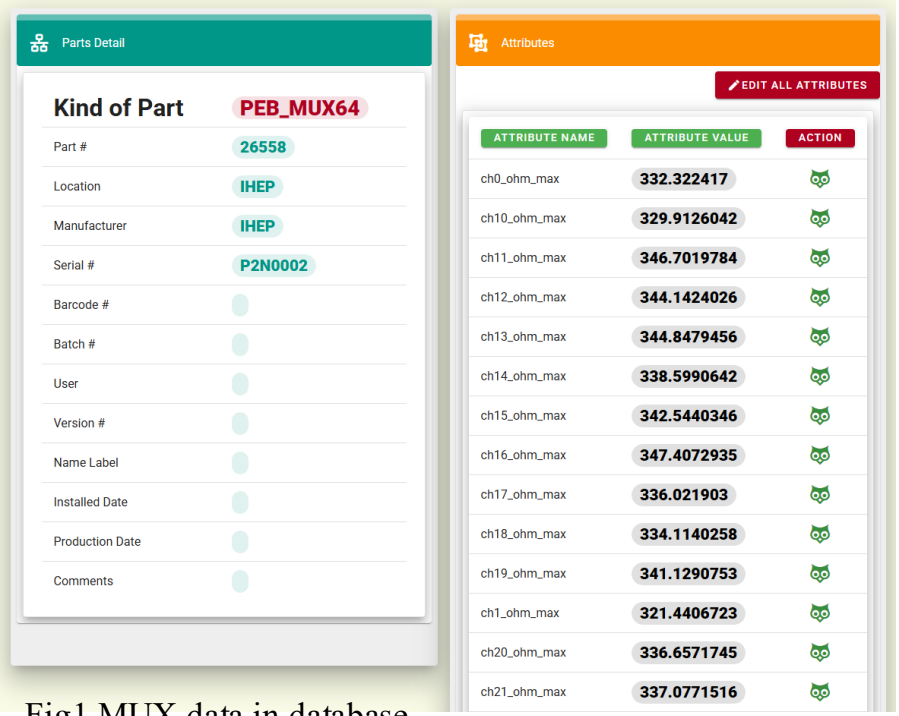


Fig1.MUX data in database

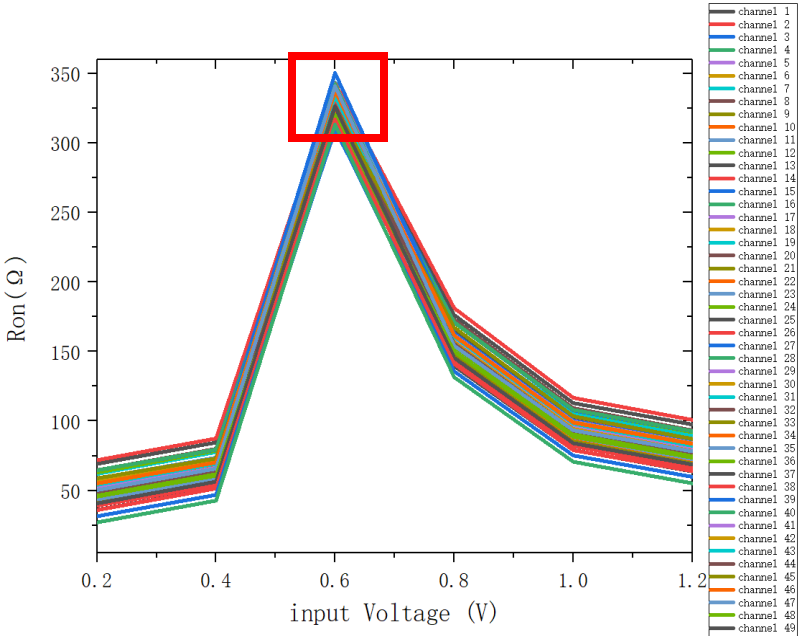


Fig2.Resistance curve

Schedule

NJU Finished MUX64 mass-production and QA/QC

- **All testing data uploaded to HGTD-DB**

Before pre-production

One quadrant with 6 shapes

Three sites design the PEBs in parallel

- **IHEP, NJU, Morocco group**

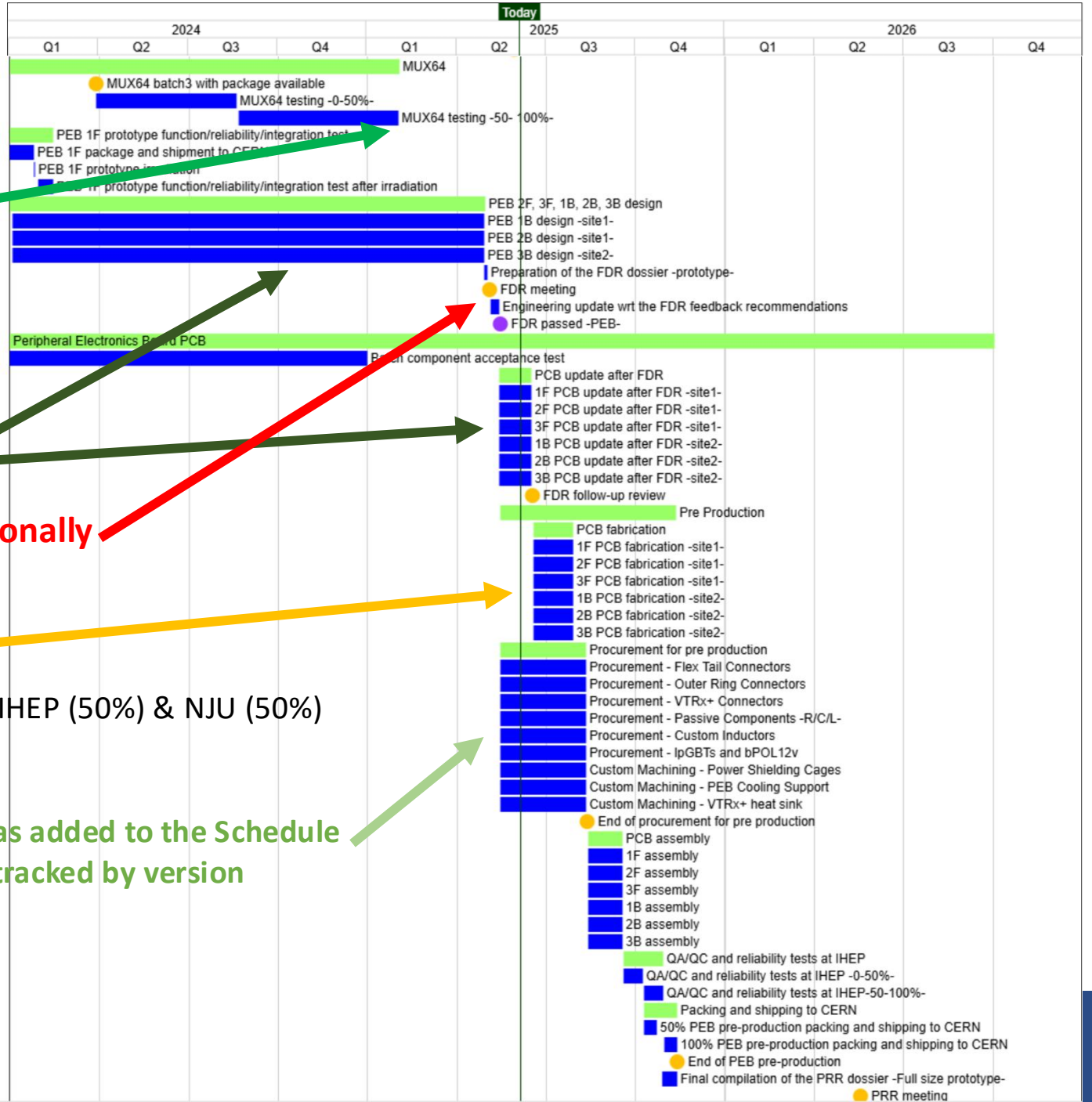
FDR on May 16th 2025, conditionally passed with follow-up actions.

Pre-production

- PCB fabrication and assembly by IHEP (50%) & NJU (50%)

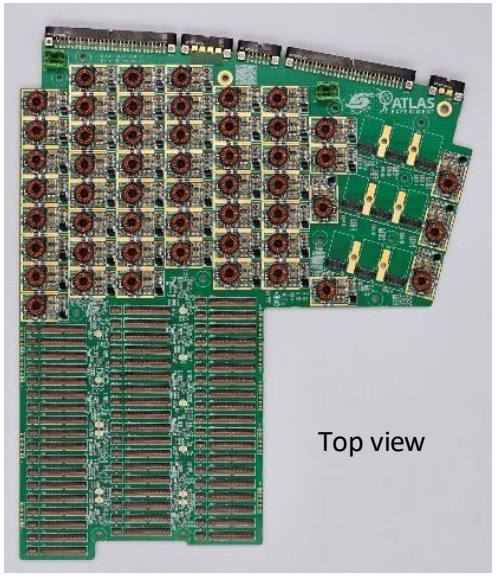
Detailed purchasing information was added to the Schedule

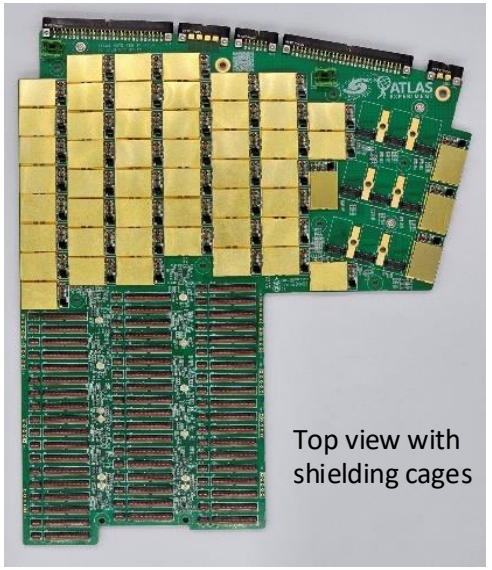
- **Components are managed and tracked by version control tool (GitLab)**

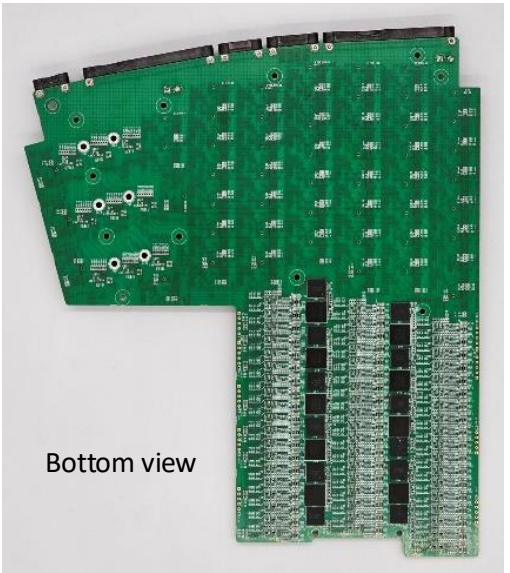


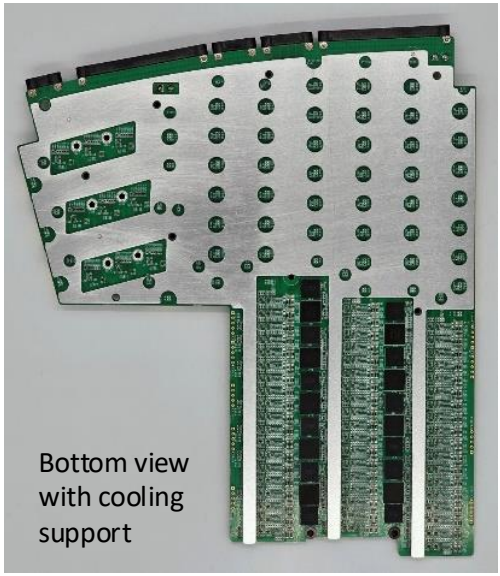
Summary

- PEB prototype finished, no major issue found
  - Finished vendor qualification
- Provide technical support in full demonstrator
  - Feedbacks from full demonstrator is important to validate the hardware
- Moving towards to pre-production









THANKS TO YOUR ATTENTION

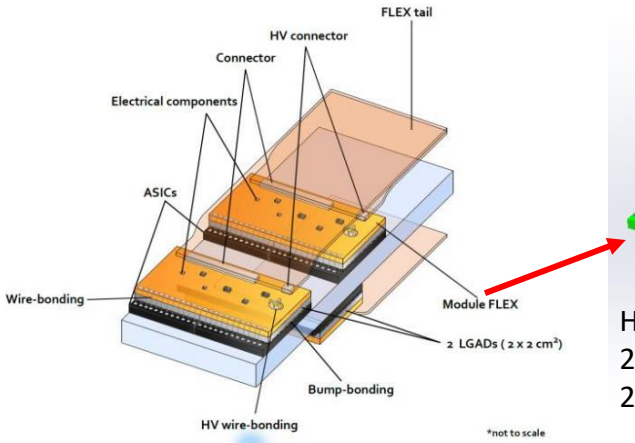
Backup

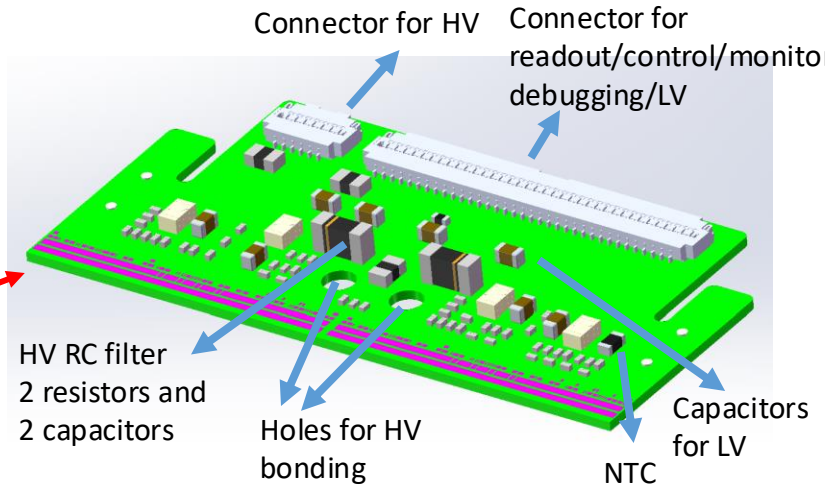
Papers (2024-2025)

Papers

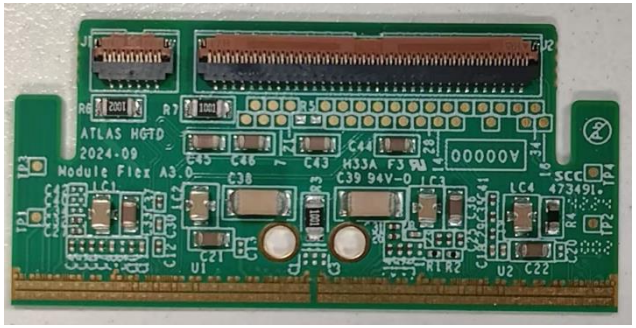
1. Ge, Z., et al. (2024). "Evaluation of the prototype Peripheral Electronics Board for the High Granularity Timing Detector." Journal of Instrumentation 19(12): C12012.
2. Ge, Z., et al. (2024). "An FPGA-based front-end module emulator for the High Granularity Timing Detector." Journal of Instrumentation 19(03): C03055.
3. Zhai, M., et al. (2024). "HGTD DC/DC converter in low temperature and magnetic field operation." Journal of Instrumentation 19(02): C02006.
4. Wang, C., et al. (2024). "Radiation tolerance of the MUX64 for the High Granularity Timing Detector of ATLAS." Journal of Instrumentation 19(03): C03044.

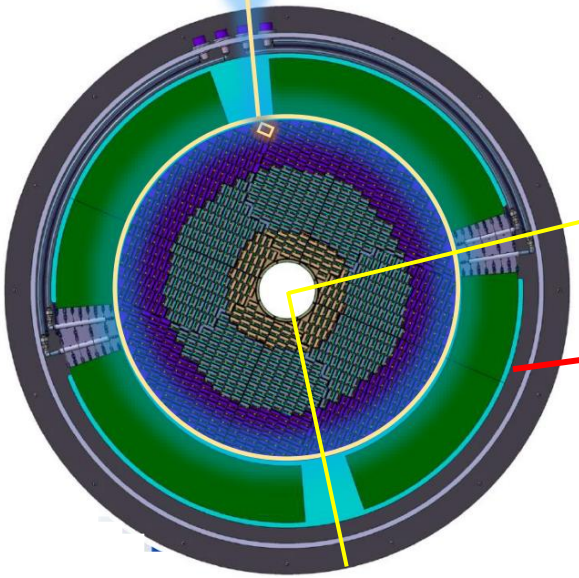
On-detector Readout Electronics – Scope

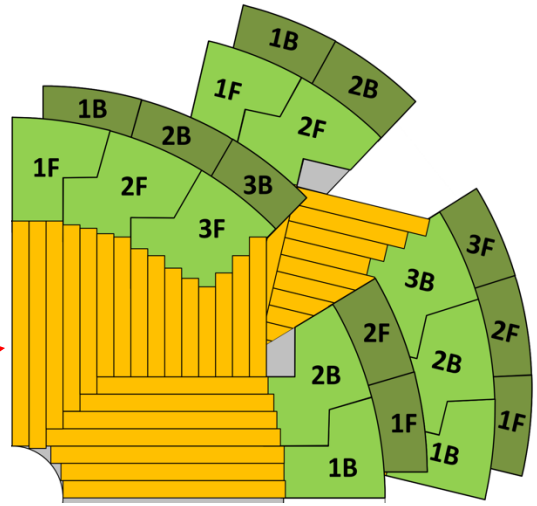




- The front-end modules are connected via flex tails, arranged in rows







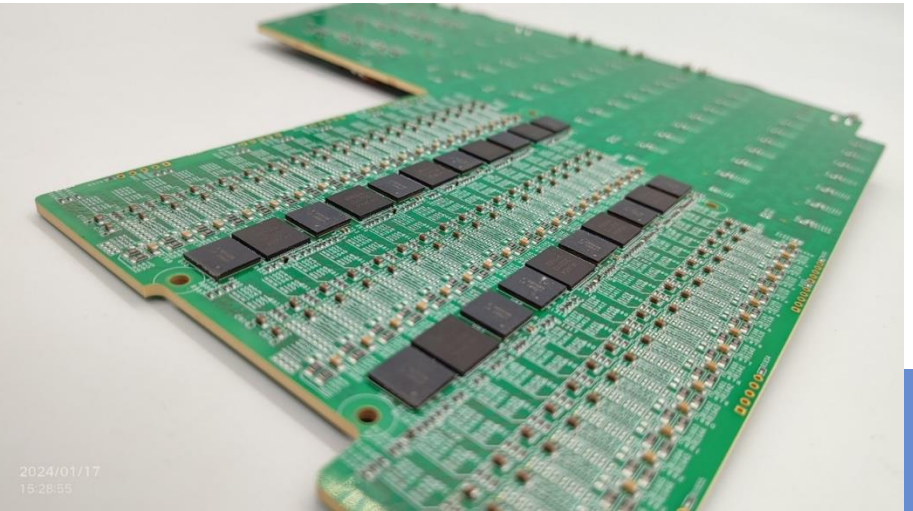
One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- PEB @ 660 < r < 920 mm
- Six types of PEB to be designed (front and back side)
  - Board 1F, 2F, 1B and 2B can be used both on front and back
    - According to the optimization of mirror structure for module layout
  - Each board covers three or more readout rows in order to have a similar number of modules

PEB Qty.	1F	2F	3F	3B	2B	1B
Pre-production	2	2	1	1	2	2
Mass-production	32	32	16	16	32	32

lpGBT v1 issues and HGTD-lpGBT status & plan

- Two separate issues, that may affect correct operation of a fraction of systems, have been discovered in 2024:
  - Stuck at power-up
    - Small fraction of chips may be completely unresponsive after power-up in some conditions, no communication possible, external reset is ineffective
    - Power cycle might restore functionality, but success of this is not guaranteed
  - Equalizer attenuation
    - Small fraction of lpGBT chips paired with VTRx+ modules may show correctable or non-correctable downlink data errors
    - Impacts systems even when equalizer functionality is not explicitly used
- HGTD have used 24 chips for prototype, the two problems mentioned here have **not** been found.
  - The sample of statistics is too small.
  - Usage details:
    - Power by bpol12v (12V->1.25V), rising time is 200 us, shared by two or three lpGBTs and VTRx+.
    - Power by bpol12v (12V->2.55V), rising time is 200 us, VTRx+.
    - One lpGBT acts as master (10 Gbps, FEC5, Transceiver, recovered clock from the data stream, boot from ROM), one or two lpGBTs acts as slave (10 Gbps, FEC5, Simplex TX, external 40 MHz reference clock from master, boot from ROM)
    - Operate at -35◦C $\pm$ 5◦C (CO_2 cooling)

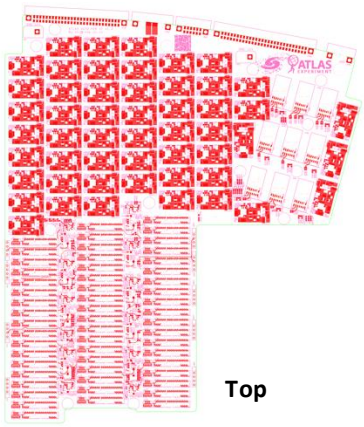


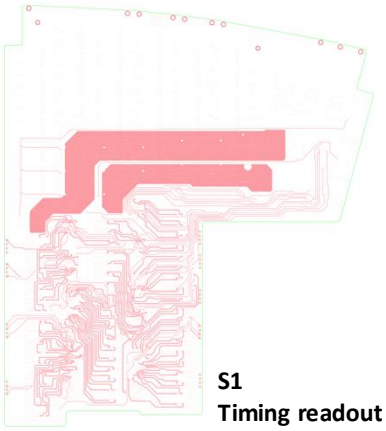
New HGTD-lpGBT plan

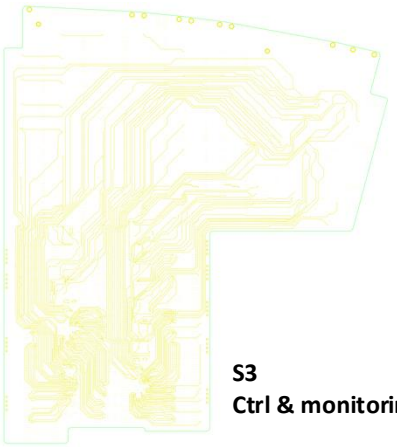
- Use the lpGBTv2 for pre-production (125 chips, middle 2025)
  - To avoid re-packaging, 184 lpGBTv2 (in one tray) have be picked up by Stefan on March 7, 2025
- Use the lpGBTv2 for mass-production (1988 chips, early 2026)

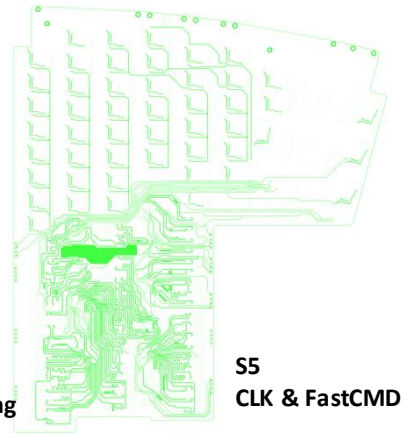
PEB 1F - routing

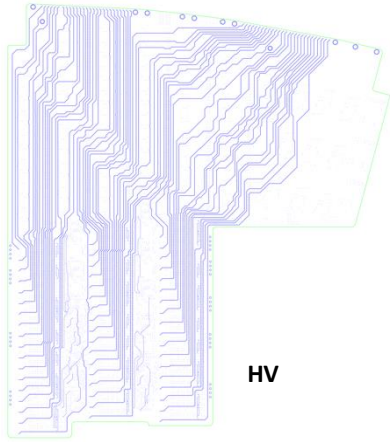
- Layer routing according to function

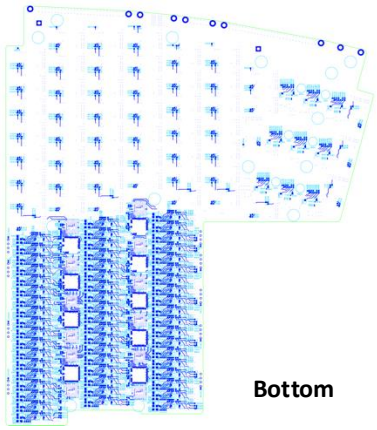

Top

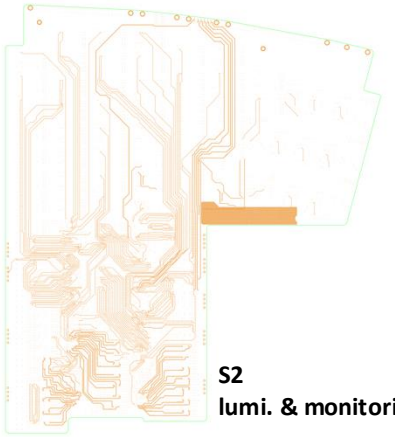

S1
Timing readout

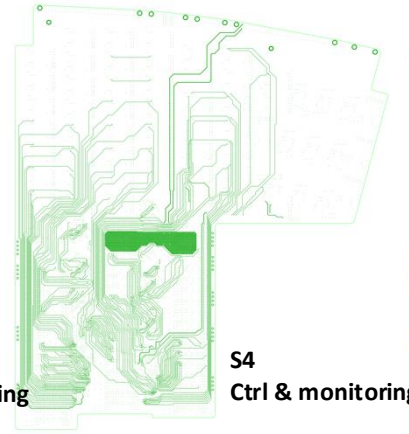

S3
Ctrl & monitoring

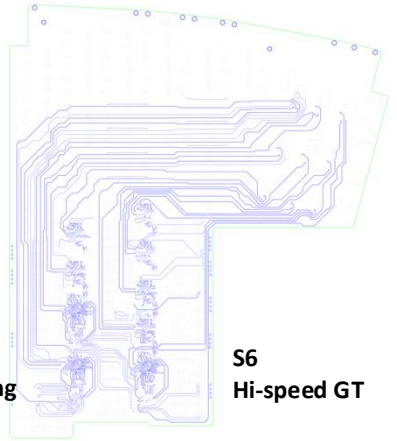

S5
CLK & FastCMD

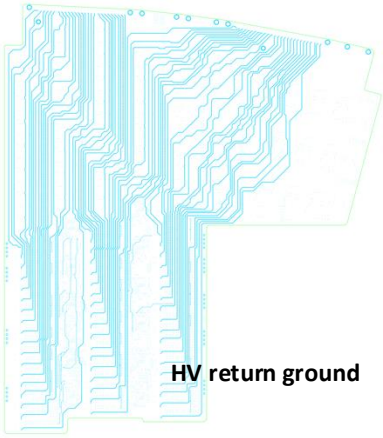

HV


Bottom

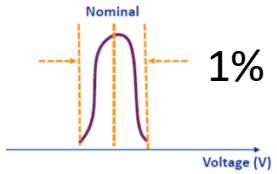

S2
lumi. & monitoring


S4
Ctrl & monitoring

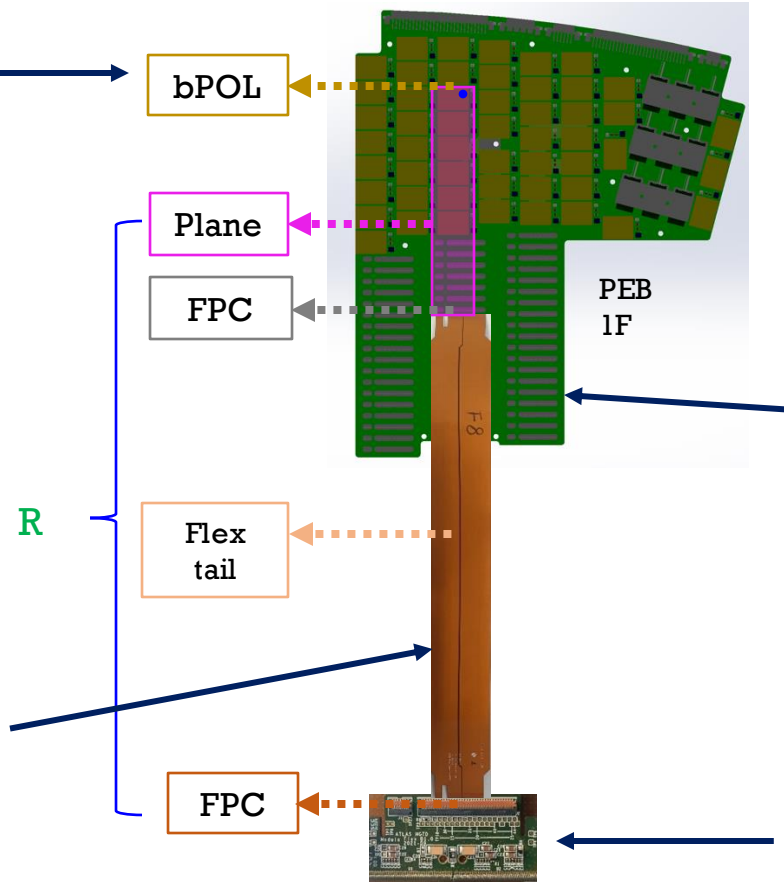

S6
Hi-speed GT

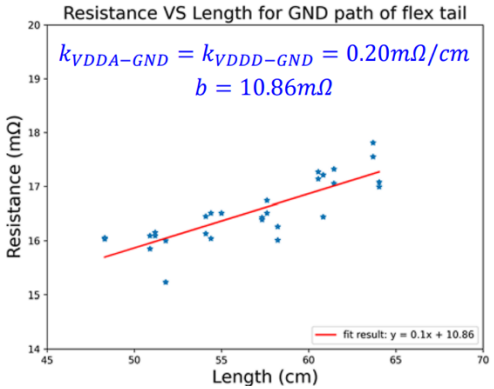

HV return ground

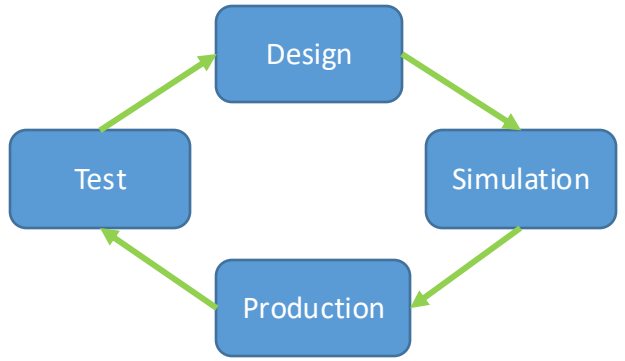
Challenges - PEB Power Settings

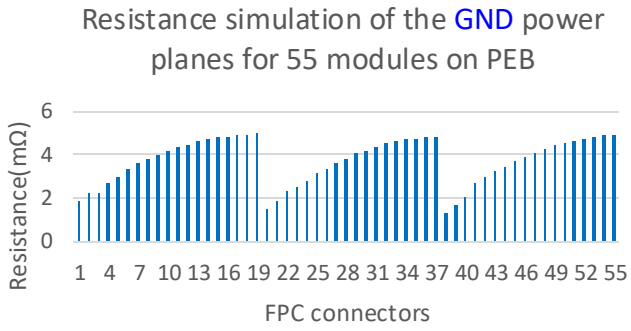


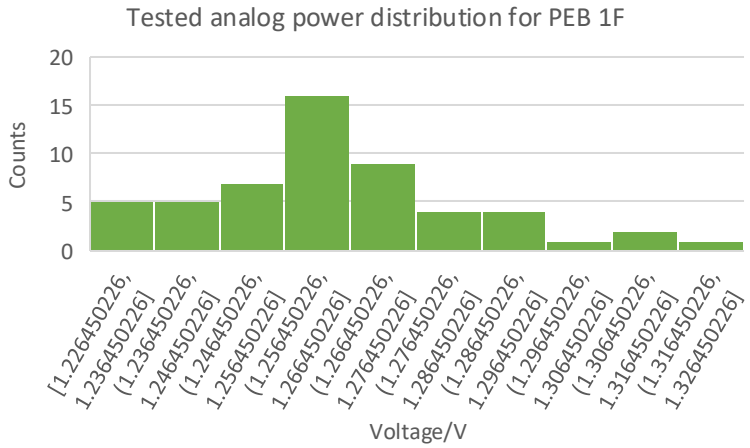
bPOL output distribution from the modular PEB











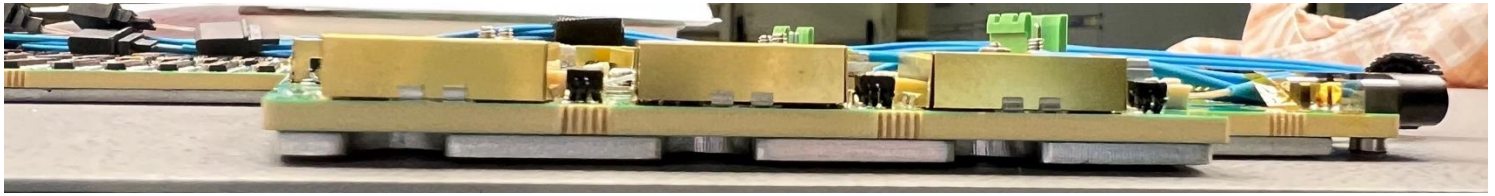
21

PEB 1F modifications/Feedbacks

In red: New from last mini-week (Feb. 6th 2024)

Feedbacks from PEB 1F

- Schematics:
  1. Modules' NTC should be pull-up by the 1.25V for lpGBT
  2. Add 100pF for VTRx+ I2C SCL
  3. Change the power of VTRx+ to 2.55V
  4. Module digital power first, then analog power
  5. Use 0.1% resistor for bPOL
- PCB:
  1. Move the capacitors of bPOL input and output more far away
  2. Modify the pastemask of the bPOL shielding cage, remove the clip



     - The soldering and height of the clamp/clip for the fixture of the copper shielding cage takes about 0.2~0.3 mm. The clamp/clip will be removed in the final version.
     - We will soldering the shielding cage directly on PCB in the final version.
     - The reason we use the clamp/clip in the prototype is convenient for maintenance and repair.
  3. Add copper thieving
     - Ref: https://resources.pcb.cadence.com/blog/2023-copper-thieving-improves-etch-and-plate-results
  4. Increase the diameter of the hole for the nut of the VTRx+ heat sink
  5. Swap the LV connector and interlock connector for 1B, 2B, 3B

WBS 8.2.2: Peripheral Electronics Board – Production Structure/Institutes

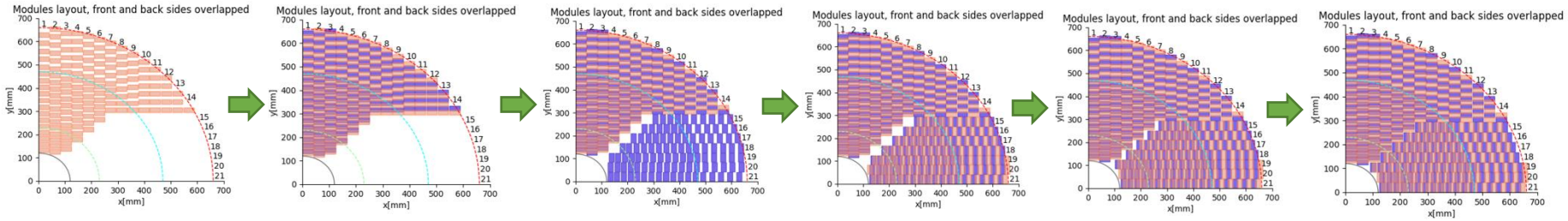
Work Responsibilities:

8.2.2	**Peripheral Electronics Board**	
8.2.2.1	Peripheral Electronics Board PCB	Beijing IHEP, Nanjing
	Design	Casablanca, Kenitra, MAScIR, Oujda, Rabat, Nikhef, Beijing IHEP, Nanjing
	Production	Beijing IHEP, Nanjing
8.2.2.2	HV and LV connectors	Sao Paulo
8.2.2.3	Flex tail connectors	Sao Paulo
8.2.2.4	lpGBT	CERN
8.2.2.5	VTRX+ optical transceivers	Casablanca, Kenitra, MAScIR, Oujda, Rabat, Nikhef, Nijmegen, Stockholm KTH
8.2.2.6	Monitor MUX	Beijing IHEP, Nanjing
8.2.2.7	DC/DC converters	CERN
8.2.2.8	Reliability test	Beijing IHEP, Nanjing

- PCB design and the components procurement
  - Casablanca, Kenitra, MAScIR, Oujda, Rabat, Nikhef, Beijing IHEP, Nanjing
- PCB production and quality assurance and quality control (QA/QC)
  - IHEP + NJU

WBS 8.2.2: Peripheral Electronics Board – Technical Progress and Status

- Module layout adjustment to reduce PEB types from 10 to 6
  - 1F, 2F, 2B and 1B are re-used at both side
  - Reduce the risk of the new design
    - The PCB placement and routing of 1F and 1B, 2F and 2B, have something in common, but readout speed of modules near boundaries are different. This need new channel arrangement for lpGBT
  - Save costs
    - The PCB NRE (Non Recurring Engineering) Cost for rigid-flex is 8~10 times to the price per unit
  - Reduce the risk on the project schedule
    - Design, production and testing
    - Each type of PEB will have different testing setup and software
- Mirror Structure
  - Python3 script is developed according to the constraints from TDR
  - Workflow - 6 steps to generate module layout



- The new layout is evaluated by mechanical design and physical simulation

WBS 8.2.2: Peripheral Electronics Board – list of items

Main chips

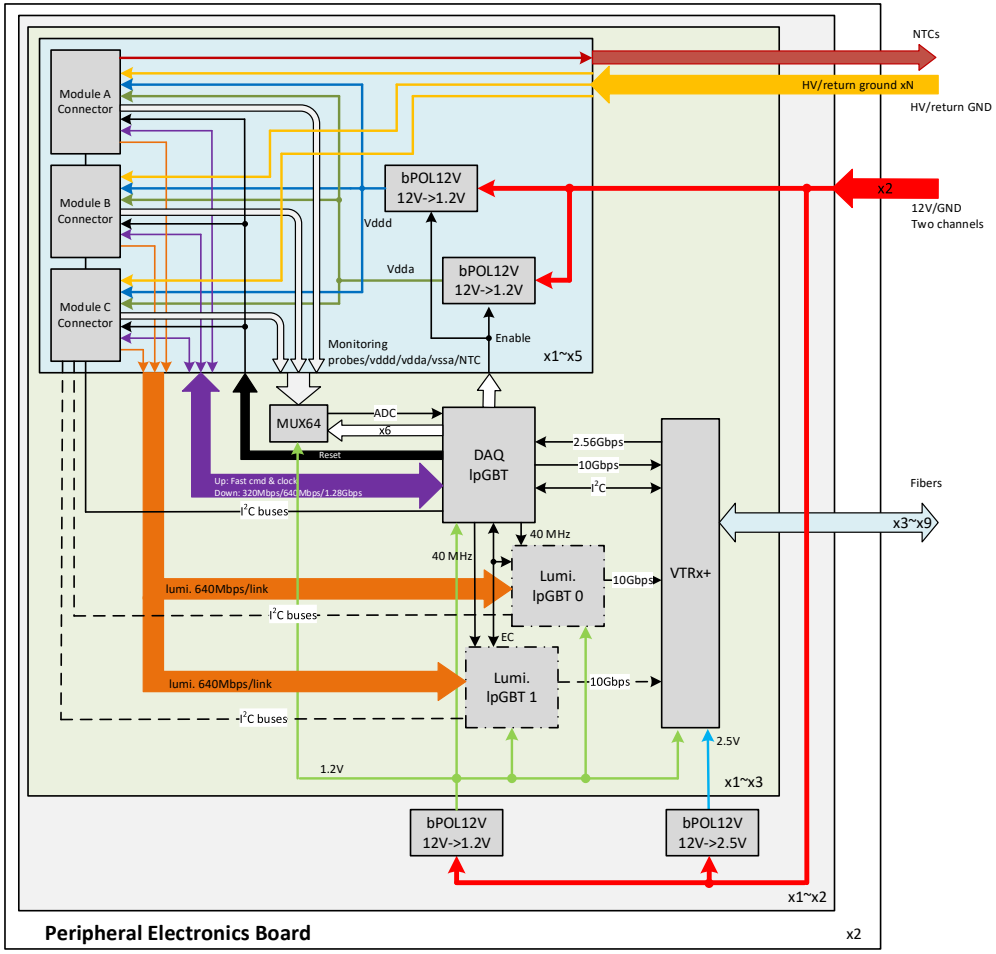
- **8.2.2.6 Monitor MUX**
  - A 64:1 multiplexer is developed by SMU to handle all voltages to be measured. Each multiplexer, which can switch the received voltages from up to 12 modules, is controlled by 6 I/O lines from one lpGBT.

From HGTD

- **8.2.2.7 DC/DC converter**
  - The peripheral electronics will contain DC-DC converters supplying the 1.2V and 2.5V required by the ALTIROC ASICs, the lpGBT ASICs and the Versatile Link.
- **8.2.2.4 lpGBT**
  - The Low Power Giga Bit Transceiver (lpGBT) is developed by CERN for the LHC upgrades. It is a radiation tolerant ASIC that can be used to implement multipurpose high speed bidirectional optical links for high-energy physics experiments.
- **8.2.2.5 VTRX+ optical transceiver**
  - The VTRX+ optical transceivers, development within the Versatile Link plus project at CERN, handle four fibers for transmission and one for receiving.

From CERN

Conceptual design of PEB



- Two LV channels
  - Each up to 12A @ 12V
- Up to 3 modules share two bPOL12v
  - One for analog power, the other for digital power
- One TDAQ lpGBT and 1~2 luminosity lpGBTs share one VTRx+
- Control
  - I2C of lpGBT
    - Module and VTRx+ configuration
    - I2C0 of TDAQ lpGBT is connected to the VTRx+ only
  - Output
    - Module reset
    - Module power on/off
    - MUX64 channel selection
- Monitoring
  - ADC of lpGBT
  - Module state monitoring
    - VDDA, VDDD, GNDA, PROBE0/1(internal state and temperature), NTC
  - PEB state monitoring
    - lpGBT voltage, temperature
    - VTRx+ RSSI(average optical power of the received light) and NTC
    - bPOL12v temperature
    - On board NTC
  - Input of lpGBT
    - bPOL12v power good signal

bPOL12V:
provide the 1.2V analog and digital voltages for the ALTIROCs

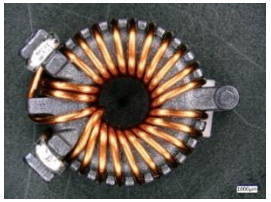
lpGBT:
Bi-directional slow control and monitoring communication between the FELIX and the lpGBT is done via the IC and EC channels.

Each lpGBT has a 8 channel multiplexed ADC.
With ~7 modules/lpGBT, an external 64-to-1 MUX is required: **MUX64**

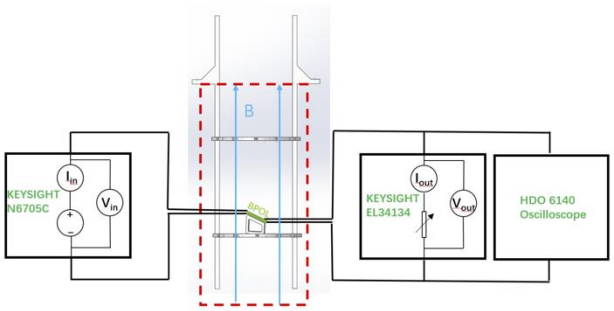
WBS 8.2.2: Peripheral Electronics Board – DC/DC converter

Bpol12V generates analog and digital 1.2 V to the front-end modules

- Height limitation in HGTD
  - < 10 mm (Including PCB and shielding case)
  - Selection for air-core inductor
    - Custom solenoid coil from CMS



- Tested in low temperature (-35 ℃), OK
- Tested in magnetic field, up to 4 T, OK

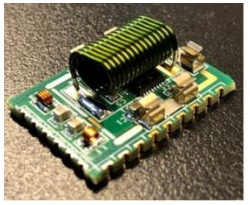


BPOL12V test system in magnetic field

Aachen module

CERN module (FEASTMP)

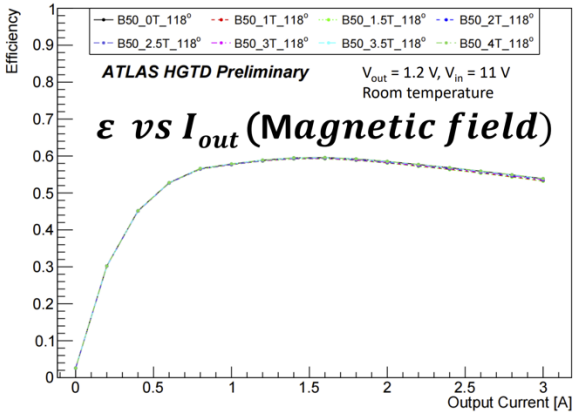
ITK EoS

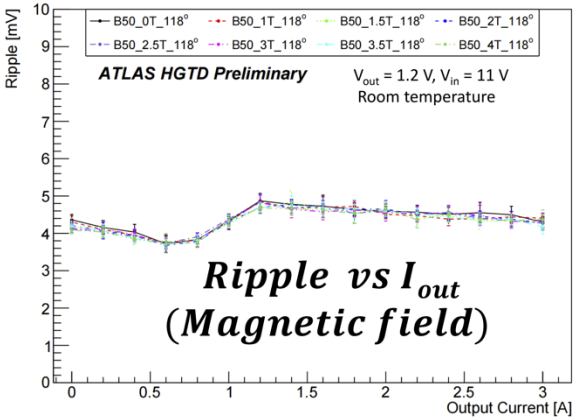


Commercial inductor

HGTD

Inductor candidates





Efficiency and ripple with respect to *Iout* in magnetic field

PCB MATERIALS

		8.2-D	-	8.2-B/C	8.2-E
		IT-170	IT-988	EM-890K	TU-883A
Dk, dielectric constant	1GHz	4	3.21	2.93	3.91
	2GHz	3.9	3.21	2.89	
	5GHz	3.9	3.21	2.88	3.9
	10GHz	3.8	3.21	2.84	3.89
	20GHz		3.21	2.81	3.86
Df, loss factor	1GHz	0.006	0.0014	0.0018	0.0024
	2GHz	0.0063	0.0014	0.0021	
	5GHz	0.0075	0.0014	0.0022	0.0031
	10GHz	0.008	0.0014	0.0024	0.004
	20GHz		0.0015	0.0025	0.0044