CEPC Silicon Tracker Progress Report (21)

Qi Yan *on behalf of the Silicon Tracker Group* May 6, 2025, IHEP

New Outline of Silicon Tracker Ref-TRD

5.1	Overview					
	5.1.1	Physics re	quirements			
	5.1.2	Specific re	equirements on Silicon Tracker			
	5.1.3	Layout op	timization and expected performance			
		5.1.3.1	Optimization boundary conditions and tool 3			
		5.1.3.2	Geometrical envelope of the tracking system			
		5.1.3.3	Layout in barrel region			
		5.1.3.4	Layout in endcap region			
		5.1.3.5	Optimization summary			
5.2	Inner s	ilicon tracke	<u>r (ITK)</u>			
	5.2.1	ITK desig	n9			
		5.2.1.1	ITK barrel design			
		5.2.1.2	ITK endcap design			
	5.2.2	Readout e	lectronics			
	5.2.3	Mechanic	al and cooling design			
		5.2.3.1	Barrel local support			
		5.2.3.2	Endcap local support			
	5.2.4	HV-CMO	S pixel sensor			
		5.2.4.1	HV-CMOS pixel sensor for CEPC			
		5.2.4.2	COFFEE1			
		5.2.4.3	COFFEE2			
	5.2.5	Future pla	<u>n</u>			
		5.2.5.1	Development of the CMOS pixel sensor			
		5.2.5.2	Module and system level development			
5.3	Outer s	ilicon tracke	er (OTK) with precision timing 30			
	5.3.1	OTK desi	gn 30			
		5.3.1.1	OTK barrel design			
		5.3.1.2	OTK endcap design			
		5.3.1.3	OTK alternative design			
	5.3.2	Readout e	lectronics			
		5.3.2.1	Front-end board			
		5.3.2.2	Concentrator card and power distribution 41			
		5.3.2.3	Slow control and monitoring			
		5.3.2.4	Clock distribution			
	5.3.3	Mechanic	al and cooling design			
		5.3.3.1	Barrel support			
		5.3.3.2	Endcap support			
	5.3.4	AC-LGAI	<u>D sensor</u>			
		5.3.4.1	AC-LGAD simulation 51			
		5.3.4.2	Testing setup			
		5.3.4.3	Pixelated AC-LGAD prototypes 53			
		5344	Strip AC-LGAD prototype and properties 55			

	5.3.5	LGAD readout ASIC					
		5.3.5.1	General requirements	57			
		5.3.5.2	ASIC architecture	58			
		5.3.5.3	Single-channel readout electronics	59			
		5.3.5.4	Data process and digital blocks	61			
		5.3.5.5	Prototype	61			
		5.3.5.6	Radiation tolerance	62			
		5.3.5.7	Monitoring	62			
		5.3.5.8	Latest ASIC submitted for tap-out	62			
	5.3.6	Future pla	an	62			
		5.3.6.1	Development of AC-LGAD strip sensor for CEPC	62			
		5.3.6.2	Development of LGAD readout ASIC	63			
		5.3.6.3	Development of mechanical and cooling system	63			
		5.3.6.4	Summary	63 64			
5.4		Survey and alignment					
	5.4.1		cal assembly and optical survey	64			
		5.4.1.1	ITK installation and survey	64			
		5.4.1.2	OTK installation and survey	65			
		5.4.1.3	Target optical survey precision	65 65			
	5.4.2						
		5.4.2.1	Global composite alignment	65			
		5.4.2.2	Alignment plan and datasets	65 66			
5.5		tector safety interlock					
5.6		m background estimation					
	5.6.1		stimation for beam background	67			
	5.6.2	ITK tolerable hit rate		67 68			
	5.6.3	OTK tolerable hit rate					
5.7	Performance						
	5.7.1		ormance of the barrel region	69			
		5.7.1.1	Momentum resolution	69			
		5.7.1.2	Roles of gaseous and silicon trackers	70			
		5.7.1.3	Particle identification performance	71 71			
	5.7.2						
		5.7.2.1	Momentum resolution performance	72			
	~	5.7.2.2	Particle identification performance	73 74			
5.8	Summa	Summary					

The structure of the Silicon Tracker chapter has been revised to align with new requirements.

Update on Silicon Tracker Ref-TDR

- Almost all suggestions from the last IDRC review have been incorporated in this revision, including those from private discussions with Ivan and Gregor .
- The structure and content have been refined for better readability.
- All the figure captions have been enhanced to meet publication standards.
- The description of the CMOS strip section has been removed, and the content of the OTK sensor and OTK ASIC sections, along with other sections, has been reduced.

It's difficult to significantly reduce the size of this chapter.