Taichu-stitching尺寸初步考虑

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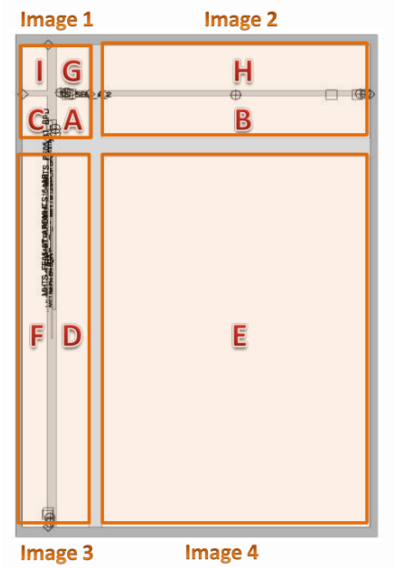
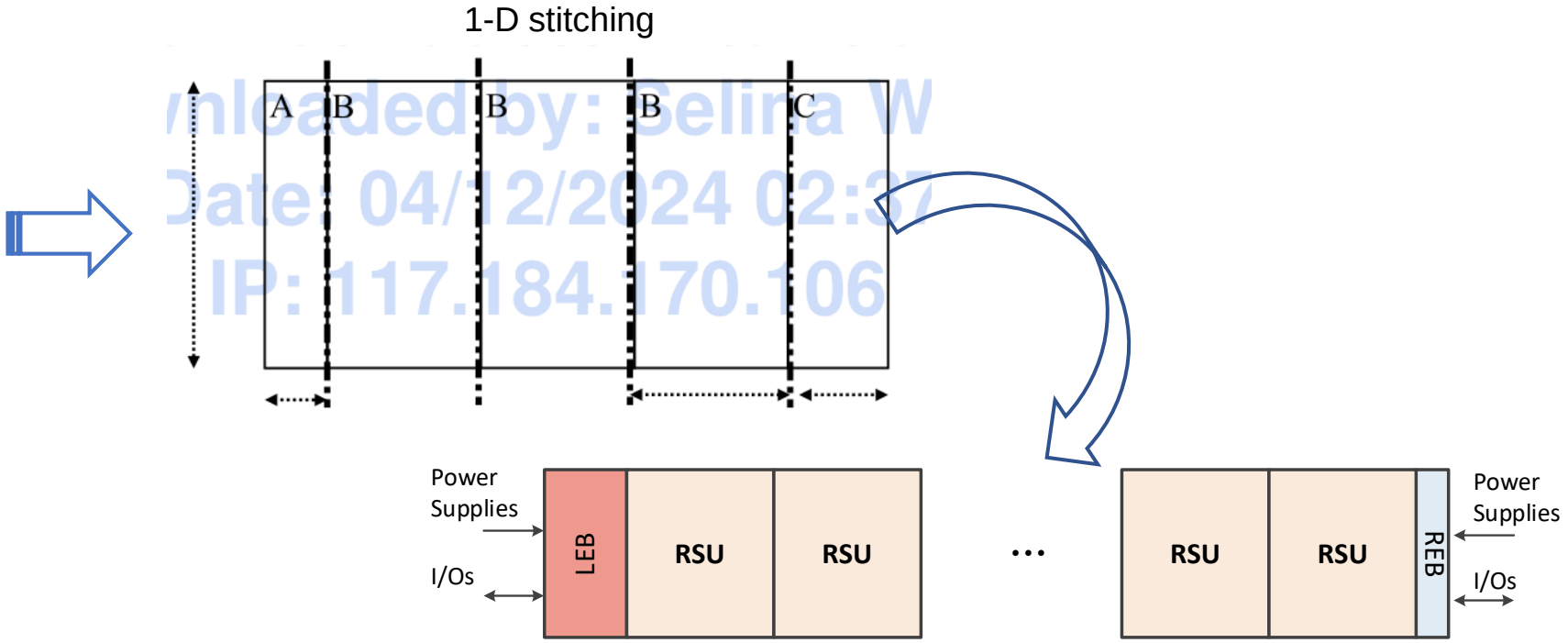
2025-5-15

Taichu-Stitching 尺寸初步考虑

- 基本尺寸边界条件
  - LEB (Left End Block): Width = 4.5 mm, including Data Aggregator, Serializer, PLL, scribe lane, etc.
    - References: ITS3 sensor: 4.5 mm; CEPC TDR 4.154 mm (@65 nm)
  - REB (Right End Block): Width = 0.6 mm, including I/O Pads, power connections, Sealring & scribe

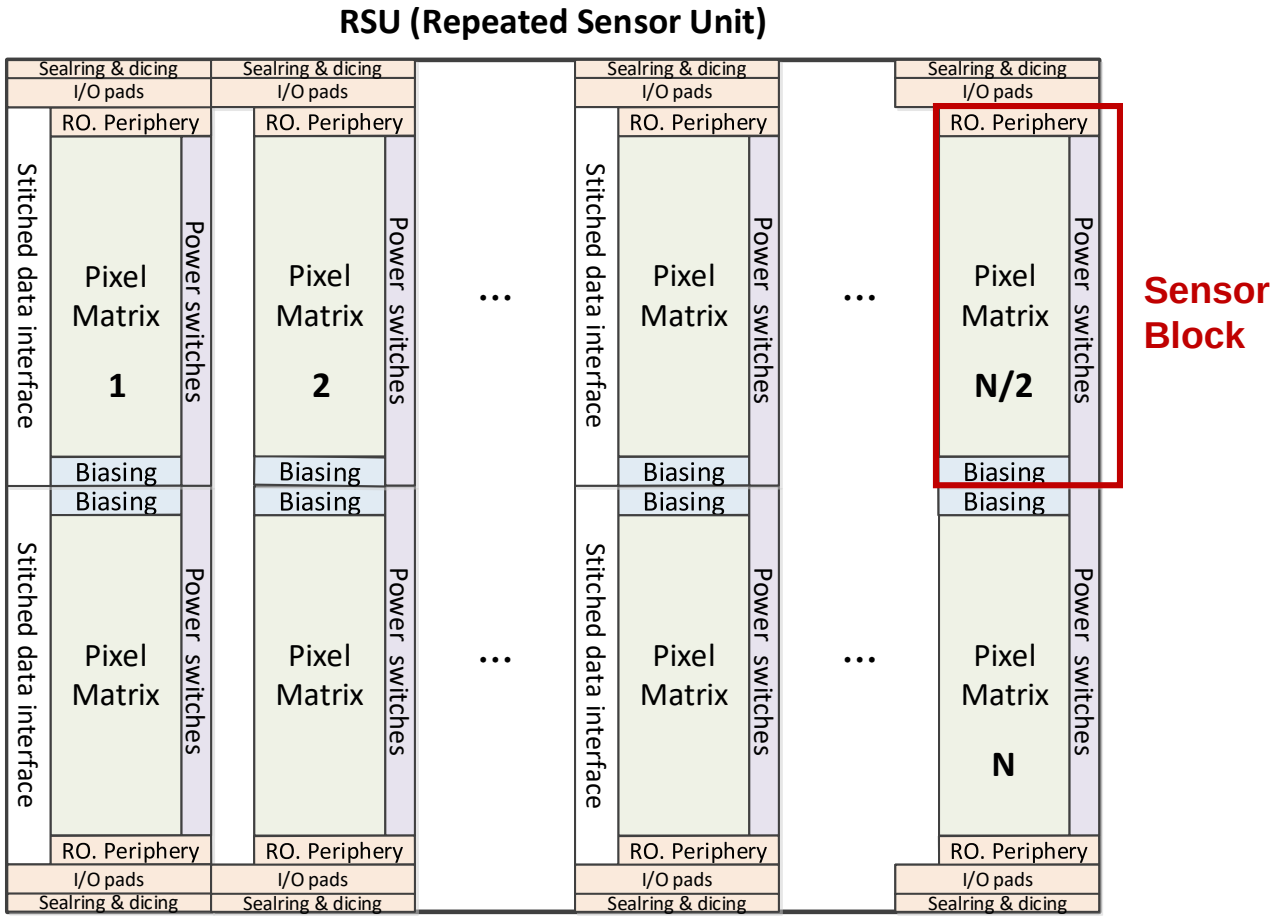


Reticle with segments



RSU (Repeated Sensor Unit) FloorPlan

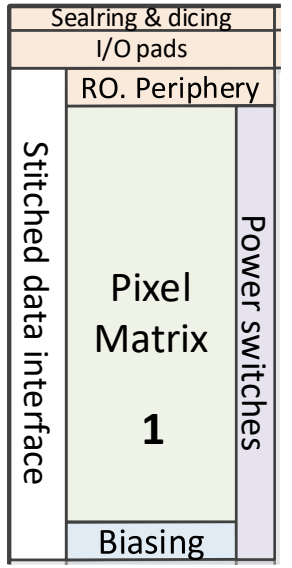
- 1 RSU includes N Sensor Blocks, 4 Stitched data interface, 2 set of I/O pads and Sealring & dicing
- Each Sensor Block has a Pixel Matrix, a Matrix Periphery, a Biasing Generator, a Power switches



Taichu-Stitching 尺寸初步考虑

- RSU各组成部分和尺寸如下：
  - 假设R, C分别代表每个Matrix的行数和列数，N代表Matrix个数。表格中25代表像素间隔为25 μm

	min. Width [μm]	min. Height [μm]	Instance numb.
RSU	N/2*(25*C+30)+200	**2*(25*R + 930)**	1
Pixel Matrix	25*C	25*R	N
Matrix Periphery	25*C +30	320	N
Biasing Generator	25*C	180	N
Power switches	30	25*R + 180	N
Stitched data interface	100	25*R + 180+320	4
Auxiliary I/O pads	RSU width	350	2
Sealring and dicing lane	RSU width	80	2



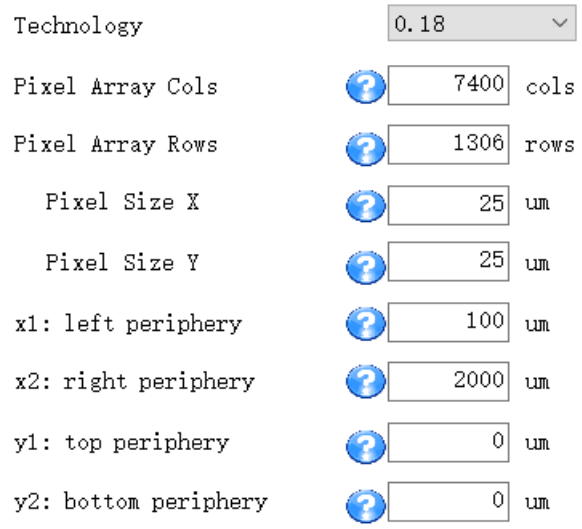
  - Half RSU Height = Matrix_H + Biasing_H + Periphery + I/O +Sealring & dicing = 25*R + 930 μm
  - RSU Width = N/2 * Width of Matrix Periphery + 2* 100 μm

- 单个Matrix面积受数据传输速率S限制：Area < S/HitRate/Cluster/Bits
  - HitRate =13.22 MHz/cm^2 (max @LowZ Bkg)，Cluster size =3, Bits/Pixel = 32 bits;

Taichu-Stitching 尺寸初步方案一

先选定RSU高度

- 初始条件：RSU采用掩模最大高度 (32650 μm) + Matrix 传输数据率@173.32 Mbps (43.33 MHz CLK x 4)
  - Matrix 行数：R = 614 （根据2(25*R + 930)=32650 计算）
  - 单个Matrix面积受传输速率限制：Area < 0.136 cm^2
    - LowZ Bkg 击中率 =13.22 MHz/cm^2，cluster size =3, Bits/Pixel = 32 bits; ➔ Area < 173.32/13.22/3/32
  - Matrix 列数 < 0.136 cm^2/614/25/25 = 35, C= 32 → Width of Matrix = 800 μm
- 使用Stitching Optimization Tool，根据设计规则计算可选子掩模尺寸组合
  - 输入参数：像素尺寸、阵列行/列数量、左/右外围电路的宽度、上/下外围电路的高度



输入参数

Horizontal Optimization Routes

Select	Seg. B Width	Horizontal Repetitions	Seg. A Width	Seg. C Width	Vertical Scribe Width	n	Pixels Lost Horiz.
☑	18000	10	600	4500	900	3	0
☐	16350	11	600	4500	350	3	0
☐	15000	12	600	4500	2400	2	0
☐	13800	13	925	4500	1475	2	0
☐	13800	13	900	4500	1500	2	1
☐	13800	13	875	4500	1525	2	2
☐	13800	13	850	4500	1550	2	3
☐	13800	13	825	4500	1575	2	4
☐	13800	13	800	4500	1600	2	5
☐	13800	13	775	4500	1625	2	6
☐	13800	13	750	4500	1650	2	7
☐	13800	13	725	4500	1675	2	8

输出可选子掩模尺寸

Taichu-Stitching 尺寸初步方案一

- 可选布局 1
  - RSU width = 17625 μm，Matrix width = 830 μm

  → N/2= [17625/830] = 21 (R = 614, C=32)

	Width [μm]	Height [μm]	Instance numb.	Percent area
RSU	17625	32650	1	100 %
Pixel Matrix	800	15350	42	89.63 %
Matrix Periphery	830	320	42	1.94 %
Biasing Generator	800	180	42	1.05 %
Power switches	30	15530	42	3.40 %
Stitched data interface	97.5	15850	4	1.057%
Auxiliary I/O pads	17625	350	2	2.14 %
Sealring and dicing lane	17625	125	2	0.77 %

Global Status Passed

	Min	Max	Current	Status
Vertical Scribe Width	160	3000	775	Pass
Horizontal Scribe Height	320	N/A	320	Pass
Total Width On Mask	0	25880	24125	Pass
Total Height On Mask	N/A	N/A	N/A	
Width Of Horzintal Repeating Segment	8500	N/A	17625	Pass
Height Of Vertical Repeating Segment	16340	32680	32650	Pass
Repetition of segment B in X directions.	2	N/A	10	Pass
Repetition of segment D in Y directions.	N/A	N/A	N/A	
Ratio Between Images Widths 2/1 (n)	1	30	3	Pass
Ratio Between Images Heights 3/1 (m)	N/A	N/A	N/A	
Product Diagonal	0	190000	184266	Pass
Number Of Exposures On Wafer	1	120	70	Pass
Pixel Repetition In X Direction	705	705	705	Pass
Pixel Repetition In Y Direction	N/A	N/A	N/A	
Width Of Non-repeating segment (A)	100	N/A	600	Pass
Width Of Non-repeating segment (C)	2000	N/A	4500	Pass
Height Of Non-repeating segment (A)	15000	N/A	32650	Pass
Height Of Non-repeating segment (G)	N/A	N/A	N/A	
Non-repeating Image Height	1020	N/A	32970	Pass
Non-repeating Image Width	1020	N/A	5875	Pass

优点：产品尺寸大（H: 32650, W: 181600）

缺点：数据接口数量太多（420），可以考虑RSU内部数据汇总，减少与左端部的数据接口数量

Taichu-Stitching 尺寸初步方案二

先选定RSU高度

- 初始条件：RSU采用掩模最大高度 (32650 μm) + Matrix 传输数据率@346.67 Mbps (43.33 MHz CLK x 8)
  - Matrix 行数：R = 614 （根据2(25*R + 930)=32650 计算）
  - 单个Matrix面积受传输速率限制：< 0.273 cm^2
  - Matrix 列数 < 0.273 cm^2/614/25/25 = 70, C = 64 → Width of Matrix = 1600 μm

- 可选布局：RUS数量 = 10, RSU width=18150 μm

  → N/2= [18150/1630] = 11，接口数量 220

进一步提高传输速率代价较大，考虑减小RUS高度

	Width [μm]	Height [μm]	Instance numb.	Percent area
RSU	18150	32650	1	100 %
Pixel Matrix	1600	15350	22	91.18 %
Matrix Periphery	1630	320	22	1.94 %
Biasing Generator	1600	180	22	1.07 %
Power switches	30	15530	22	1.73 %
Stitched data interface	110	15850	4	1.18 %
Auxiliary I/O pads	18150	350	2	2.14 %
Sealring and dicing lane	18150	125	2	0.77 %

Taichu-Stitching 尺寸初步方案三

先选定RSU高度

- 初始条件：RSU采用TDR方案高度 (17450 μm) + Matrix 传输数据率@173.32 Mbps (43.33 MHz CLK x 4)
  - Matrix 行数：R =310（根据2(25*R + 930)=17450 计算）
  - 单个Matrix面积受传输速率限制：< 0.136 cm^2
  - Matrix 列数 < 0.136 cm^2/310/25/25 = 70, 取C= 64 → Width of Matrix = 1600 μm
  - 可选布局：RUS数量 = 10, RSU width = 18150 μm

    → N/2= [18150/1630] = 11，接口数量220

- RSU采用TDR方案高度 (17450 μm) + Matrix 传输数据率@346.67 Mbps
  - N = 12, RUS数量10，接口数量120 ; R=310, C = 118, RSU width= 18150 μm.

	Width [μm]	Height [μm]	Instance numb.	Percent area
RSU	18150	17450	1	100 %
Pixel Matrix	1600	7750	22	86.13%
Matrix Periphery	1630	320	22	3.62 %
Biasing Generator	1600	180	22	2.00 %
Power switches	30	7930	22	1.65 %
Stitched data interface	110	8250	4	1.15 %
Auxiliary I/O pads	18150	350	2	4.01 %
Sealring and dicing lane	18150	125	2	1.43 %

Taichu-Stitching 尺寸初步方案四

先选定传输数据率

- 初始条件：Matrix 传输数据率@ 173.32 Mbps
  - 单个Matrix面积受传输速率限制：< 0.136 cm^2
    → Matrix 像素数量 R*C < 21760
  - 根据设计规则，16420 μm < RSU高度 < 32680 μm (291< R < 616)，RSU width > 8500 μm → RSU 像素个数 > 582 x 332

  ➔ N > 582 x 332/21760 ➔ N > 9
- 遍历N = 10、12、14… 2n，通过stitch tool计算满足设计规则的布局，找到能满足条件的最小的N
  - N=20, RSU数量 = 9，接口数量 =180，R= 304, C = 70

Select	Seg. B Width	Horizontal Repetitions	Seg. A Width	Seg. C Width	Vertical Scribe Width	n	Pixels Lost Horiz.
☐	18825	9	675	4500	1100	3	15
☐	18825	9	650	4500	1125	3	16
☐	18825	9	625	4500	1150	3	17
☑	18825	9	600	4500	1175	3	18
☐	15450	11	600	4500	2625	2	0
☐	14150	12	600	4500	1975	2	0
☐	13050	13	925	4500	1100	2	0
☐	13050	13	900	4500	1125	2	1

	Width [μm]	Height [μm]	Instance numb.	Percent area
RSU	18825	17075	1	100 %
Pixel Matrix	1750	7600	20	82.75 %
Matrix Periphery	1780	320	20	3.54 %
Biasing Generator	1750	180	20	1.96 %
Power switches	30	7780	20	1.45 %
Stitched data interface	512.5	8100	4	5.17 %
Auxiliary I/O pads	18825	350	2	4.10 %
Sealring and dicing lane	18825	87.5	2	1.02 %

Taichu-Stitching 尺寸初步方案五

先选定传输数据率

- 初始条件：Matrix 传输数据率@ 259.98 Mbps
  - 单个Matrix面积受传输速率限制：< 0.204 cm^2
    → Matrix 像素数量 R*C < 32640
  - 根据设计规则，16420 μm < RSU高度 < 32680 μm (291< R < 616)，RSU width > 8500 μm → RSU 像素个数> 582 x 332

  ➔ N > 582 x 332/32640 ➔ N > 6
- 遍历N = 8、10、12… 2n，通过stitch tool计算满足设计规则的布局，找到能满足条件的最小的N
  - N=14, C = 64, R =508, RSU数量 = 9，接口数量=126

Select	Seg. B Width	Horizontal Repetitions	Seg. A Width	Seg. C Width	Vertical Scribe Width	n	Pixels Lost Horiz.
☐	13250	8	625	4500	1500	2	15
☐	13250	8	600	4500	1525	2	16
☐	11800	9	825	4500	575	2	0
☐	11800	9	800	4500	600	2	1
☐	11800	9	775	4500	625	2	2
☐	11800	9	750	4500	650	2	3
☐	11800	9	725	4500	675	2	4
☐	11800	9	700	4500	700	2	5
☐	11800	9	675	4500	725	2	6
☐	11800	9	650	4500	750	2	7
☐	11800	9	625	4500	775	2	8
☑	11800	9	600	4500	800	2	9
☐	10650	10	600	4500	225	2	0

	Width [μm]	Height [μm]	Instance numb.	Percent area
RSU	11800	27300	1	100 %
Pixel Matrix	1600	12700	14	88.31 %
Matrix Periphery	1630	320	14	2.27 %
Biasing Generator	1600	180	14	1.25 %
Power switches	30	12880	14	1.68 %
Stitched data interface	195	13200	4	3.20 %
Auxiliary I/O pads	11800	350	2	2.56 %
Sealring and dicing lane	11800	100	2	0.73 %

Taichu-Stitching 尺寸初步方案六

先选定传输数据率

- 初始条件：Matrix 传输数据率@ 259.98 Mbps
  - 单个Matrix面积受传输速率限制：< 0.204 cm^2
    → Matrix 像素数量 R*C < 32640
  - 根据设计规则，16420 μm < RSU高度 < 32680 μm (291< R < 616)，RSU width > 8500 μm → RSU 像素个数> 582 x 332

  ➔ N > 582 x 332/32640 ➔ N > 6
- 遍历N = 8、10、12… 2n，通过stitch tool计算满足设计规则的布局，找到能满足条件的最小的N
  - N=14, C =100, R = 320, RSU数量 = 9，接口数量=126

Select	Seg. B Width	Horizontal Repetitions	Seg. A Width	Seg. C Width	Vertical Scribe Width	n	Pixels Lost Horiz.
☐	18150	9	750	4500	800	3	12
☐	18150	9	725	4500	825	3	13
☐	18150	9	700	4500	850	3	14
☐	18150	9	675	4500	875	3	15
☐	18150	9	650	4500	900	3	16
☐	18150	9	625	4500	925	3	17
☑	18150	9	600	4500	950	3	18
☐	16350	10	850	4500	2825	2	0
☐	16350	10	825	4500	2850	2	1
☐	16350	10	800	4500	2875	2	2

	Width [μm]	Height [μm]	Instance numb.	Percent area
RSU	18150	17900	1	100 %
Pixel Matrix	2500	8000	14	86.18 %
Matrix Periphery	2530	320	14	3.49 %
Biasing Generator	2500	180	14	1.94 %
Power switches	30	8180	14	1.06 %
Stitched data interface	220	8500	4	2.30 %
Auxiliary I/O pads	18150	350	2	3.91 %
Sealring and dicing lane	18150	100	2	1.12 %

总结

- 考虑RSU内部独立读出Matrix的读出数据率（ LowZ Bkg 击中率 =13.22 MHz/cm^2，cluster size =3, Bits/Pixel = 32 bits）使用Stitch Tool 计算RSU、LEB、REB尺寸和可行性布局，初步考虑以下几个备选：

	RSU Height [um]	RSU Width [um]	Matrix 行数 R	Matrix 列数 C	Matrix 个数 N	RSU 个数	读出端口数量	Matrix读出速率 [Mbps]	数据位宽* [bits/data]	芯片尺寸 [mm x mm]
1	32650	17625	614	32	42	10	420	173.32	32	32.65 x 181.35
2	32650	18150	614	64	22	10	220	346.67	32	32.65 x 186.60
3	27300	11800	508	64	14	9	126	259.98	30	27.30 x 111.30
4	17900	18150	320	100	14	9	126	259.98	31	17.90 x 168.45
5	17450	18150	310	64	22	10	220	173.32	31	17.45 x 186.60
6	17450	18150	310	118	12	10	120	346.67	31	17.45 x 186.60
7	17075	18825	304	70	20	9	180	173.32	32	17.08 x 174.53

- 经初步讨论，考虑选择方案2和3，其中方案2将采用每个RSU内部数据汇总为6对读出端口方式，即总读出端口减小至60对，传输速率为1.39 Gbps。需要RSU内部集成PLL，下一步会给出具体方案。
- 方案3按照每个Matrix一对读出端口输出，共计126对，传输线所占面积将在下一版方案里考虑。

*数据结构: 8 bit timestamp + column addr. + row addr. + Matrix ID.

Backup

HitRate from Electronics TDR

From Wei Wei

Critical Input from Sub-Det & MDI

Figure 11.1

	Vertex	ITKB	ITKE	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Chn/chip	512*1024/Stch	512*128		128		128	4~16 @common SiPM ASIC				
Data Width	32bit/hit	42bit/hit		40~48bit/hit		48bit/hit	48bit/hit				
Module Size/Link	168.15cm² Half Inner layer	56.00cm² 14 chip/module		128.00cm² 8*4cmSensor/module		461.44cm² Module size	2000 chn 1000 dual bar @1cm with 0.1MIP th		600 GS 120 cell*5 PCB/Aggr Brd		Aggr Brd
Higgs Bkg (MHz/cm²)	3.351	9.45e-4	4.16e-3	1.02e-3	1.40e-3	5.1e-3	0.0165	0.0675	3.0e-4	7.95e-3	2.1e-6
Higgs Data rate/Link(Mbps)	18,031.59	2.22	9.77	6.27	8.57	112.96	1,584	6,480	8.64	228.96	<10
LowZ Bkg (MHz/cm²)	13.22	1.53e-3	5.97e-3	1.82e-3	2.34e-3	5.55e-3	0.0225	0.0975	1.05e-3	1.23e-02	2.67e-6
LowZ Data rate/Link(Mbps)	71,157.78	3.60	14.04	11.15	14.38	122.93	2,160	9,360	30.24	354.24	<10
HighZ Bkg (MHz/cm²)	40.79	5.69e-3	0.021	5.63e-3	7.31e-3	-	0.116	0.501	3.3e-3	7.95e-02	8.87e-6
HighZ Data rate/Link(Mbps)	219,494.63	13.37	50.45	34.56	44.88	-	11,088.00	48,096.00	95.04	2,289.60	<10
Detector Channel/module	1882 equiv chips @Stch & Ladder	2376 modules	1236 modules	7040 modules	6368 modules	496 modules	0.96M chn 480 modules	0.52M chn 260 modules	3.38M chn 5536 Aggr Brds	2.24M chn 3072 Aggr Brds	43.2k ch 72 Aggr Brds
Full Data rate @Higgs (Gbps)	1,983.879	5.281	12.079	44.119	54.579	56.028	760.320	1,684.80	47.831	703.365	<0.72
Full Data rate @LowZ (Gbps)	7,828.952	8.550	17.355	78.506	91.552	60.972	1,036.800	2,433.60	167.409	1,088.225	<0.72
Full Data rate @HighZ (Gbps)	24,149.333	31.770	62.357	243.302	285.808	-	5,322.240	12,504.960	526.141	7,033.651	<0.72

- 1.5 safety factor used for bkgrd rate; VTX includes synchrotron radiation, others not considered

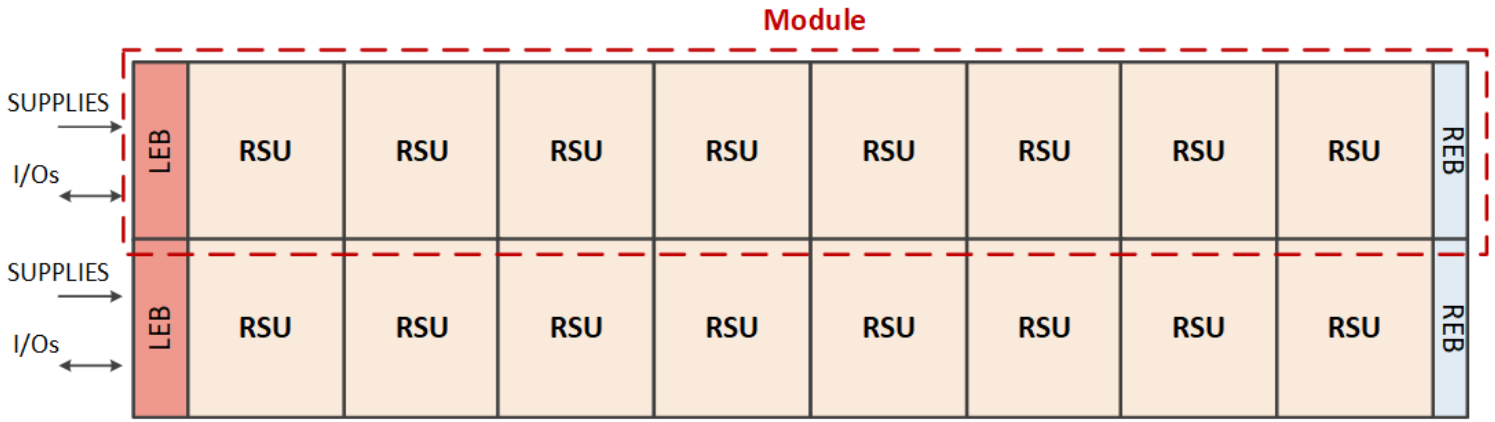
Related to the IDRC recommendation: R.2&3 (Trigger)

4

VTX Ref_TDR

- RSU各组成部分及左右端部模块的尺寸

	Pixel Matrix	Bias	periphery	Stitched interface	switches	RSU	Supply (LEB)	Supply (REB)
Height [mm]	8.409	0.106	0.177	8.409	8.409	17.277	17.277	17.277
Width [mm]	3.296	10	10	0.055	0.019	20	4.154	1.385



Floor Plan of Layer 0