Development of Monolithic Active Pixel Sensors for Future Collider Experiments

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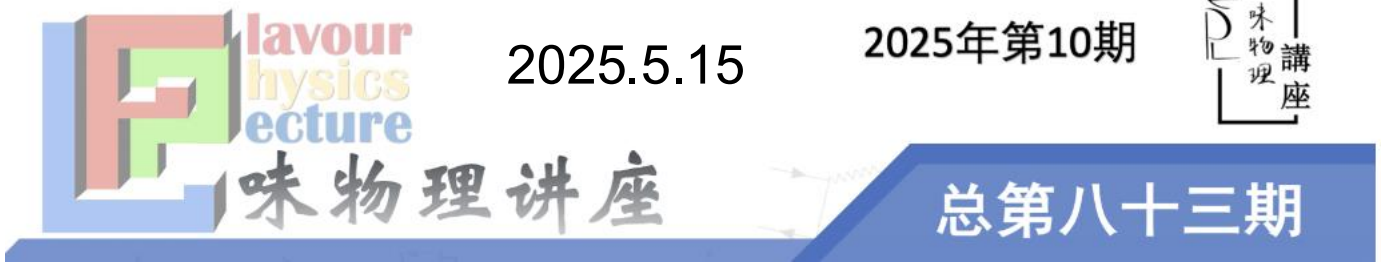
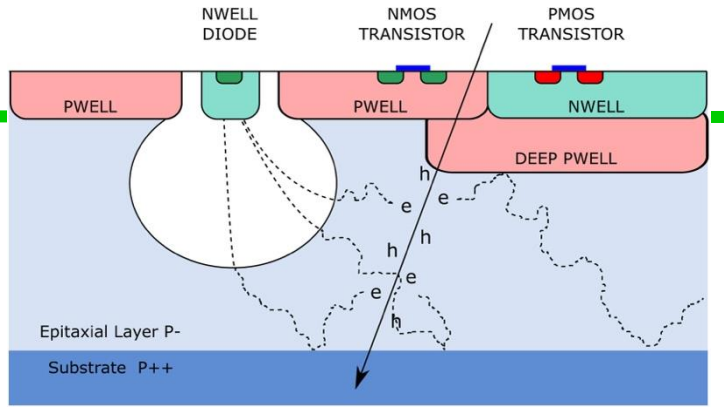
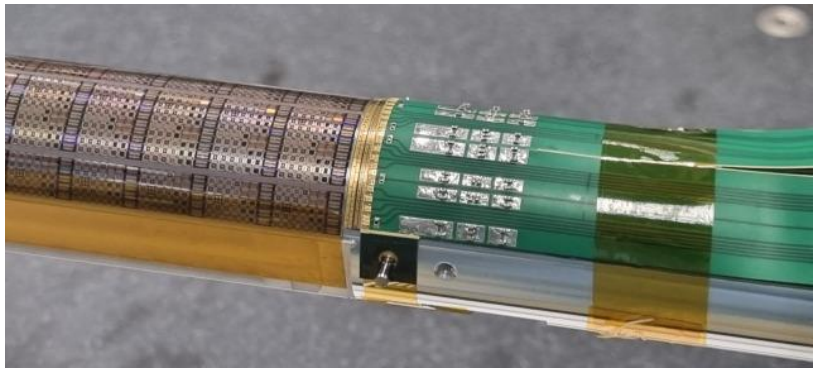


Outline



- Introduction to MAPS
- R&D MAPS for STCF
  - Introduction to STCF and the tracking requirements
  - CharTPix overview
  - MAPS simulation study
  - CharTPix prototype chips design
  - CharTPix-TJ-v0.1 preliminary characterization results
- Prospect of MAPS development
- Summary

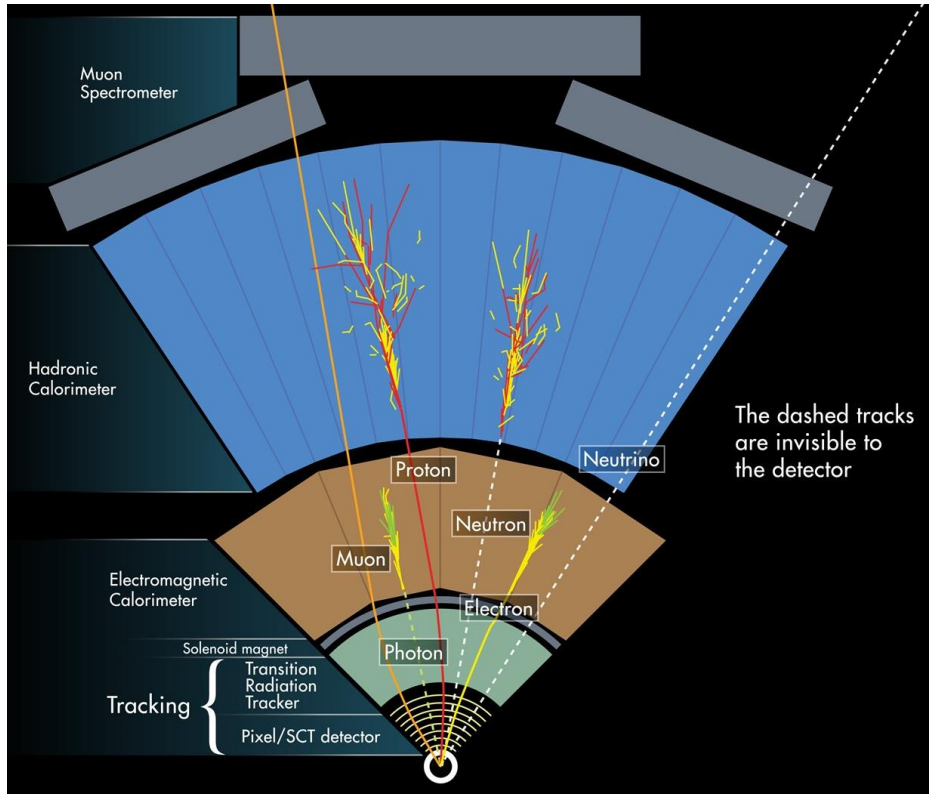
超级陶粲装置
Super Tau-Charm Facility

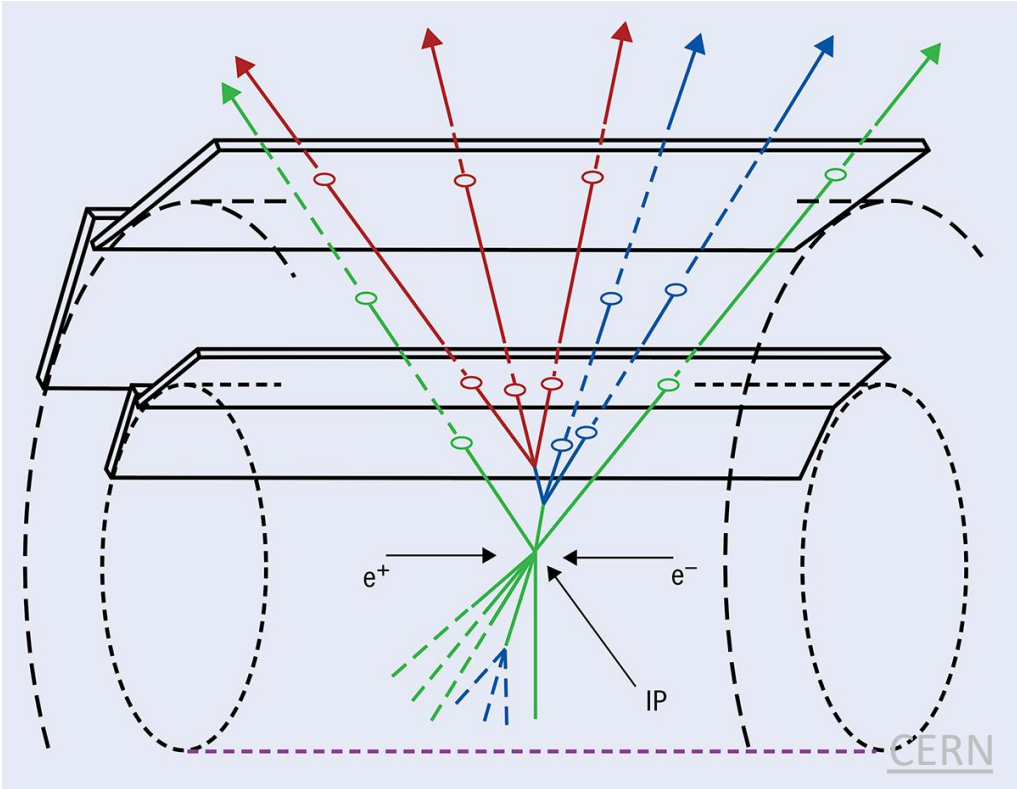


Introduction to MAPS

Tracking and Vertexing

- Tracking and vertexing are indispensable for a typical collider experiment
- Excellent impact parameter resolution is mandatory for reconstruction of secondary vertices
  - Heavy flavor vertex (c and b vertex)

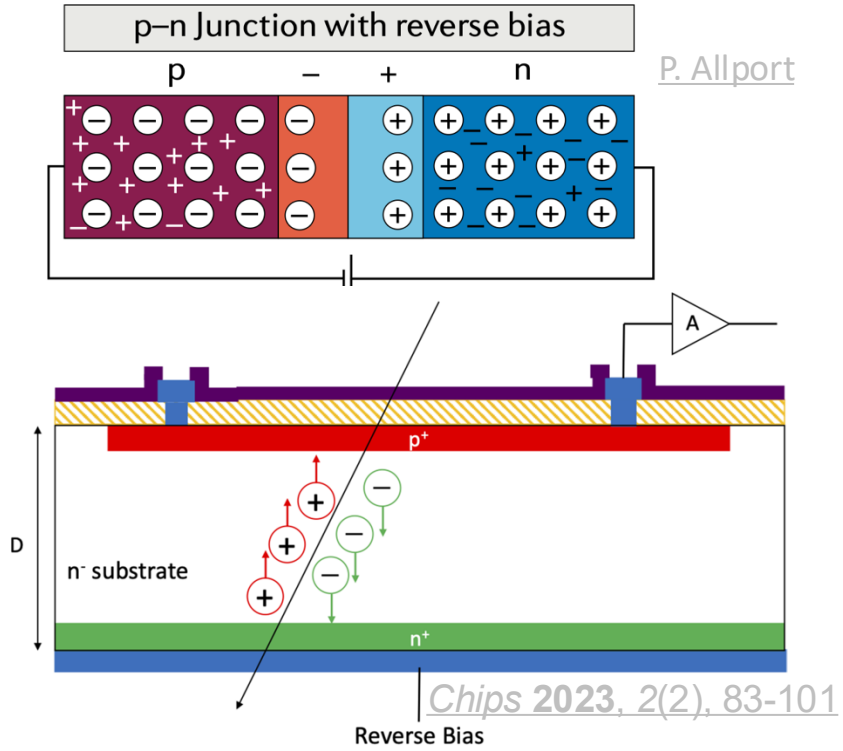




Silicon detectors

- Widely used in HEP experiments for vertexing and tracking
  - High signal-to-noise ratio
  - Excellent spatial resolution (better than 10μm)
  - Excellent timing resolution (better than 1ns)
  - Compact, high-rate capability, readout speed, radiation hardness …

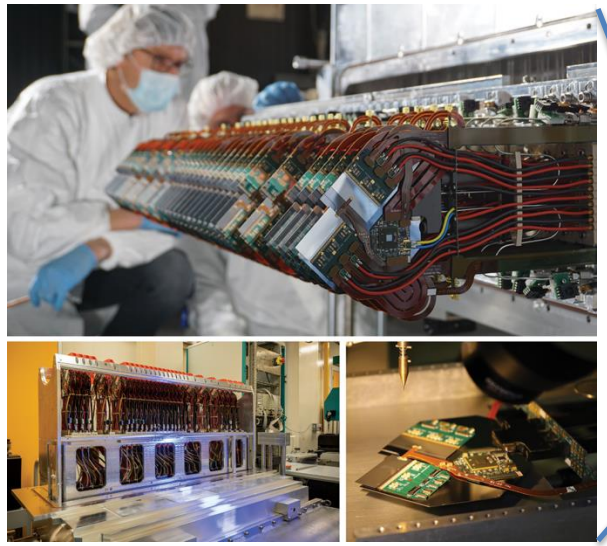
UT

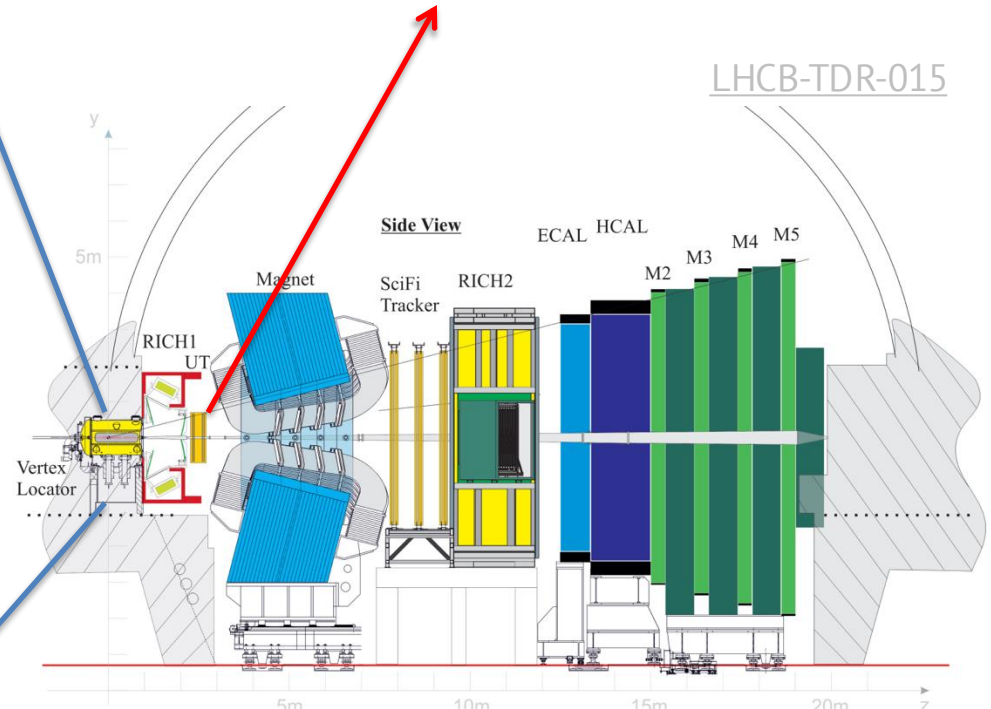


P. Allport

Chips **2023**, *2*(2), 83-101

VELO

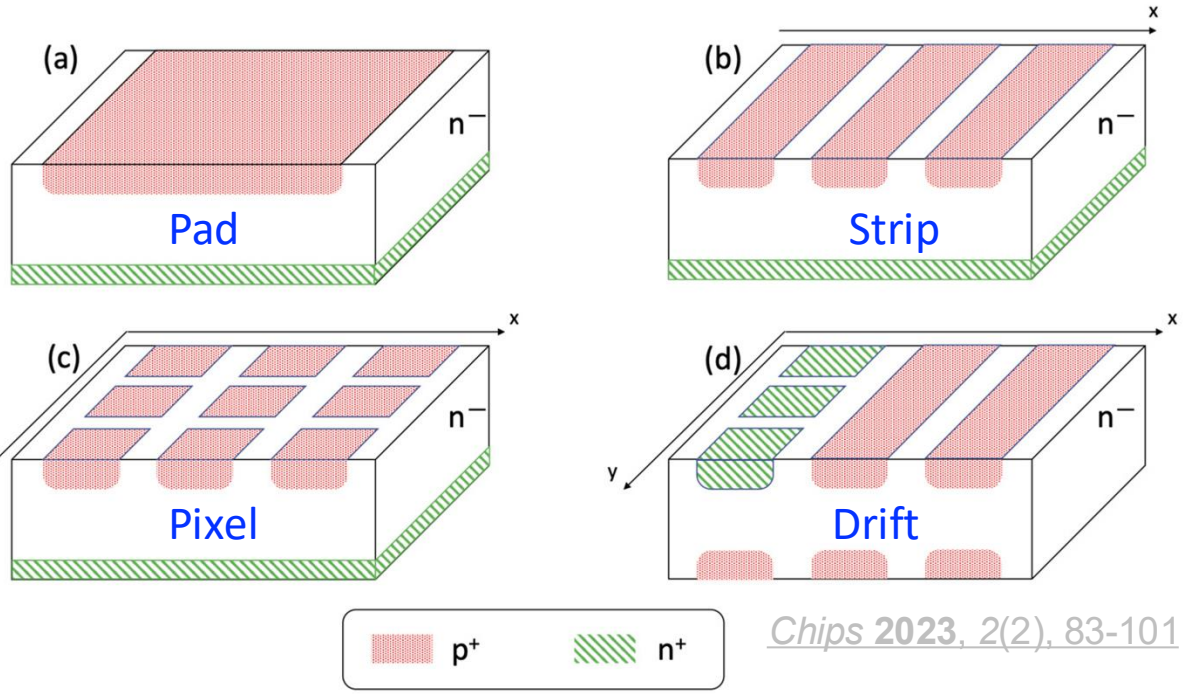




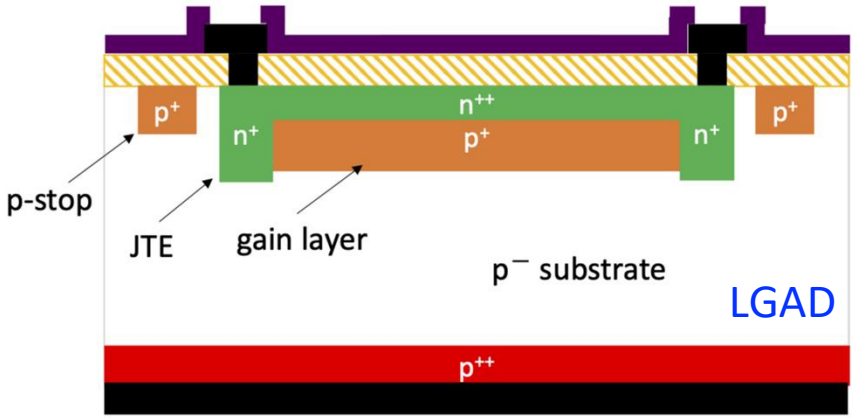
LHCB-TDR-015

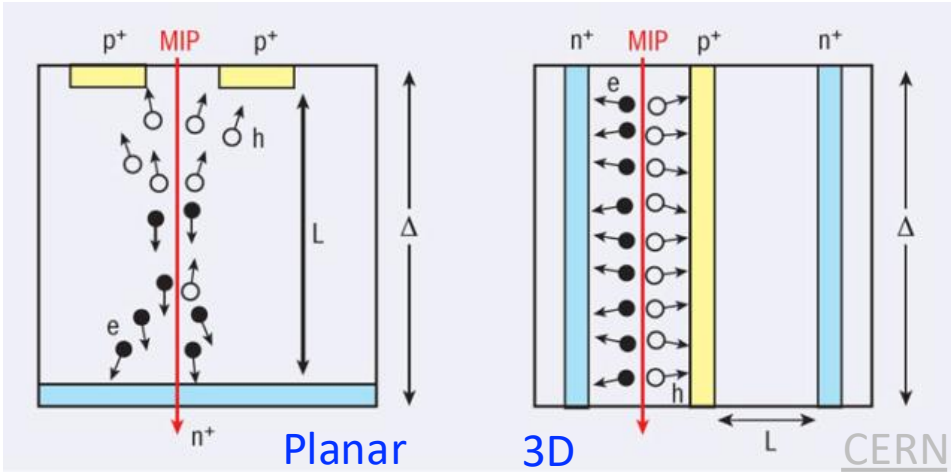
Common silicon detectors types

- Geometry
  - Planar: Pad, 1D (strip), 2D (pixel)
  - 3D
- Signal internal amplification
  - No gain
  - With avalanche gain: LGAD, APD…
- Readout architecture
  - Hybrid
  - Monolithic



Chips **2023**, *2*(2), 83-101



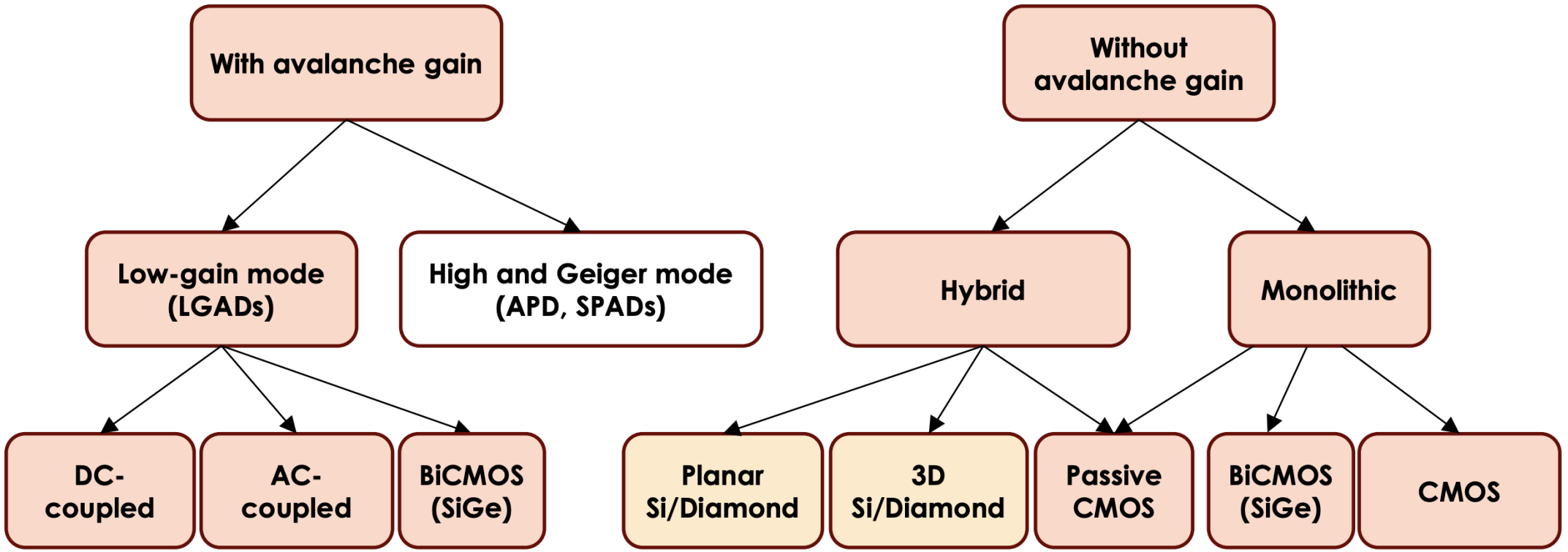


Common silicon detectors types

ECFA
European Committee for Future Accelerators

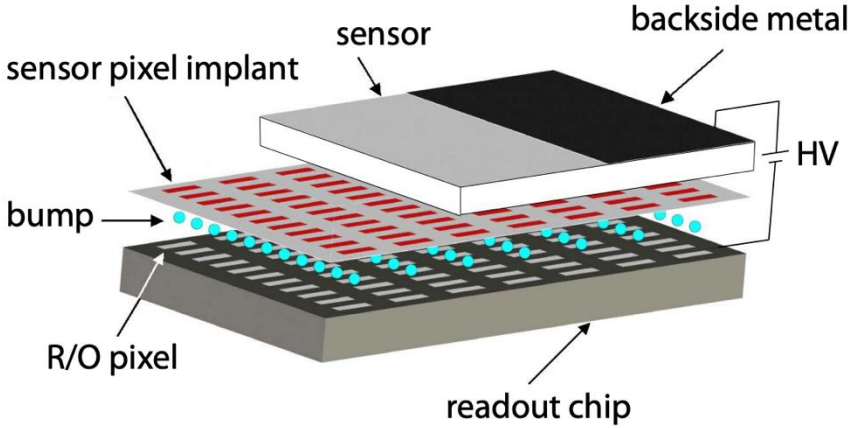
ECFA Detector R&D Roadmap, TF3(2021)

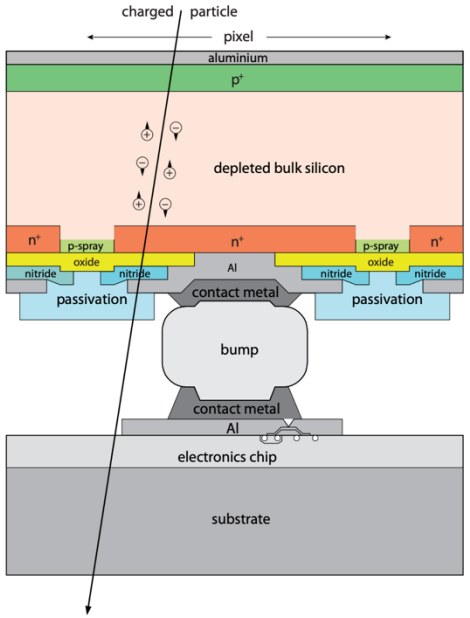
Solid state detectors for future (4D) trackers



Silicon pixels: Hybrid vs Monolithic

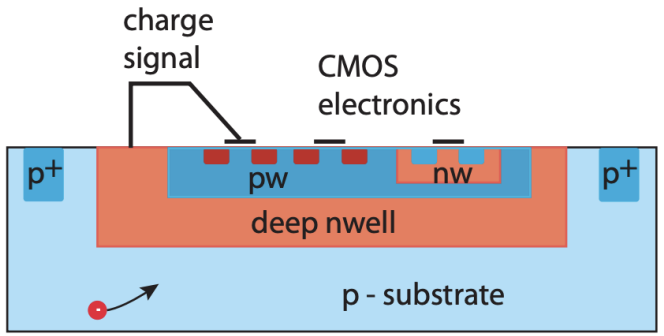
Radiation hardness
High hit-rate



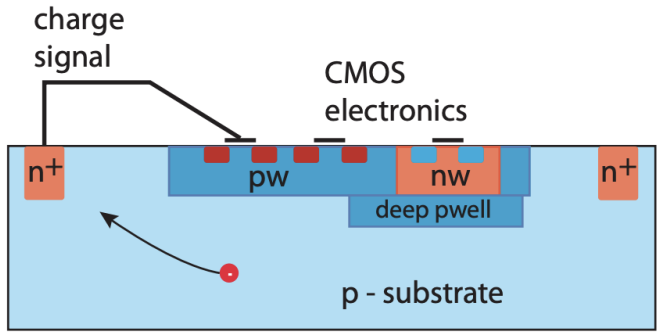


Hybrid pixels:

- Radiation hard
- Mature technologies, widely used in ATLAS/CMS/LHCb
- Disadvantages：
  - Hybridization: complex, expensive
  - Relatively large material budget



(a) Large fill-factor



(b) Small fill-factor

Monolithic pixels:

- High granularity
- Low material budget
- Lower cost, based on commercial CMOS technologies
- Disadvantages：
  - Less radiation hardness

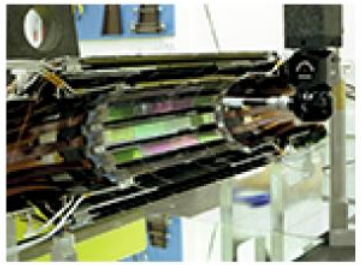
Granularity, Low mass

Rept.Prog.Phys. 81 (2018) 6, 066101

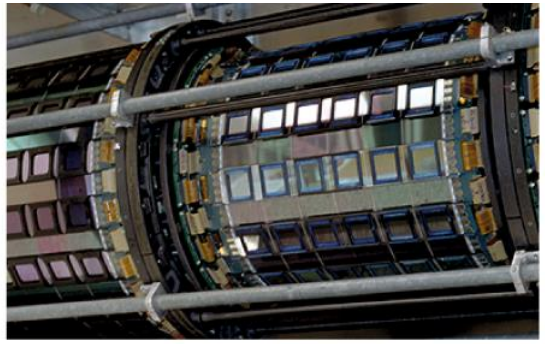
Evolution of silicon detectors in HEP

Philip Allport, *Nat Rev Phys* **1**, 567–576 (2019)

- Silicon strips
- Multiplexing ASICs
- CCDs



DELPHI



CDF

- CMOS MAPS
- Silicon-on-insulator pixels
- Vertical 3D integration

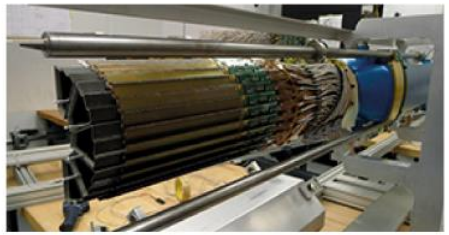
CMS

1980 **1990** **2000** **2010**

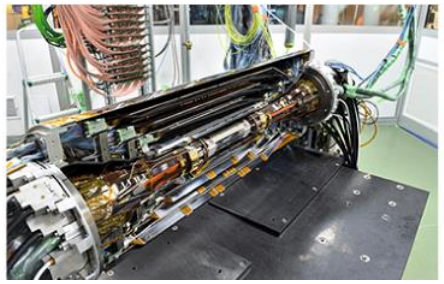
NA14

- Hybrid planar pixels
- Drift detectors
- DEPFET
- Hybrid 3D pixels

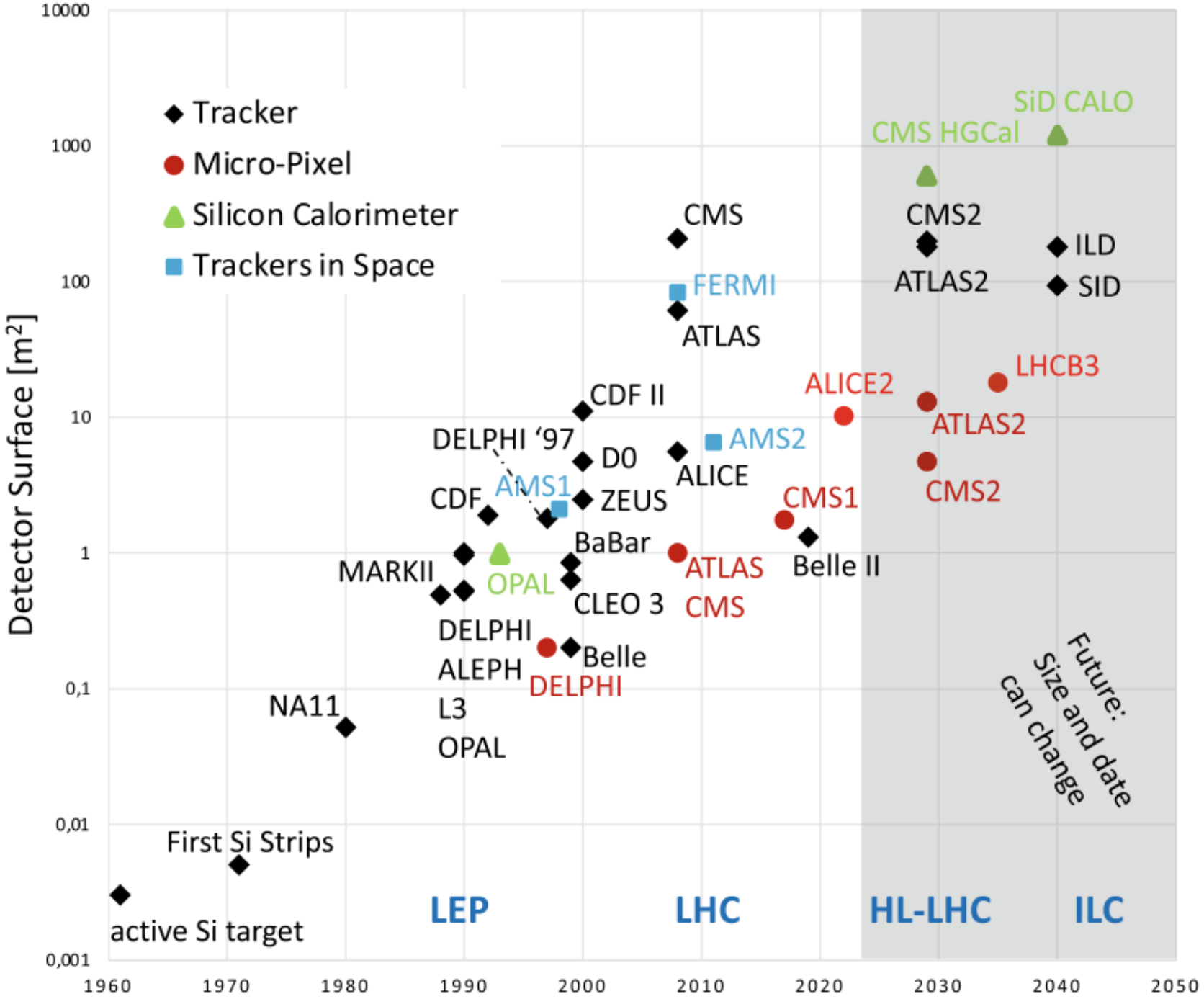
STAR



Belle II

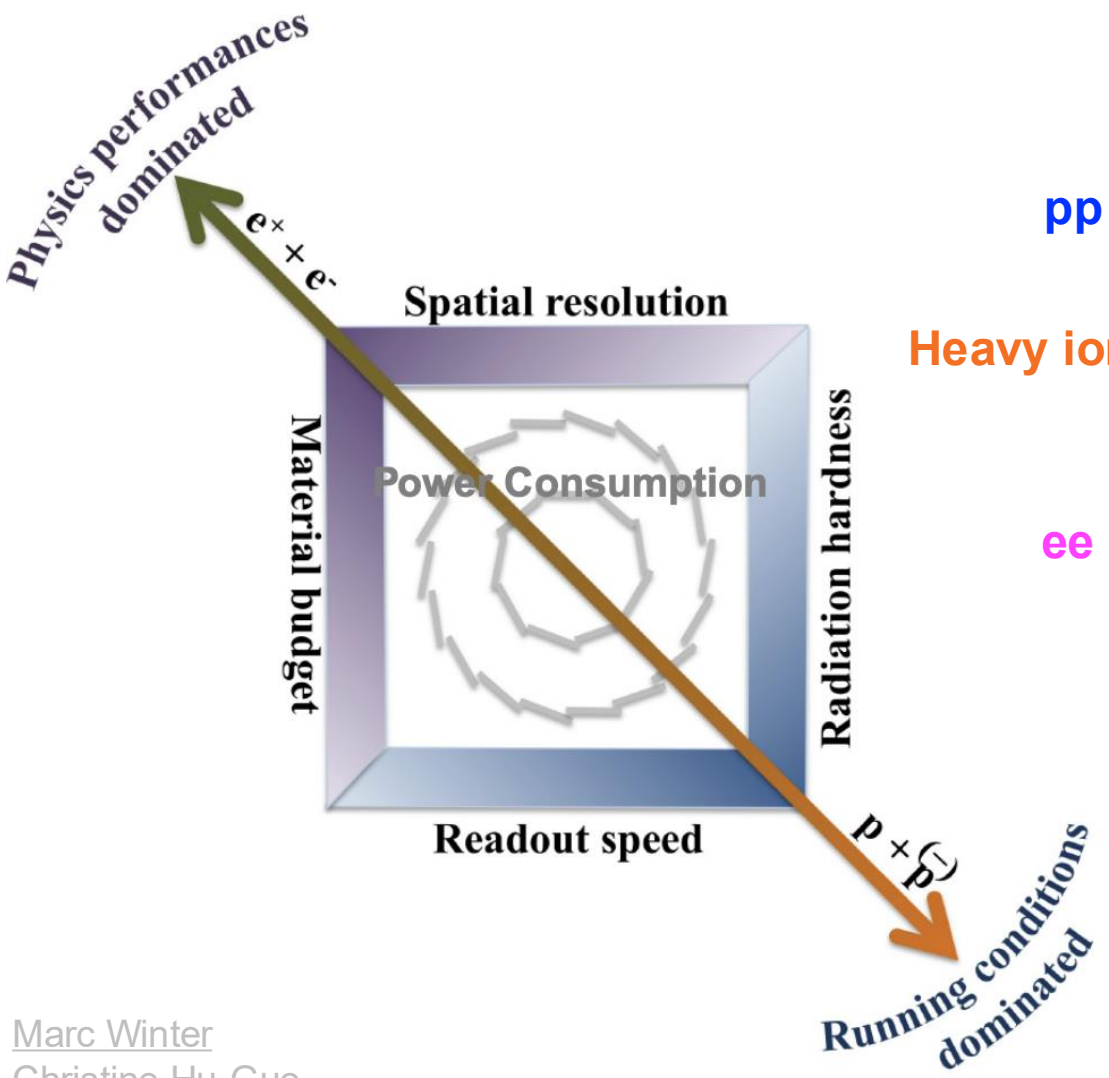


- Depleted MAPS
- Fast-timing detectors
- Hybrid MAPS



Frank Hartmann

The Challenges of a Vertex Detector



Marc Winter
Christine Hu-Guo

	Fluence [n_{eq}/cm^2 per lifetime]	Ion. Dose [Mrad per lifetime]
pp: LHC (10^{34} $cm^{-2}s^{-1}$)	2 x 10^{15}	79
pp: HL-LHC (10^{35} $cm^{-2}s^{-1}$)	2 x 10^{16}	>500
Heavy ion: LHC HI (6 x 10^{27} $cm^{-2}s^{-1}$)	10^{13}	0.7
Heavy ion: RHIC (8 x 10^{27} $cm^{-2}s^{-1}$)	few 10^{12}	0.2
ee: SuperKEKB (10^{35} $cm^{-2}s^{-1}$)	~3 x 10^{12}	10
ee: ILC (10^{34} $cm^{-2}s^{-1}$)	10^{12}	0.4
CEPC	2~6×10^{12}	1~3 Mrad/year

N. Wermes, CERN Seminar, 29/11/2013 Lifetime: LHC, HL-LHC: 7 years; ILC: 10 years; others: 5 years

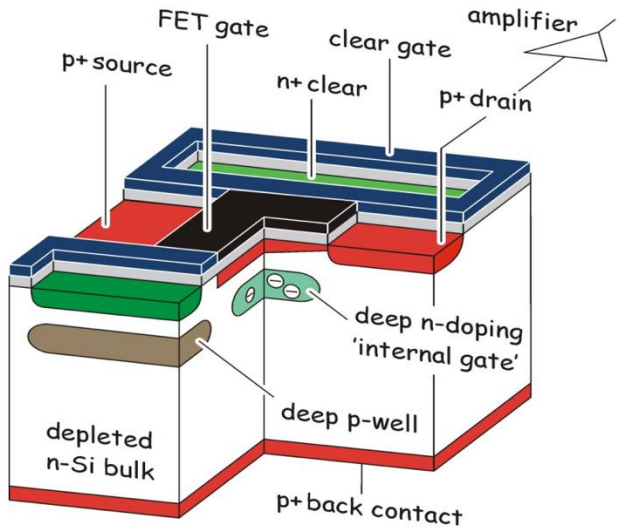
- Conflict between physics performance driven parameters and running condition constraints
- Ultimate performance on all specifications cannot be reached simultaneously
- There is no single technology best suited to all applications
- Motivation for continuous R&D

Monolithic pixels

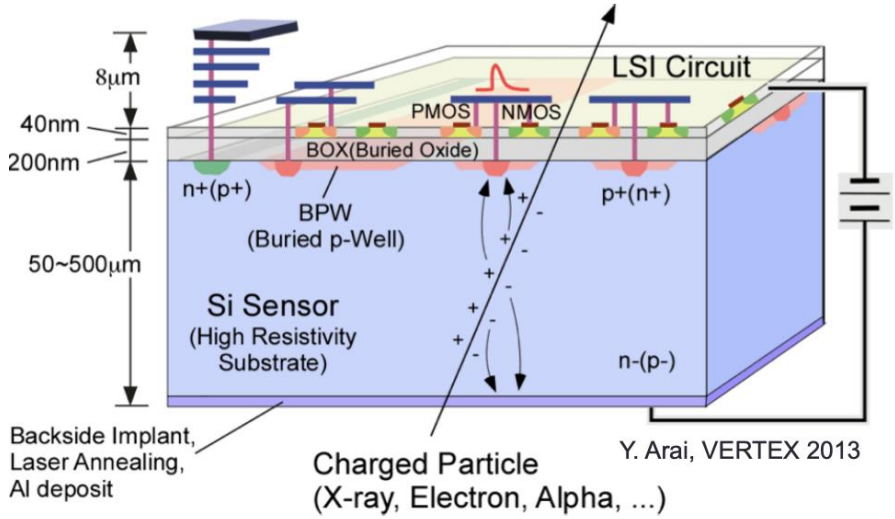
- Ideally one would like to achieve:
  - Low capacitance → low power consumption
  - Good S/N
  - ~ns time resolution
  - High rate-capability (>10 MHz/mm^2)
  - Full depletion → radiation tolerance

No unique solution for all yet, but some aspects addressed

- DEpleted P-channel Field Effect Transistor(DEPFET)
  - Eg. Belle2 vertex detector
- Silicon-on-insulator (SOI)
- CMOS
  - High-resistivity CMOS
  - High-voltage CMOS



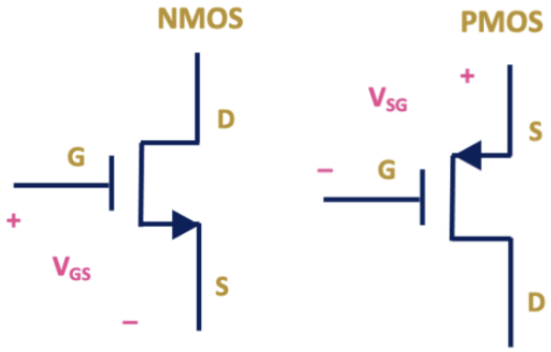
DEPFET *Front.in Phys.* 10 (2022) 896212

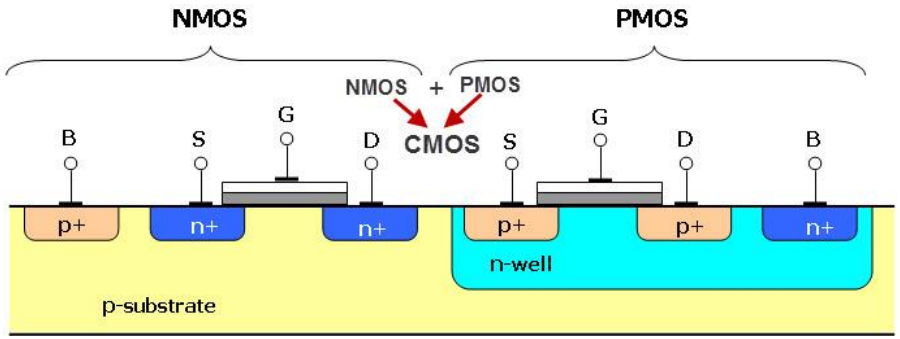


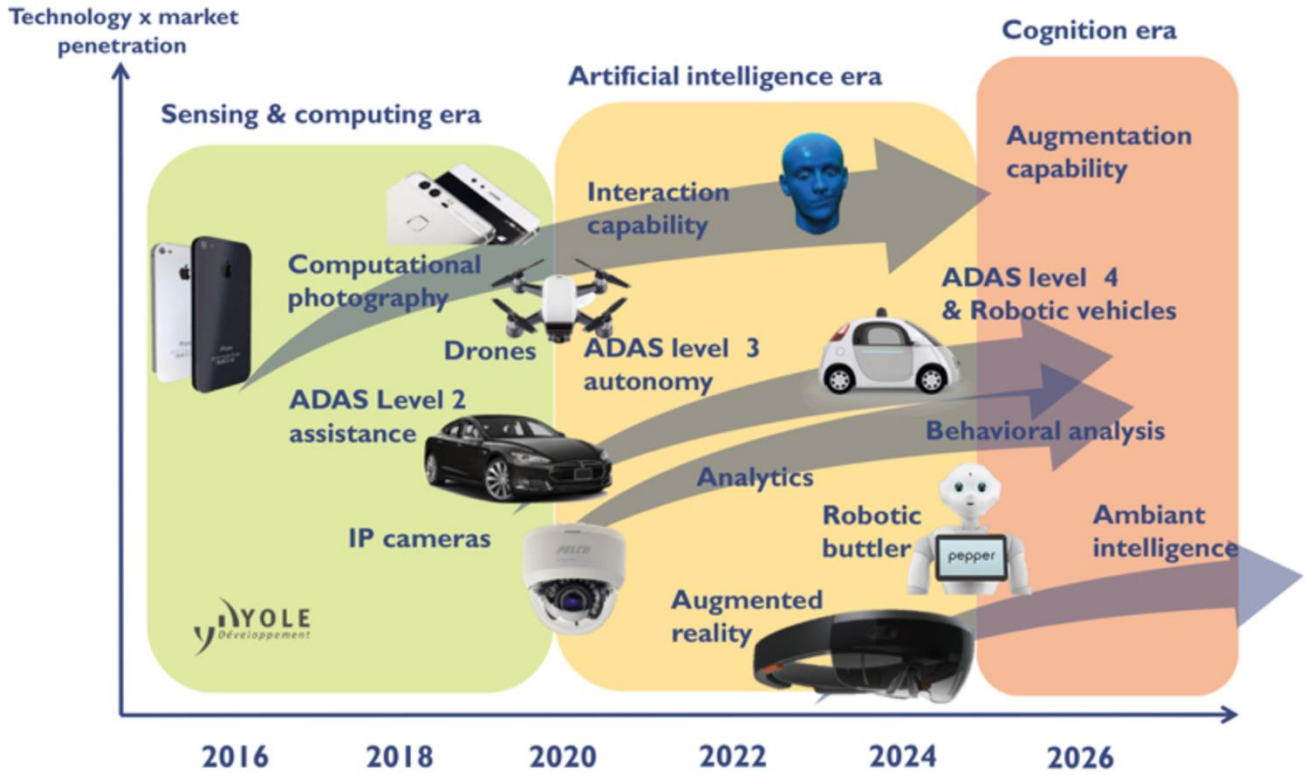
SOI

CMOS Technology

- C.M.O.S. ≡ Complementary Metal-Oxide-Semiconductor







SK Hynix Hi-5022Q, 1/2.8″ Format, 50MP Resolution, 0.64µm Pixel Pitch, Stacked Back-Illuminated CMOS Image Sensor Device Essentials Folder

TechInsights

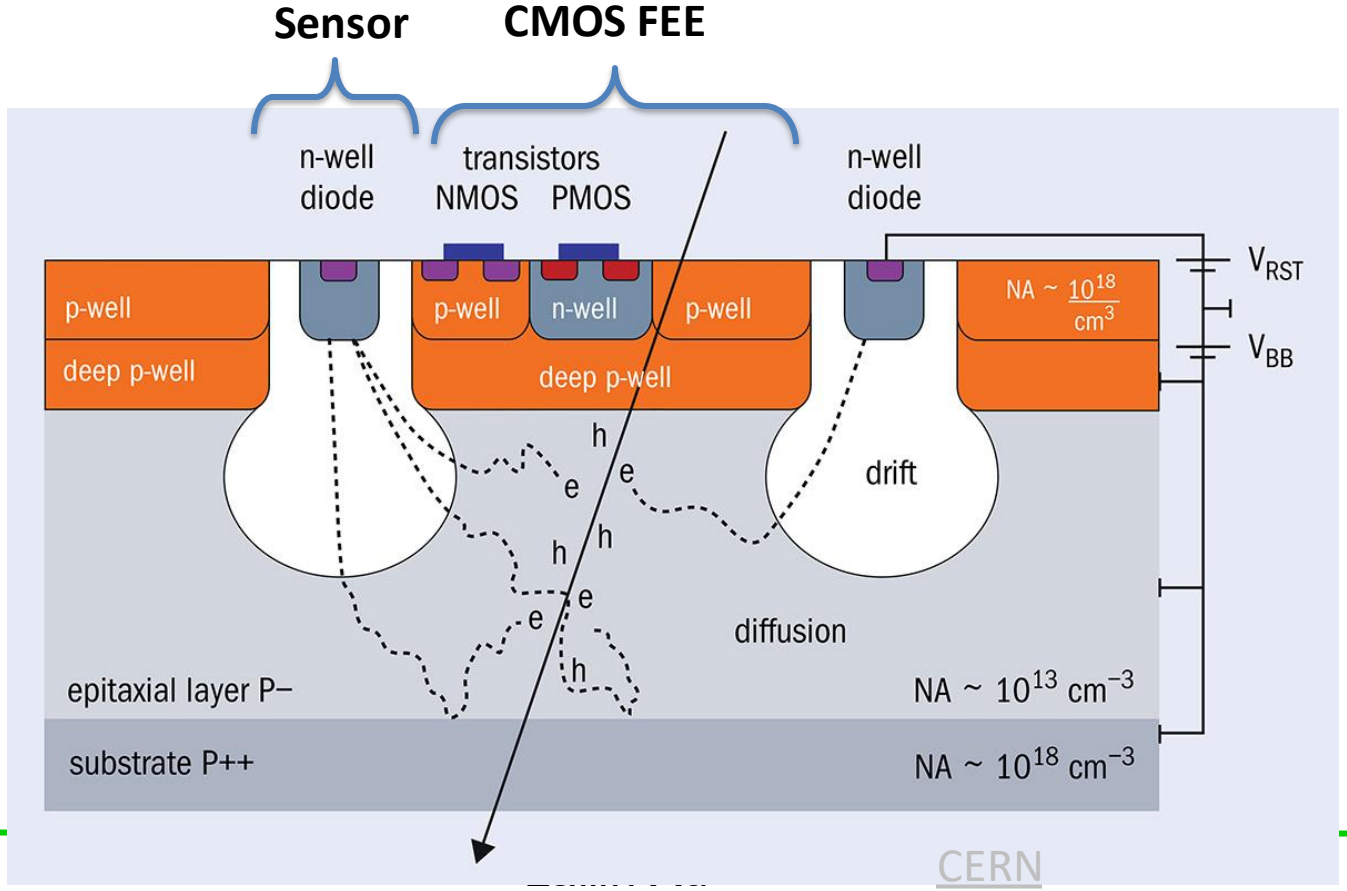
Why is it so popular?

- Reliable (industry-standard)
- Low-power consumption
- Low-cost
- Scalable (millions of transistors are integrated into a single chip)

Moore's law: The number of transistors in a dense integrated circuit (IC) doubles about every two years

CMOS MAPS

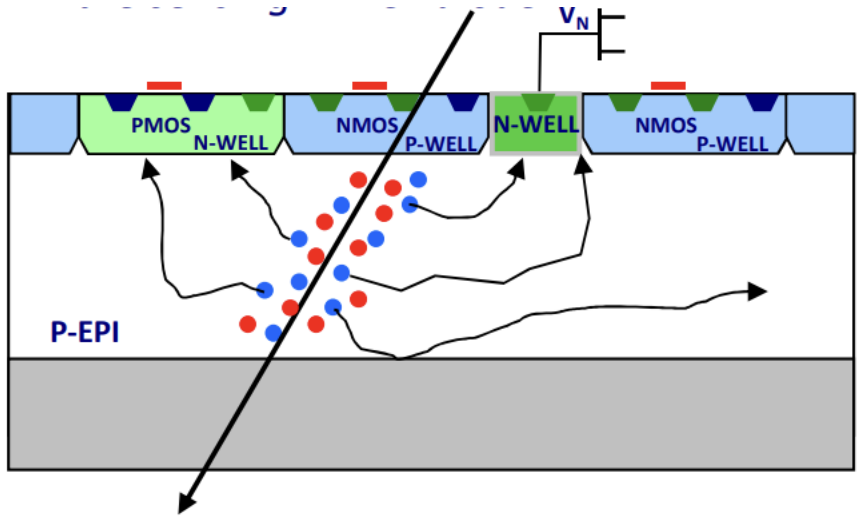
- CMOS pixel sensors exploit the fabrication processes used in industry for mass production of integrated circuits
- CMOS MAPS: sensor + FEE in the same die
  - Integration of sensitive volume (epitaxial layer) and front-end read-out electronics(FEE) on the same substrate



MAPS Process Evolution

1st generation of CMOS MAPS, 2000

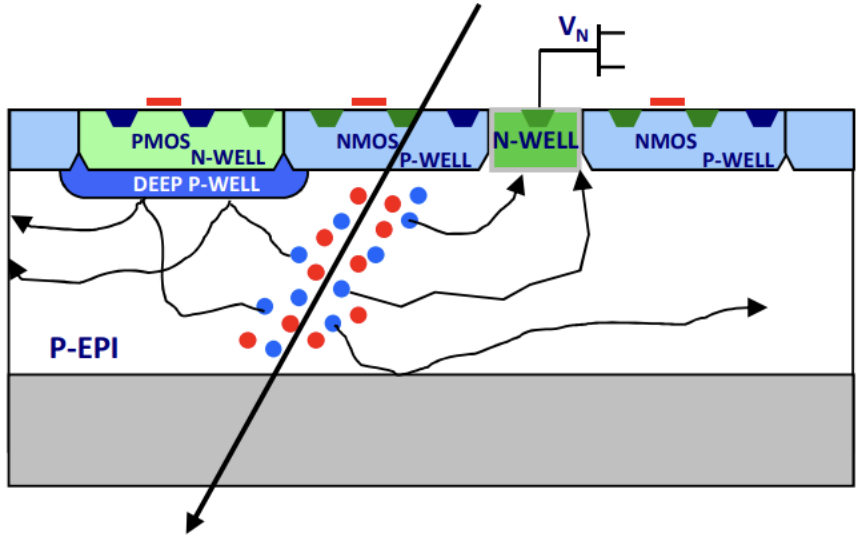
Twin well process: 0.6-0.35 μm



- Use of PMOS in pixel array is not allowed: any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode
- Limits choice of readout architecture strategy
- Already demonstrate excellent performances

2nd generation of CMOS MAPS, 2010

Quadruple well process (deep P-well): 0.18 μm



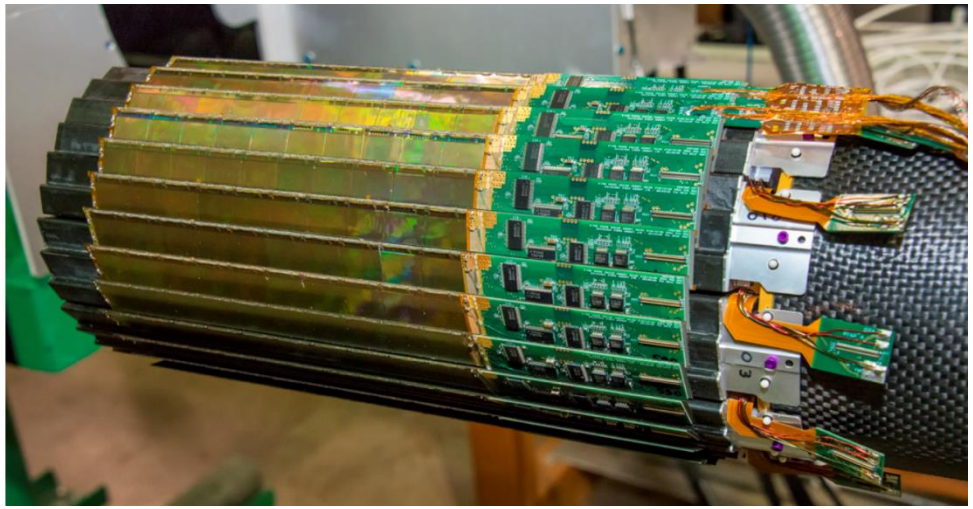
- N-well used to host PMOS transistors is shielded by deep P-well
- Both types of transistors can be used
- Widens choice of readout architecture strategies

STAR Heavy Flavour Tracker (HFT) at RHIC

- Installed in 2013, the first MAPS based vertex tracker at a collider experiment

arXiv:1710.02176

  - MIMOSA family developed by IPHC Strasbourg
  - 0.35 μm twin-well CMOS technology (N-well, P-well)
    - With only NMOS transistors, not fully CMOS
  - Charge collection mostly by diffusion



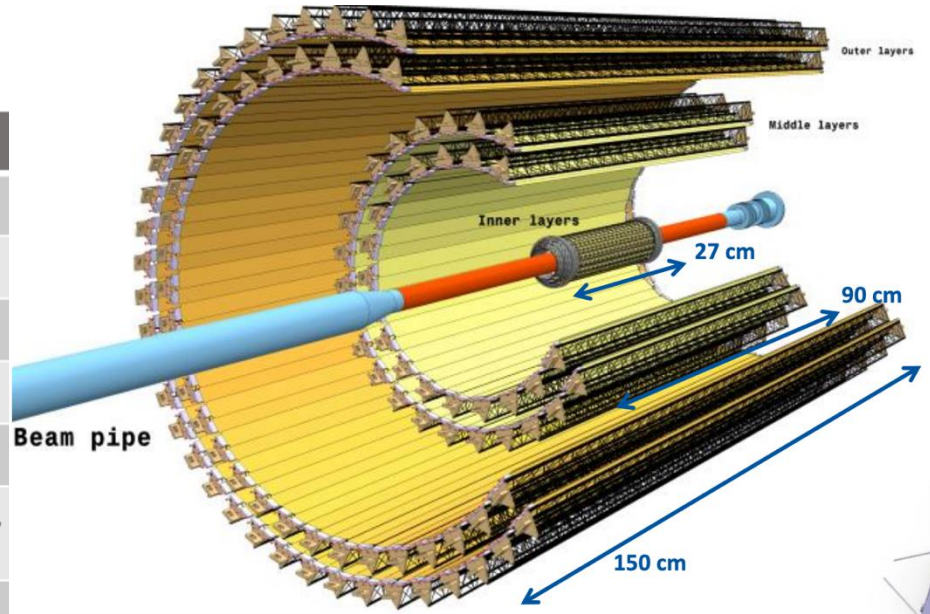
- Pixel size 20.7 μm x 20.7 μm (hit res. 6 μm)
- Rolling shutter architecture (185.6 μs)
- Chips thinned to 50 μm
- 356 M pixels ~0.16 m2
- Material budget: 0.37 % X_0 per layer
- Radiation environment:
  - 20~90 kRad / year
  - 2×10^{11}~10^{12} 1MeV n_{eq}/cm^2

ALICE ITS2 Upgrade

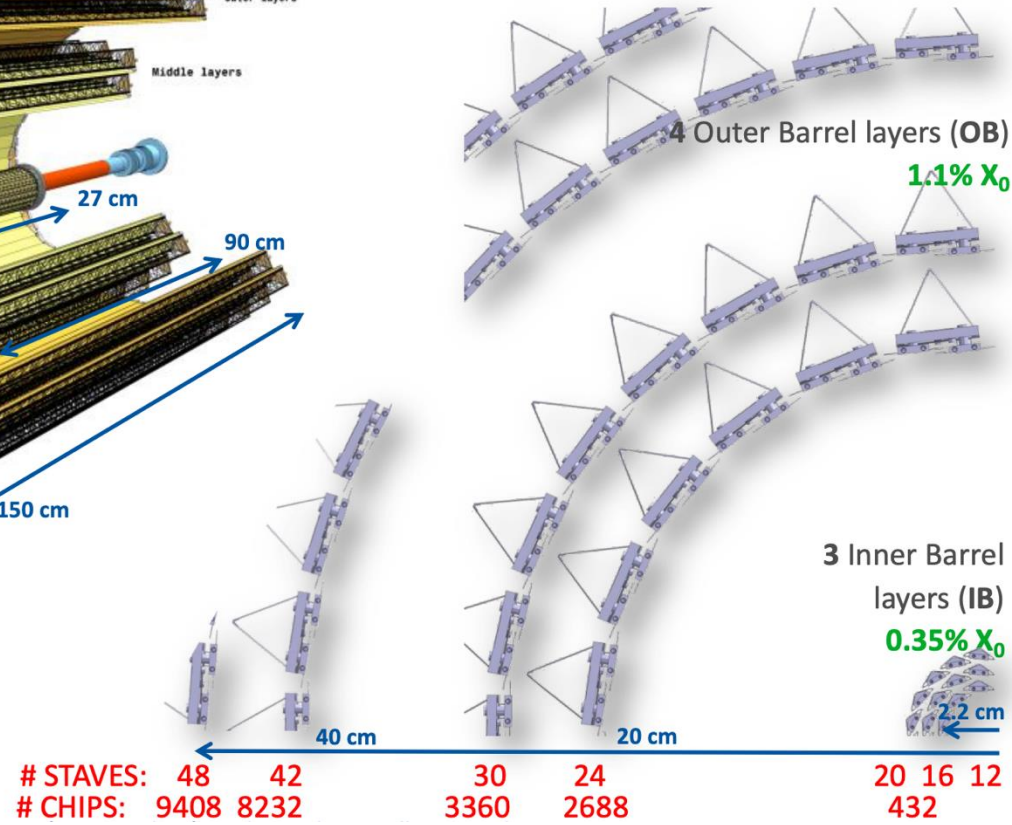
ALICE-TDR-017
NIMA1032(2022)166632

- ITS2: an all-pixel version based on MAPS

	ITS1	ITS2
Technology	Hybrid, drift, strip	MAPS
Layers	6	7
Spatial resolution	12 µm x 100 µm	5 µm x 5 µm
Radius	39 – 430 mm	22 mm – 400 mm
Pseudorapidity	$-1 \leq \eta \leq 1$	$-1.4 \leq \eta \leq 1.4$
Material budget	~ 1.14% X_0	~ 0.3% X_0 (inner barrel), ~ 1% X_0 (outer barrel)
Readout capability	1 kHz	>100 kHz (Pb-Pb), >1 MHz (pp)



10 m² sensitive area
24120 CMOS Pixel Sensors
~12.5 Gpixels



Fully installed and operational since May 2021

G. Rinella

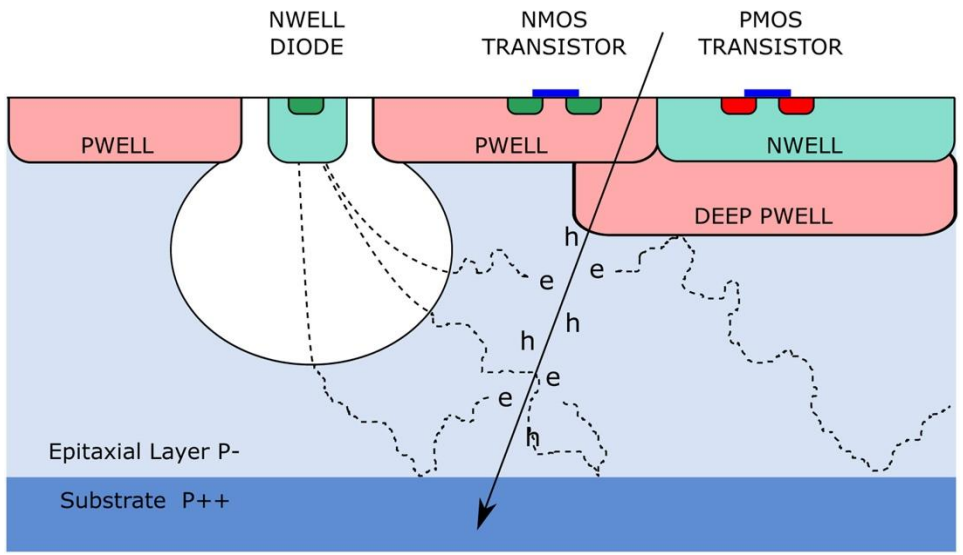
ALICE ITS2 Upgrade: ALPIDE

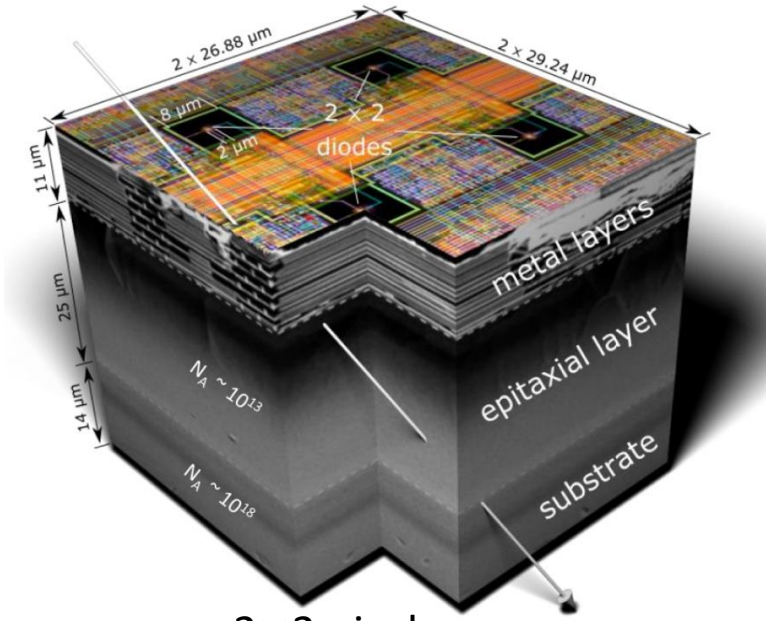
NIMA824(2016)434-438

ALPIDE(ALice PIxel DEtector) technology

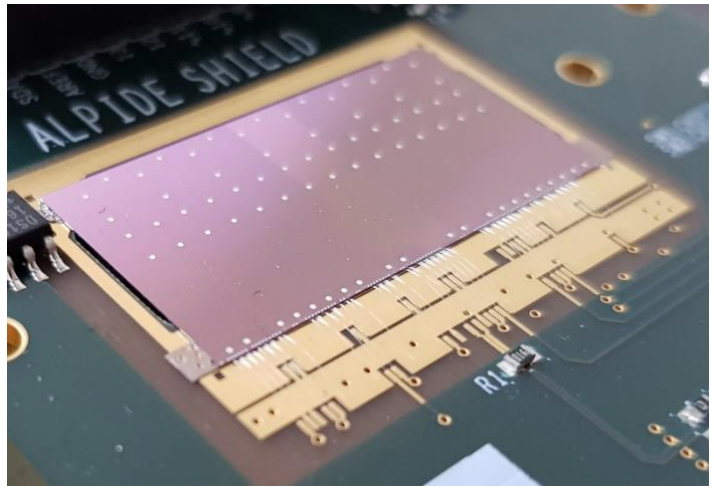
- Tower Jazz CMOS 0.18 μm
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (~25 μm) on p-type substrate
- Deep p-well allows to have PMOS and NMOS inside the pixel cell
- Pixel pitch ~ 30 μm
- Small n-well diode (2 μm diameter) → low capacitance → large S/N

Parameter	Value
Chip dimensions	15 mm × 30 mm ($r\varphi \times z$)
Spatial resolution	5 μm
Detection efficiency	>99 %
Fake-hit rate	$\ll 1 \times 10^{-6}$ /event /pixel
Power density	<40 mW/cm^2
TID radiation hardness	>270 krad
NIEL radiation hardness	$>1.7 \times 10^{12}$ 1 MeV n_{eq}/cm^2



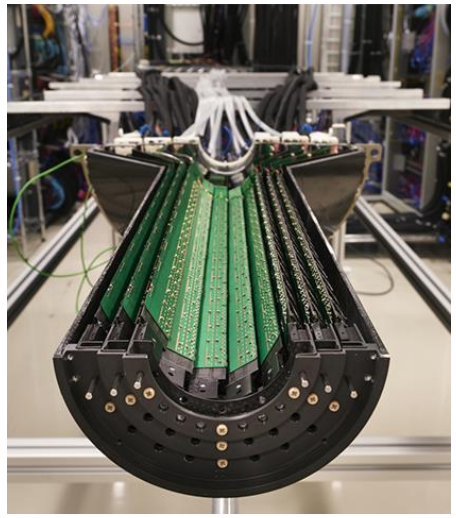


2×2 pixel array



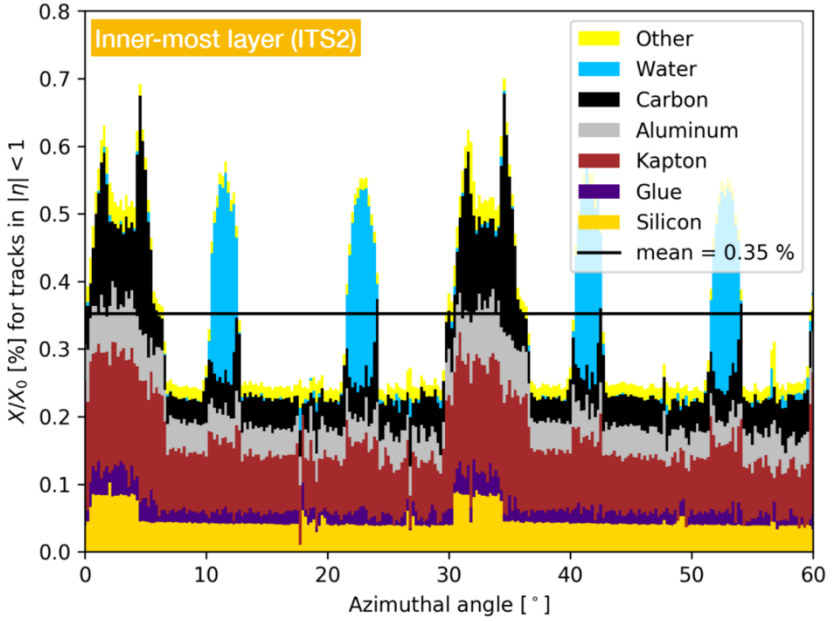
ALPIDE chip: 1.5cm ×3cm

ALICE ITS2 Upgrade: ALPIDE



Inner-most layer:

- Power density < 40 mW/cm^2
- X/X_0: 0.35%



ALPIDE development: large investment of efforts and time

W. Snoeys

2012 **Explorer**
20μm x 20μm and 30μm x 30μm pixels (analogue readout)
pixel geometry, starting material, sensitivity to radiation

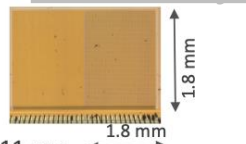
2013 **pALPIDEss-0**
Matrix with 64 columns x 512 rows
22 μm x 22 μm pixels
In-pixel discrimination and buffering
Zero suppression within pixel matrix

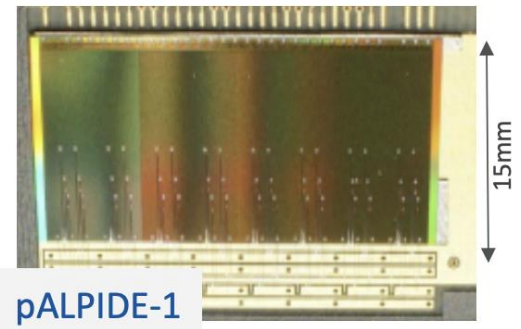
2014 **pALPIDE-1**
First full-scale prototype
Pixel pitch: 28 μm x 28 μm
4 sectors with pixel variants
1 register/pixel, no final interface

Apr 2015 **pALPIDE-2**
4 sectors with pixel variants
Optimization of circuits
Allowing integration in ITS modules
No high-speed serial output

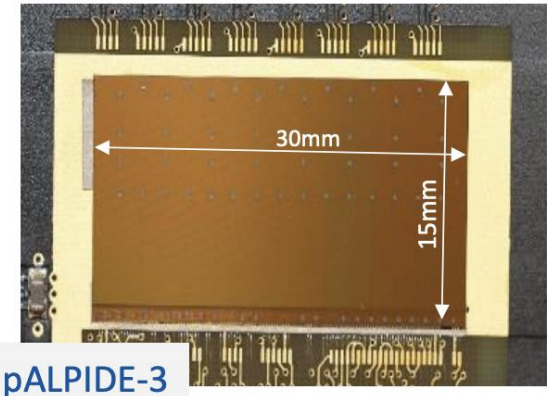
Oct 2015 **pALPIDE-3**
8 sectors with pixels variant
All Communication Features
(no ADC, no Temp Sens)

Aug 2016 **ALPIDE**
Single pixel variant
All features and optimization





pALPIDE-1



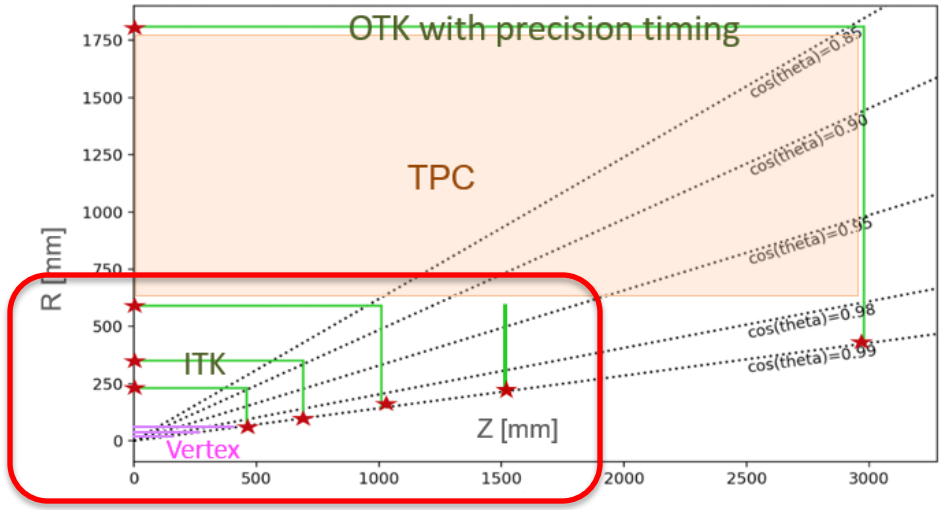
pALPIDE-3

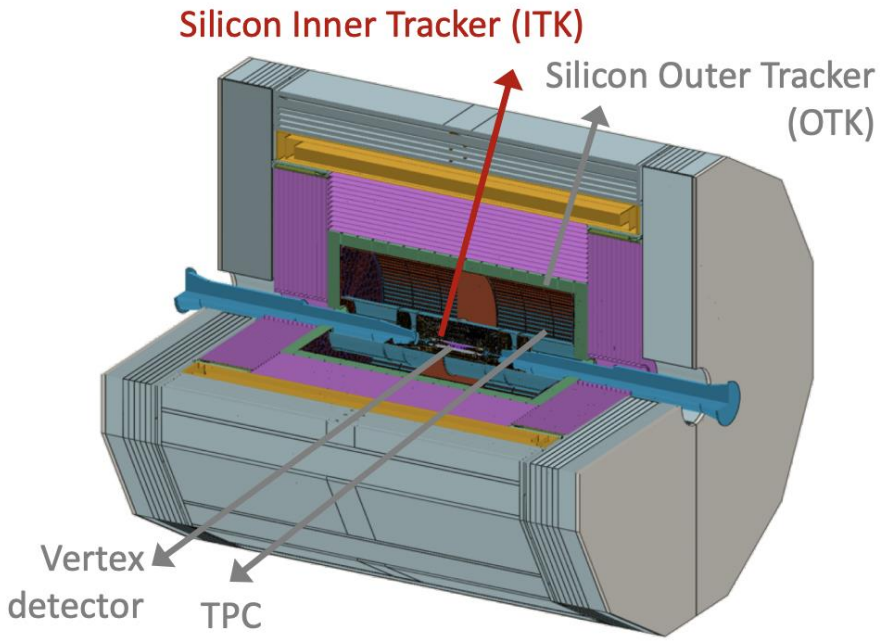
MAPS development for CEPC

- Detector Key Specifications and Ref-TDR

System	Technologies	
	Baseline	Backup / Comparison
Beam pipe	Φ20 mm	
Vertex	CMOS + Stitching	CMOS Si Pixel
Tracker	CMOS Si Pixel ITK	SSD + RO Chip, CMOS SSD
	Pixelated TPC	PID Drift Chamber
	AC-LGAD OTK	SSD / SPD OTK
		LGAD ToF

Jianchun Wang, CEPC workshop, 2024.10

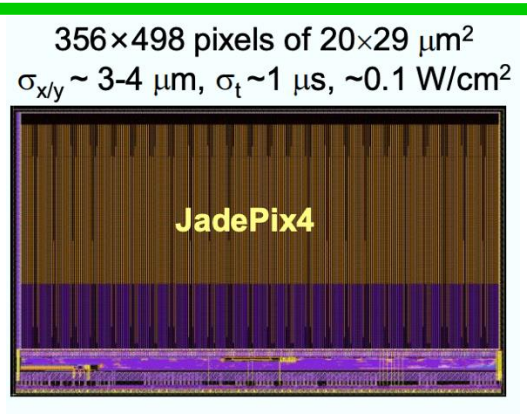


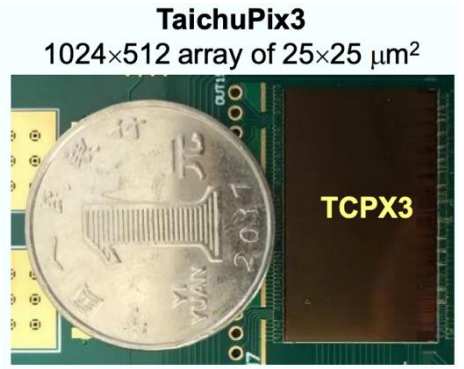


MAPS development for CEPC: vertex detector

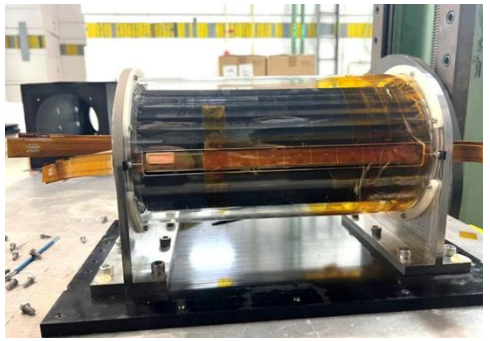
Key specifications:

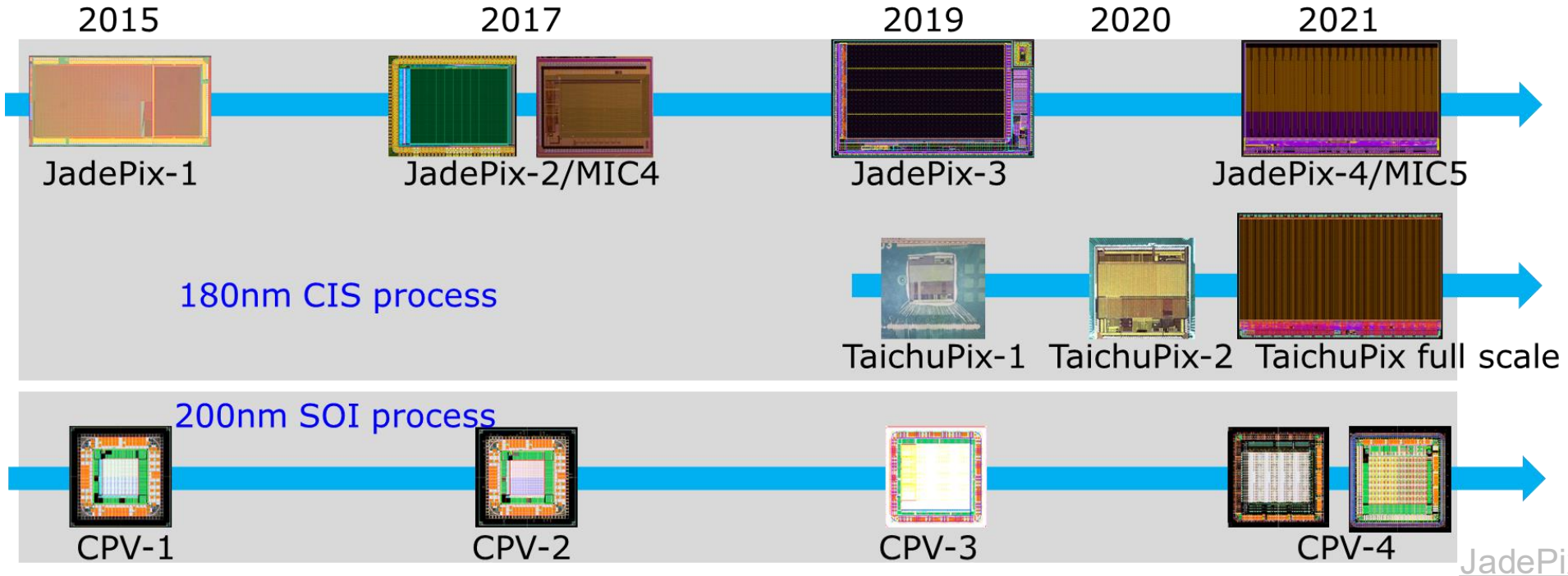
- Single point resolution 3~5 μm
- Low material (0.15% X_0 / layer)
- Low power (< 50 mW/cm^2)
- Radiation hard (1 Mrad/year)





Vertex prototype with TaiChuPix3





Based on TowerJazz 180nm CIS process

Testbeam measurements: spatial resolution ~ 5 μm, efficiency > 99%

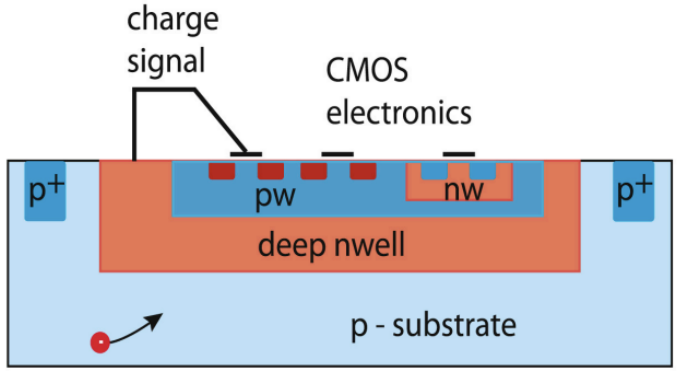
Jianchun Wang, CEPC workshop, 2024.10

JadePix3: NIM A 1048 (2023) 167967
TaichuPix3: NIMA 1059 (2024) 168945

MAPS development for CEPC: inner tracker

CEPC Ref-detector Inner Tracker, key challenges

- ~15 m^2 → cost-effectiveness crucial
- < 10 μm spatial resolution required by momentum resolution
- A few ns timing resolution to tag 23ns bunches at Z-pole
- Low material budget (<1% X_0 per layer)



Team:

IHEP, CAS / KIT / Zhejiang U / Hunan U / Shandong U / NPU / Dalian Minzu U ⋯

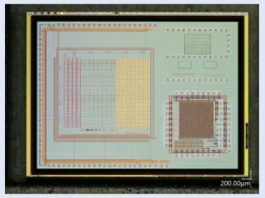
COFFEE

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

COFFEE 2

First HVCMOS 55nm prototype chip

- Breakdown at -70V
- Responsive to laser, X-ray and beta-ray sources

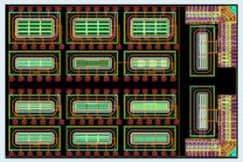


Goal: Full-size full functioning sensor chip ~2027

⋯ 2022 2023 2024 2025 ...

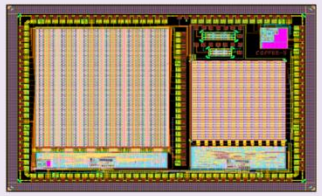
COFFEE1

- Prototype in LL process
- Validation of deep N-well structure
- Breakdown at -9V



COFFEE3

- Two pixel arrays with data-driven readout
- Designed for good timing resolution and moderate power consumption

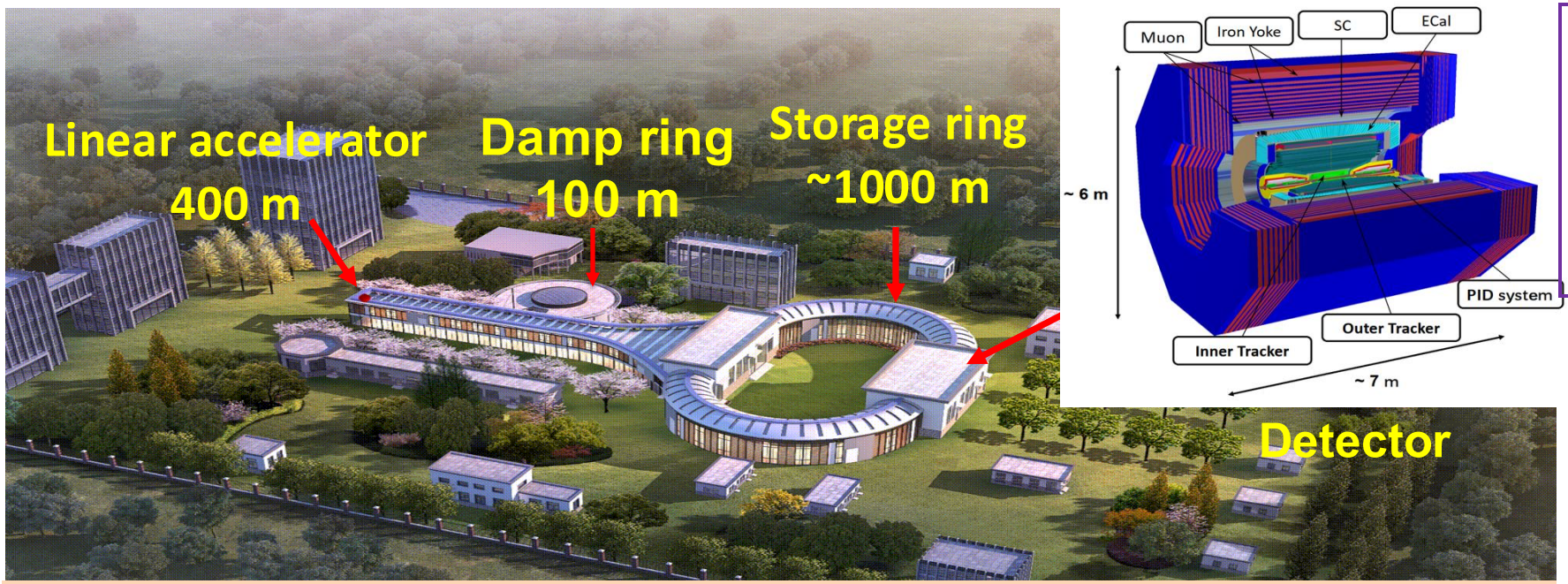


Based on SMIC 55nm HV-CMOS process

Yiming Li
NIMA 1069 (2024) 169905

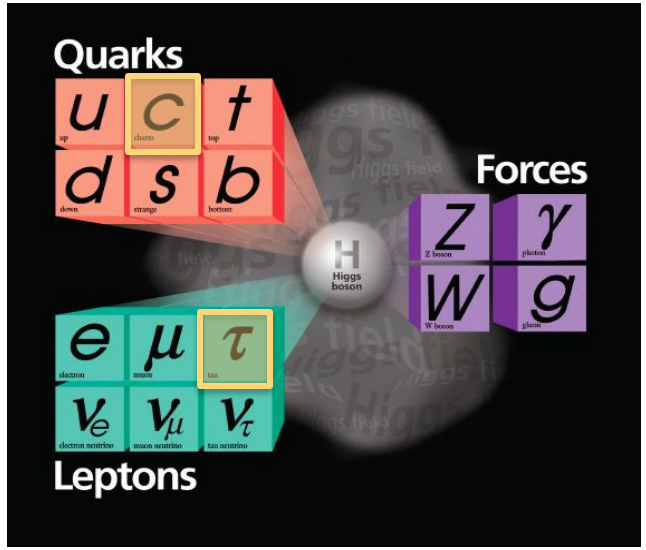
STCF and the tracking requirements

Super Tau Charm Facility (STCF)



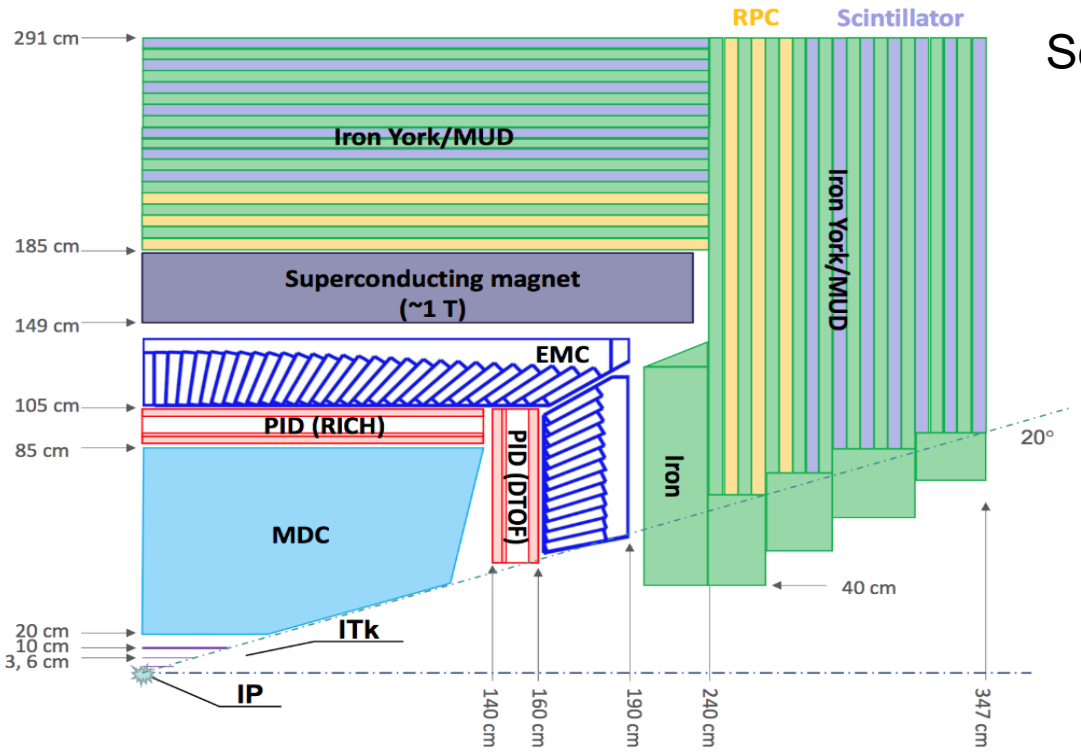
A next-generation high-luminosity e^+e^- collider operating in the $\tau - charm$ energy region

- Energy range: E_{cm} = 2-7 GeV
- Peak luminosity >0.5×10^{35} cm^{-2} s^{-1} at 4 GeV
- Potential for an upgrade to increase lumi. and realize polarized beam



- 1 ab^{-1} data expected per year
- Generate an unprecedentedly large number of τ leptons, particles made of c quarks
- Important playground for study of QCD, exotic hadrons, flavor and search for new physics

Conceptual design



Solid angle coverage: 93%·4π (polar angle: 20°~160°)

Inner tracker(ITK)
- <0.35%X_0/layer
- σ_{xy}<100 μm

Main drift chamber(MDC)
- σ_{xy} < 130 μm
- σ_p/p~ 0.5% @ 1GeV
- dE/dx ~ 6%

Particle identification(PID)
- π/K (K/p) 3~4σ sepa. up to 2 GeV/c

Electromagnetic calorimeter(EMC)
- E range : 0.025~3.5 GeV
- σ_E @1GeV: Barrel 2.5%; Endcap 4.0%
- Pos. res. : 5 mm

Muon detector(MUD)
- 0.4 ~ 2.0 GeV
- π suppression > 30

FRONTIERS OF PHYSICS

REPORT
Volume 19 / Issue 1 / 14701 / 2024

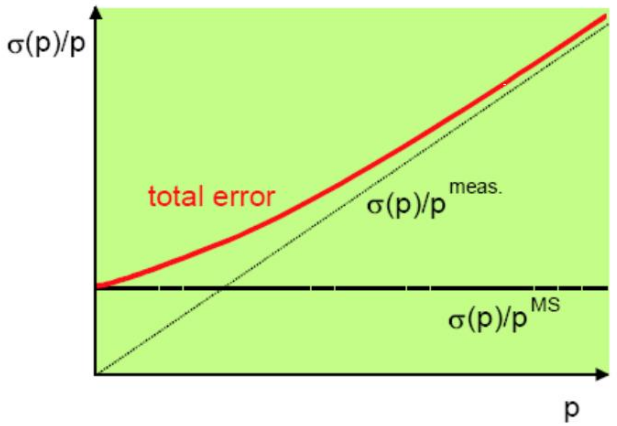
STCF conceptual design report (Volun
Physics & detector

Front. Phys. 19, 14701 (2024)

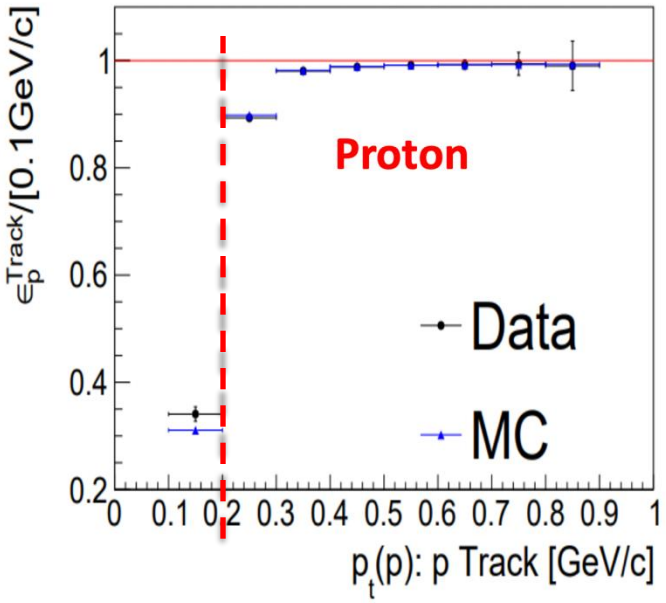
Process	Physics Interest	Optimized Sub-detector	Requirements
$\tau \to K_s\pi\nu_\tau$, $J/\psi \to \Lambda\bar{\Lambda}$, $D_{(s)}$ tag	CPV in τ sector, CPV in hyperon sector, Charm physics	Tracker	acceptance: 93% of 4π; trk. effi.: > 99% at p_T > 0.3 GeV/c; > 90% at p_T = 0.1 GeV/c σ_p/p = 0.5%, $\sigma_{\gamma\phi}$ = 130 μm at 1 GeV/c

Detector considerations

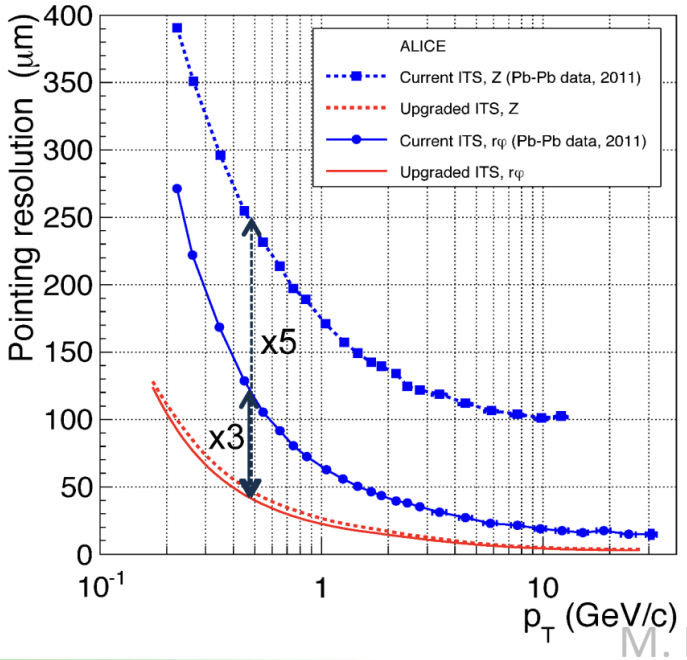
- Tracking challenges at low p_T
  - Momentum resolution: Multiple Coulomb scattering
  - Track reconstruction efficiency
- Low material budget is essential

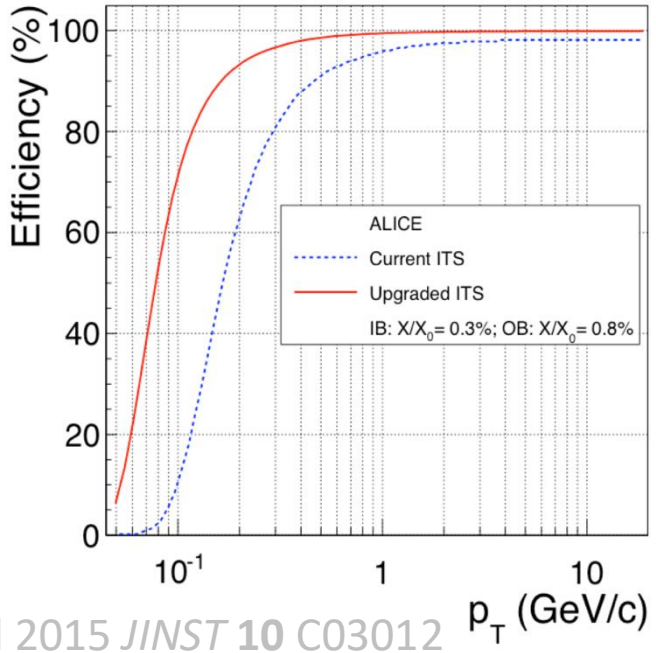


BESIII tracking efficiency



ALICE ITS2 Upgrade Tracking Performance :
1.14%X_0 → 0.3%X_0 (inner layers)

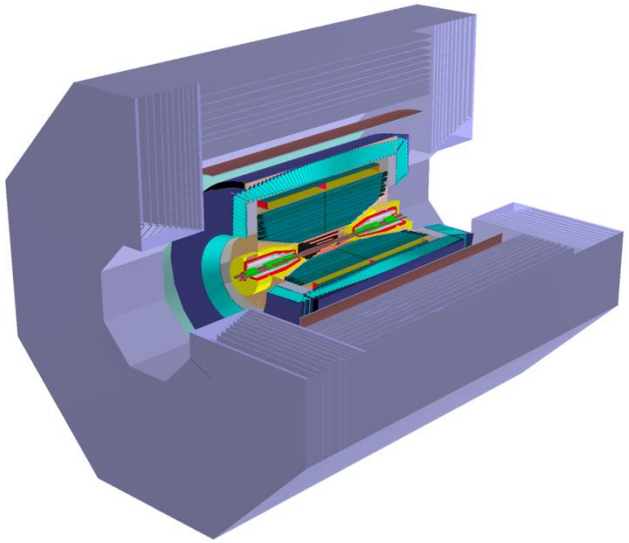


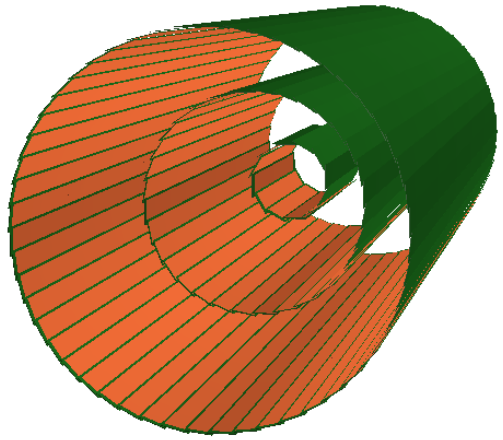


M. Keil 2015 *JINST* **10** C03012

Conceptual design of the MAPS tracker

- To meet the physics requirements of the Inner Tracker:
  - Tracking efficiency: >99% @ $p_T > 0.3\ GeV$; >90% @ $p_T > 0.1\ GeV$
- A preliminary design of the MAPS based Inner Tracker (ITKM)
  - Three layers of silicon pixel detectors, with radii of 36mm, 98mm, 160mm (beam pipe: 30mm)
  - Acceptance: polar angle of 20º~160º
- Total area: 1.3m^2





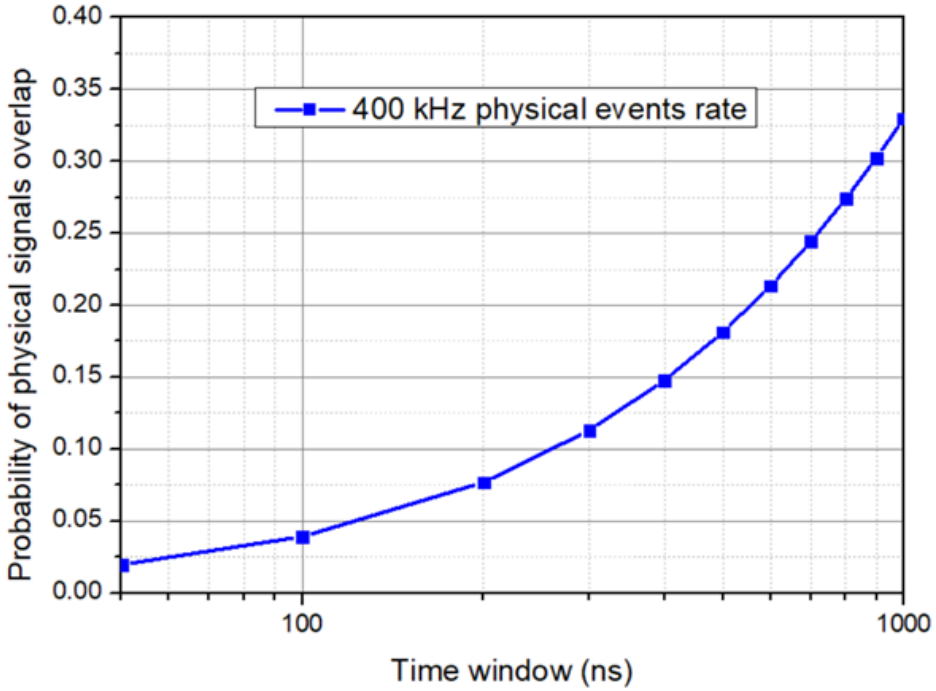
Layer	Radius (mm)	Length (cm)	Area (cm^2)
1	36	19.8	447.5
2	98	53.9	3315.9
3	160	87.9	8838.6

Geometry/layout still being optimized
Might extend to 4 or more layers

Design targets

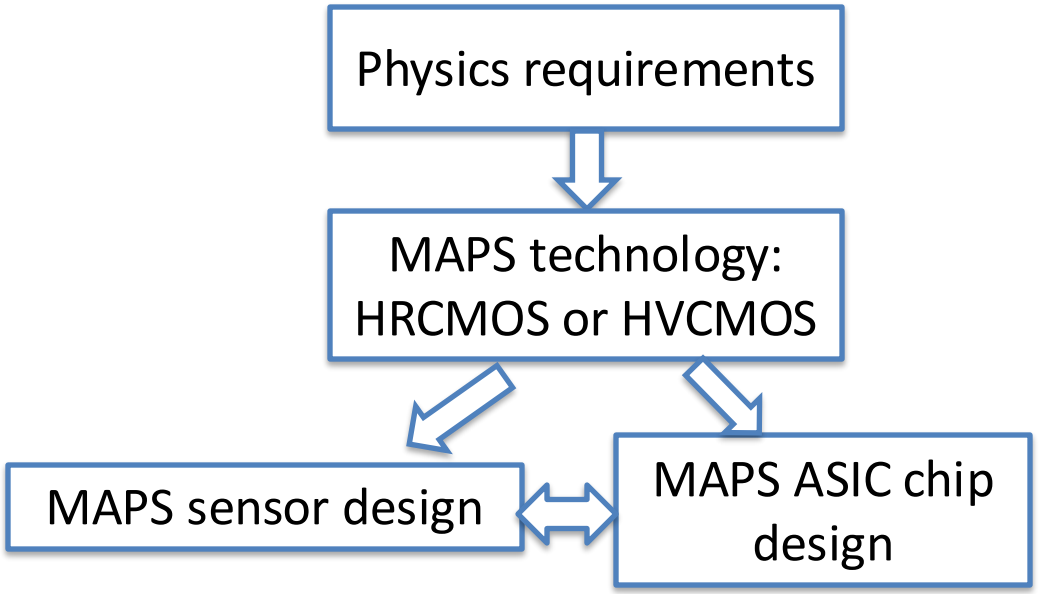
- Requirements on the STCF MAPS
  - Power consumption: $\leq 100 mW/cm^2$
  - Material budget per layer: $\leq 0.35\% X_0$
  - Spatial resolution: $\leq 30 \mu m$
  - Time resolution: $\leq 20\text{ns}$ (to deal with the pileup issue at high luminosity)
  - Hit rate capability: $\geq 1\text{MHz}/cm^2$
  - Time-over-threshold (TOT) measurement:
    - Time-walk correction
    - Correction of multi-coulomb scattering in track finding

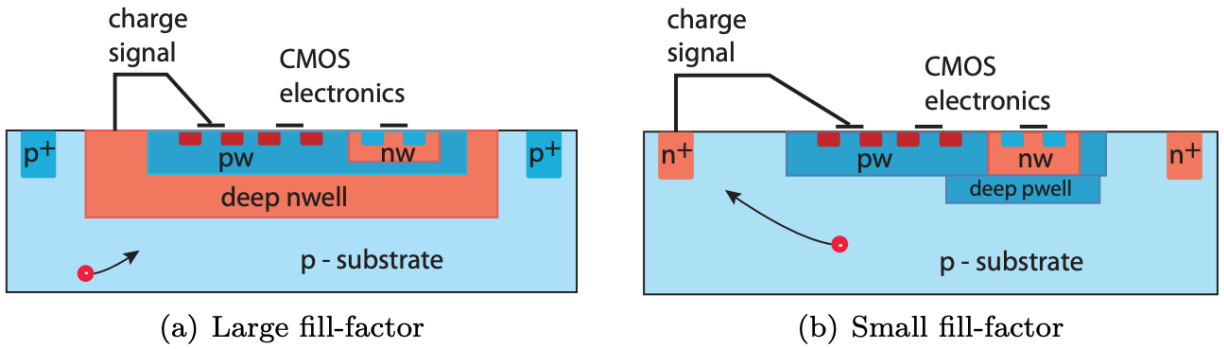
Probability of pileup(with an event rate of 400 kHz @ J/ψ, bunch crossing of 4ns):
- 4% within 100ns
- 8% within 200ns



MAPS R&D for STCF: CharTPix overview

MAPS R&D roadmap





(a) Large fill-factor (b) Small fill-factor

Unlike hybrid pixels, where the sensor and ASIC readout can largely be designed and optimized independently, MAPS integrate the sensor and ASIC, requiring a fully co-designed approach

CMOS MAPS also heavily relies on the underlying fabrication technology and process

Large fill-factor: HV-CMOS
- Pros: timing, radiation hardness
- Cons: capacitance, power consumption

Small fill-factor: HR-CMOS
- Pros: spatial resolution, capacitance, power consumption
- Cons: timing, radiation hardness

To reduce the power consumption, a small fill-factor design is preferred for the STCF MAPS
(Similar to the MAPS technology for ALICE and CEPC)

MAPS R&D roadmap

MAPS ASIC chip design

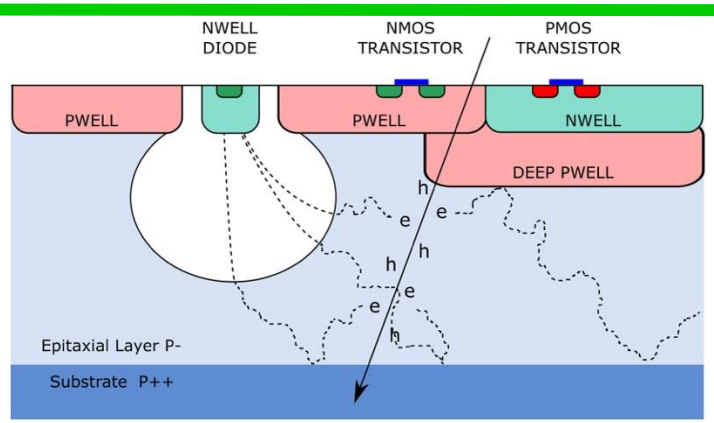
CMOS technology

Foreign mature technologies

- Tower 180nm CIS
- TPSCo 65nm CIS

Domestic technologies under development

- HLMC 55nm CIS
- GSMC 130nm CIS
- Nexchip 90nm CIS
- IRay 180nm CIS



HR-CMOS is based on the commercial CMOS imaging process (CIS), but the original CIS process is not ideal for MAPS:

- Very thin epitaxial layer (a few μm) → limited amount of ionized charge carriers
- Very low resistivity (~$\Omega \cdot$cm) → limited depletion zone, charge carriers transportation dominated by the slow diffusion
- Only three wells (N-well, P-well, Deep N-well) → only NMOS transistors can be used

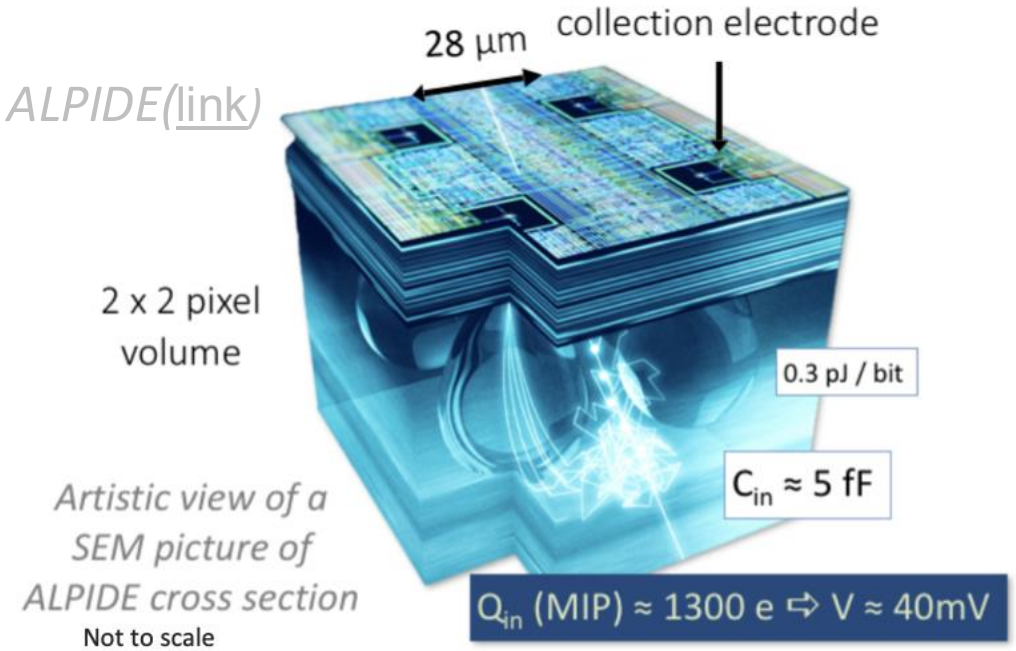
Need process modifications:

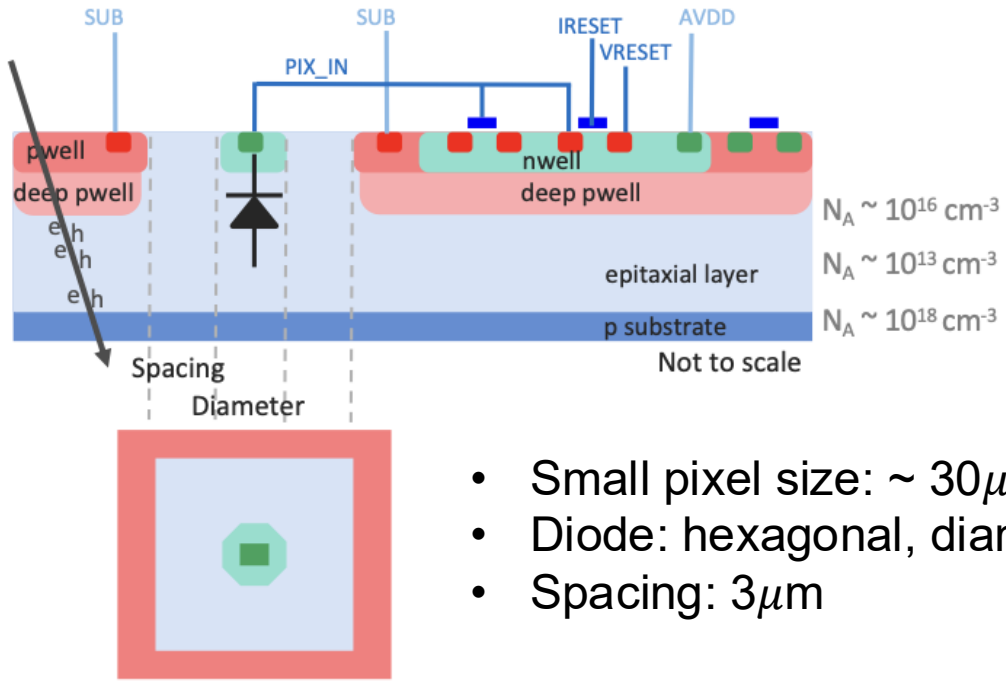
- Thick epitaxial layer: ~ 20 μm
- High resistivity (> k$\Omega \cdot$cm)
- Quad-wells (N-well, P-well, Deep N-well, Deep P-well)

Needs lots of recourses and investment, and most foundries are reluctant to customize the fabrication process

Sensor design

- Layout and geometries of the sensor design is crucial for the performance
  - Diode shape/size, deep P-well, distance between the diode & the deep P-well, etc
  - Doping concentration, depth, etc
- ALPIDE design team has done lots of optimization and provides a good reference

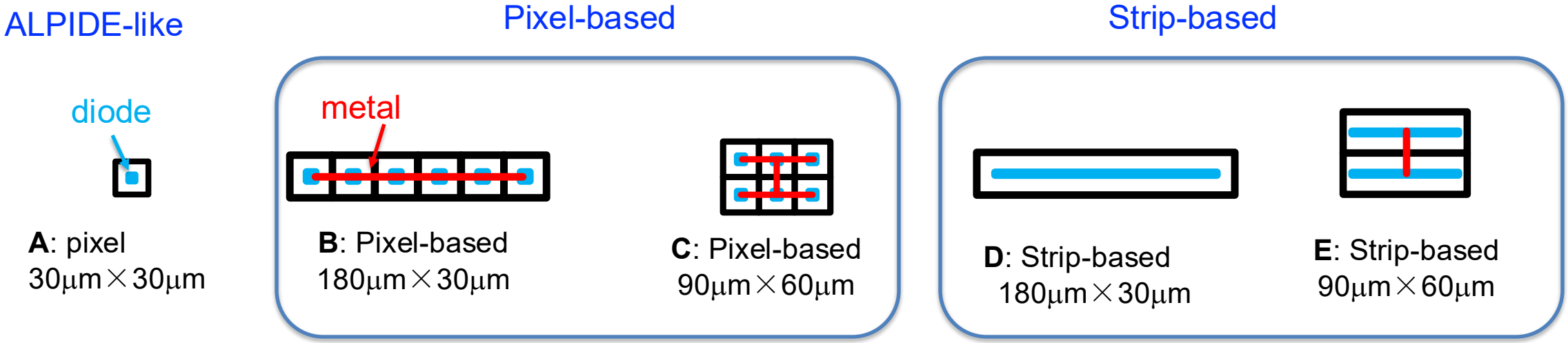




- Small pixel size: ~ 30μm×30μm
- Diode: hexagonal, diameter 2μm
- Spacing: 3μm

CharTPix Sensor design

- Pixel size considerations
  - Higher priority on the power consumption than the spatial resolution → larger pixel size to reduce the power consumption density
  - Three different designs
    - Pixel-based: analog connected small pixels ($1 \times 6 \rightarrow 1, 2 \times 3 \rightarrow 1$) using metal lines
    - Strip-based: extended diode size in one direction
    - Superpixel based: digital connected small pixels



Design technologies

- Three different CIS technologies are being explored
  - Default: 180nm CIS with high-resistivity epitaxial wafers
    - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$; epi thickness: ~20 μm
    - Eg: Tower 180nm(ALPIDE)

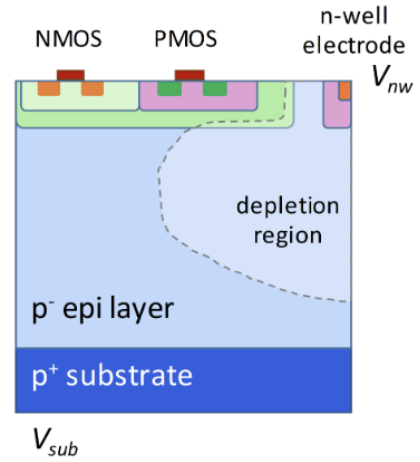
    - Mature technology, well validated
    - Foreign technologies

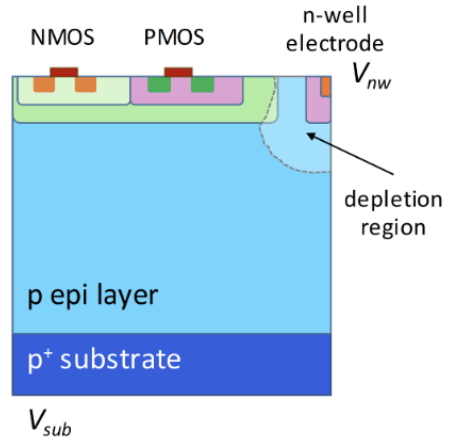
  - 90nm CIS with low-resistivity epi wafers:
    - Resistivity: $\gtrsim 10\Omega \cdot cm$; epi thickness: 10~20 μm

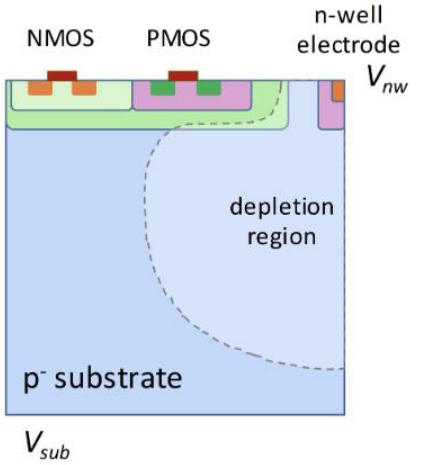
    - Domestic technology under development
    - Performance limited by the low resistivity
    - Advantage of smaller process node

  - 130nm CIS with high resistivity substrates:
    - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$, no epi layers

    - Domestic technology under development
    - Advantage of smaller process node
    - High voltage beneficial to improve the timing performance (eg. MALTA2)



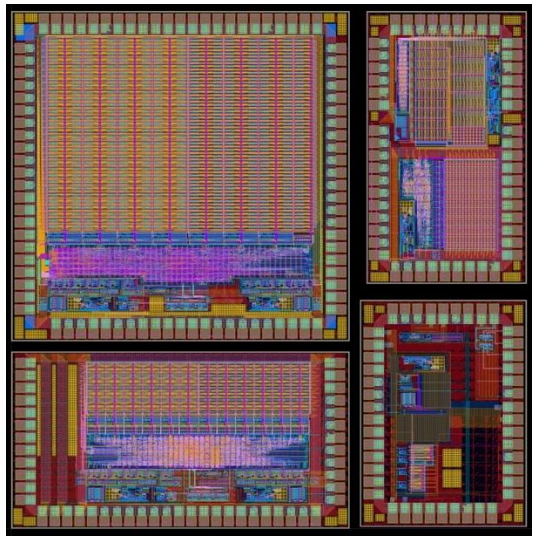




CharTPix protypes

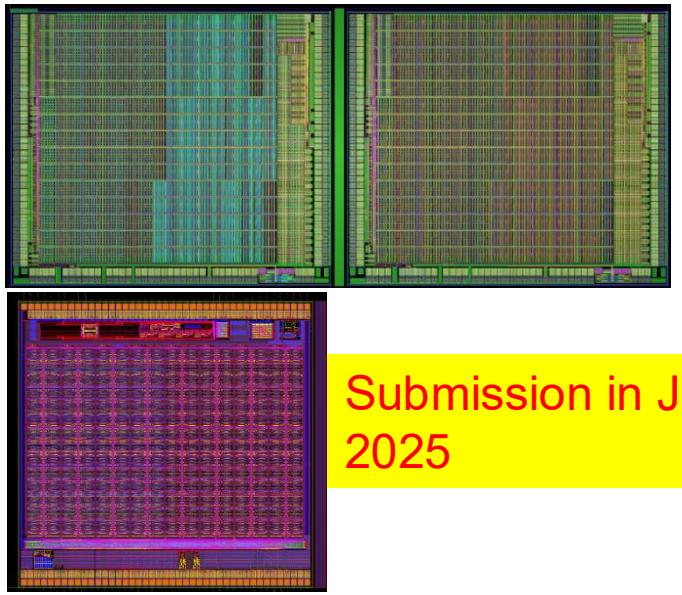
Prototype MAPS design under three different technologies

TowerJazz180nm
- Mature process in HEP (ALPIDE, TJ-Monopix)
- **Baseline techno**
- Low res substrate + high res (>1kΩ · cm) EPI



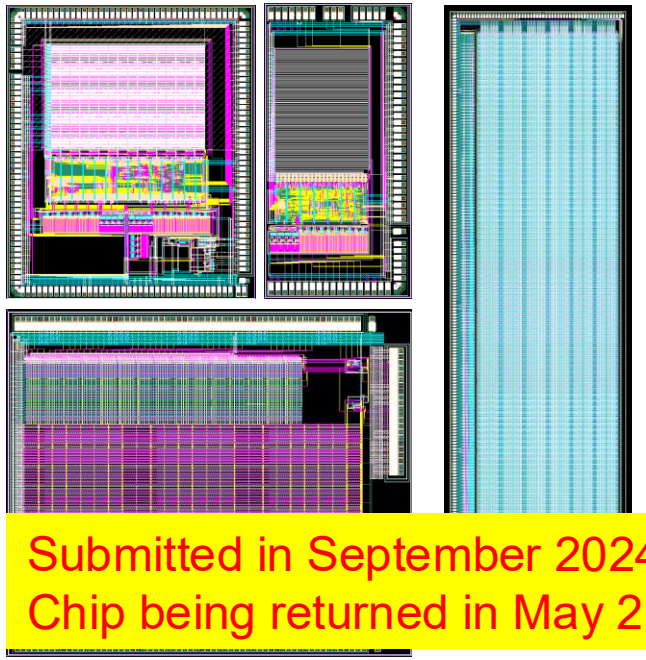
Submitted in March 2024
Chip returned in Dec 2024

NexChip BCIS90nm
- **Local techno**
- Low res EPI (10Ω · cm)



Submission in Jan 2025

GSMC130nm
- **Local techno**
- High res substrate, no EPI

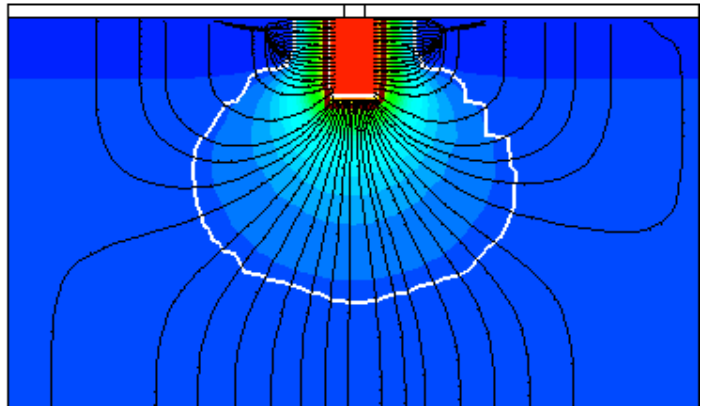


Submitted in September 2024
Chip being returned in May 2025

MAPS R&D for STCF: Sensor simulation study

Sensor simulation methodology

- Simulation plays a key role in MAPS design and optimization
  - Developing a new sensor is a highly complex process and sensor submissions are time-consuming and costly
  - Necessary to precisely simulate the sensor response to charged particles
- TCAD(Technology Computer-Aided Design): model semiconductor devices using finite element methods
  - Electric field and electrostatic potential
  - Transient simulations of sensor response as a function of time
- Monte Carlo: stochastic response based on Gean4
- Combination of TCAD and Geant4 is preferred



Allpix²

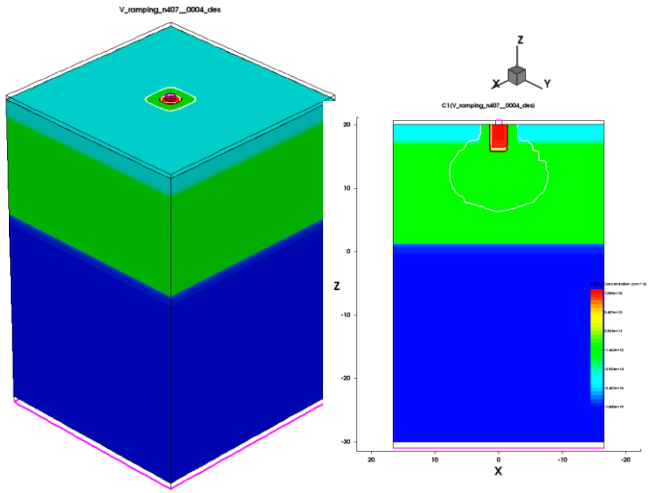
TCAD simulation

TCAD simulation in different technologies

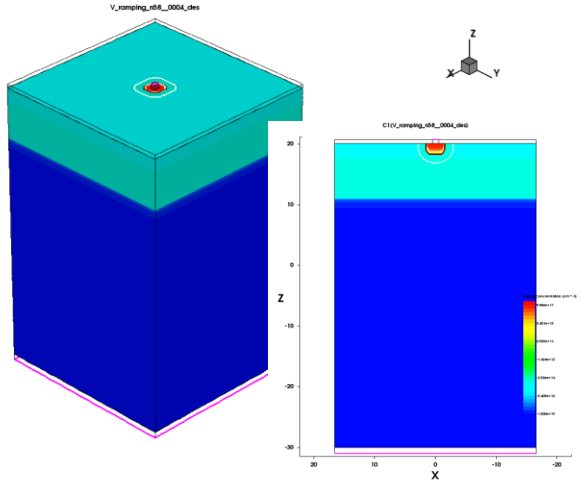
- Pixel size: $30\mu m \times 30\mu m$
- N-well size $2\mu m$
- NW-DPW spacing $2\mu m$

Technology	Sensor capacitance
TJ180nm	2.7fF
BCIS90nm	1.7fF
GSMC130nm	2.7fF

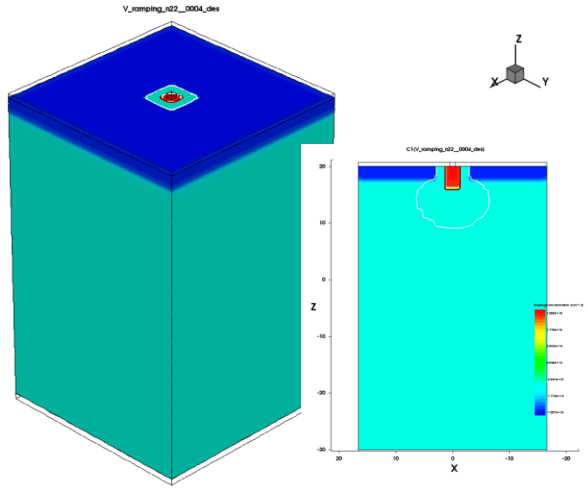
$V_{nw} = 0.8\text{V}$ $V_{sub} = -6\text{V}$



TJ180nm



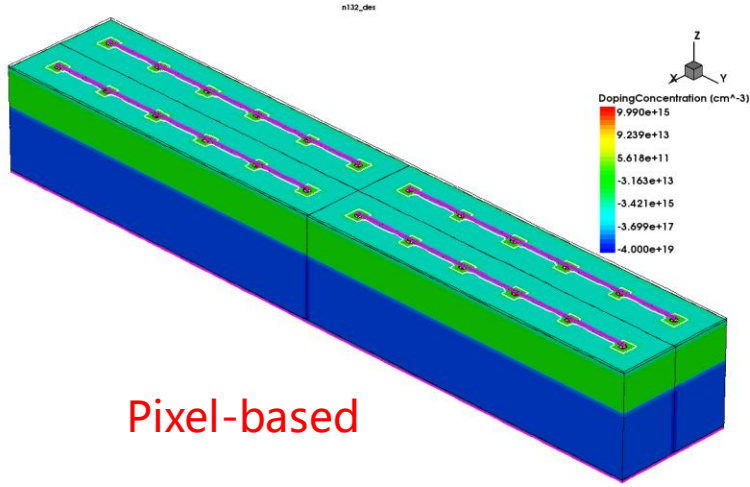
BCIS90nm



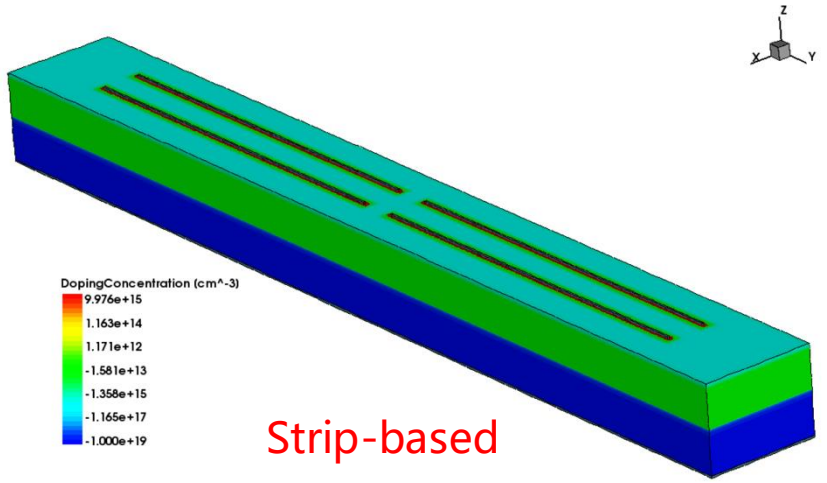
GSMC130nm

TCAD simulation

- Strip Sensor
  - Rectangular: 30μm×180μm
  - Diode : 2μm×150μm
  - Spacing: 2μm
  - -6V bias
  - Depletion depth: 12μm
- Sensor capacitance
  - Single pixel: 2 fF
  - Pixel-based pixel: 12 fF
  - Strip-based pixel: 30 fF

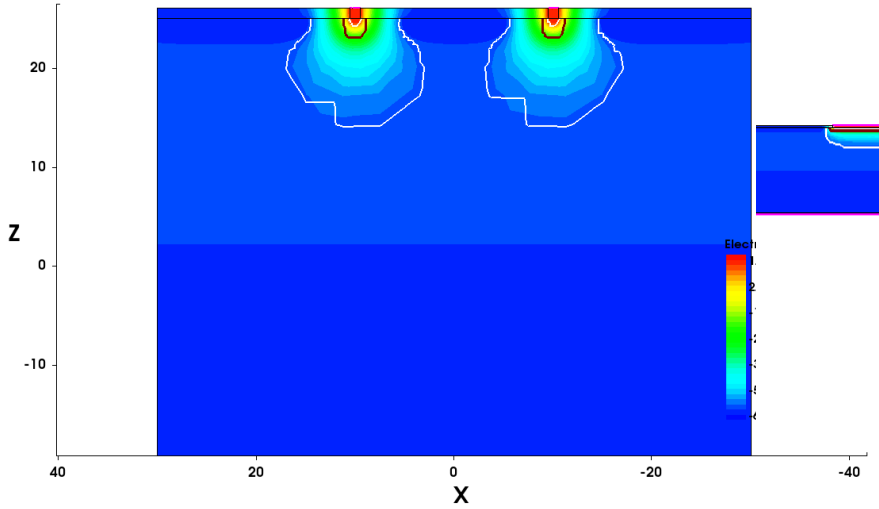


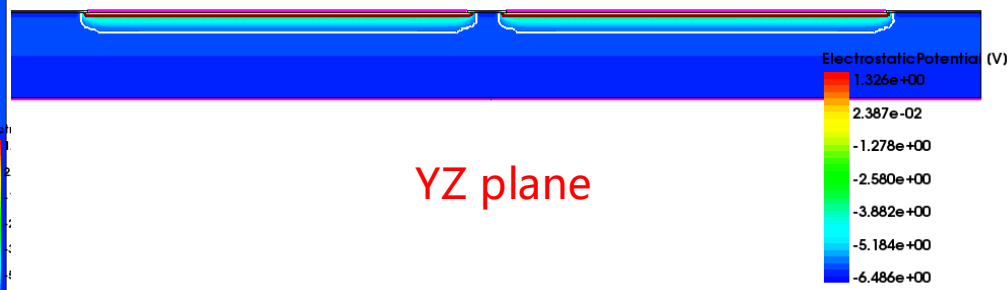
Pixel-based



Strip-based

XZ plane



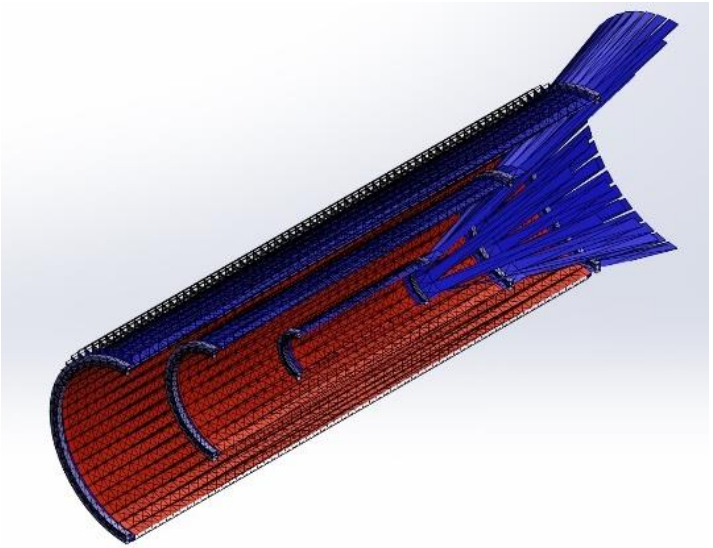


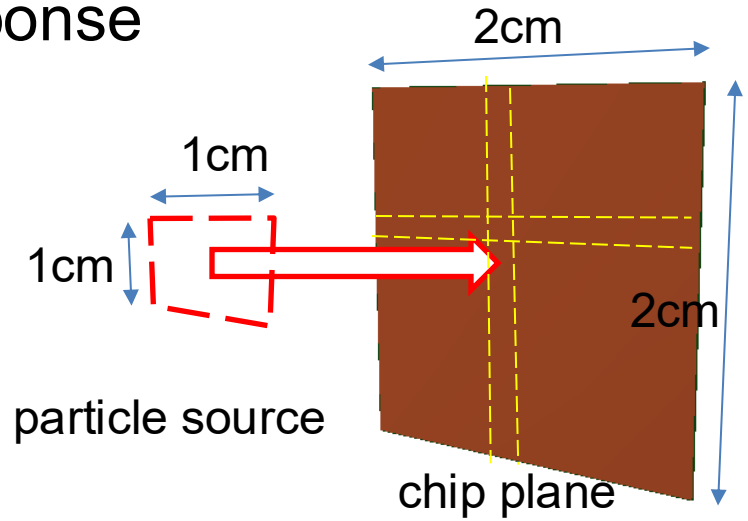
YZ plane

STCF ITKM simulation

- MC simulation of the entire inner tracker system under the STCF simulation framework
  - OSCAR: the offline software of Super Tau Charm Facility
- Chip + Flex + Carbon fiber support
  - ~0.27% X_0 for layer 1&2
  - ~0.29% X_0 for layer 3
- MIP: 1Gev μ^- perpendicularly, randomly incident
- Ionization & charge collection simulation
- Full digitization process considering pre-amplifier response

arXiv:2211.03137



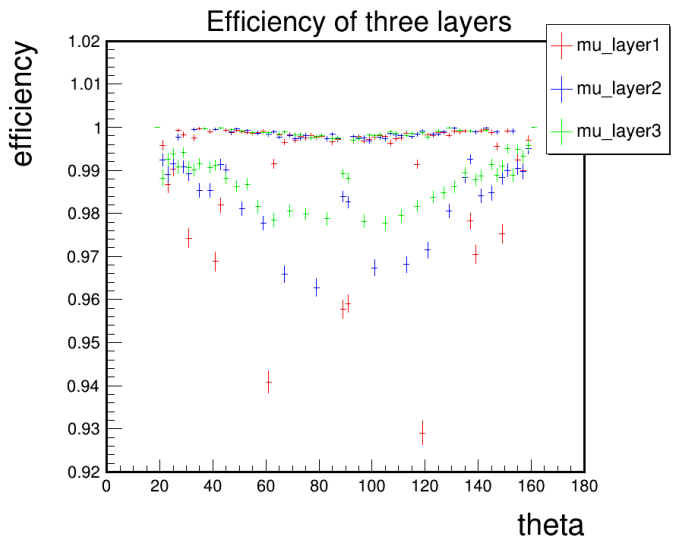


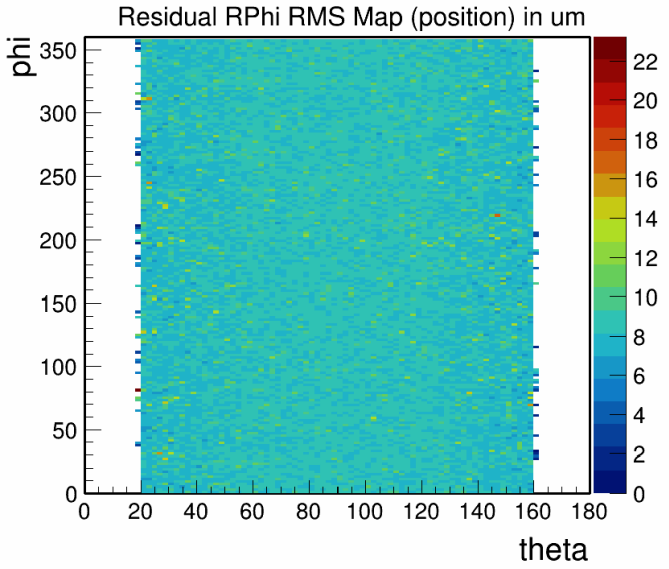
STCF ITKM simulation

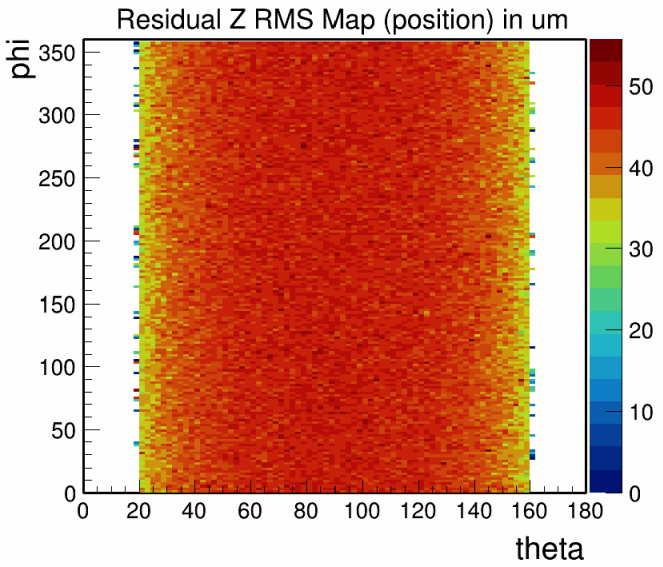
- Pixel type:
  - TJ180nm, 170μm×30μm, n-well connect
- Simulation settings:
  - 1GeV μ^-, θ range 20°-160°
  - Pixel threshold: 300e

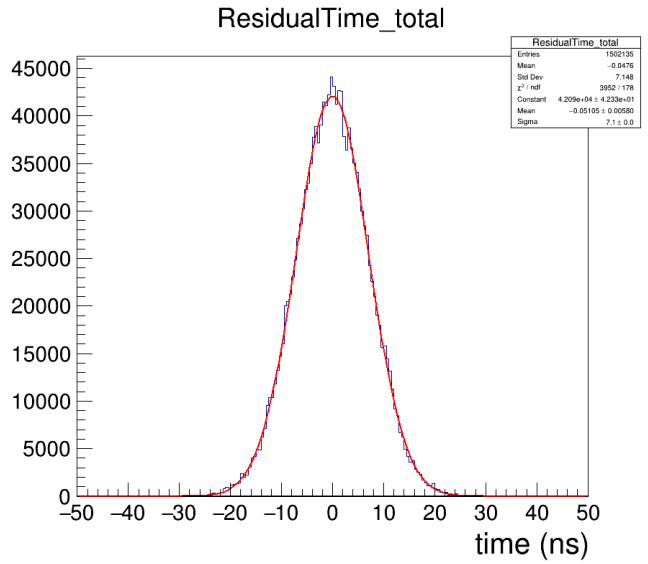
✓ Average detection efficiency 99.2%
✓ Position resolution: $\sigma_z = 33.5\mu m$, $\sigma_{rphi} = 6.8\mu m$
✓ Time resolution (sensor only) 7.1ns

A MAPS based Inner Tracker can meet the physics requirements of STCF





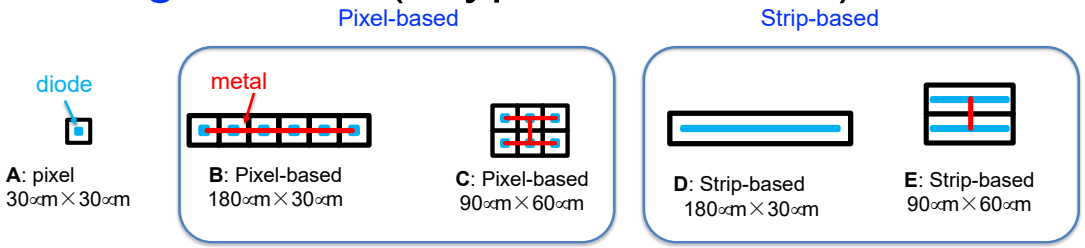




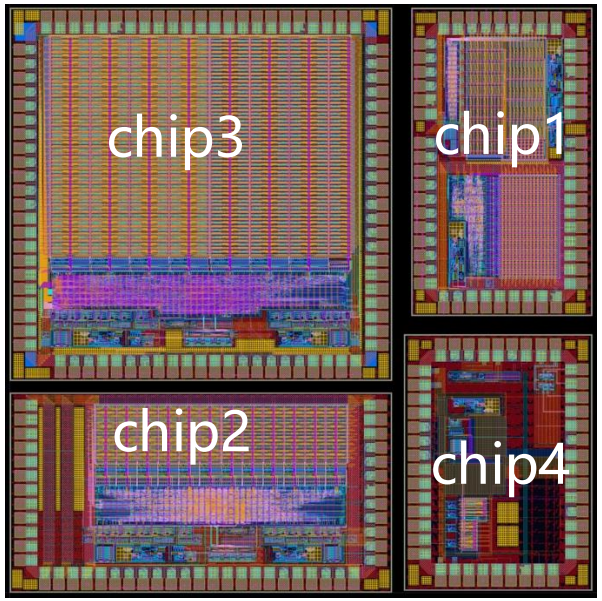
MAPS R&D for STCF:
CharTPix prototype chips design

Prototype chips

- Designed 4 prototype chips based on the TJ 180nm technology
  - Chip 1: ALPIDE-like small pixels, 0/1 digital readout
  - Chip 2: large pixels ($96\mu m \times 60\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 3: large pixels ($170\mu m \times 31\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 4: 3T analog readout (5 types of sensors)



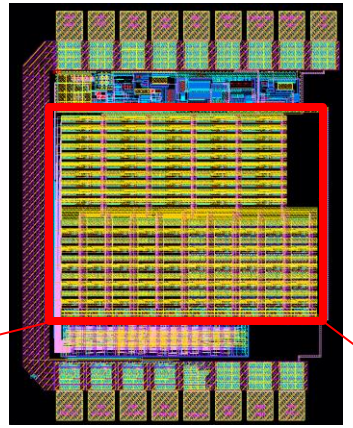
	Chip1	Chip2		Chip3		Chip4
Pixel size (μm×μm)	28.1x30.1	96.4x59.6		170.0x31.0		Mixed
Sensor	ALPIDE-like	Strip-based	Pixel-based	Strip-based	Pixel-based	Mixed
Pixel array	16x30	8x12	8x12	60x8	60x7	Mixed
Readout	Token	Token		Token		Analog readout
ToA & ToT	X	√		√		X

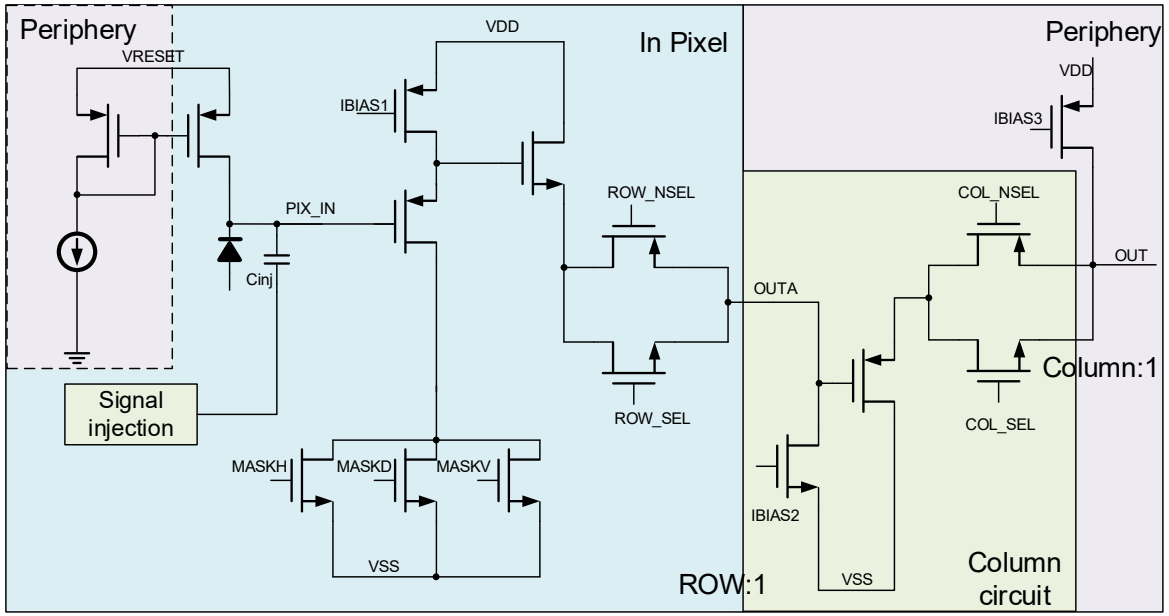


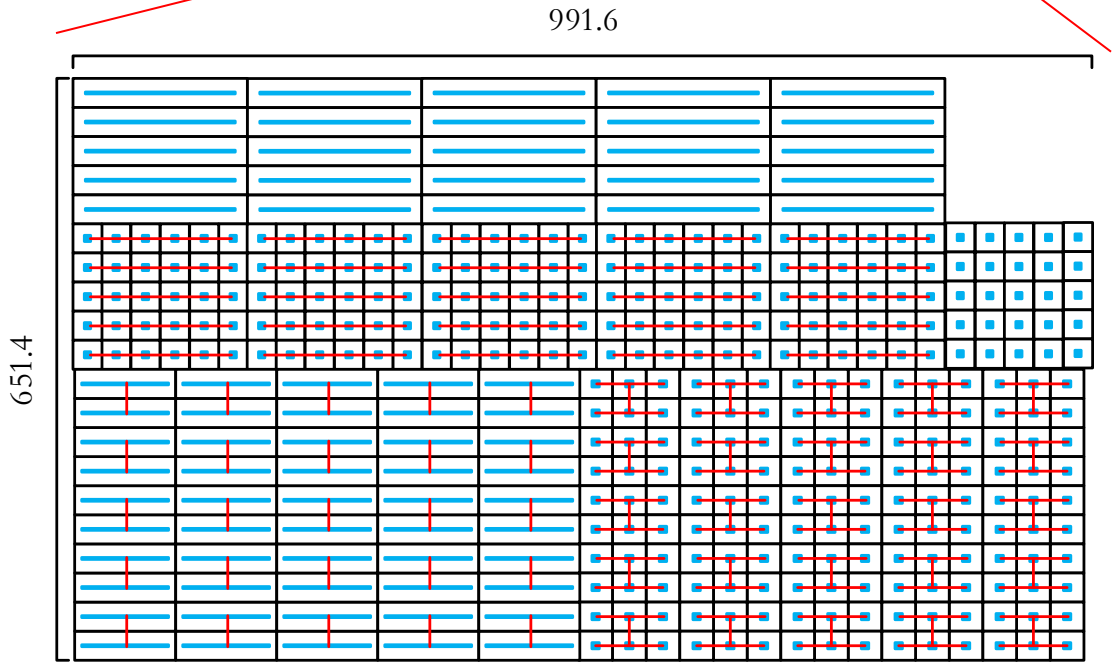
Total area: 5 mm×5 mm
Submitted in 2024 Q1

CharTPix-TJ Chip4

- To study performance of different pixel layout
- 5×5 array for each type of pixel
- Pure analog readout: source follower + matrix parallel readout

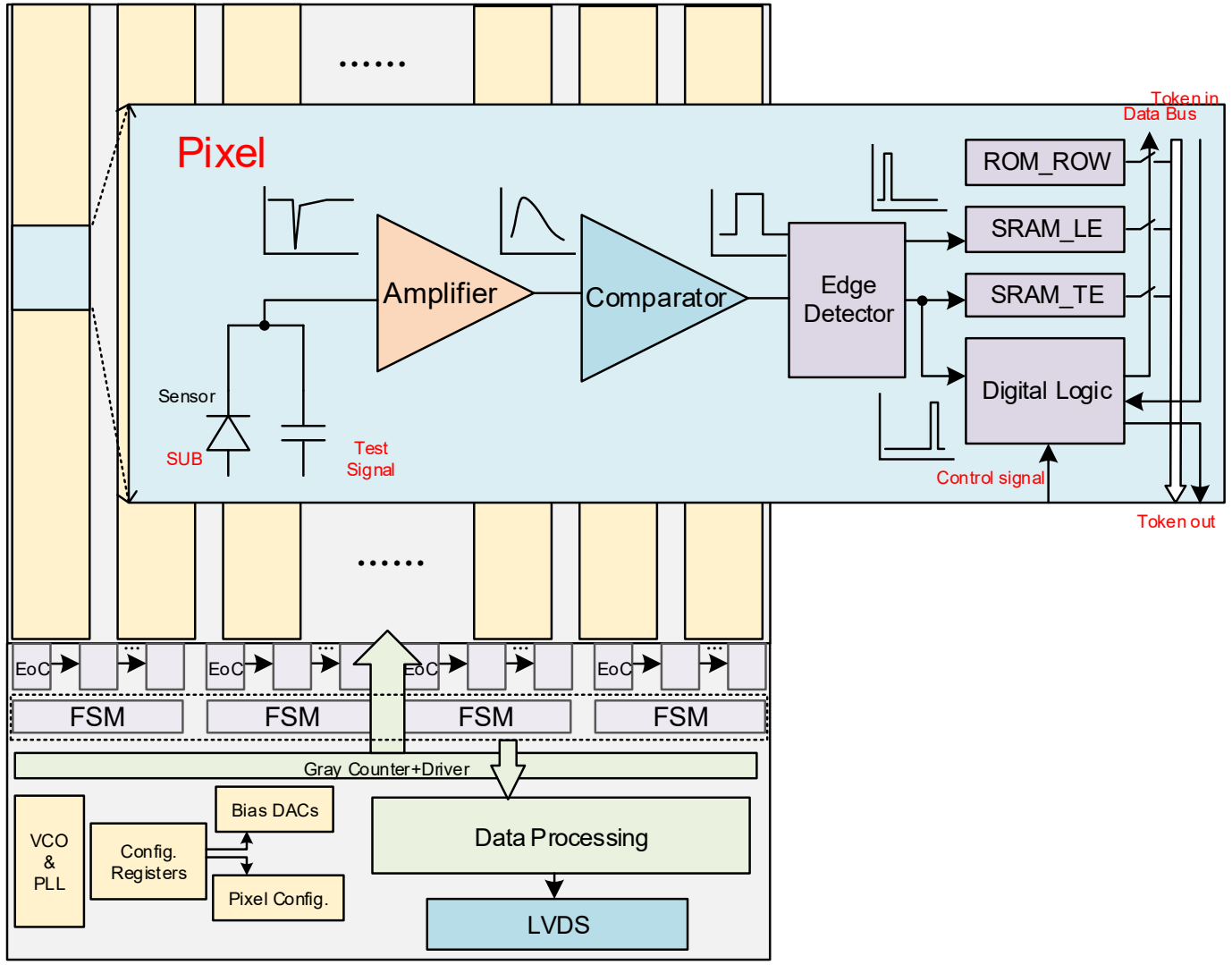






CharTPix-TJ Chip2,3: Readout architecture

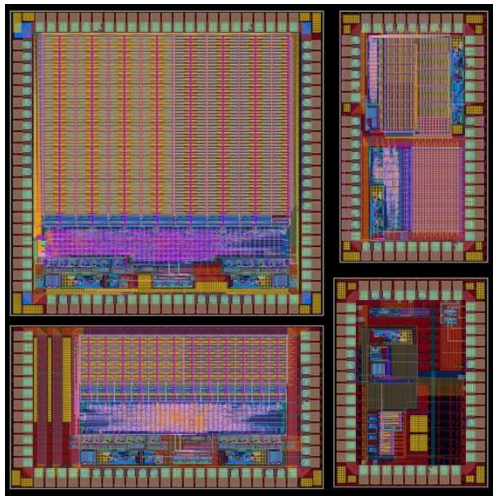
- In-pixel circuits
  - Analog amplifier, comparator
  - Priority readout
  - SRAM, ROM
  - Charge injection
- Digital readout
  - End-of-column driver
  - Column level priority logic
  - Data processing module
  - Serializer
  - PLL, LVDS
- Analog configuration
  - VDAC×2, IDAC
  - Bandgap, EoC current mirror
  - I2C
- Test points



CharTPix prototypes

Foreign mature technologies

TowerJazz 180nm

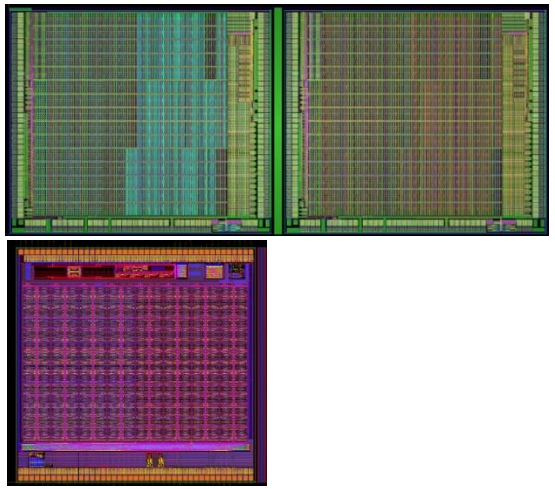


Submitted in March 2024
Chip returned in Dec 2024

A 2nd version is also being submitted with many improvements

Domestic technologies under development

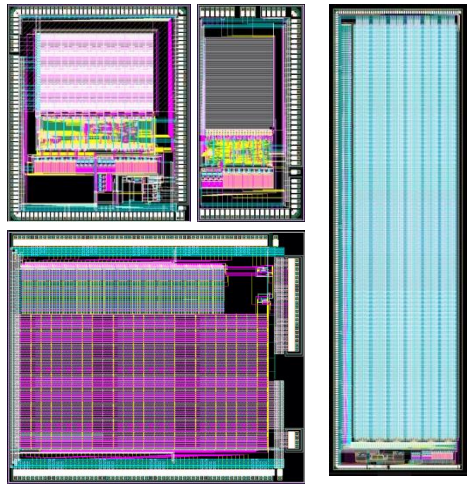
Nexchip BCIS 90nm



Submission in Jan 2025

- To verify process modification (Diode, Deep P-well)
- In-pixel VCO to improve timing performance (6ns expected)

GSMC 130nm



Submitted in September 2024
Chip being returned in May 2025

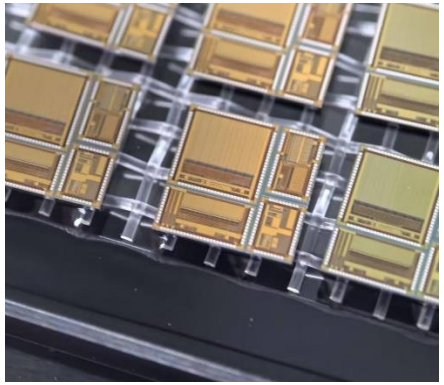
- To verify the novel SuperPixe concept
- To verify the high-resistivity substrate process

MAPS R&D for STCF: CharTPix-TJ-v0.1 preliminary characterization results

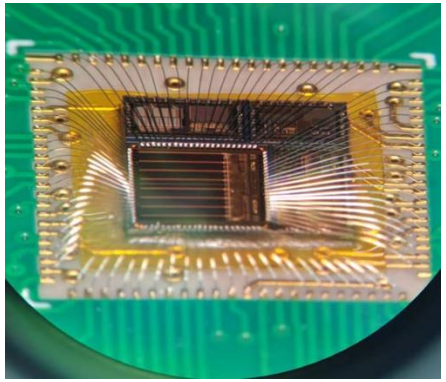
Test system

Chips received in Dec 2024

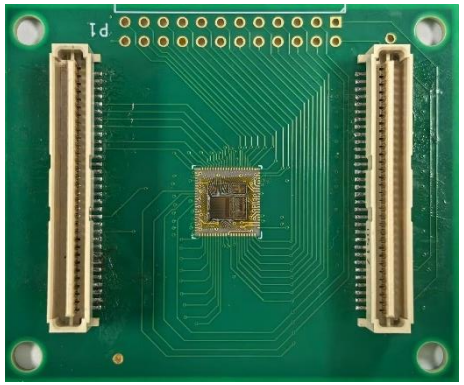
- Chip3 is being tested now
- Test preparation for the other three chips ongoing



CharTPix-TJ-v0.1 chips

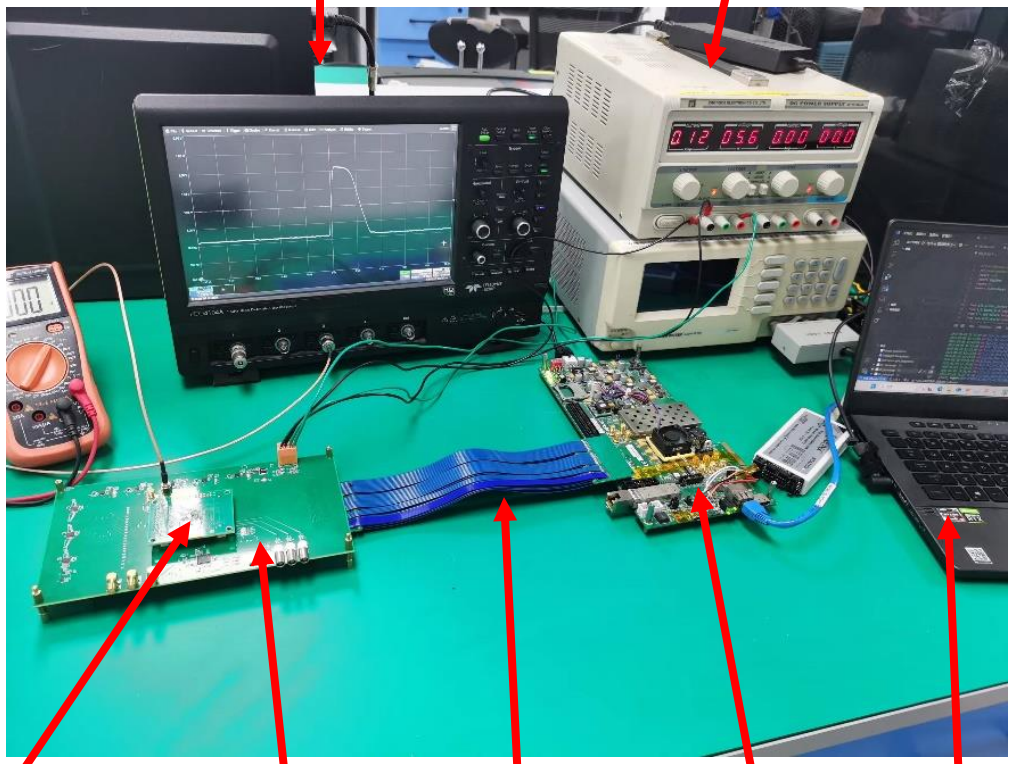


After wire bonding



Carrier board

MAPS test system
(developed from the JadePix test system)
JINST 16 (2021) 07, P07052

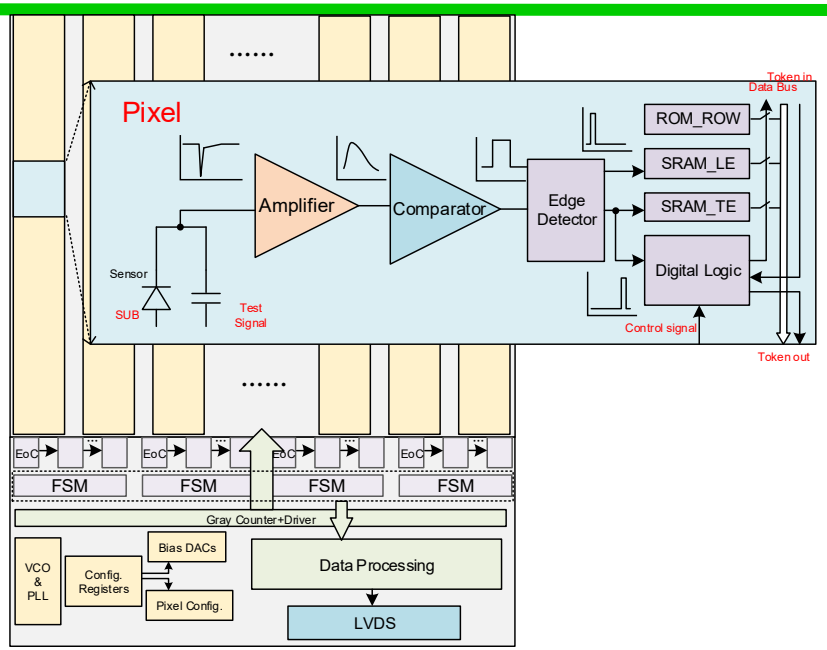


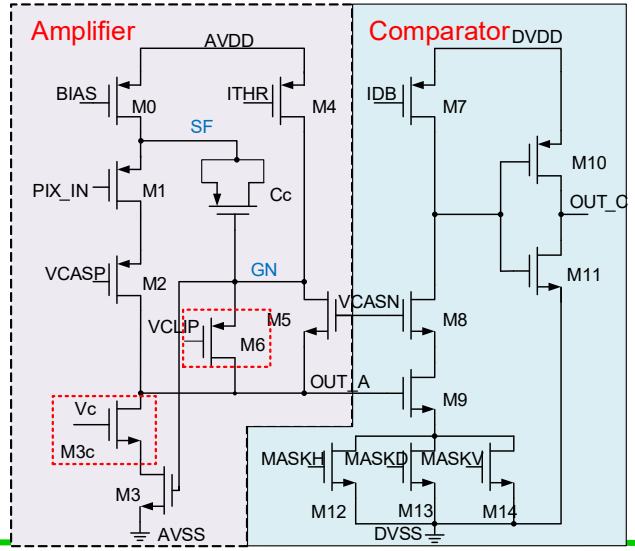
MAPS characterization

Basic functionality verification:
- Chip configuration
- Verification of all modules

Working point tuning:
- DAC setting of analog front-ends
- Threshold, noise(ENC), fake-rate

Performance measurements:
- Basic properties: threshold, threshold RMS and temporal noise
- Charge collection efficiency
- Detection efficiency
- Spatial resolution
- Timing resolution

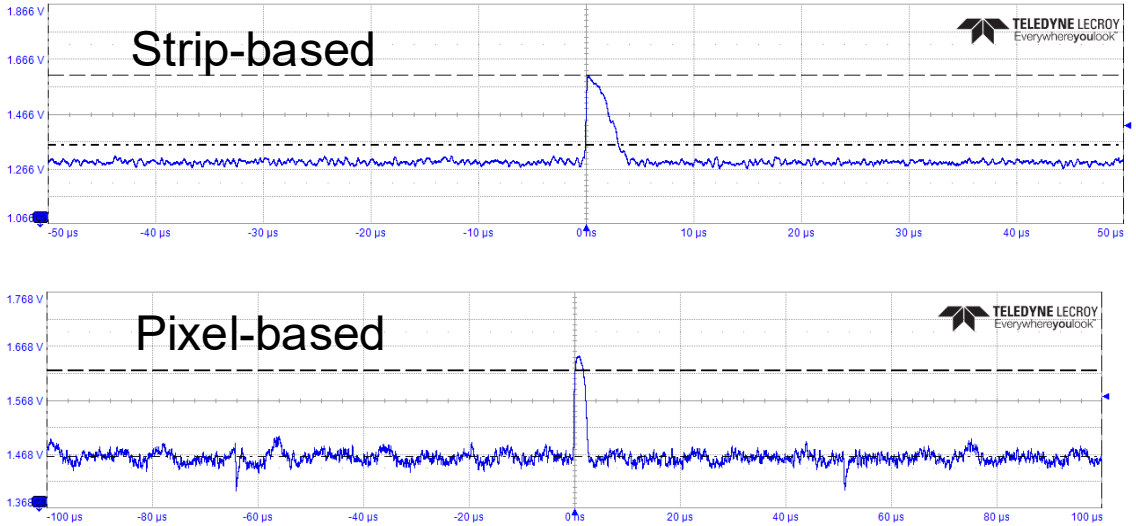


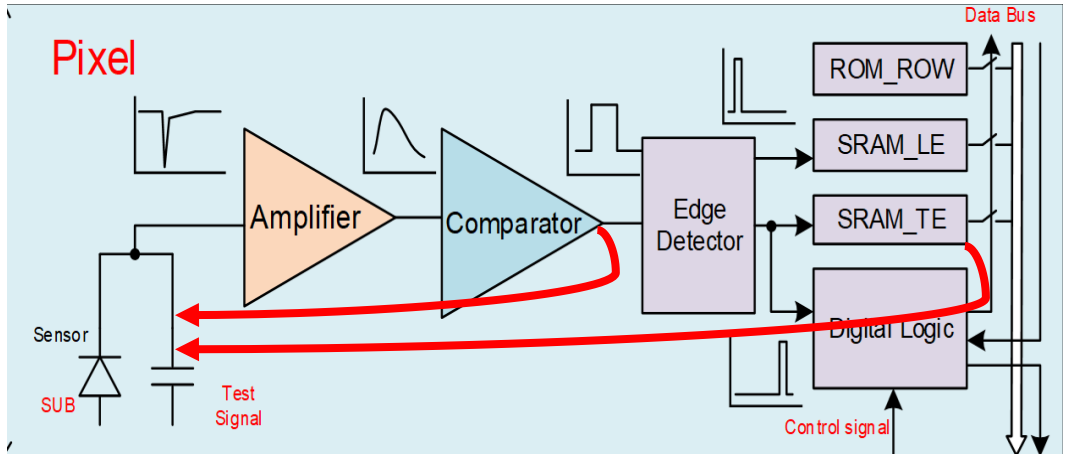


Methods:
- **Radioactive source**: Fe-55 (X-ray), Sr-90 (β-source)
- **Laser**
- **Testbeam**

Cross-talk problem

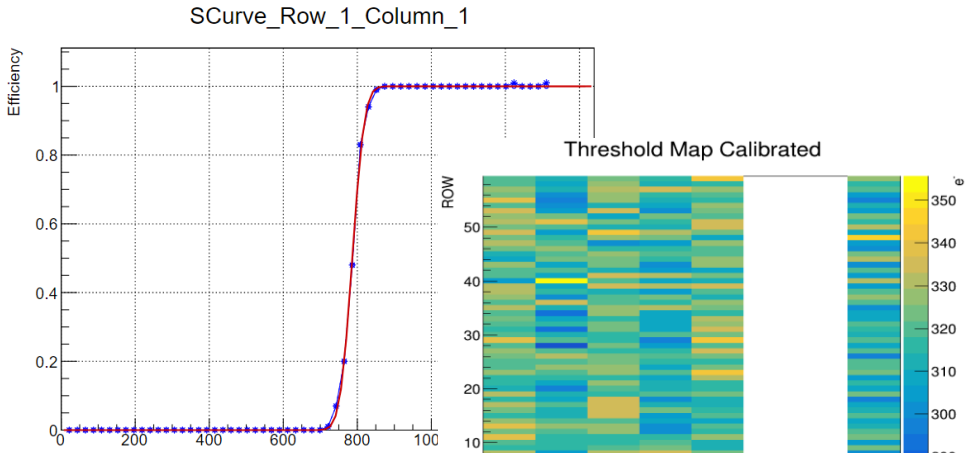
- Initial test of Chip3 indicates the chip is generally functioning well ☺
- But unfortunately a cross-talk problem is found ☹
  - The in-pixel digital circuit (comparator, priority logic) can induce charges on unfired pixels
  - The issue has been thoroughly investigated
  - Problem identified and fixed in a new version of design
- For now, can test only one pixel at a time

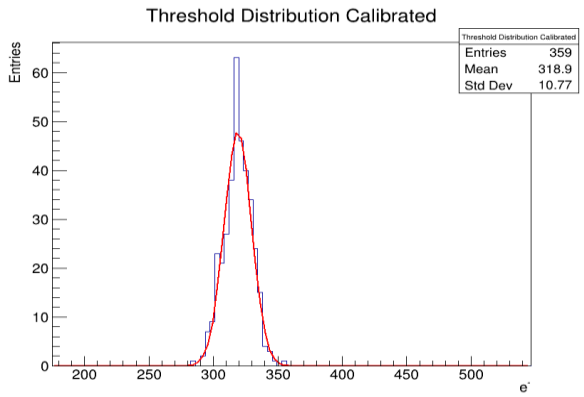


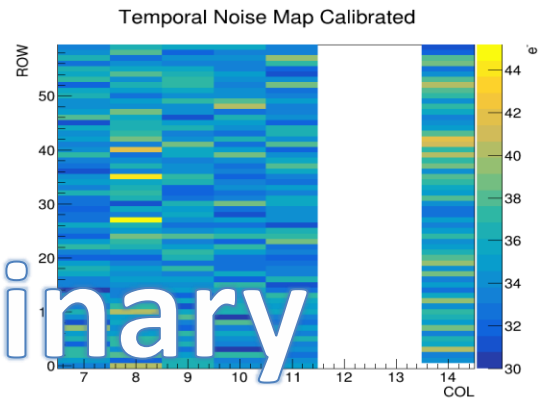


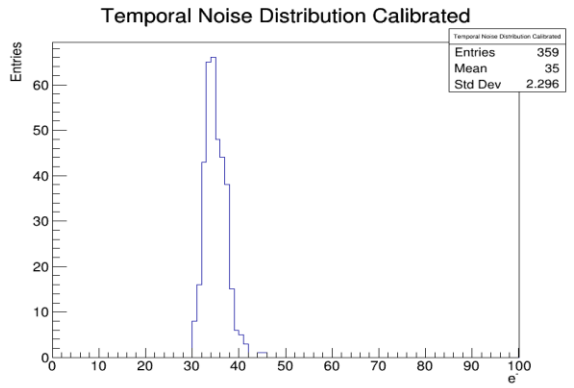
Threshold and noise

- Use the “S-curve” method to measure the threshold and noise
- Chip can be operated up to -6V









Preliminary

Strip-based

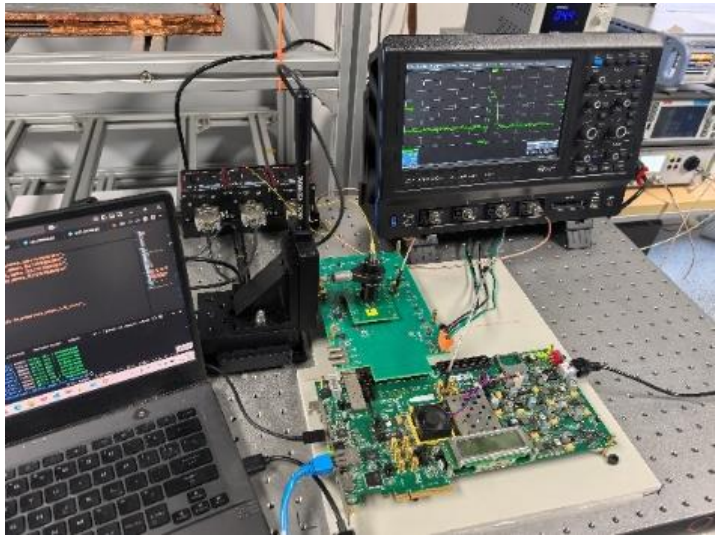
Bias/V	Thr_mean/e	Mismatch/e	TN/e
-2	343	8.2	45.5
-3	389	17.3	52.6
-4	325	8.7	37.0
-5	295	8.9	34.3
-6	298	10.6	36.8

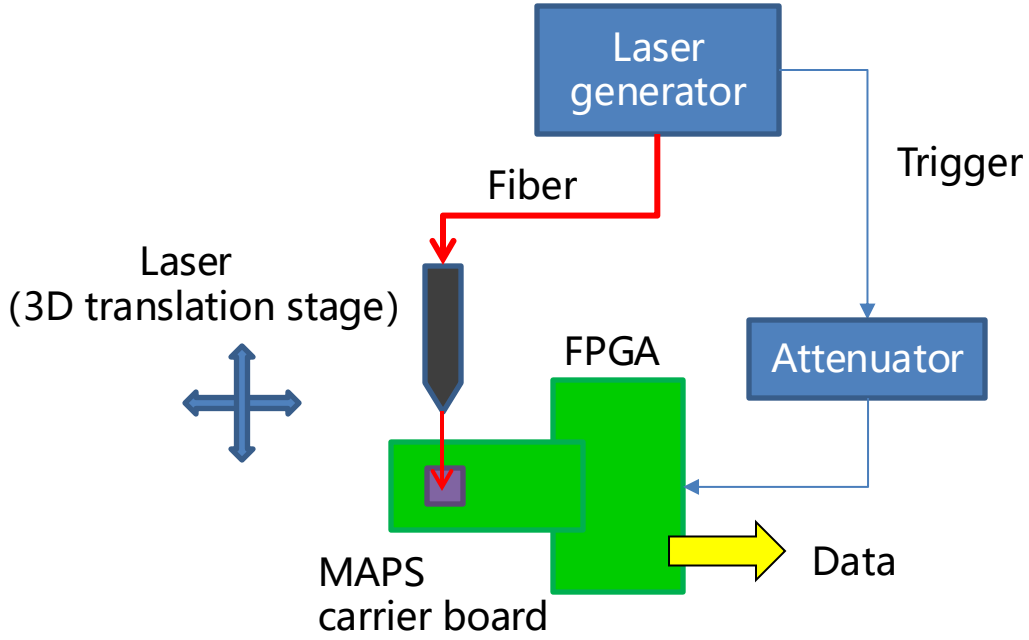
Pixel-based

Bias/V	Thr_mean/e	Mismatch/e	TN/e
-2	268	7.2	16.1
-3	235	2.8	15.3
-4	212	0.8	15.4
-5	178	5.3	11.3
-6	182	7.1	12.1

Laser test results

- Pico-second infrared laser can be used to excite charge carriers inside the sensor
  - Beam spot size can reach ~10μm; laser intensity tunable
  - High-precision 3D motorized translation stage (step size < 1μm)

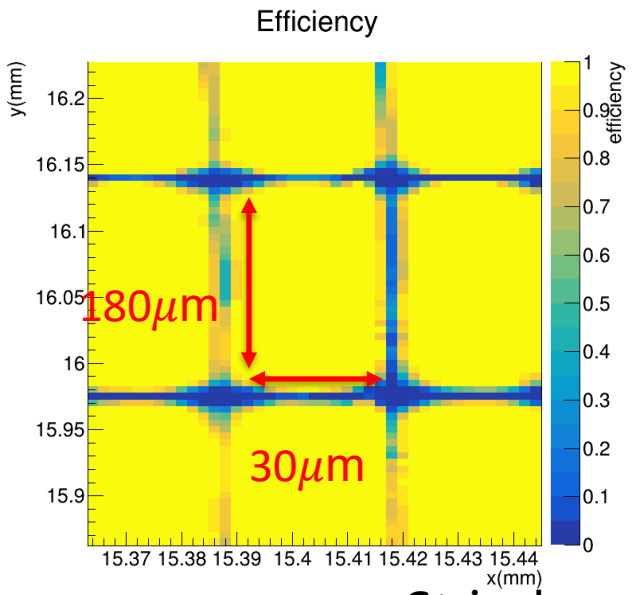




- Calibrate the laser intensity using the S-curve method (laser intensity → induced charge)
- Use the laser as the trigger to measure the detection efficiency

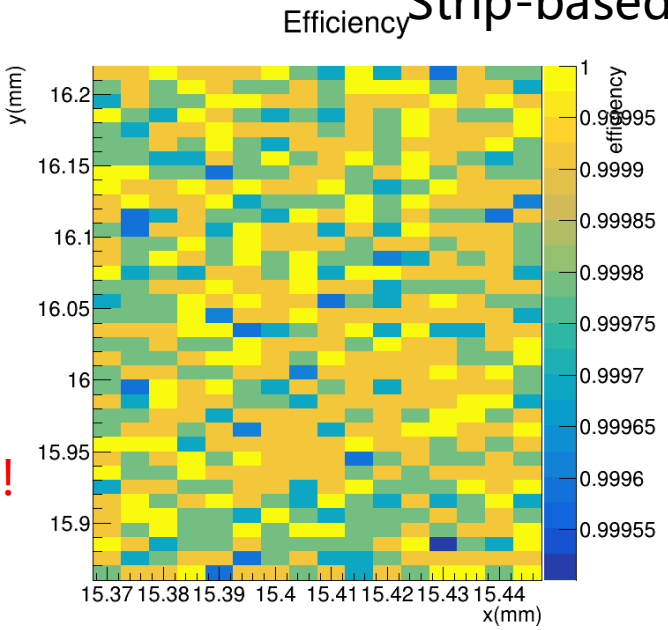
Laser test results: efficiency

With laser intensity equivalent to **600e-** (~0.375MIP)



91.62%

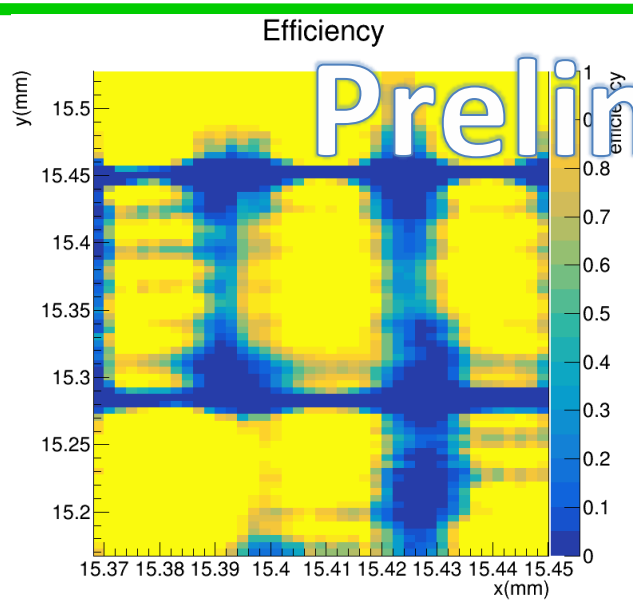
Strip-based



99.99%

With laser intensity equivalent to **1600e-** (~1MIP)

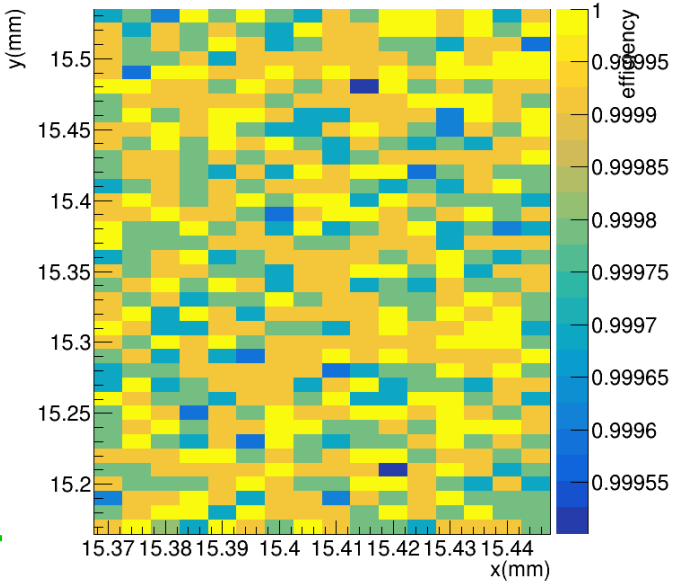
Almost 100% efficient!



Preliminary

70.22%

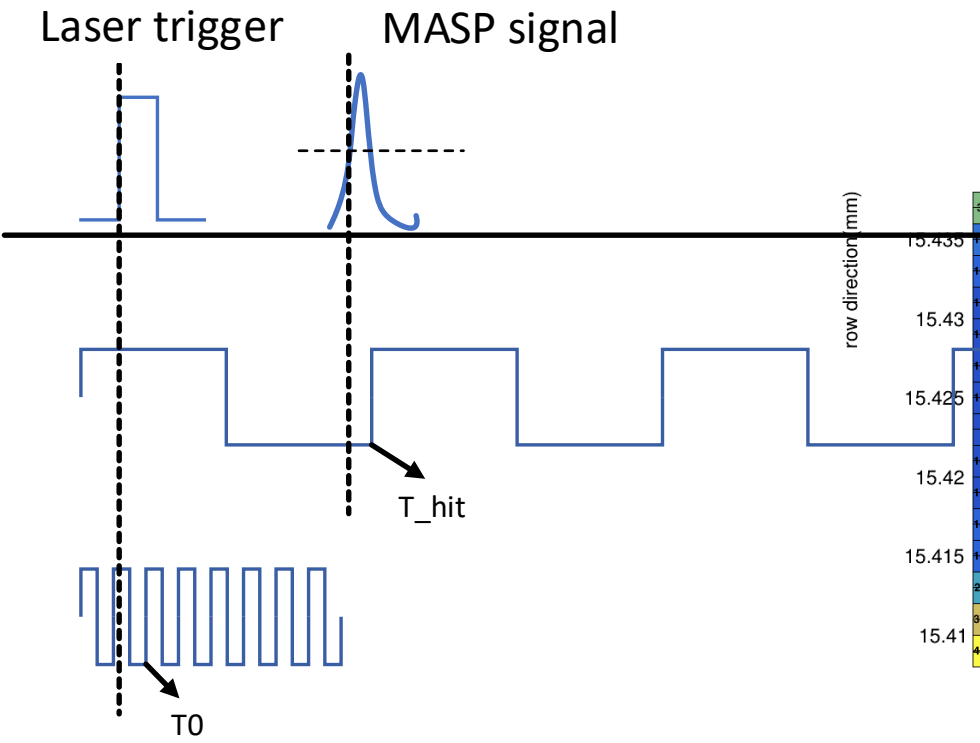
Pixel-based



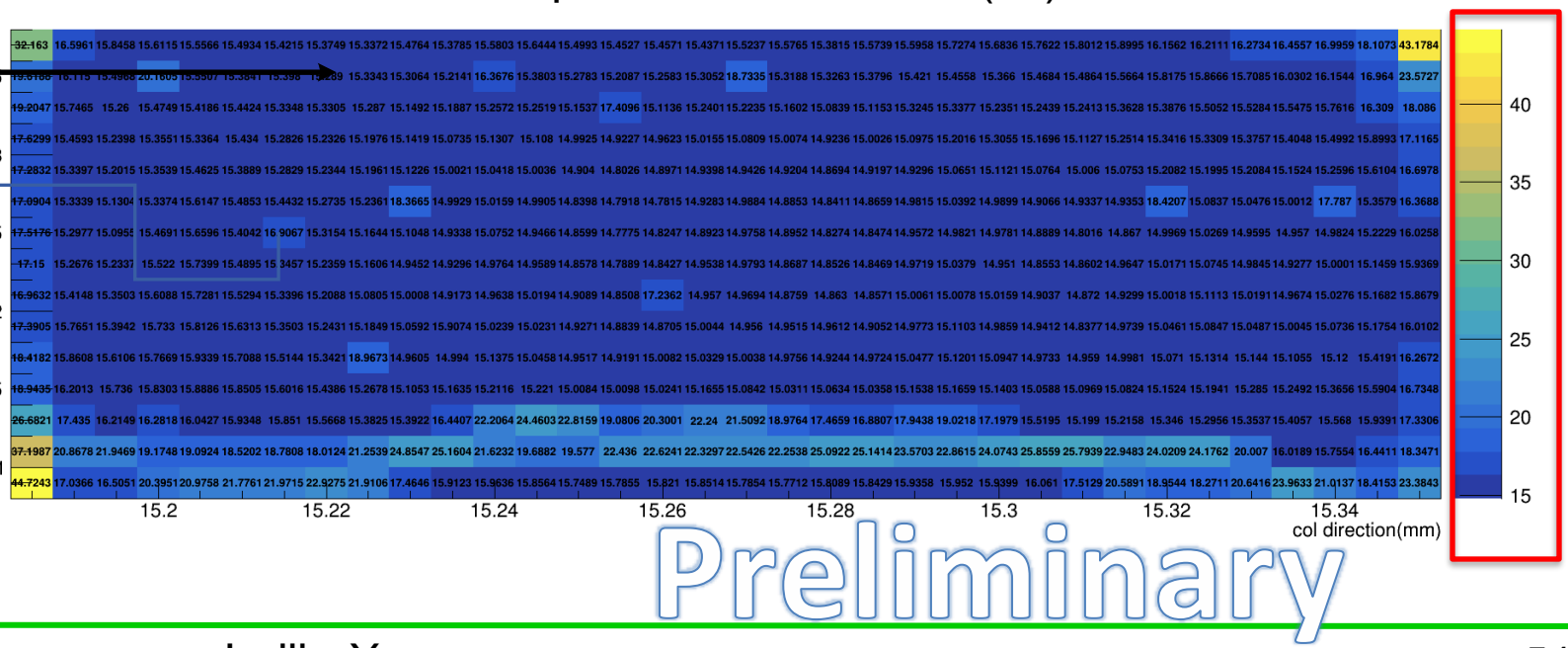
99.99%

Laser test results: timing resolution

- The laser test system can also be used to measure the timing resolution
  - The laser trigger to provide a reference time (with a 320MHz clock)
  - Measure the time difference between the ToA recorded by the MAPS and the trigger



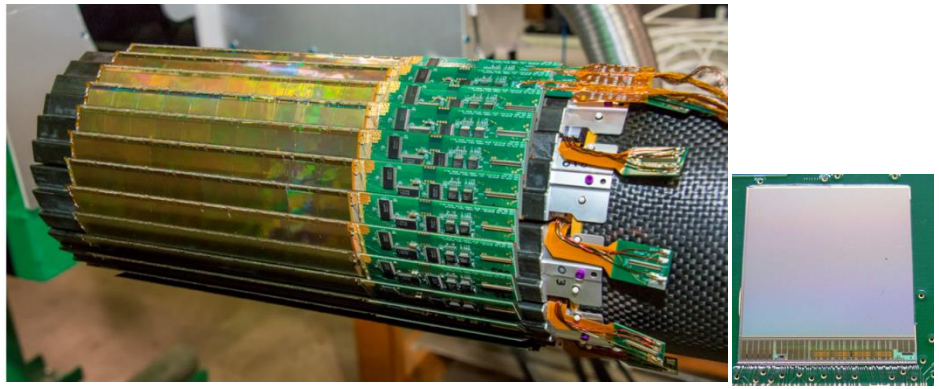
Timing resolution better than 40ns with the laser intensity equivalent to 1600e- (1MIP)



Preliminary

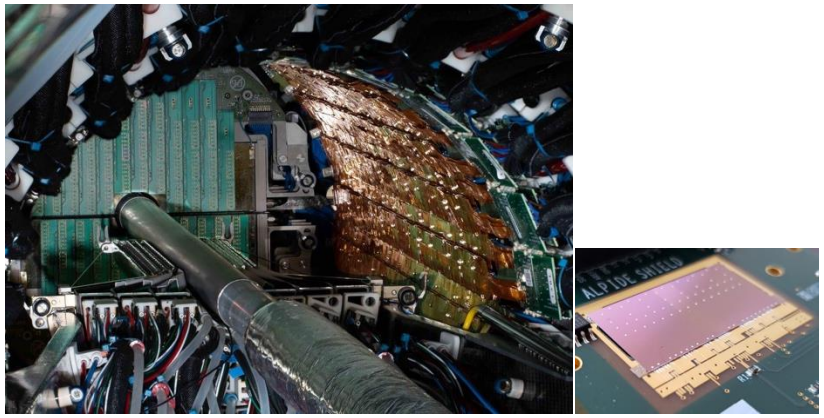
Prospect of MAPS development

CMOS MAPS development trend



1st generation of CMOS MAPS

MIMOSA28 (ULTIMATE) in STAR@RHIC
- Twin well 0.35 μm CMOS
- 21 μm pitch
- Integration time 190 μs
- 150 mW/cm^2 power consumption
- NIEL: few 10^{12} 1 MeV n_{eq}/cm^2



2nd generation of CMOS MAPS

ALPIDE in ALICE ITS2@LHC
- Quadruple well 0.18 μm CMOS
- 30 μm pitch
- Integration time <10 μs
- 40 mW/cm^2 power consumption
- NIEL: few 10^{13} 1 MeV n_{eq}/cm^2

What's next?

CMOS MAPS development trend

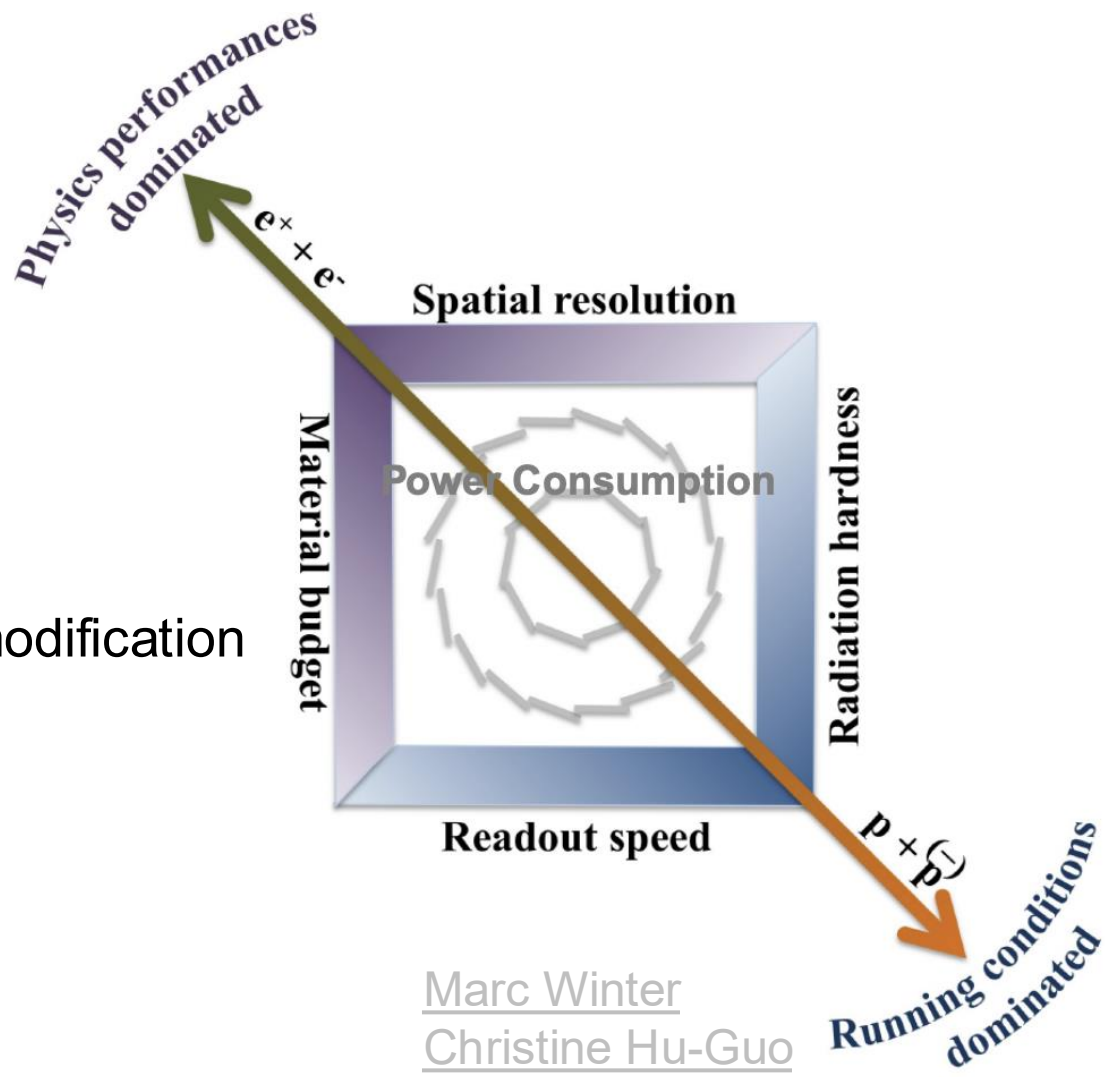
Driver 1: commercial CMOS technology evolution

- CMOS technologies with smaller feature size (28nm?):
  - smaller transistors, more metal layers
  - faster read-out, higher circuit density, lower power consumption

- Stitching with wafer scale chips

Driver 2: requirement from HEP experiments

- Faster readout speed → smaller feature size, process modification
- More radiation hard → process modification
- Better spatial resolution → smaller feature size
- Lower material budget → stitching



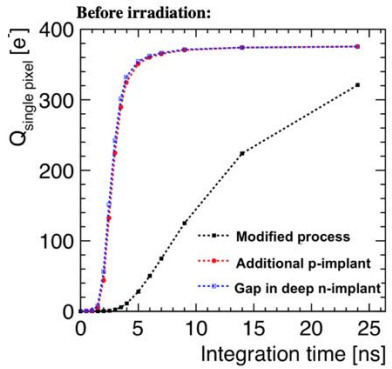
Marc Winter
Christine Hu-Guo

More radiation hard

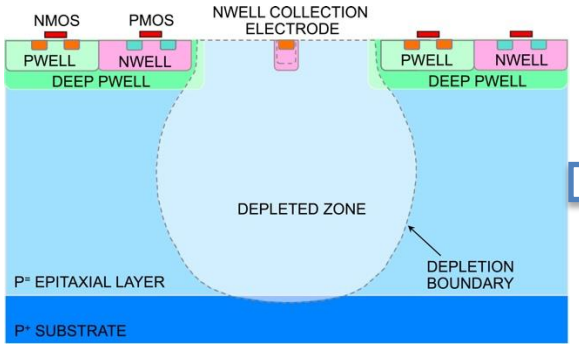
2.5th generation MAPS

- Radiation tolerance:
  - CMOS circuit typically more sensitive to ionizing radiation
  - Sensor to non-ionizing radiation (displacement damage)
- How to improve it? Full depletion!
  - More radiation hardness
  - Better time resolution
  - More efficient charge collection → better efficiency
- Need process modification

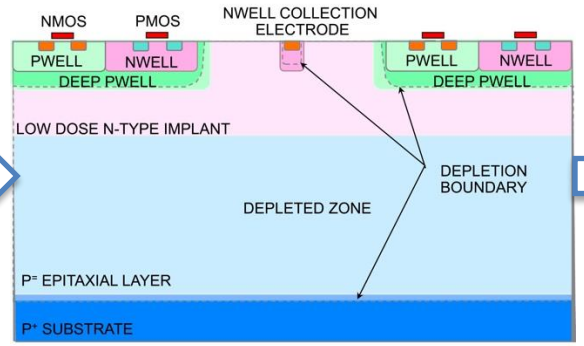
NIMA 938 (2019) 41–50	Dose (MGy)	Fluence (10^{16} 1 MeV n_{eq}/cm^2)
ALICE ITS	0.01	10^{-3}
LHC	1	0.3
HL-LHC 3ab^{-1}	5	1.5
Central tracker FCC	400	60



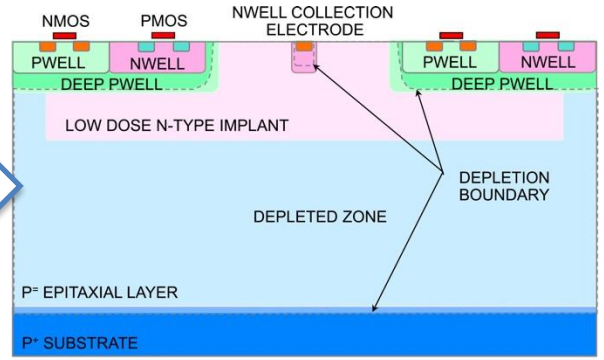
NIMA 871(2017) 90-96



Standard,
not fully depleted (ALPIDE)

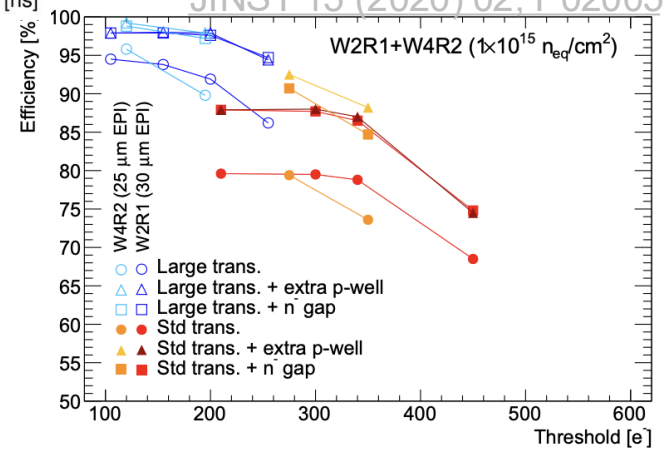


Modified with a n-planar layer,
fully depleted under bias

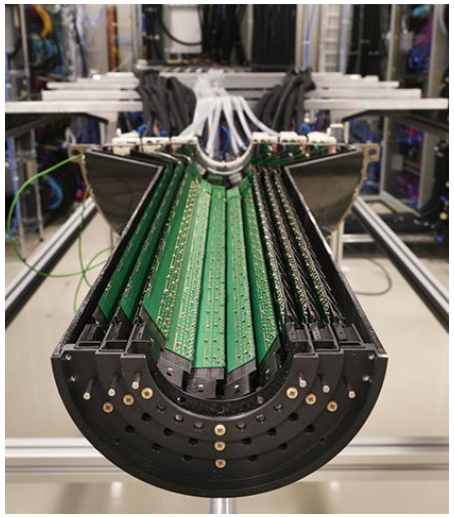


Modified with a gap,
Further improvements

JINST 15 (2020) 02, P02005



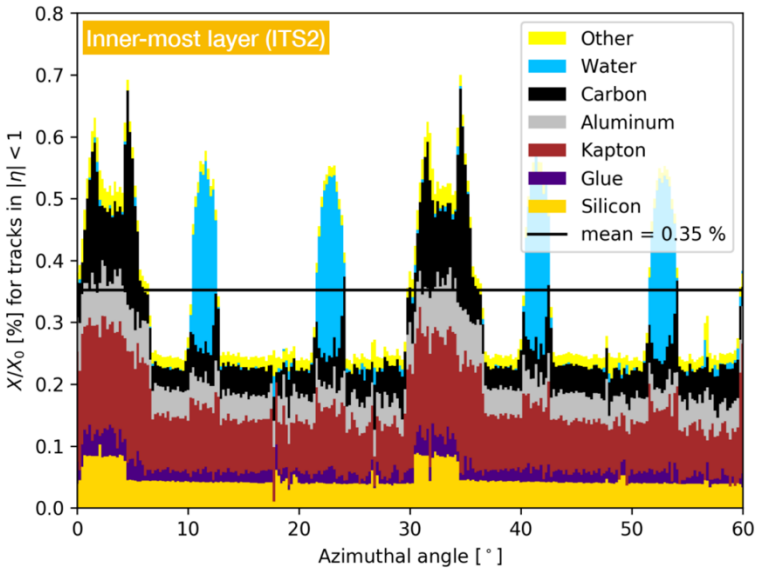
Lower material budget

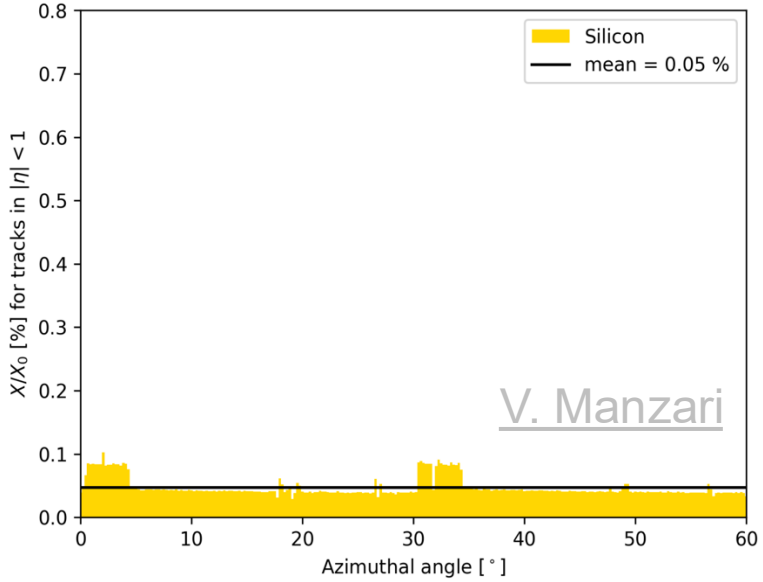


Material effect dominates the tracking performance at the low momentum region

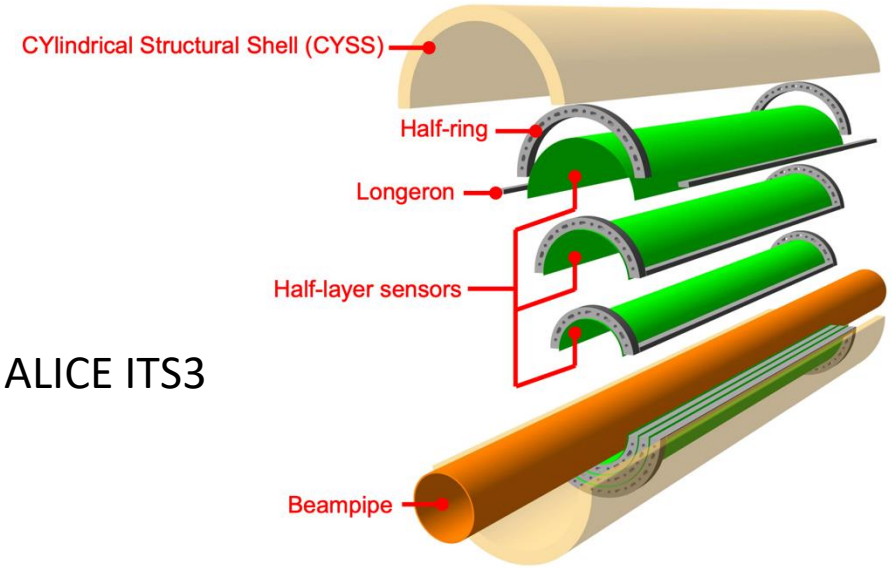
How to reduce the material budget?

- Reduce power consumption → air cooling!
- Reduce support materials → event self-supporting!





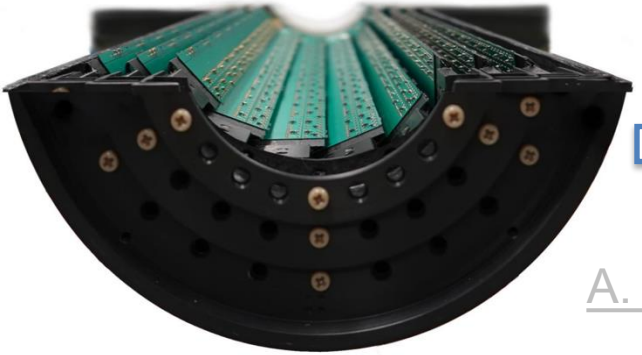
ALICE ITS3



3rd generation MAPS

ALICE ITS3

Wafer scale sensors with Stitching



ITS2 half Inner barrel

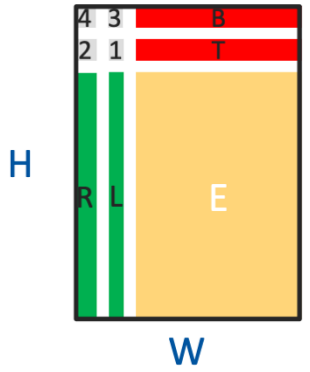
A. Kluge

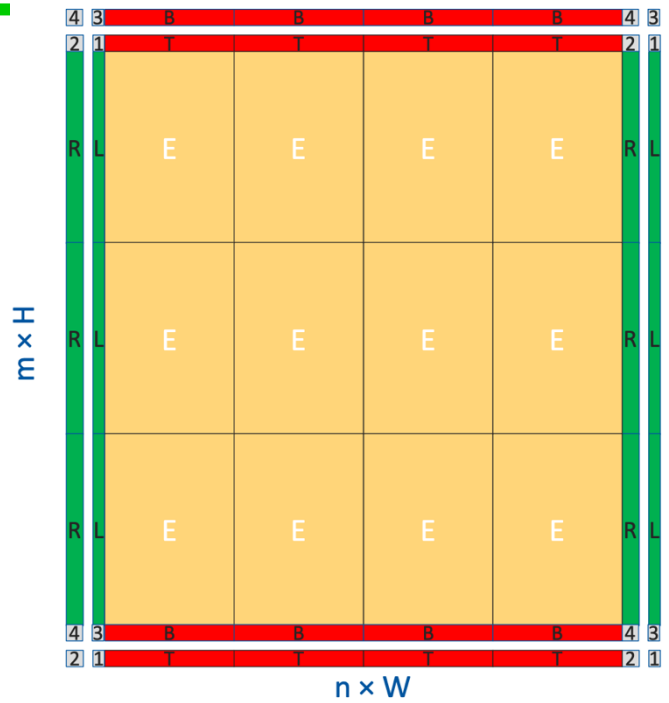
ITS3 Engineering Model 1

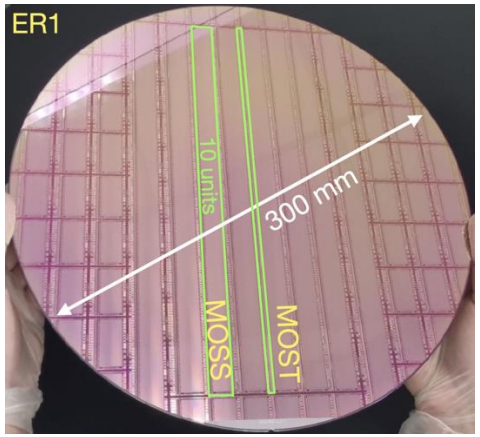
0.36% X_0 per layer
radius 1st layer = 24 mm

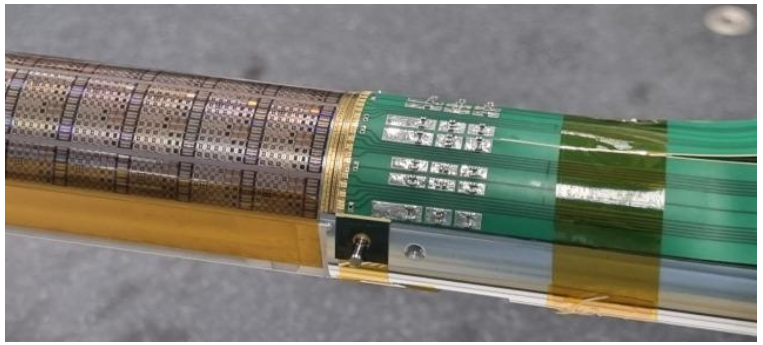
50 µm thick sensors ~ 0.07% X_0
Material budget:0.09% X_0 per layer
1 st layer 24 mm →19 mm

Design Reticle
(typ. 2×3 cm)

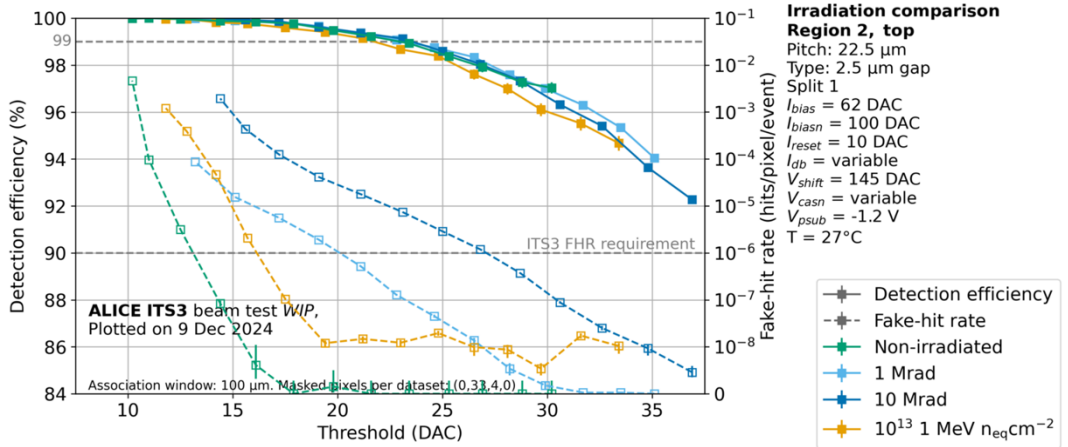








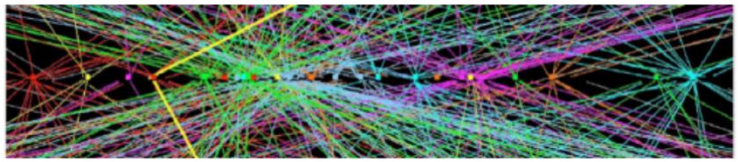
arXiv:2502.13591



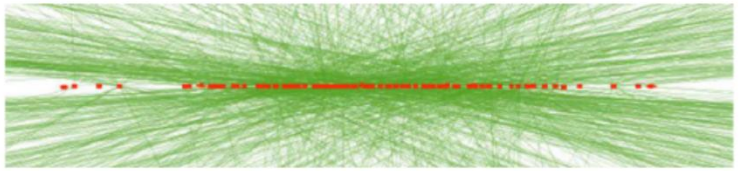
Enabling 4D tracking

NIMA 979(2020) 164383	HL-LHC	SPS	FCC-hh	FCC-ee	CLIC	$\mu\mu$ Col.
Fluence $[n_{eq} / \mathrm{cm}^2 / y]$	10^{16}	10^{17}	10^{17}	$< 10^{10}$	$< 10^{11}$	
Hit rate $[\mathrm{s}^{-1}\mathrm{cm}^{-2}]$	2–4G	8G	20 G	20 M	240 k	
Inn. tracker $[\mathrm{m}^2]$	10	0.2	15	1	1	
Out. tracker $[\mathrm{m}^2]$	200	–	400	200	140	
Pixel size $[\mu\mathrm{m}^2]$	50×50	50×50	25×50	25×25	25×25	
Time res [ps]	50	40	10	1k	5k	50–100

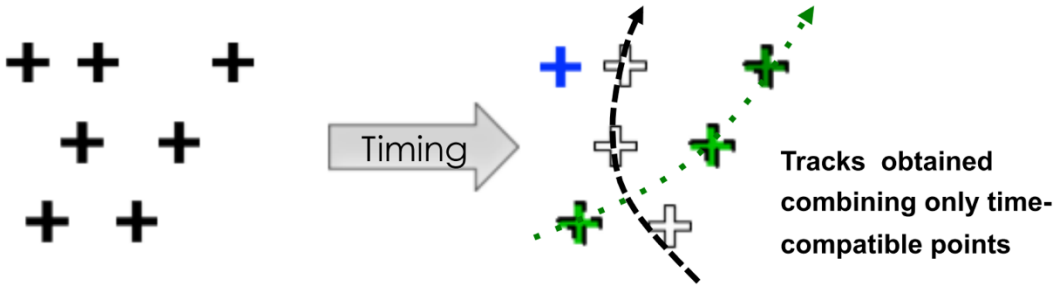
Current LHC: ~25 vertices



High-Luminosity LHC: ~200 vertices



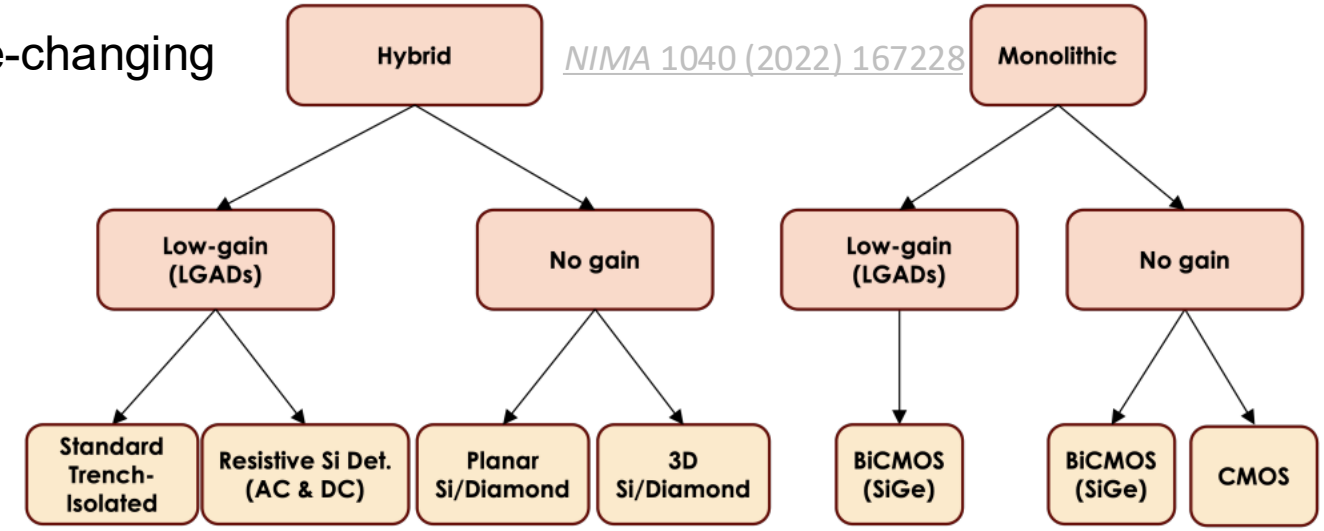
Precision timing at the level of 10-30ps will be a game-changing capability → LHCb VELO Upgrade II is aiming this!



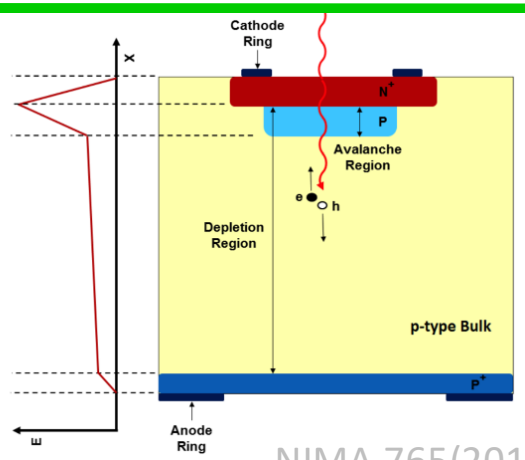
Rep. Prog. Phys. **81** 026101(2018)

R&D activities in sensors for 4D tracking

NIMA 1040 (2022) 167228

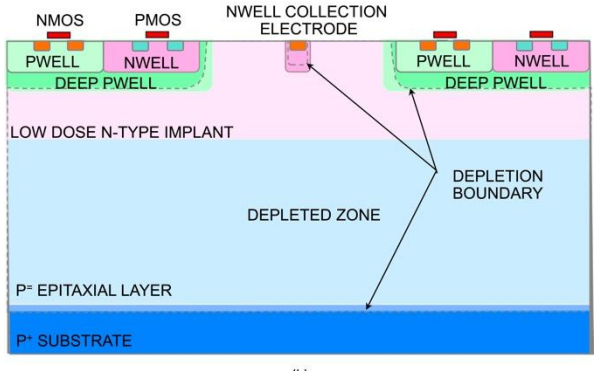


Enabling 4D tracking

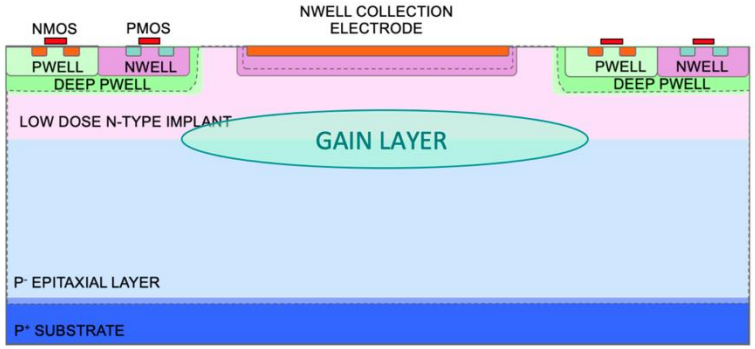


NIMA 765(2014) 12-16

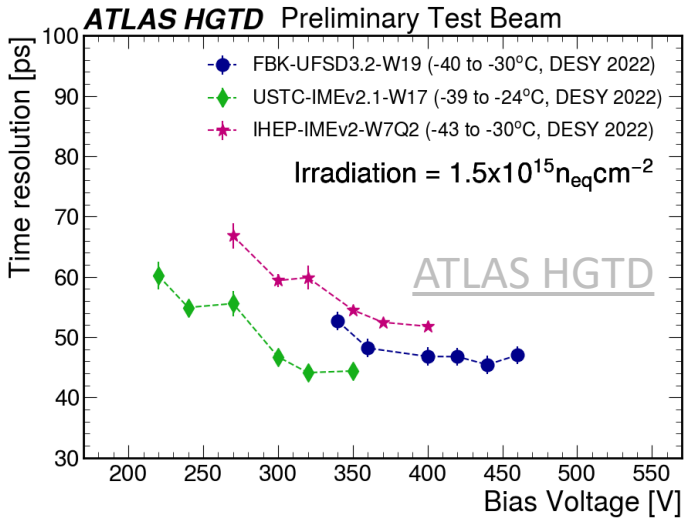
LGAD (low-gain avalanche diodes): ultra fast timing silicon detectors (~30ps unirradiated)



MAPS: excellent spatial resolution

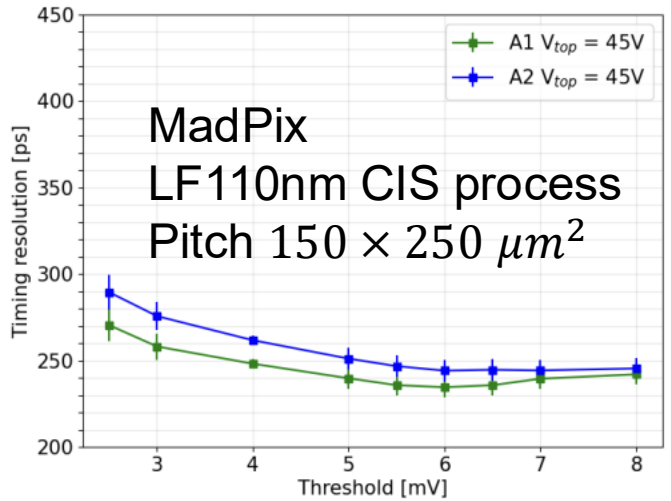


MAPS with internal gain: 4D tracking!



CMOS MAPS with internal gain looks very promising, but still many challenges:

- Process modification and verification
- Front-end design



arXiv:2406.19906

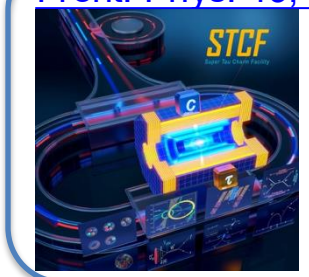
MAPS development in China

- CERN has been leading the 3rd generation MAPS technology development
  - 2nd generation MAPS technology already very matures (ALPIDE in ALCIE ITS2)
  - 2.5th generation also validated (Depleted MAPS)
  - 3rd generation: 65nm CIS process with stitching under very rapid development (ALICE ITS3)
- Unfortunately, no mature 2nd generation MAPS technology available in China yet
- Fortunately, many R&D ongoing
  - Lots of efforts on HR-CMOS development, eg:
    - JadePix, TaichuPix, MIC for CEPC
    - NuPix for HIAF
    - CharTPix for STCF
  - MAPS with stitching
    - BESIII inner tracker
    - CEPC vertex detector for Ref-TDR
  - HV-CMOS also actively being developed (CEPC tracker, LHCb mighty tracker etc)

Summary

- CMOS Monolithic Active Pixel Sensor, a cutting-edge technology, offers a promising option for vertexing & tracking detector in future collider experiments
  - Already successfully applied in HEP experiments (eg ALICE ITS2) with high detection efficiency and excellent spatial resolution
  - Also proposed for future experiments: ALICE ITS3, ALICE3, CEPC, STCF etc
- A MAPS based inner tracker is also proposed for the Super Tau-Charm Facility experiment
  - Existing MAPS could not fulfill the STCF requirement
  - Intensive R&D ongoing, with a focus on development of domestic technology
  - Preliminary test results promising
- Future R&D
  - Fully depleted MAPS
  - Stitching with wafer scale sensors, bent sensors
  - CMOS with internal gains for 4D tracking

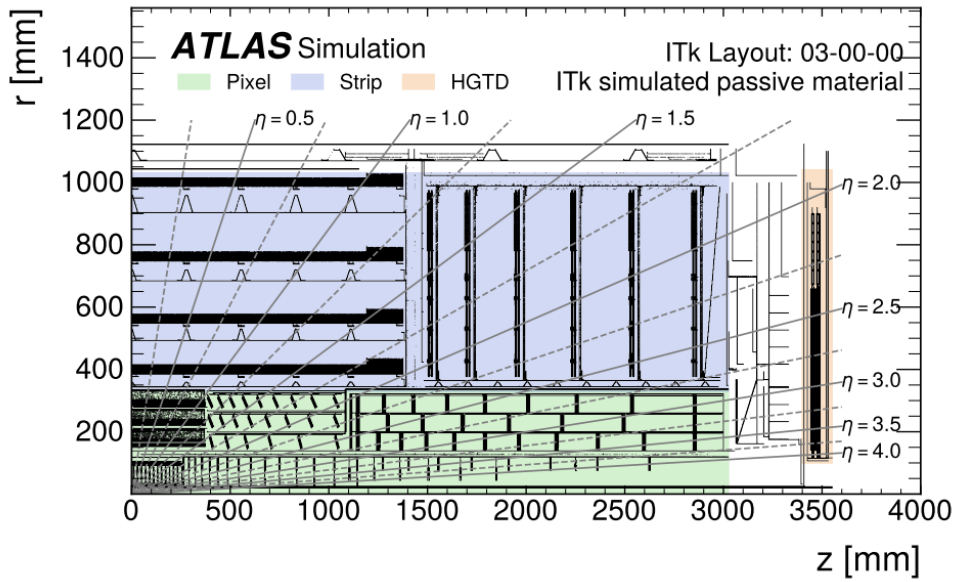
Front. Phys. 19, 14701 (2024)



- Power consumption: $\leq 100\mathrm{mW}/cm^2$
- Low material budget per layer: $\leq 0.35\%\ X_0$
- Spatial resolution: $\leq 30\mu m$
- Time resolution: $\leq 20\mathrm{ns}$

Backup

Pixels for HL-LHC



ATLAS:

- ~ 165 m^2 silicon strips
- ~ 13 m^2 silicon pixels (currently 2m^2)

ATLAS-TDR-030
ATLAS-TDR-025

Outer pixel layers (O(10m^2))

- NIEL ≈ 10^{15} n_{eq}/cm^2
- TID ≈ 100 Mrad
- rate ≈ 300 MHz / cm^2

Inner layers (O(1m^2))

- NIEL ≈ 5×10^{15} to 2×10^{16} n_{eq}/cm^2
- TID ≈ 1 Grad
- rate ≈ 3-4 GHz / cm^2

CMS:

- ~ 220 m^2 silicon strips
- ~ 5-6 m^2 silicon pixels (currently 2m^2)

CMS-TDR-014

LHCb U2 VELO ASIC

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Lifetime fluence [1×10^{16} 1 MeV n_{eq}/cm^2]	> 6	> 1
TID lifetime [MGy]	> 28	> 5
Sensor Timestamp per hit [ps]	≤ 35	≤ 35
ASIC Timestamp per hit [ps]	≤ 35	≤ 35
Hit Efficiency [%]	≥ 99	≥ 99
Power per pixel [µW]	≤ 23	≤ 14
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

LHCb
Upgrade 1:

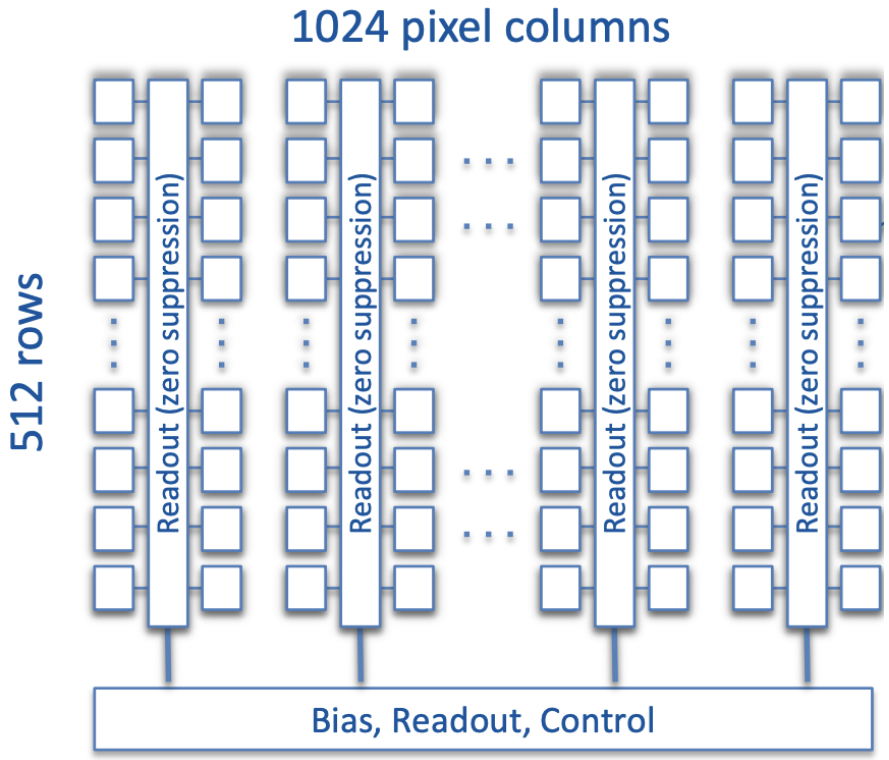
- VELO: silicon strips → silicon pixels
- Tracker Turicensis → Upstream Tracker

Upgrade II:

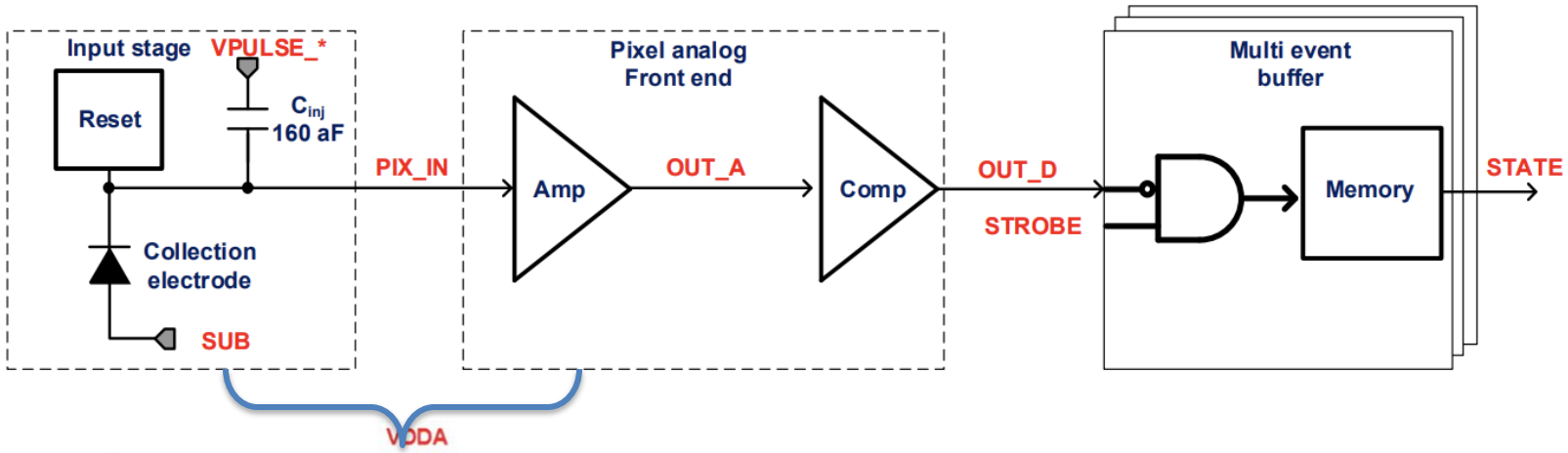
- VELO with 4D tracking, <50ps timing resolution per hit
- UT with CMOS
- SciFi → Mighty Tracker (HV-CMOS + SciFi)

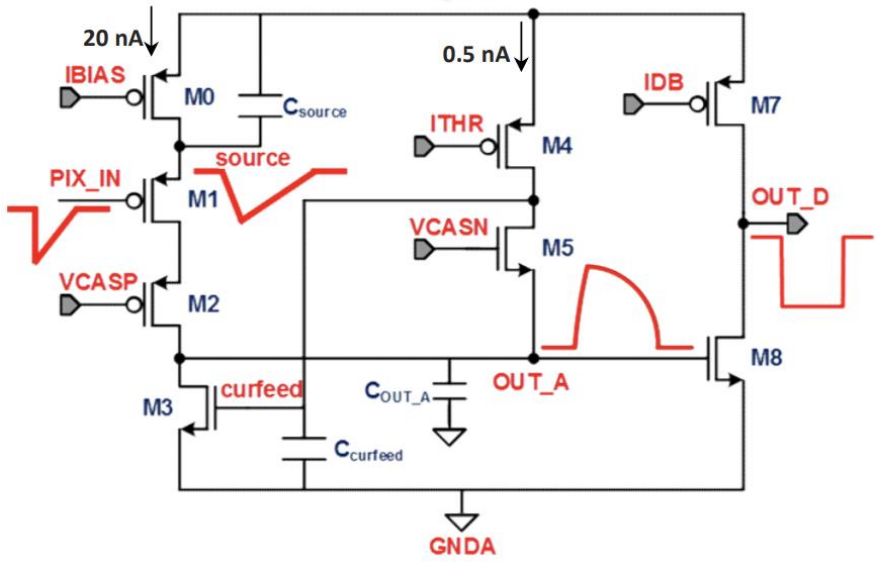
LHCB-TDR-023

ALPIDE features



The ALPIDE architecture: based on in-pixel hit discrimination and zero suppression readout by priority encoding





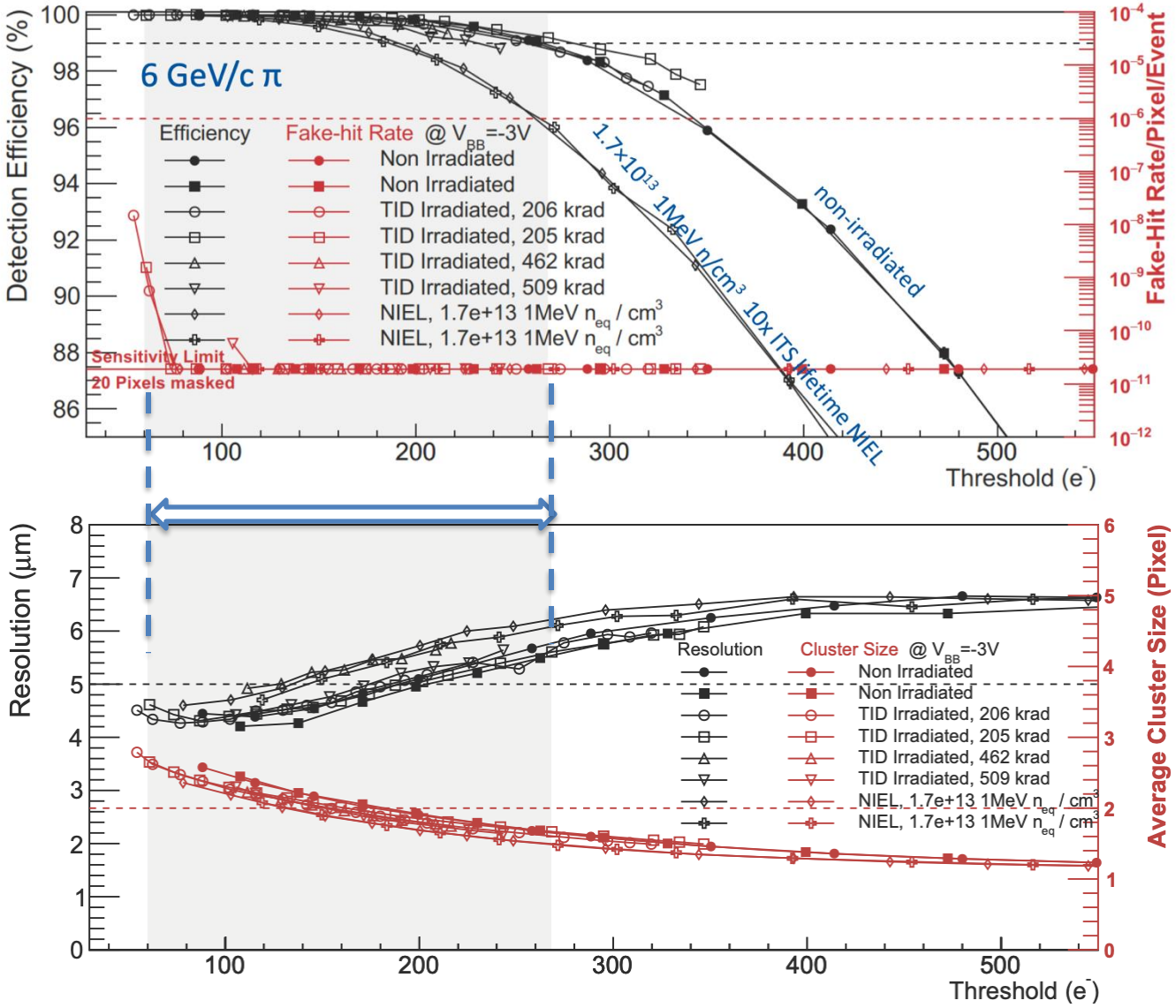
Performance:

- Threshold 92e, ENC 2e (simulation)

Front-end: continuously active, low-power, in-pixel discriminating

D. Kim et al 2016 JINST 11 C02042

ALPIDE features



Testbeam measurements

- Large operational margin to meet the design requirements:
  - detection efficiency >99%
  - fake-hit rate <10^{-6} pixel/event
- Resolution of 5 μm at a threshold of 200 electrons

Nuclear Physics A 967 (2017) 900–903

Other MAPS development

Liang Zhang 2023
Jerome Baudot 2022

Chip	Process	Pixel array	Pixel size	Main Institute	Target	Comment	
MIMOSA28	350 nm OPTO	928 × 960	20.7 × 20.7 μm^2	IPHC	rad. hard	STAR	Twin-well HR-CMOS
WCPS	350 nm OPTO	644 × 3600	30 × 120/160/200 μm^2	SDU/IHEP/HIT	low material budget	Stitching	
ALPIDE	TJ 180 nm	512 × 1024	28 × 28 μm^2	CERN	high granularity	ALICE ITS	Quad-well HR-CMOS
MIMOSIS	TJ 180 nm	504 × 1024	30.24 × 26.88 μm^2	IPHC	rad. hard high granularity	CBM Micro-Vertex	
MALTA	TJ 180 nm	224 × 512	36.4 × 36.4 μm^2	CERN	high granularity	HL-LHC	
TJ-Monopix2	TJ 18 0nm	512 × 512	33.04 × 33.04 μm^2	CERN/Bonn	rad. hard	HL-LHC	
TaichuPix	TJ 180 nm	512 × 1024	25 × 25 μm^2	IHEP/IFAE/CCNU/SDU/NWPU/NJU	High granularity, rad. hard, fast readout	CEPC	
MIC4	TJ 180 nm	128 × 64	25 × 25 μm^2	CCNU	Fast readout	CEPC	
JadePix3	TJ 180 nm	192 × 512	16 × 26 μm^2 16 × 23.11 μm^2	IHEP/CCNU/SDU	position resolution and low power	CEPC	
Nupix-A1	130 nm	128 × 64	30 × 30 μm^2	IMP SLIMP	heavy-ion experiments	HIRFL & HIAF	
ATLASpix3	AMS/TSI 180 nm	372 × 132	150 × 50 μm^2	KIT/CPPM	rad. hard	ATLAS	HV-CMOS
RD50-MPW3	150 nm HVCOMS	64 × 64	62 × 62 μm^2	RD50	rad. hard high granularity	HL-LHC FCC	
MuPix10	TSI 180 nm	250 × 256	80 × 80 μm^2	University of Heidelberg	rad. hard	Mu3e	
LF-Monopix2	LF 150 nm	340 × 56	50 × 150 μm^2	Bonn	rad. hard	HL-LHC	
MightyPix1	TSI 180 nm	320 × 29	165 × 55 μm^2	University of Liverpool	rad. hard	LHCb upgrade	
SOFIST	SOI 200 nm	128 × 128	36 × 36 μm^2	KEK	high granularity, fast readout	ILC	SOI
CPV-4	SOI 180 nm	128 × 128	21.04 × 17.24 μm^2	IHEP	high granularity	CEPC	

Detector considerations

- Physics requirements

BESIII tracking performance

	Sub-system	BESIII
MDC	Single wire $\sigma_{r\phi}$ (μm)	130
	σ_p/p (1 GeV/c)	0.5%
	σ (dE/dx)	6 %

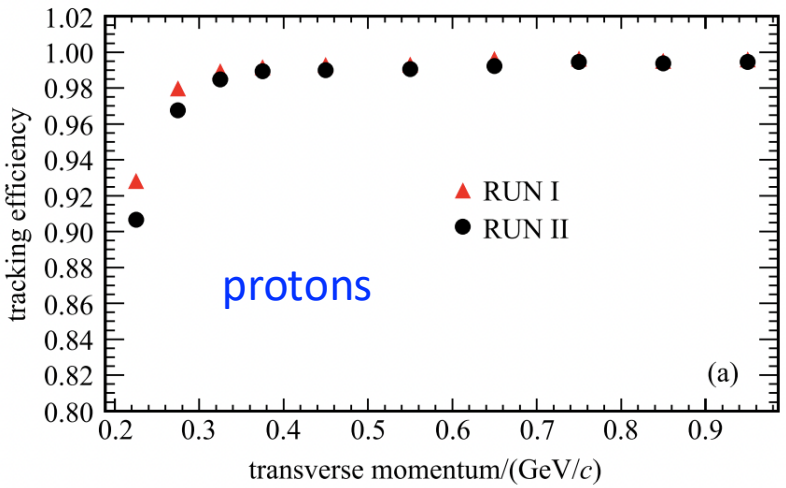
Vertex resolution: σ_{d0} ~0.2 mm; σ_{z0} ~ 1.mm

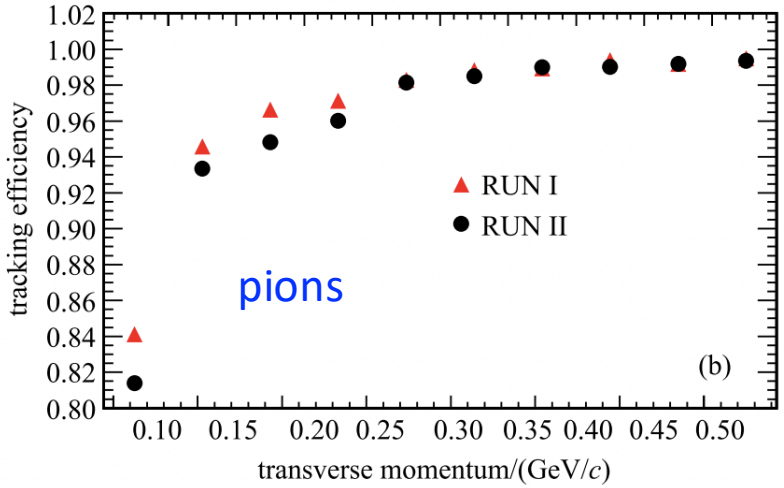
- ❖ No stringent requirements on vertexing
- ❖ The main challenge is the tracking at the low momentum region (p_T < 100 MeV)

Process	Physics Interest	Optimized Sub-detector	Requirements
$\tau \to K_s \pi \nu_\tau$,	CPV in τ sector,		acceptance: 93% of 4π; trk. effi.:
$J/\psi \to \Lambda\bar{\Lambda}$,	CPV in hyperon sector,	Tracker	> 99% at p_T > 0.3 GeV/c; > 90% at p_T = 0.1 GeV/c
$D_{(s)}$ tag	Charm physics		σ_p/p = 0.5%, $\sigma_{\gamma\phi}$ = 130 μm at 1 GeV/c

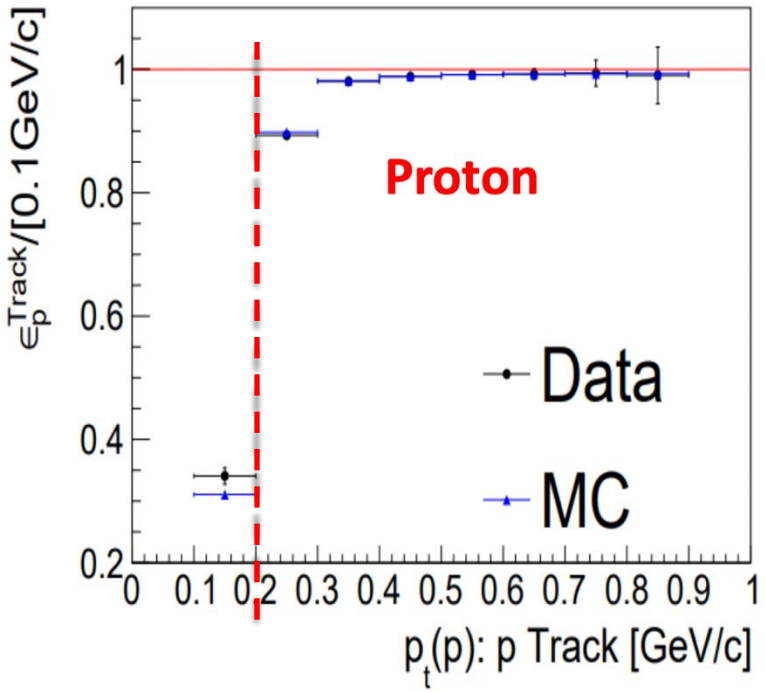
Detector considerations

- The challenge at the low p_T region
  - For BESIII, the tracking efficiency drops sharply below 100MeV
- There is strong physics motivation to go to low p_T region
- Excellent impact parameter resolution is mandatory for reconstruction of secondary vertices



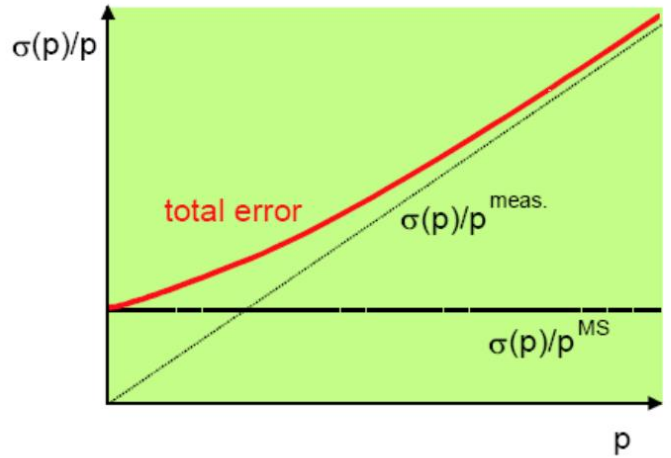


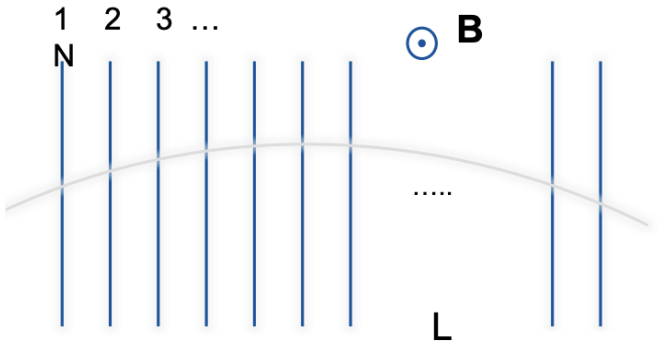
BESIII tracking efficiency,
Chin.Phys.C 40 (2016) 2, 026201



Detector considerations

- Tracking challenges at low p_T
  - Momentum resolution: Multiple Coulomb scattering
  - Track reconstruction efficiency
- Low material budget is essential





$$\frac{\sigma(p)}{p_{\mathrm{T}}} = \frac{\sigma(p)}{p_{\mathrm{T}}}\bigg|^{\text{track error}} \oplus \frac{\sigma(p)}{p_{\mathrm{T}}}\bigg|^{\mathrm{MS}}$$

$$\frac{\sigma(p)}{p_{\mathrm{T}}}\bigg|^{\text{track error}} \approx \frac{\sigma_{r\phi}[m]p_{\mathrm{T}}[\mathrm{GeV}]}{0.3B[T](L[m])^2}\sqrt{\frac{720}{N+4}}$$

Position resolution: O(10μm) on hybrid and down to O(1-3μm) on MAPS

$$\frac{\sigma(p)}{p_{\mathrm{T}}}\bigg|^{\mathrm{MS}} \approx \frac{0.0542}{\beta B[T]L[m]}\sqrt{\frac{X_{\mathrm{tot}}}{X_0}}$$

Multiple scattering: Thin detectors on light carbon fiber supports

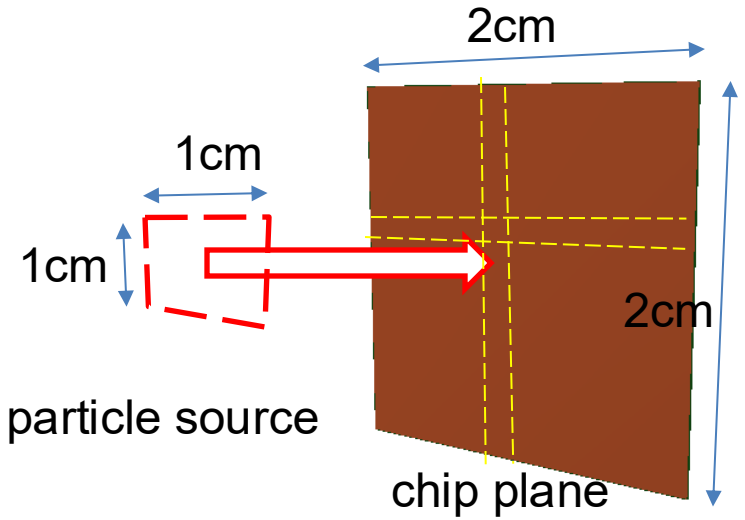
X_{tot}/X_0: Total material budget

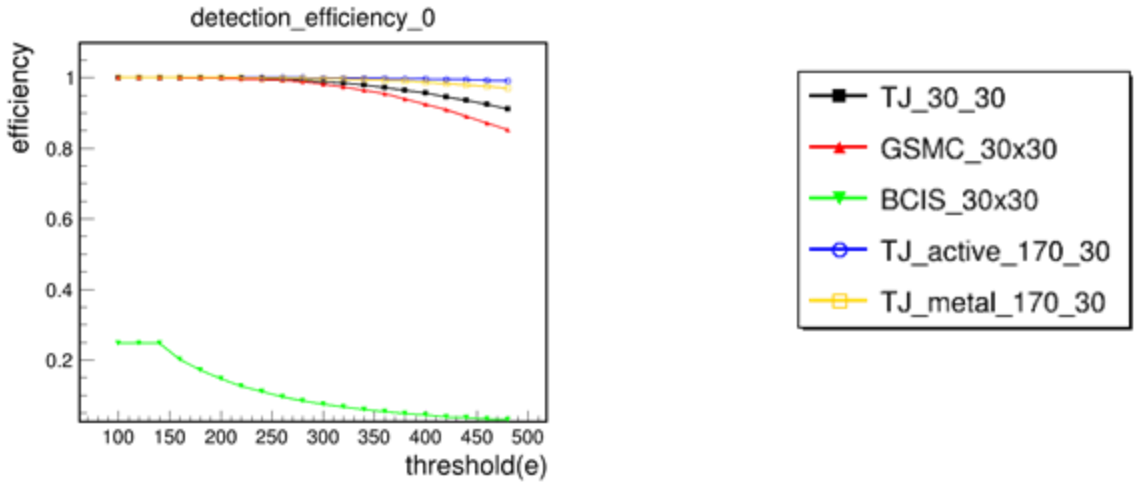
Particle Detectors, C. Grupen, B. Schwartz

MC simulation

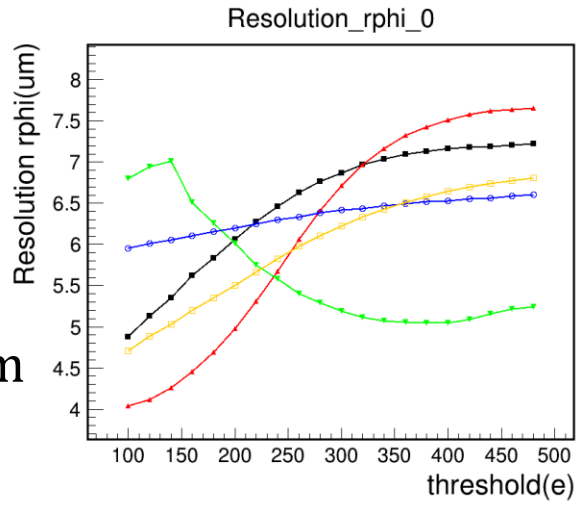
- MIP: 1Gev μ^- perpendicularly, randomly incident
- Ionization & charge collection simulation under the STCF simulation framework
  - OSCAR: the offline software of Super Tau Charm Facility

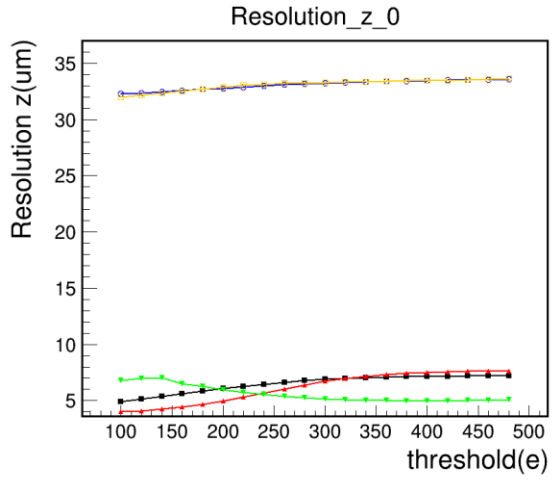
arXiv:2211.03137





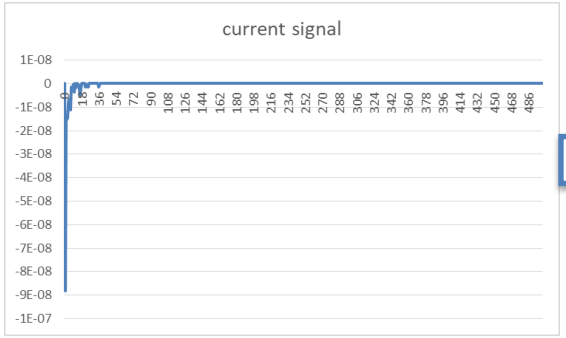
- Good detection efficiency for all technologies except for BCIS90, >98% @300e threshold
- Spatial resolution: $4\mu m$ ~ $8\mu m$ in the $30\mu m$ pitch direction
- In the $170\mu m$ pitch direction, spatial resolution ~$30\mu m$

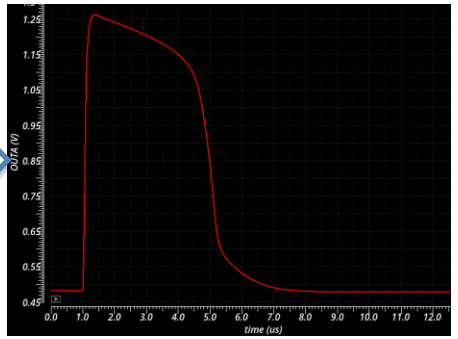


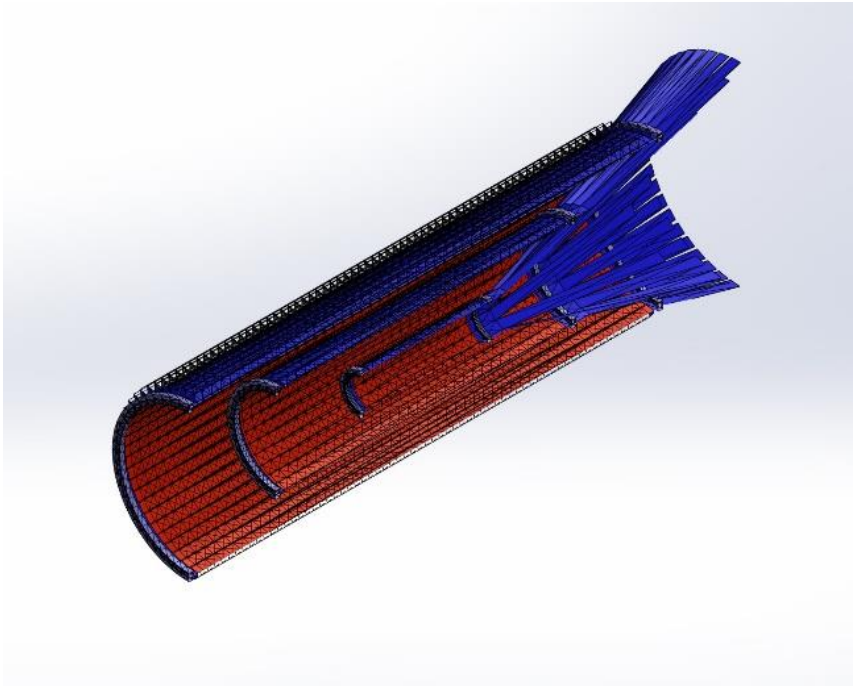


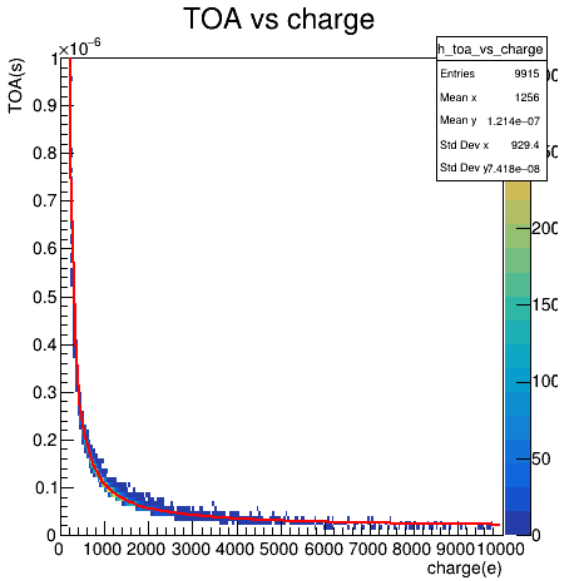
STCF ITKM simulation

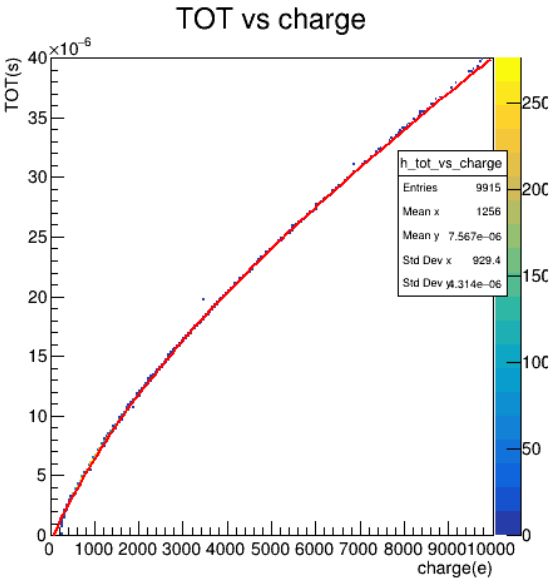
- MC simulation of the entire inner tracker system
- Chip + Flex + Carbon fiber support
  - ~0.27% X_0 for layer 1&2
  - ~0.29% X_0 for layer 3
- Full digitization process considering pre-amplifier response



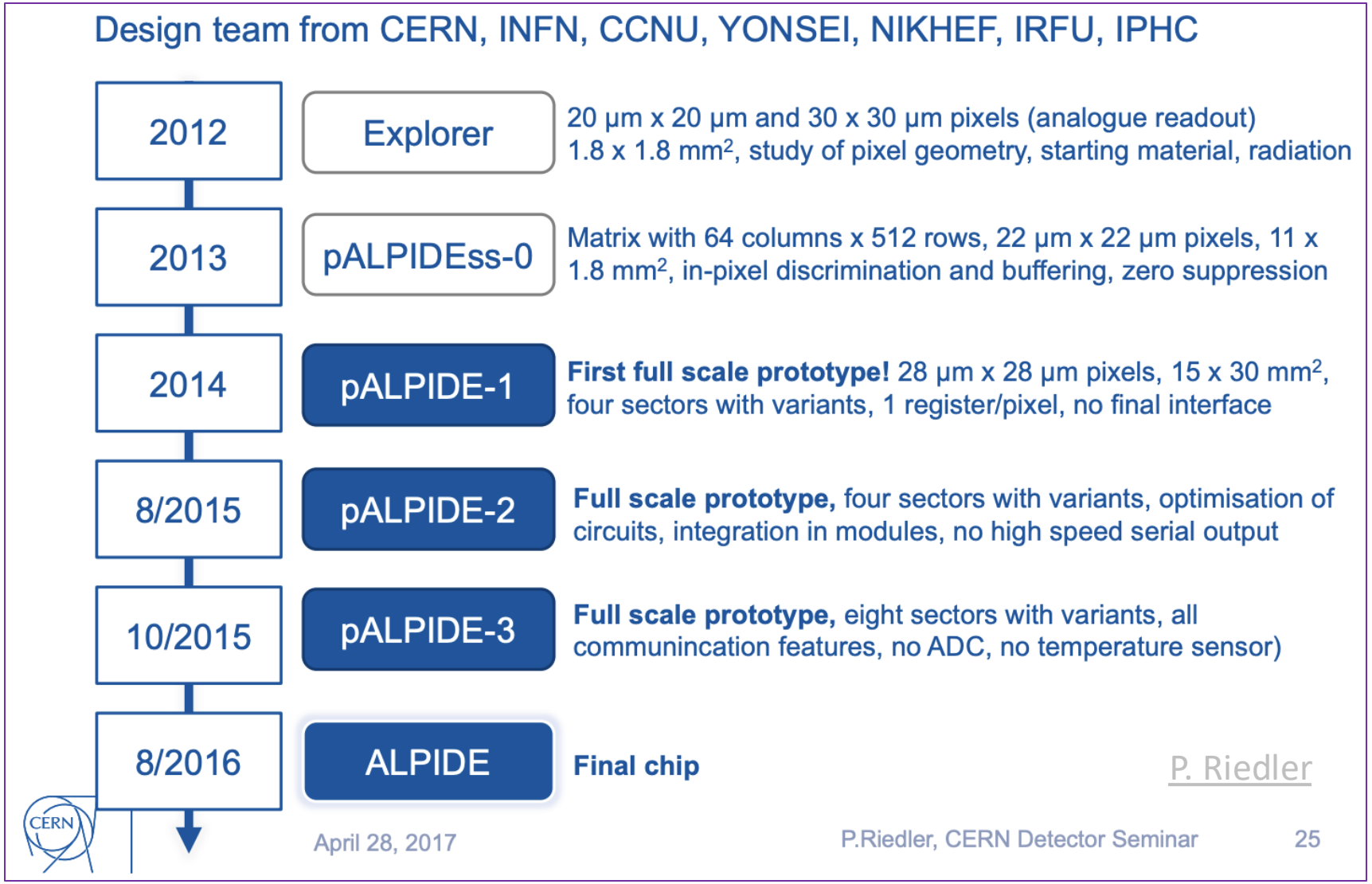








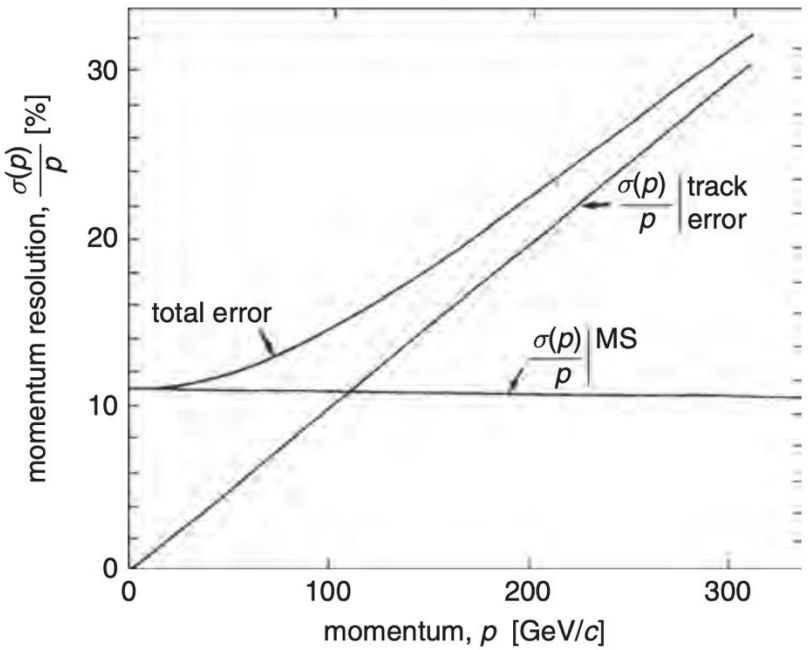
ALPIDE Development

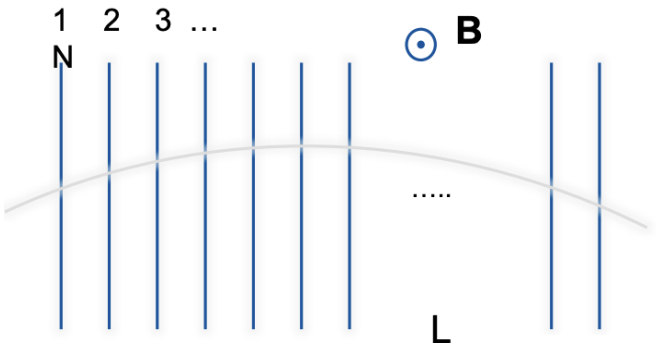


Tracking

Particle Detectors, C. Grupen, B. Schwartz

- Momentum resolution





$$\frac{\sigma(p)}{p_{\mathrm{T}}} = \frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{track error}} \oplus \frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{MS}}$$

$$\frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{track error}} \approx \frac{\sigma_{r\phi}[m]p_{\mathrm{T}}[\mathrm{GeV}]}{0.3B[T](L[m])^2}\sqrt{\frac{720}{N+4}}$$

Position resolution: O(10μm) on hybrid and down to O(1-3μm) on MAPS

$$\frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{MS}} \approx \frac{0.0542}{\beta B[T]L[m]}\sqrt{\frac{X_{\mathrm{tot}}}{X_0}}$$

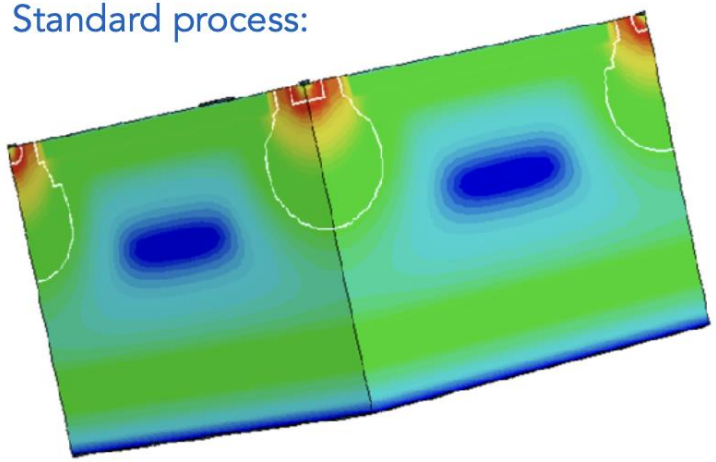
Multiple scattering: Thin detectors on light carbon fiber supports

X_{tot}/X_0: Total material budget

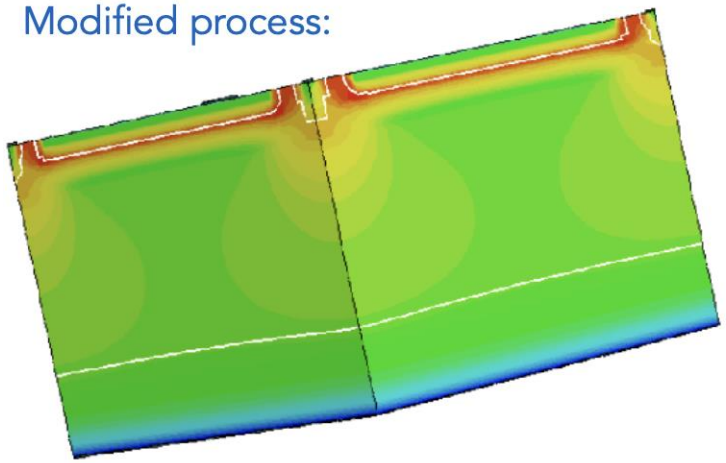
Process modification: simulation

Magdalena Munker

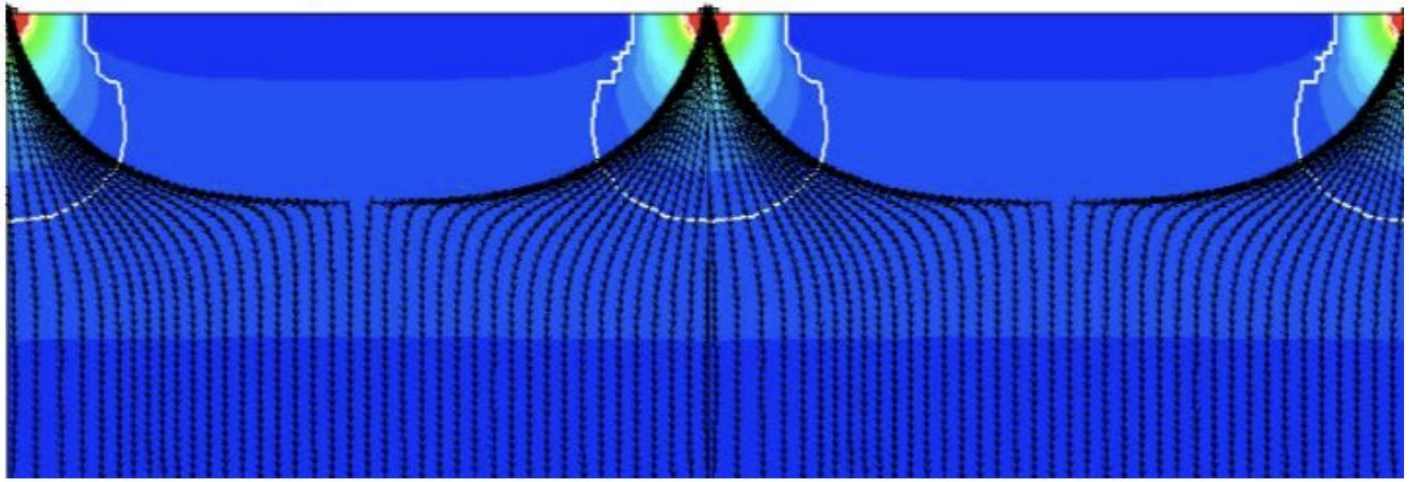
Standard process:



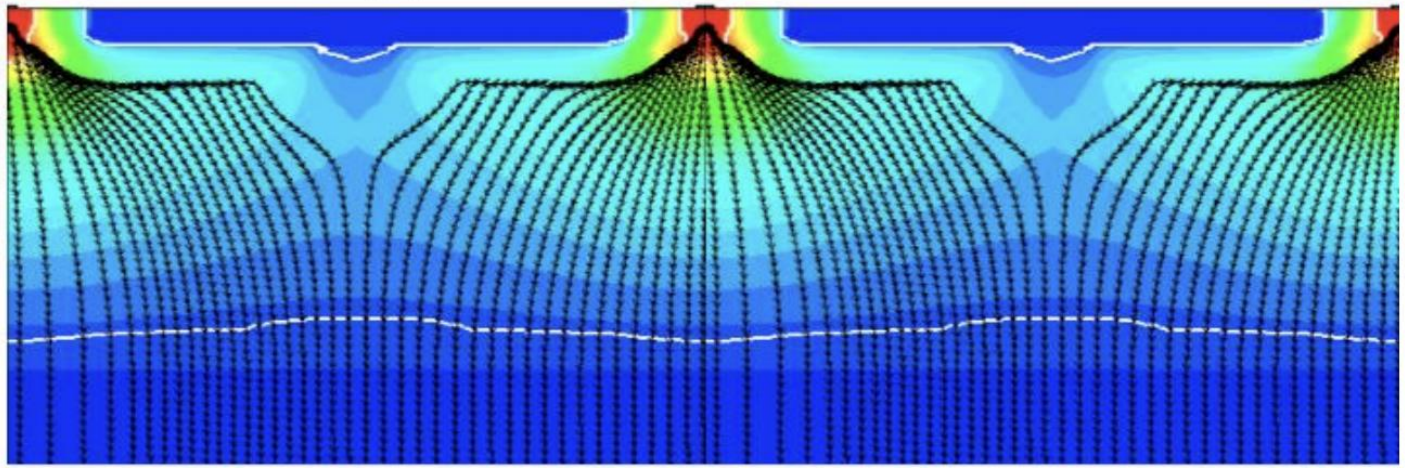
Modified process:



Standard – ALPIDE like sensor



Modified with gap sensor



Expected tracking performance for STCF

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