数字信号处理在核物理实验中的应用

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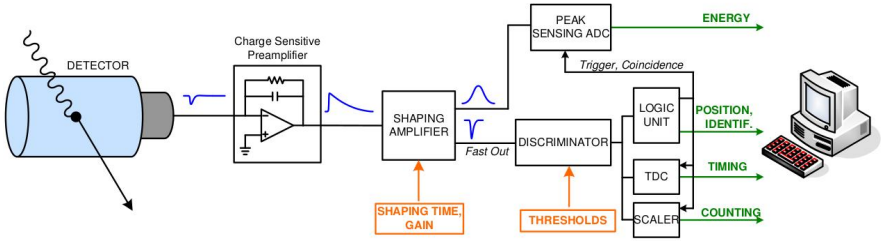
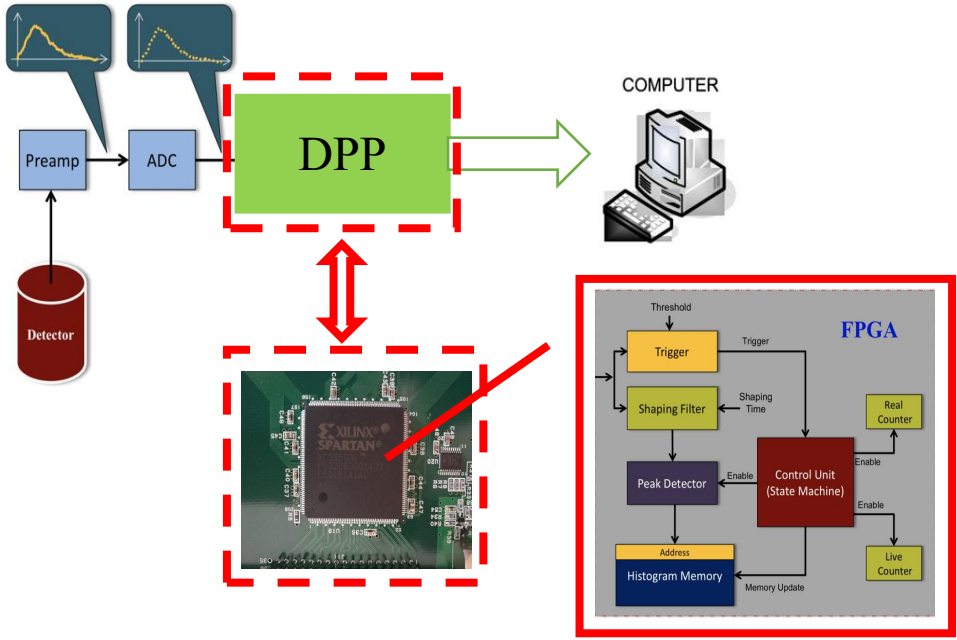
- 引言
- 常见数字信号处理算法
- 近期进展
- 未来展望

模拟与数字化系统信号处理流程





- 通过硬件进行信号处理和生成触发，

  最后才数字化

- 记录的信息：脉冲高度/粒子到达时间

- 不同的探测器需要不同的信号处理模块

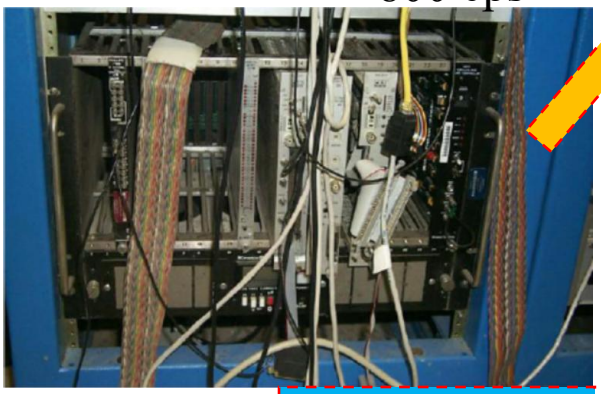
- 单个模块可以完成模拟电子学多个模块的功能
- 尽可能早的 A/D 转换，尽可能晚的数据压缩，保存完整的原始信息。
- 多参数分析：能量、时间、脉冲形状，所有信息来自同一个数据流

  减少尺寸、线缆、功耗以及每通道的成本

- 高可靠性和可重复性
- 灵活性：不同数字算法能够随时设计和加载到同一个硬件

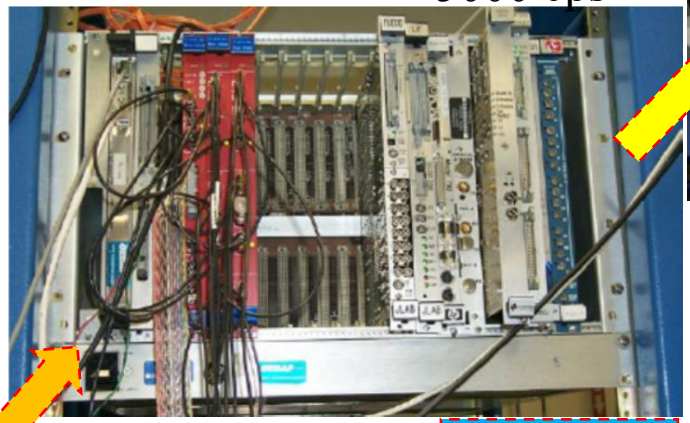
数据获取系统的演变

~ 800 cps



CAMAC

~ 5000 cps



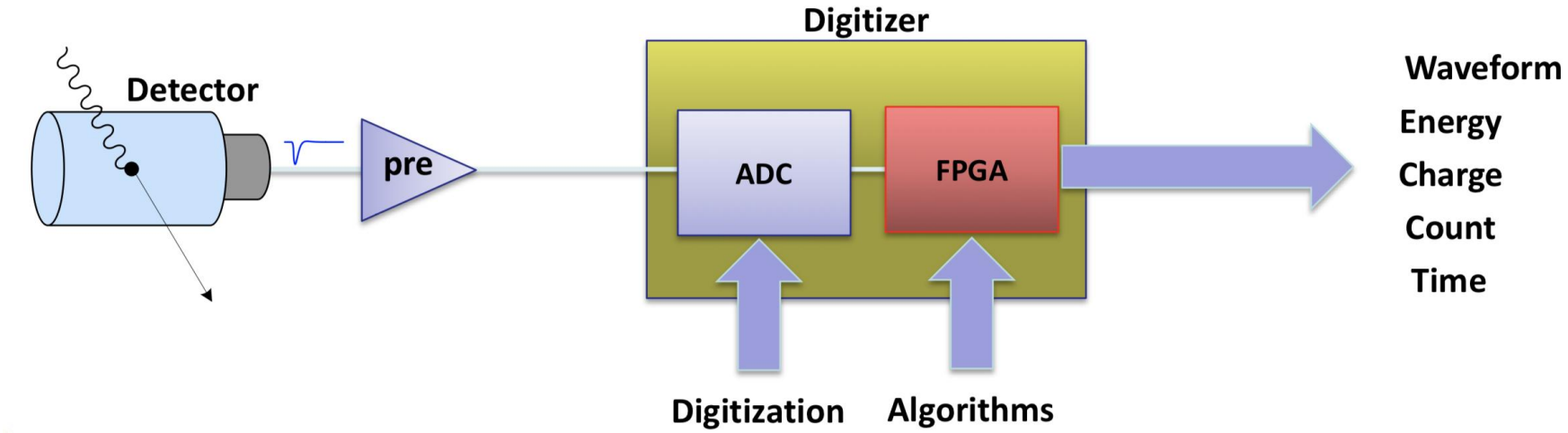
VME

>20000 cps

Digital

	CAMAC	VME	Digital
模数转换时间	> 100 us	~ 10 us	< 1 ns
计数率	< 1000/s	~ 5000/s	> 20000/s
数据传输	< 1MB/s	~ 20-25 MB/s	> 100 MB/s

数字信号处理



数字脉冲处理的目标是实现模拟模块的全数字化版本，例如整型放大器、甄别器、QDCs、峰值灵敏 ADCs、TDCs、计数器、符合单元等。

数字滤波：

- 性能优于模拟滤波
- 数字滤波是可编程的
- 数字滤波的特性是可预测的
- 一般来说，复杂的数字滤波器比模拟滤波器便宜

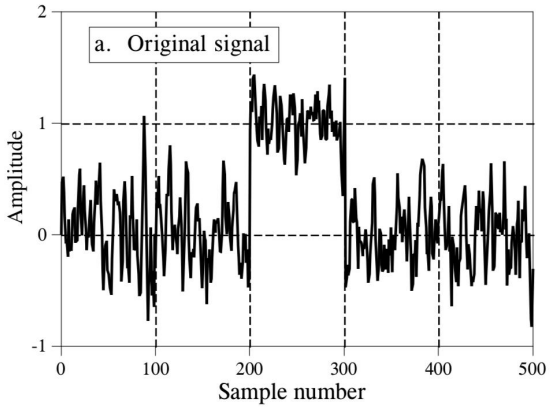
算法：

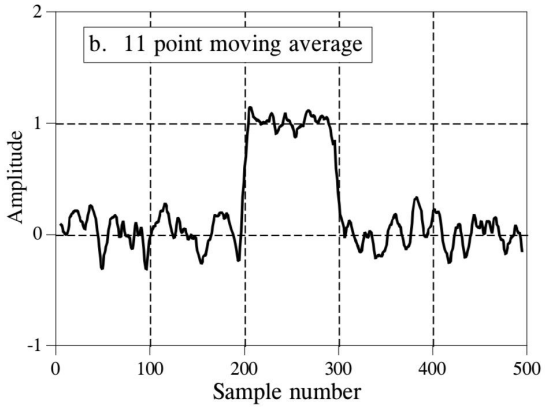
- Trigger filter,
- energy filter,
- time filter
- etc.

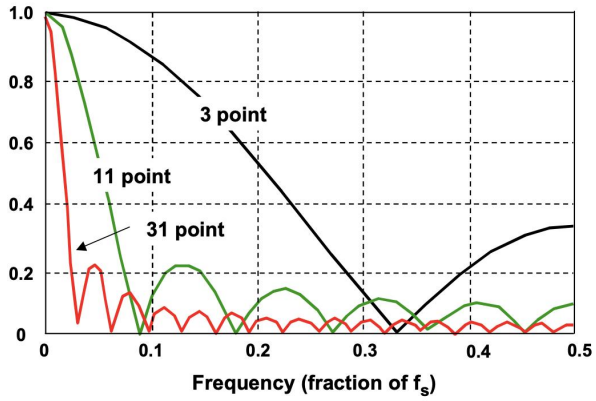
移动平均滤波（累加器）

移动平均通常用于平滑存在噪声的数据。它是信号处理最常见的滤波器之一。

长度为 N 的移动平均可写为：$$y[n] \equiv \frac{1}{N} \sum_{i=-N+1}^{0} x[n+i],$$







滤波器通常写成递归的形式，方便在 FPGA 中高效地实现。

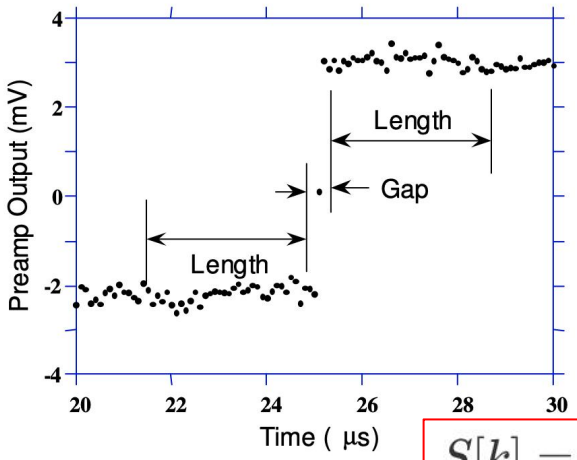
$$y[n] = x[n-N+1]/N + \ldots + x[n]/N$$

$$y[n+1] = x[n-N+2]/N + \ldots + x[n+1]/N,$$

$$y[n+1] = y[n] + (x[n+1] - x[n-N+1])/N.$$

每个 y[n] 的新值计算只需要两个加法运算，而不是直接定义所需要的 N 个加法。

梯形滤波--能量



$$S[k] = \sum_{i=k-L+1}^{k} x[i] - \sum_{i=k-2*L-G+1}^{k-L-G} x[i]$$

Moving average　　Moving average

递归形式，4个加法运算

$$S[k] = S[k-1] + x[k] - x[k-L] + x[k-2*L-G] - x[k-L-G]$$

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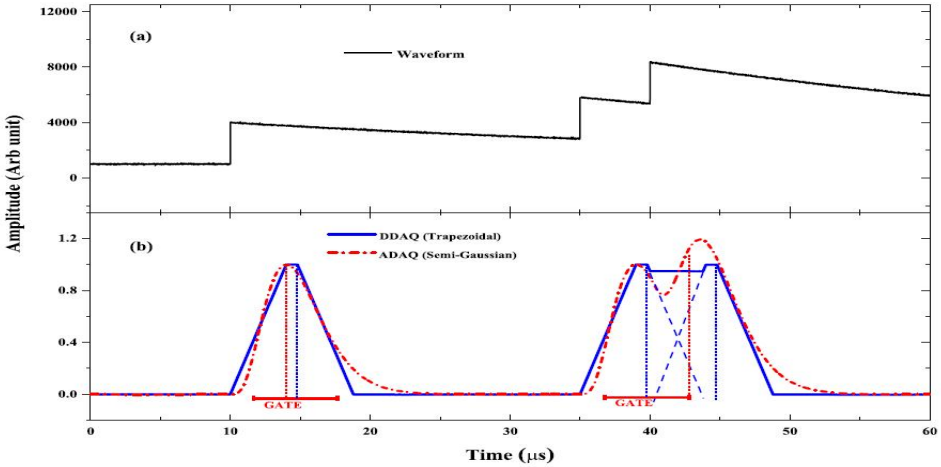

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- 数字整形器有更少的堆积，即使在相同的 FWHM 下。
- 数字系统的堆积时间是非常清楚的：由于脉冲固定，在固定的时间之后不再属于堆积。

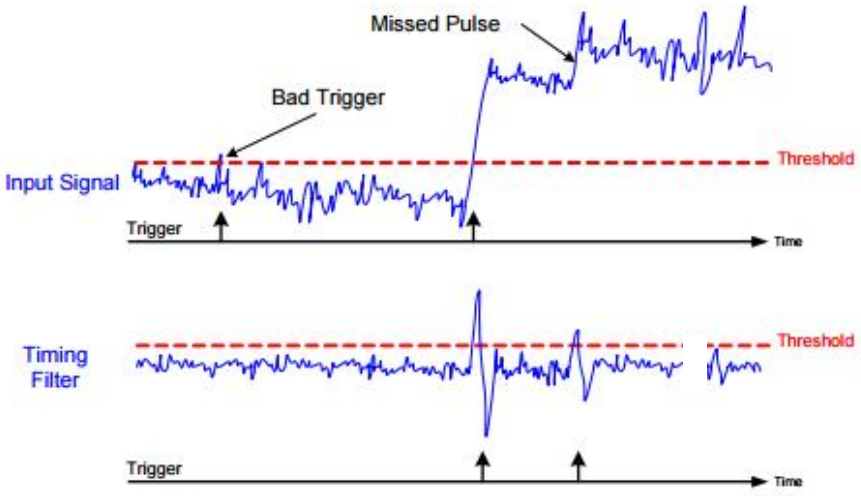
触发滤波

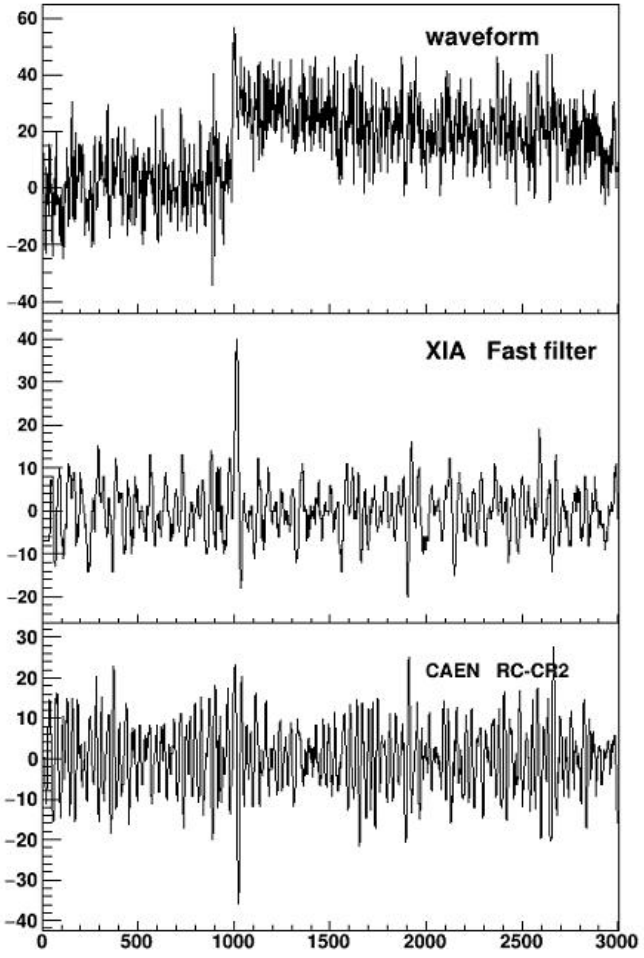
- 触发数据采集、分析
- 确定波形记录的时间窗
  - 触发前后的时间窗长度

示波器的自触发:

- 一旦输入信号幅度超过设定的阈值就产生触发
- 基线晃动或者堆积造成的假触发可能导致丢失重要事件

数字滤波器能够抑制噪声、消除基线。

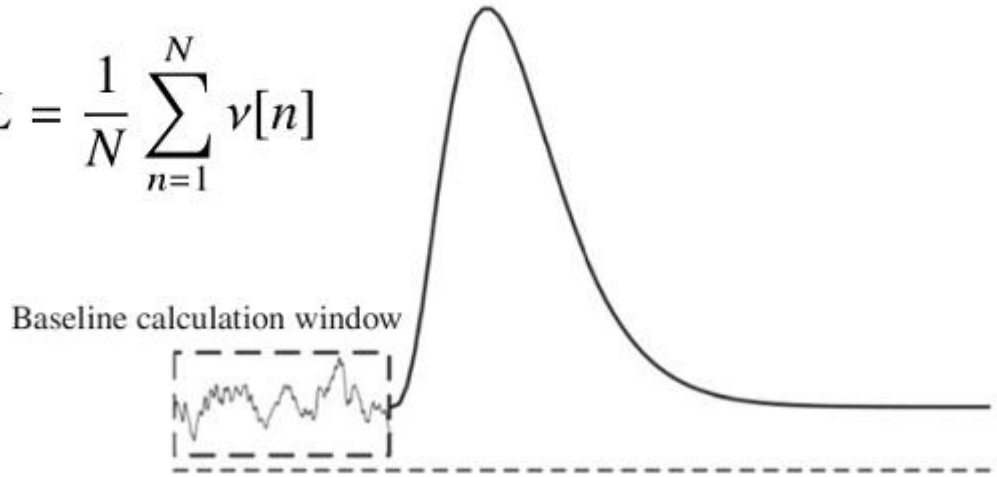


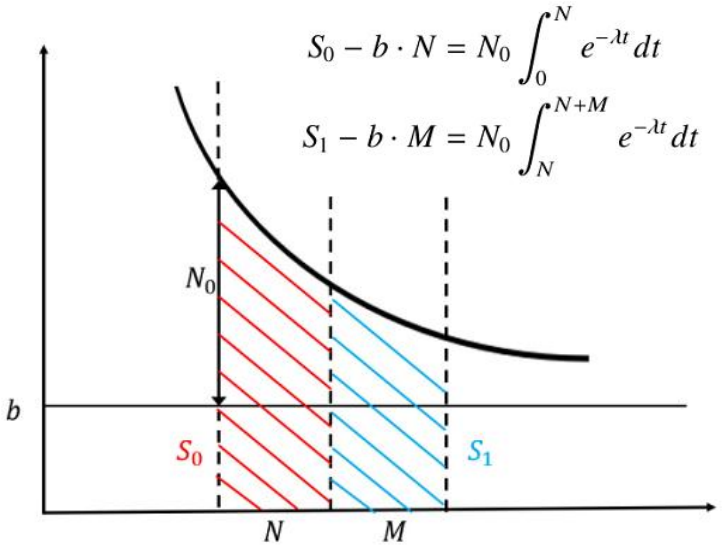


基线跟踪

基线的偏置通常可以通过计算脉冲之前的平均基线得到，通过对原始采样点扣除该平均值来进行基线修正。

$$BL = \frac{1}{N}\sum_{n=1}^{N} v[n]$$





$$b = \frac{S_0 - A \cdot S_1}{N - A \cdot M}$$

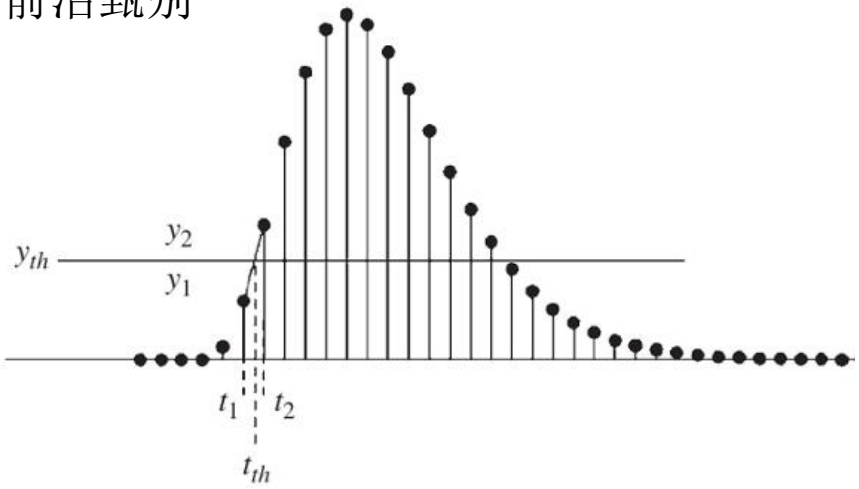
$$A = \frac{1 - e^{-\lambda N}}{e^{-\lambda N} - e^{-\lambda(N+M)}}$$

- 对于指数衰减的脉冲，几个半衰期之后可认为它衰减到基线。
- 只要距离前一个脉冲足够远，则可以认为回归到基线水平。
- 即只要当前脉冲距离前一个脉冲超过 几倍半衰期，那么在这个区间内的数据则可用于基线的评估。

测量脉冲连续两段区域的积分，即可得到当前的基线偏置

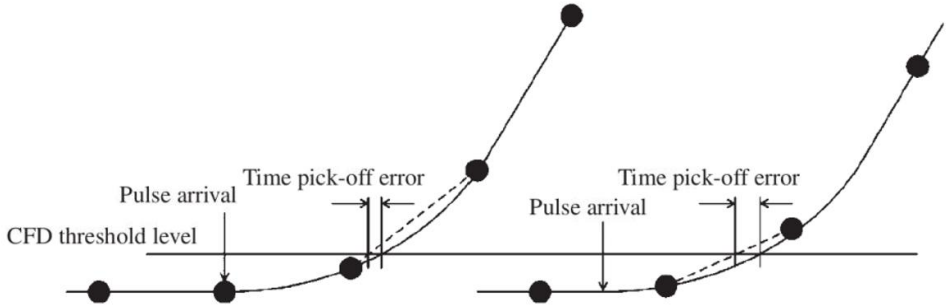
时间测量

前沿甄别

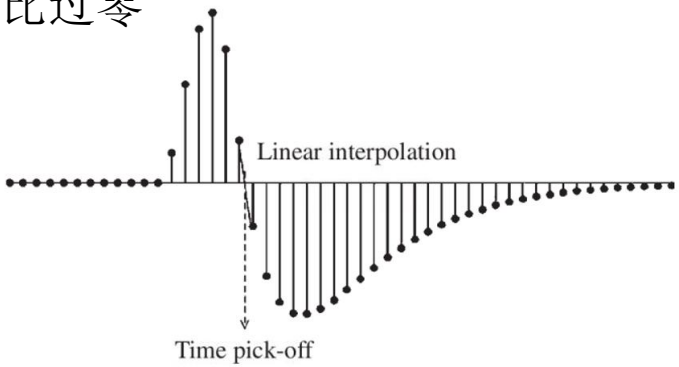


$$t_{th} = t_1 + (y_{th} - y_1)\frac{t_2 - t_1}{y_2 - y_1}$$

恒比定时

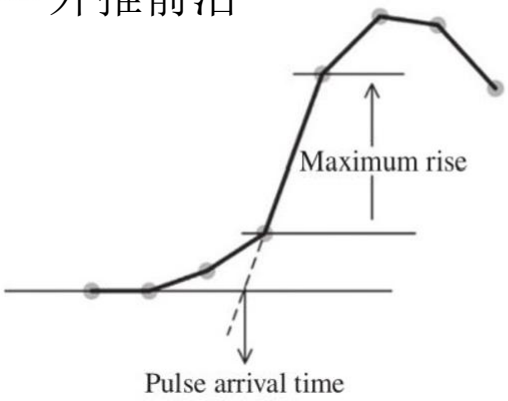


恒比过零

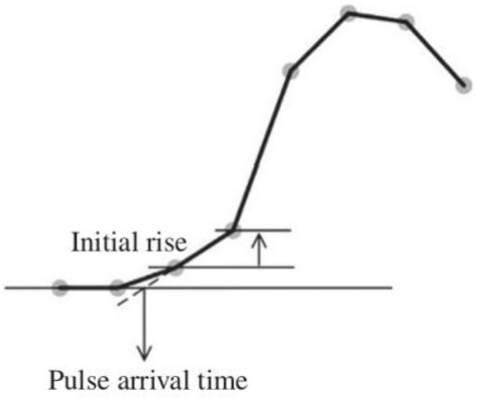


$$y[n] = x[n] - ax[n-k]$$

(a) 外推前沿

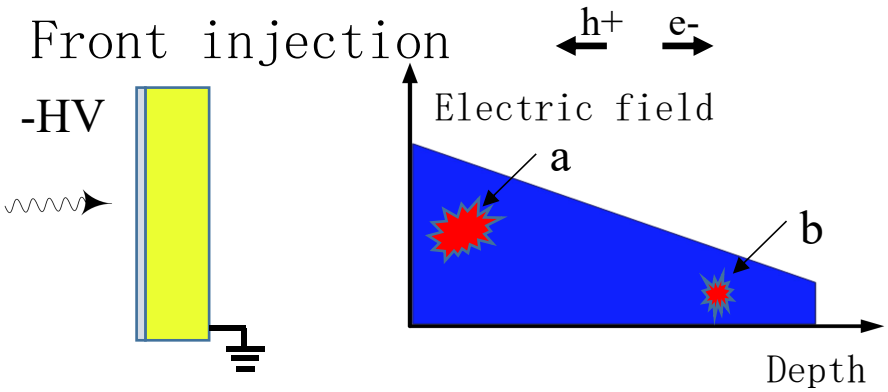


(b)

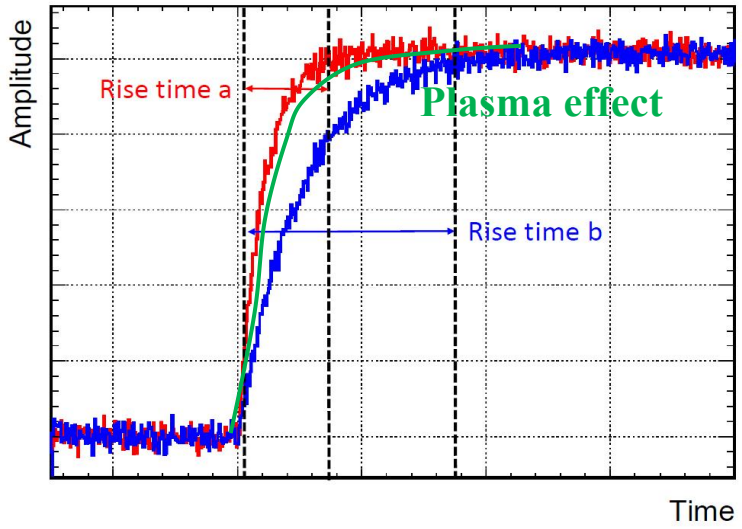


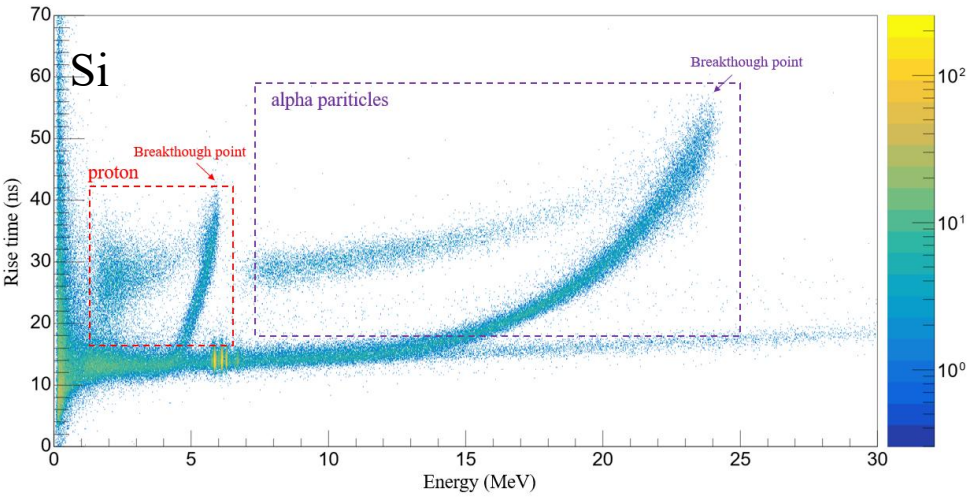
由于数字化系统的相位差问题，插值算法的时间性能受到极大的限制。

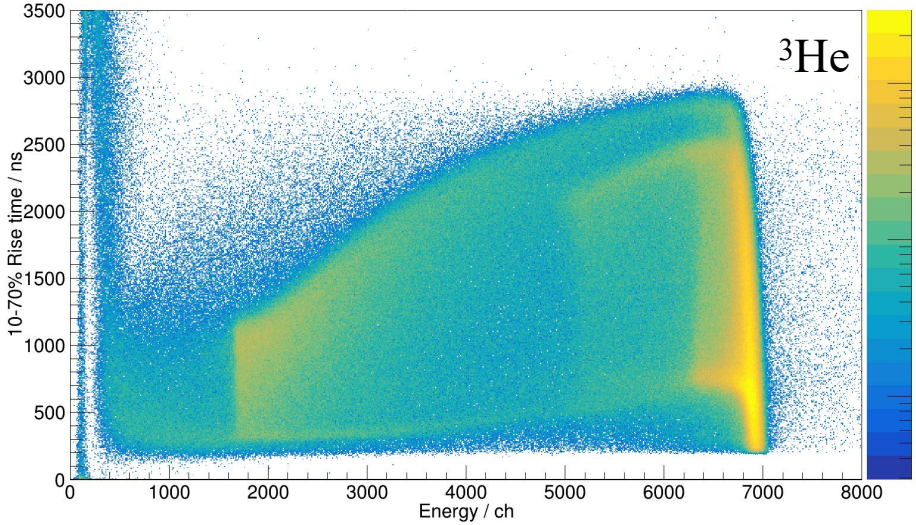
脉冲形状甄别—上升时间提取



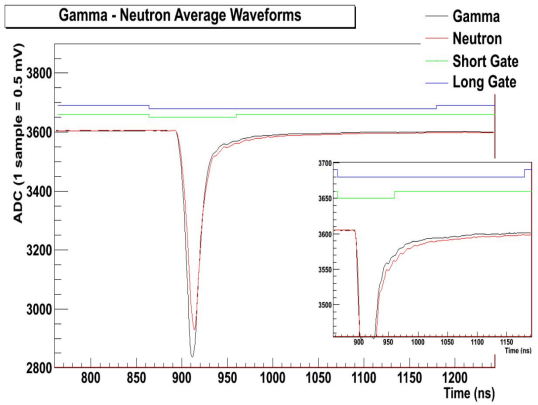
Leading edge: mainly by drift of holes

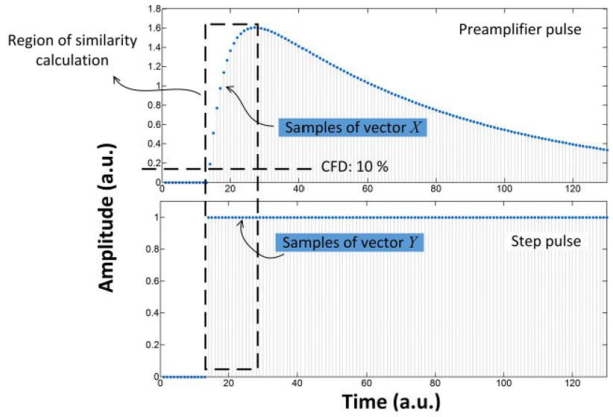




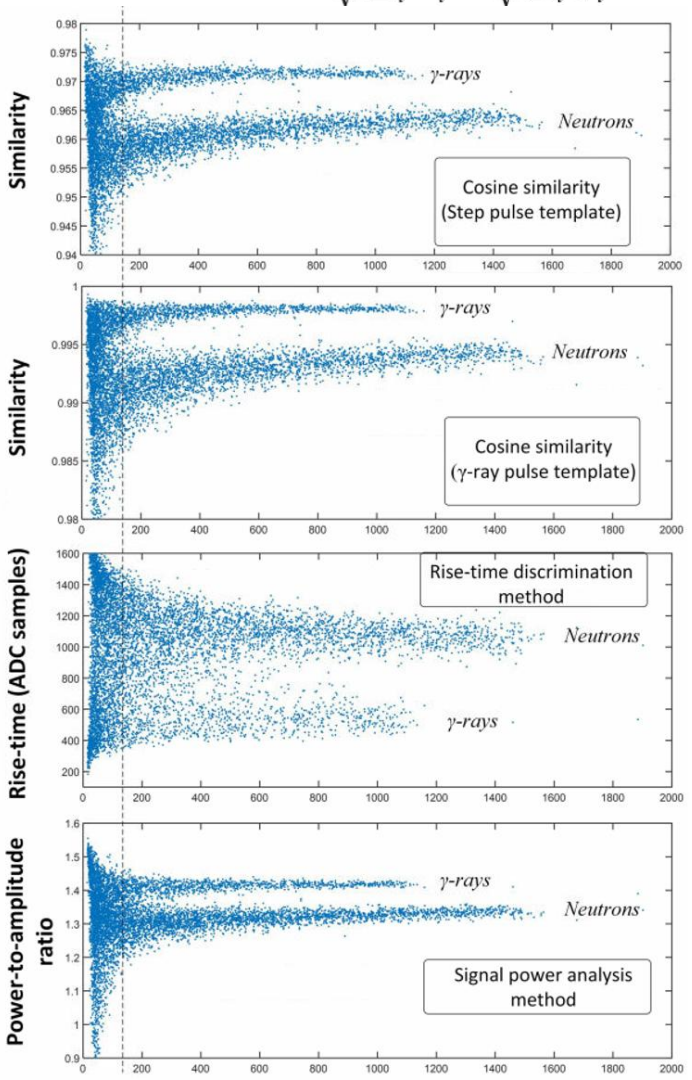


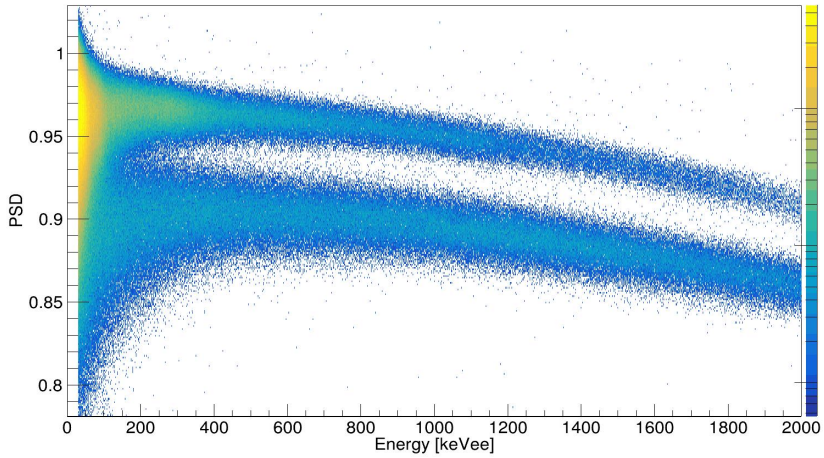
脉冲形状甄别 — 长短门积分、余弦相似度





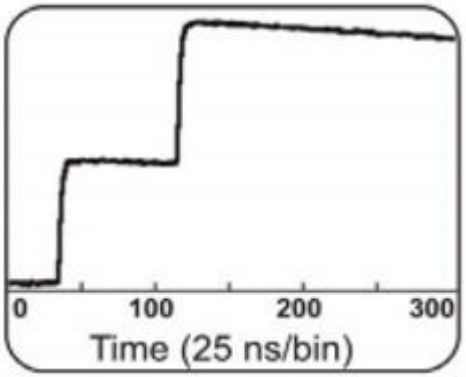
$$\cos\theta = \frac{x \cdot y}{|x||y|} = \frac{\sum_{i=1}^{p} x_i y_i}{\sqrt{\sum_i^p x_i^2} \times \sqrt{\sum_i^p y_i^2}}$$



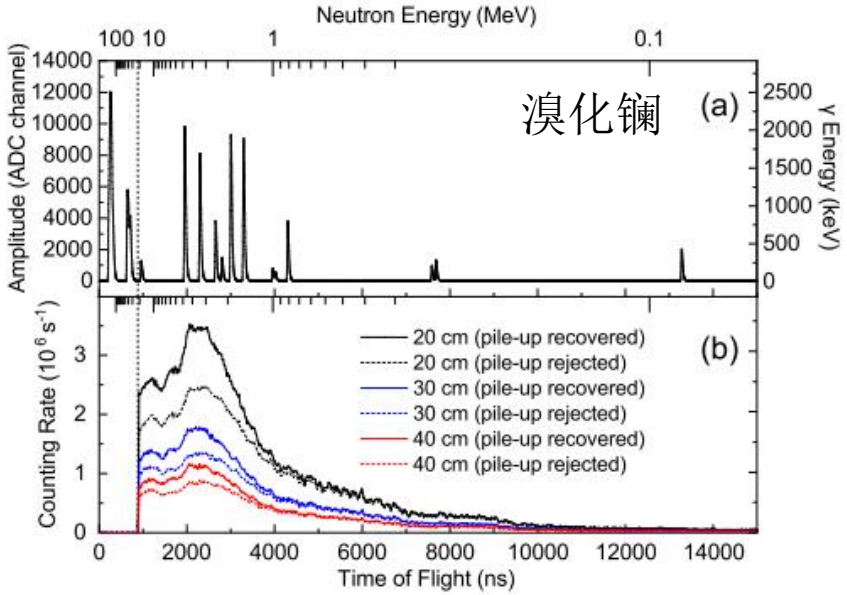


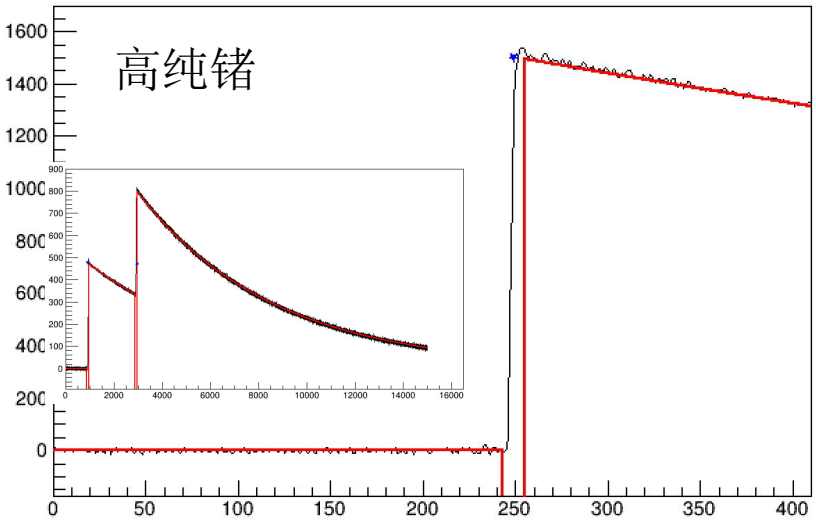
是否记录波形？

waveform : 500 Hz of 1 us long traces(12bit) at 100 MSPS,
Data stream： ~100 kB/second/channel = 360 MB/hour/channel！

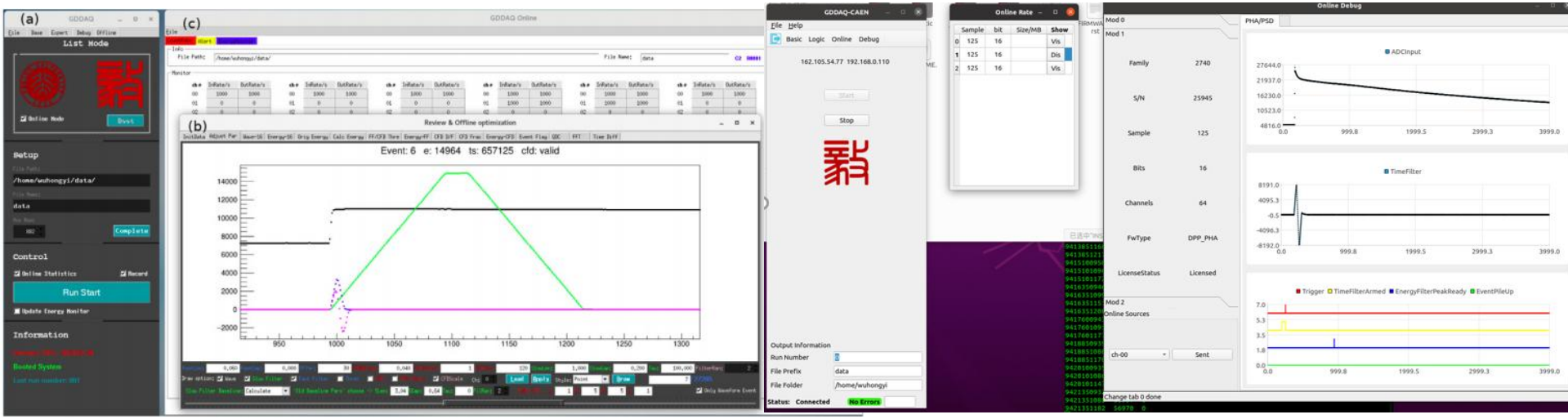


- 仅当必要时候才记录波形
  - 脉冲形状分析，堆积信号
- 记录特定时间段的波形
  - 脉冲前沿、高精度定时分析





软件进展



https://github.com/wuhongyi/PKUXIADAQ

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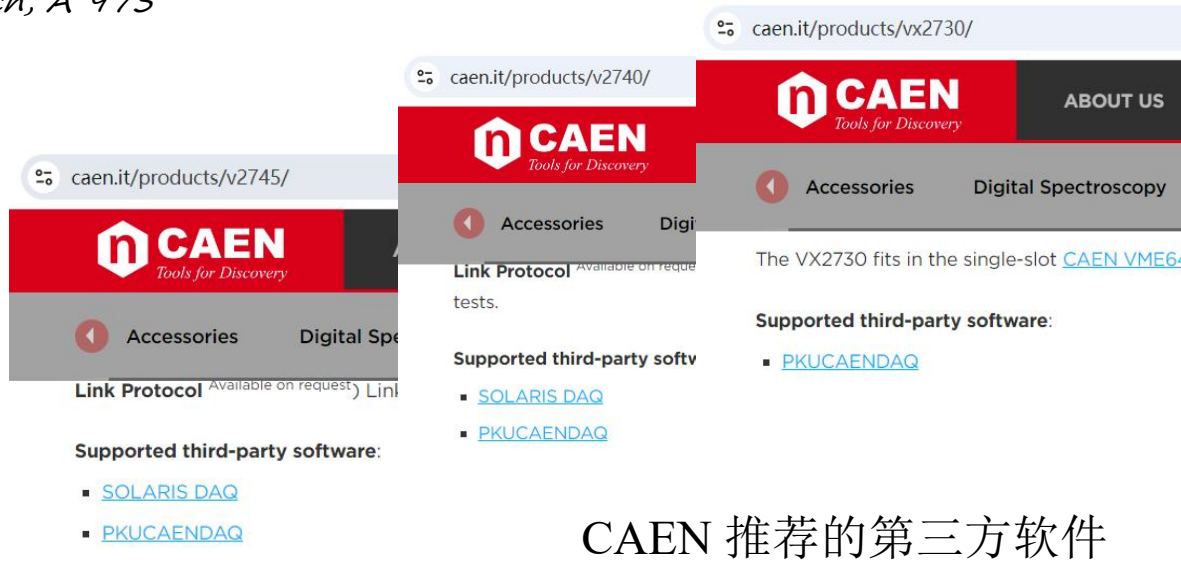
https://github.com/wuhongyi/PKUCAENDAQ

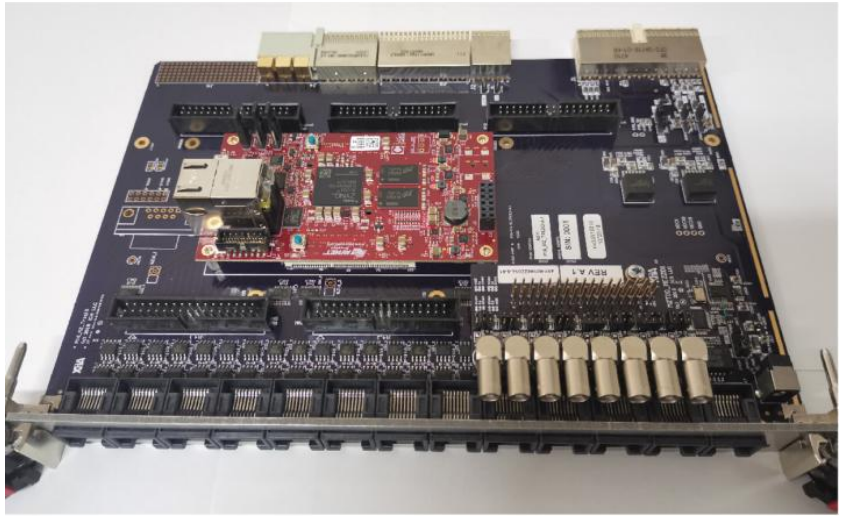
- 支持 XIA Pixie-16

- 支持 CAEN 27xx 系列
  - ✓ DPP-PHA
  - ✓ DPP-PSD
  - ✓ DPP-ZLE
  - ✓ DPP-DAW
  - ✓ SCOPE
  - ✓ OPEN-FDK



CAEN 推荐的第三方软件

硬件、固件进展



2018年，与 XIA 合作开发 MZTIO 可编程逻辑模块

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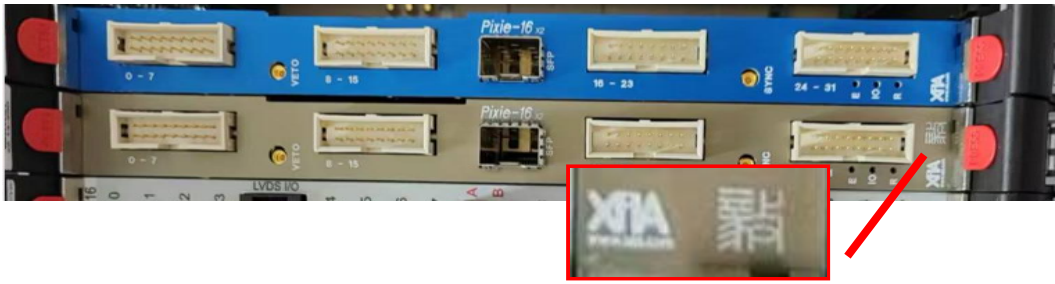
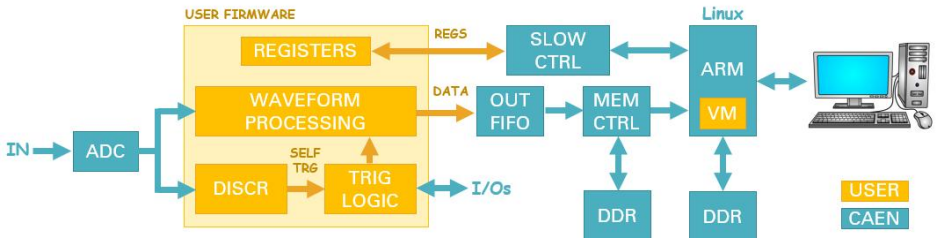


2019年，参与 XIA Pixie-16 新一代采集模块的开发

Sci-Compiler: graphical FPGA programming tool with precompiled modules (logic, filters, ...)
FDK: FW development kit with VHDL templates, simulation models, signal inspection, etc.



XIA LLC
MUTUAL NONDISCLOSURE AGREEMENT

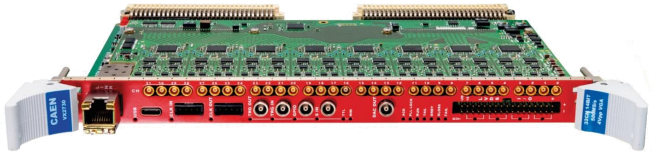
THIS MUTUAL NONDISCLOSURE AGREEMENT (hereinafter this "*NDA*") effective this _3rd___ day of ___June_____, 2021__ (hereinafter the "Effective Date"), by and between XIA LLC (hereinafter XIA), and the entity identified below (hereinafter the "Company"):

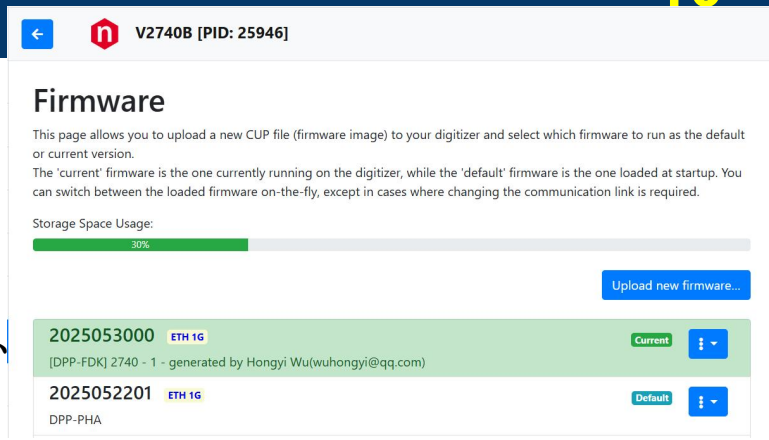
	- *XIA* -	- *Company* -
Company:	XIA LLC	Peking University
Address:	2744 East 11th St, Suite H2 Oakland, CA 94601 USA	No.5 Yiheyuan Road Haidian District, Beijing, China 100871
Telephone:	510-401-5760	
Facsimile:	510-401-5761	
Email:	support@xia.com	

2021年，基于 XIA 的硬件进行 FPGA 固件开发

2024 年，基于 CAEN 平台进行实验专用固件的开发。
获得 FDK 专家模式，开发固件在 GitHub 供大家使用。

开放 FPGA



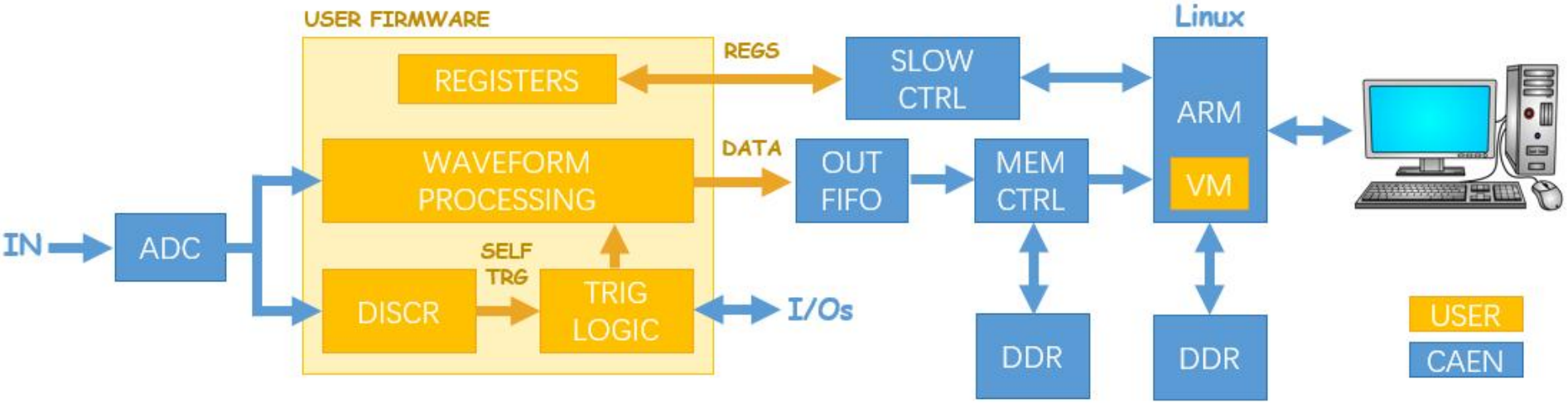


CAEN 提供基础设施：ADC 数据流、数据缓存和传输、

控制用户实现数据处理、参数提取和触发控制的算法

Sci-Compiler: 图形化 FPGA 编译工具（搭积木方式）

FDK: 固件开发工具包，带有 VHDL 模板，仿真模型，信号检测等等



最佳梯形整型？

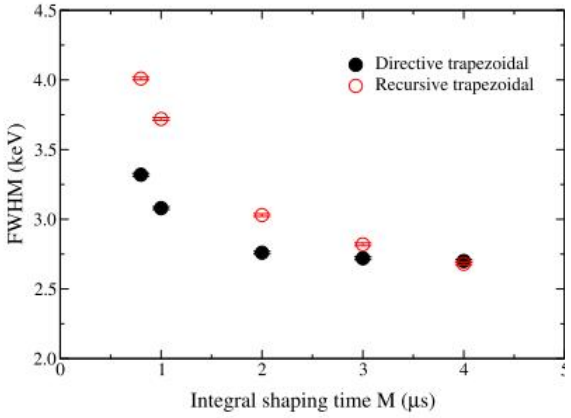
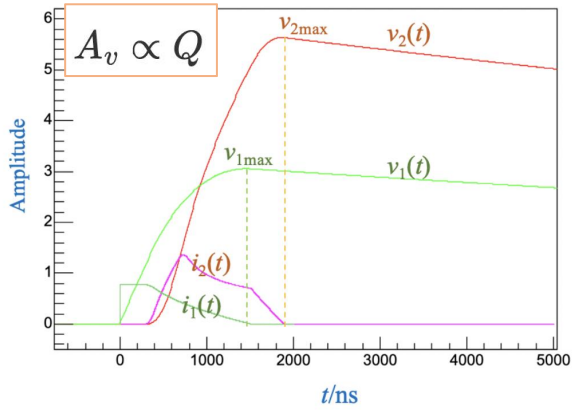


Fig. 3. The energy resolution for a 1332-keV γ ray determined by different trapezoidal algorithms for a counting rate at ~40 kHz, and different integral shaping times M.

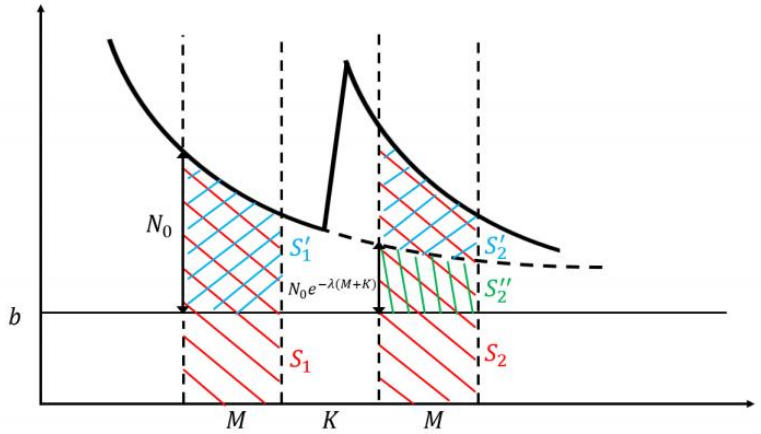


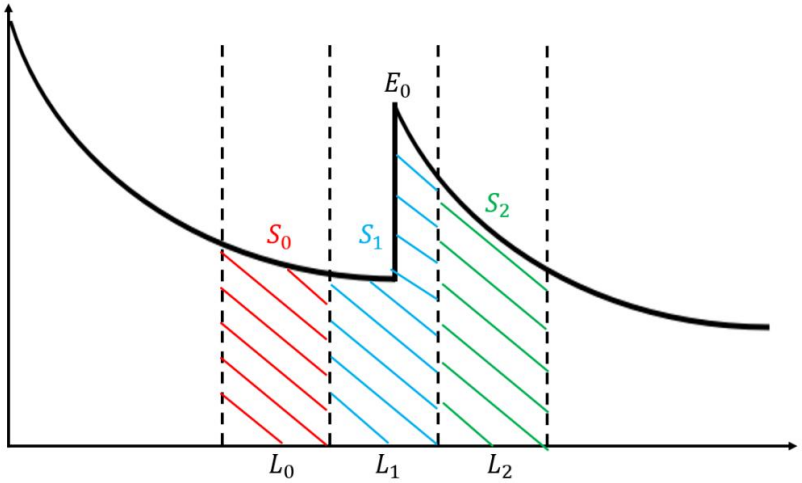
$$A_v = \sum_{n=0}^{\infty} v[n] = -\frac{1}{C_f}\sum_{n=0}^{\infty}(\sum_{k=0}^{\infty} e^{-k/\tau} i[n-k])$$

$$= -\frac{1}{C_f}\sum_{k=0}^{\infty} e^{-k/\tau}(\sum_{n=0}^{\infty} i[n-k])$$

$$= -\frac{1}{C_f}\frac{1}{1-e^{-1/\tau}}Q$$

脉冲面积与能量成正比。





$$E = S_2'/M = \frac{S_2 - S_1 e^{-\lambda(M+K)}}{M} - b(1 - e^{-\lambda(M+K)})$$

$$E_0 = (1-b_1)A_T = -\frac{(1-b_1)b_1^{L_0}}{1-b_1^{L_0}}S_0 + (1-b_1)S_g + \frac{1-b_1}{1-b_1^{L1}}S_1$$

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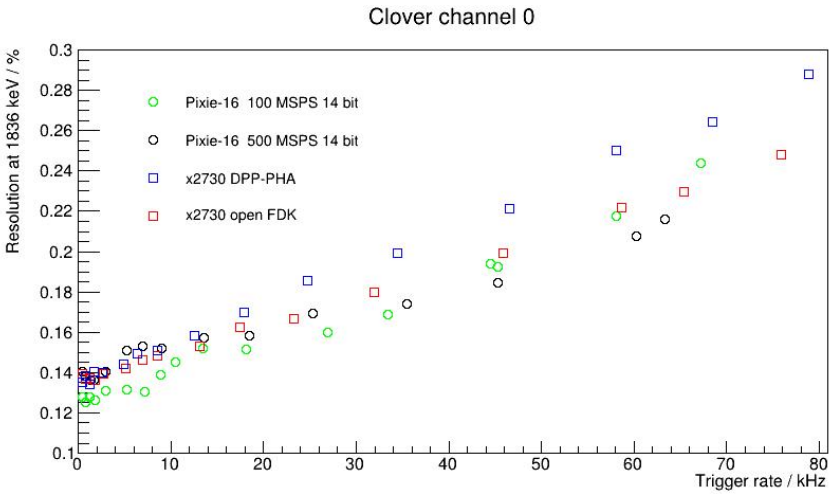
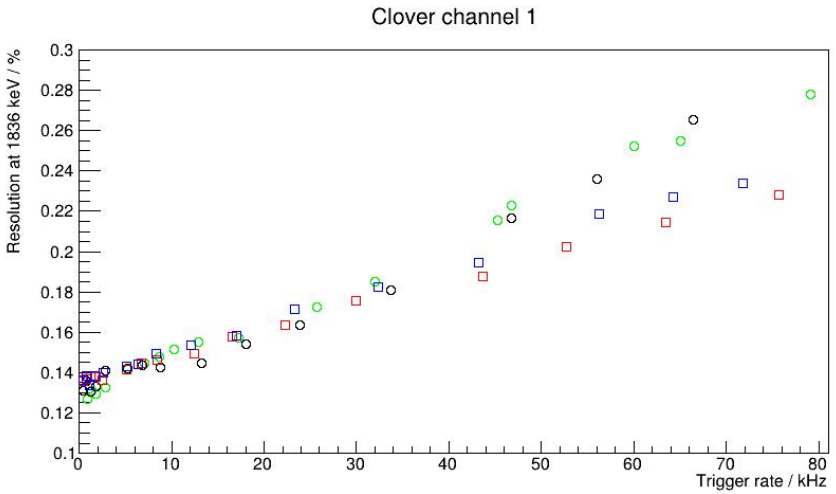
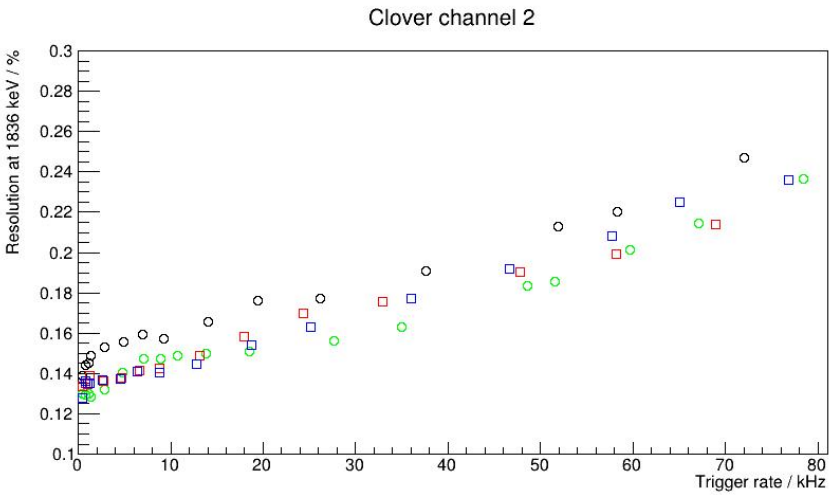
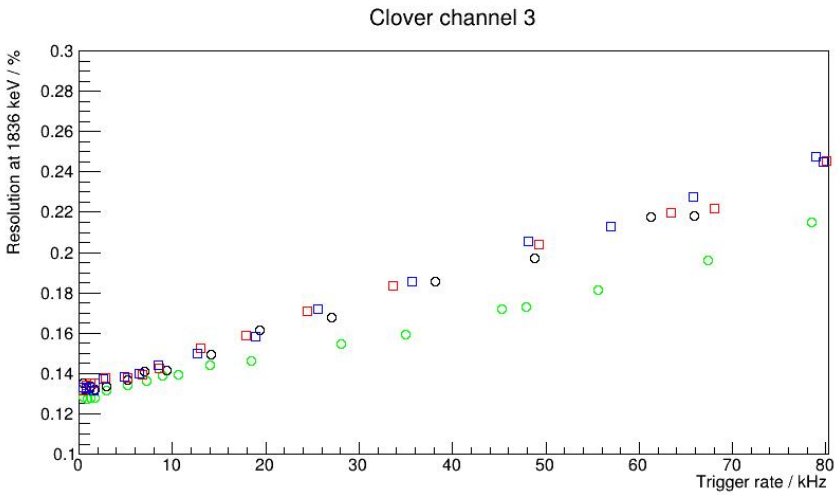
三段积分计算脉冲能量
规避浮点运算

高纯锗探测器测试结果

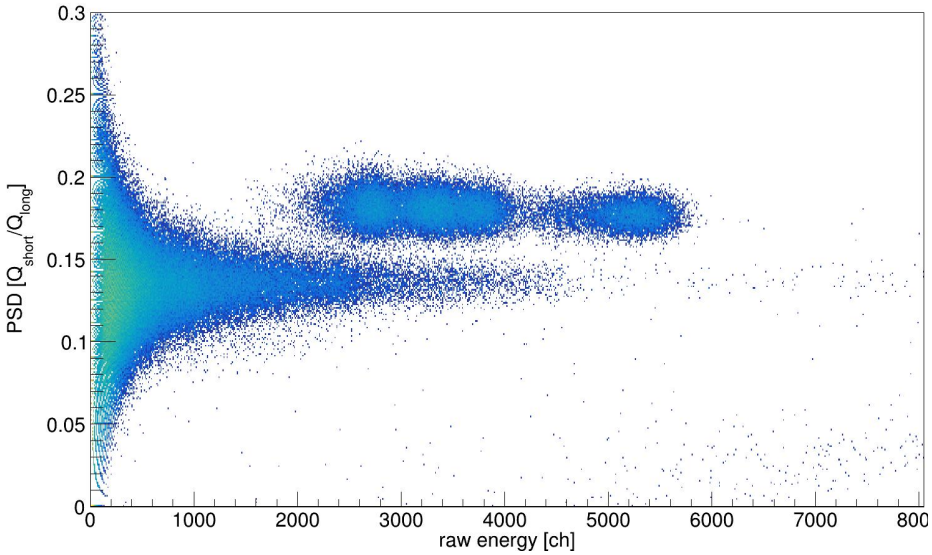

Clover channel 0
Resolution at 1836 keV / %
Trigger rate / kHz
Pixie-16 100 MSPS 14 bit
Pixie-16 500 MSPS 14 bit
x2730 DPP-PHA
x2730 open FDK

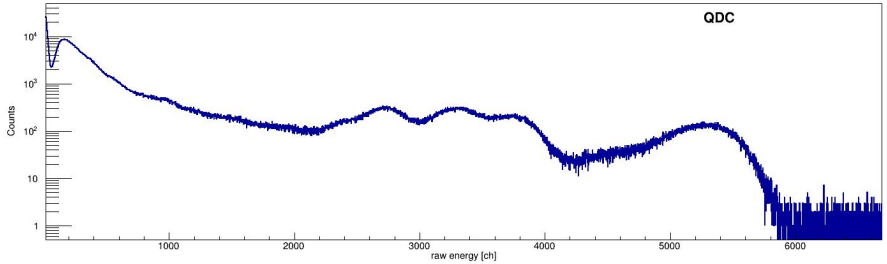

Clover channel 1
Resolution at 1836 keV / %
Trigger rate / kHz

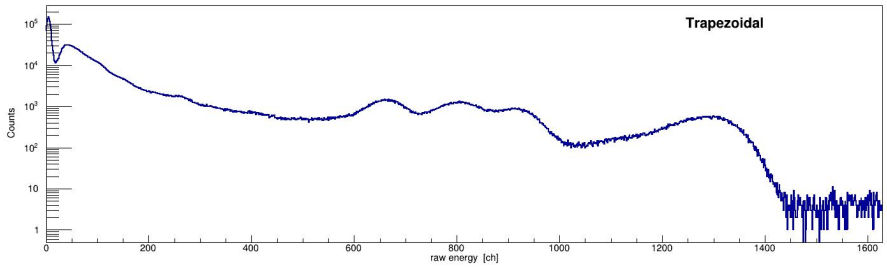

Clover channel 2
Resolution at 1836 keV / %
Trigger rate / kHz

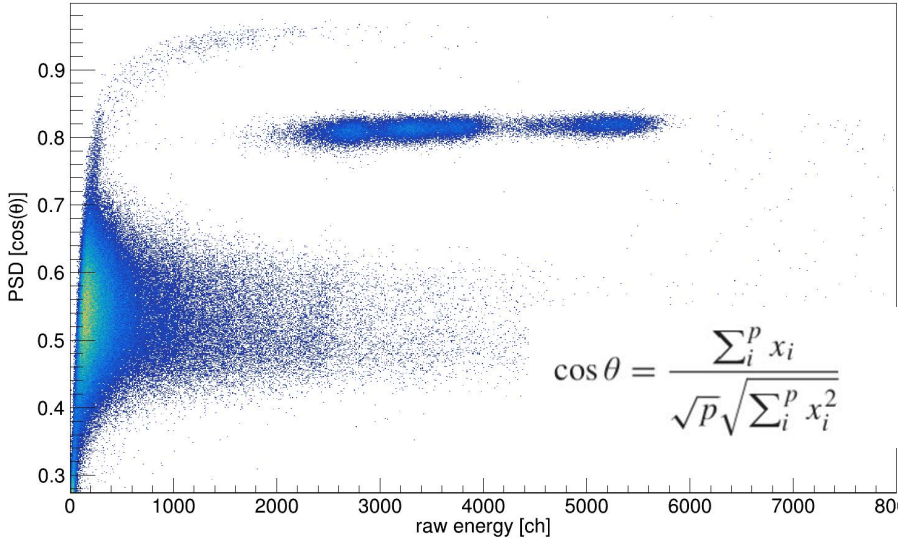

Clover channel 3
Resolution at 1836 keV / %
Trigger rate / kHz

氟化钡探测器测试结果

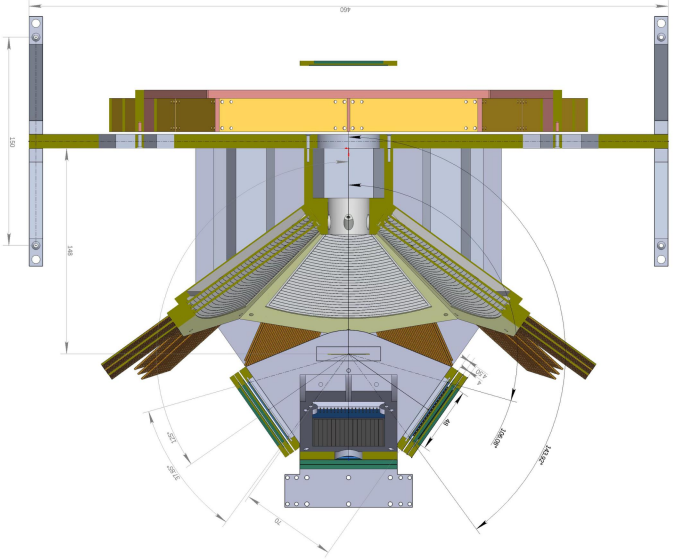

PSD [Q_short/Q_long]
raw energy [ch]

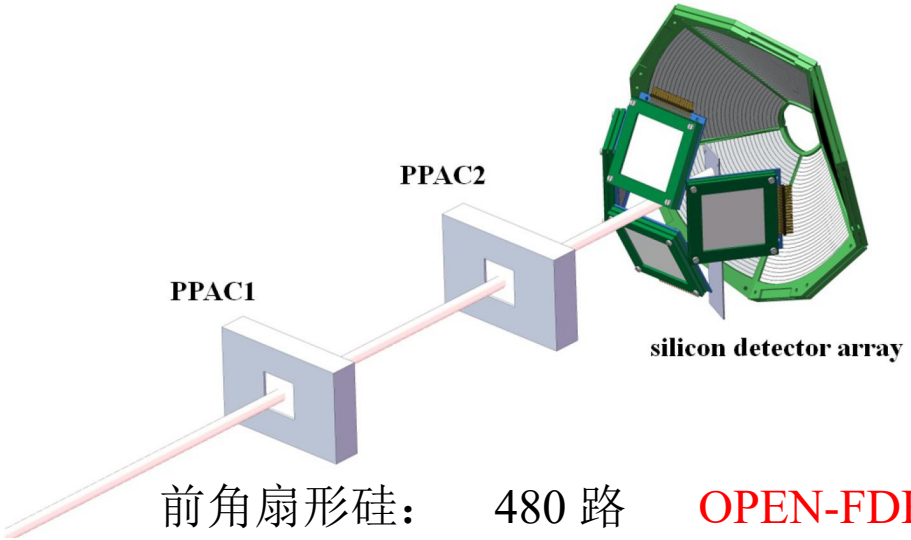

QDC
Counts
raw energy [ch]


Trapezoidal
Counts
raw energy [ch]

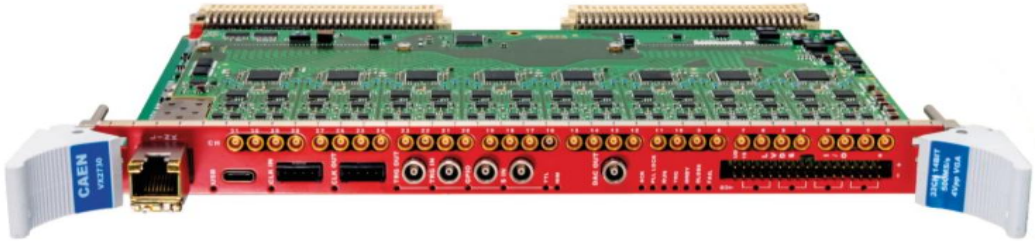

PSD [cos(θ)]
raw energy [ch]
$\cos\theta = \frac{\sum_i^p x_i}{\sqrt{p}\sqrt{\sum_i^p x_i^2}}$

Reaction mechanisms of $^{10}C+^{120}Sn$ system at energies around the Coulomb barrier





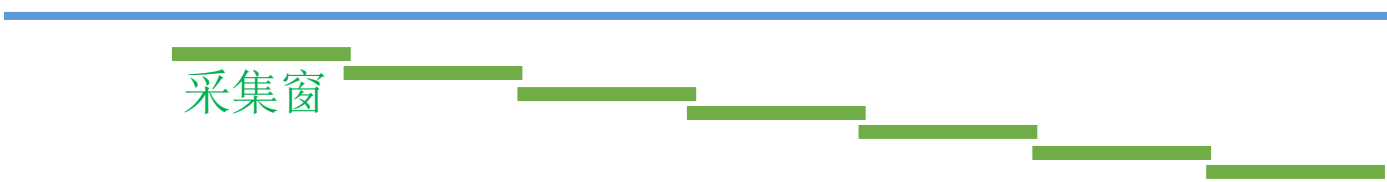
前角扇形硅： 480 路 OPEN-FDK
背角和零度硅：148 路 OPEN-FDK
PPAC： 10 路 DPP-PSD

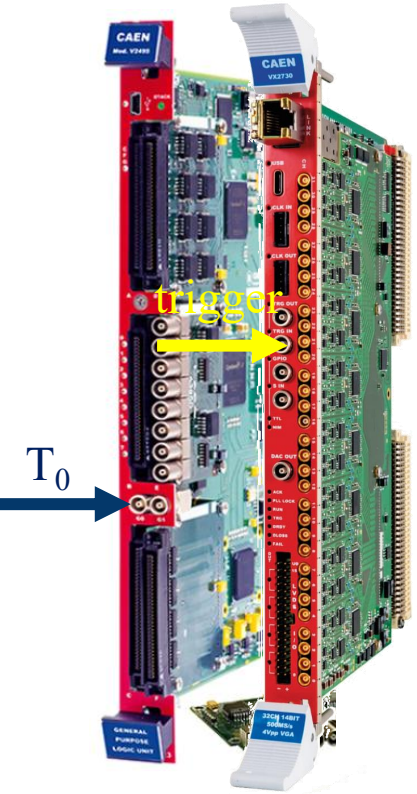


VX2730 500MSPS 14BIT

V2740/V2745 125MSPS 16BIT

超长波形采集



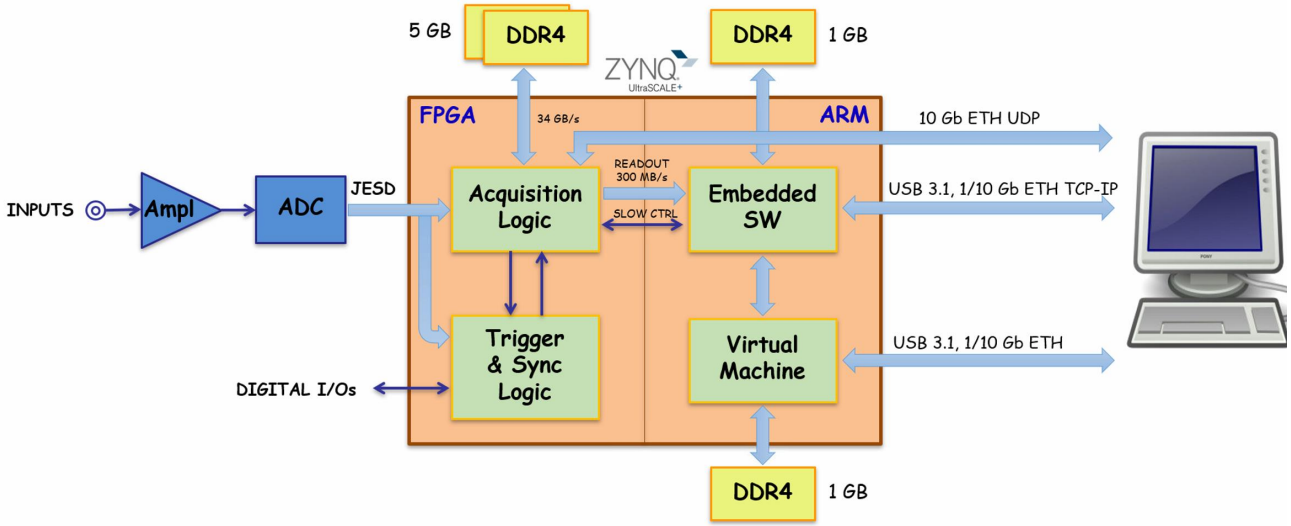


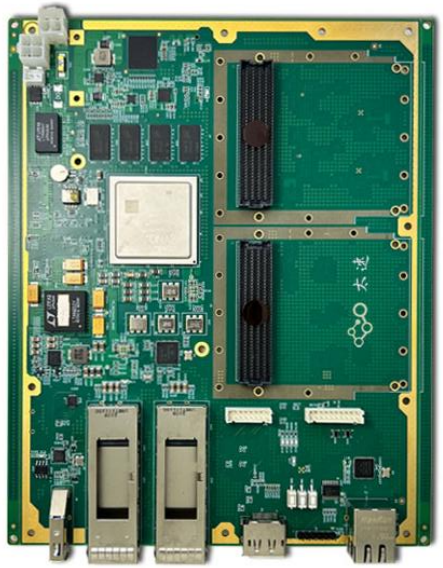
- SCOPE 模式
- 硬件大缓存

以 VX 2730 连续采集 2 s 波形为例：
每个脉冲记录 10 ms，当接收到 T_0 信号之后，间隔 10 ms 连续发送 200 个 trigger。

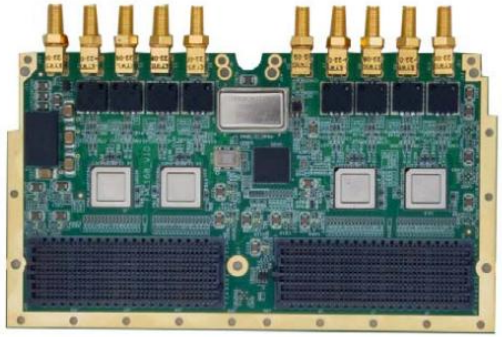
测试表明，VX2730 当仅启动一通道时，在千兆网传输模式下，最长可连续记录 5.7 s。

下一步计划--硬件国产化





125M – 64 ch　34 pin 接口　大规模硅阵列、CsI 阵列、TPC
125M – 32 ch　MCX 接口　HPGe 高精度测量　可调增益
500M – 32 ch
1G　- 16 ch



预留更高采样率
10G　1-2 ch
5G　2-4 ch
3G　4-8 ch

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Tools for Discovery