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碲锌镉探测器低噪声前端读出芯片及数据采集系统设计

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摘要：本文设计了用于碲锌镉探测器的低噪声前端读出芯片。每个芯片包含 16 个并行通道，每个通道由两级放大的电荷灵敏前放、4 阶半高斯成形电路、漏电流补偿电路、甄别器和输出驱动放大器组成。芯片采用了 Chartered 0.35μm 工艺完成了流片，初步测试结果表明芯片工作正常。整个通道的增益范围为 100~400mV/fC，达峰时间调节范围为 1~4μs。在最大增益、1.33μs 达峰时间时测得的零电容噪声为 70e，噪声斜率为 20e/pF。本文还介绍了美国 BNL 设计的一款峰检测及去随机化专用集成芯片以及基于该芯片的 USB 数据采集板，采用该数据采集板可以连接 2 个前端 ASIC 芯片构成 32 通道的碲锌镉探测器数据采集系统。

关键词：碲锌镉；室温半导体探测器；低噪声；专用集成电路；数据采集；

Design of Low Noise Front-end ASIC and DAQ System for CdZnTe Detector

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Abstract：A low noise front-end ASIC has been designed for CdZnTe detector. This chip contains 16 channels and each channel consists of a dual-stage charge sensitive preamplifier、4th order semi-Gaussian shaper、leakage current compensation circuit、discriminator and output buffer. This chip has been fabricated in Chartered 0.35μm CMOS process, the preliminary results show that it works well. The total channel charge gain can be adjusted from 100mV/fC to 400mV/fC and the peaking time can be adjusted from 1μs to 4μs. The minimum ENC at zero input capacitance measured at maximum charge gain and 1.33μs peaking time is 70e with noise slope of 20e/pF. The peak detector and derandomizer (PDD) ASIC developed by BNL and an associated USB DAQ board are also introduced in this paper. Two front-end ASICs can be connected to the PDD ASIC on the USB DAQ board and compose a 32 channels DAQ system for CdZnTe detector.

Key words：CdZnTe; room temperature semiconductor detector; low noise; ASIC; DAQ

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