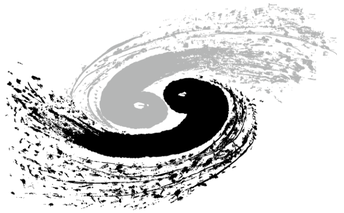
中国科学院大学
University of Chinese Academy of Sciences

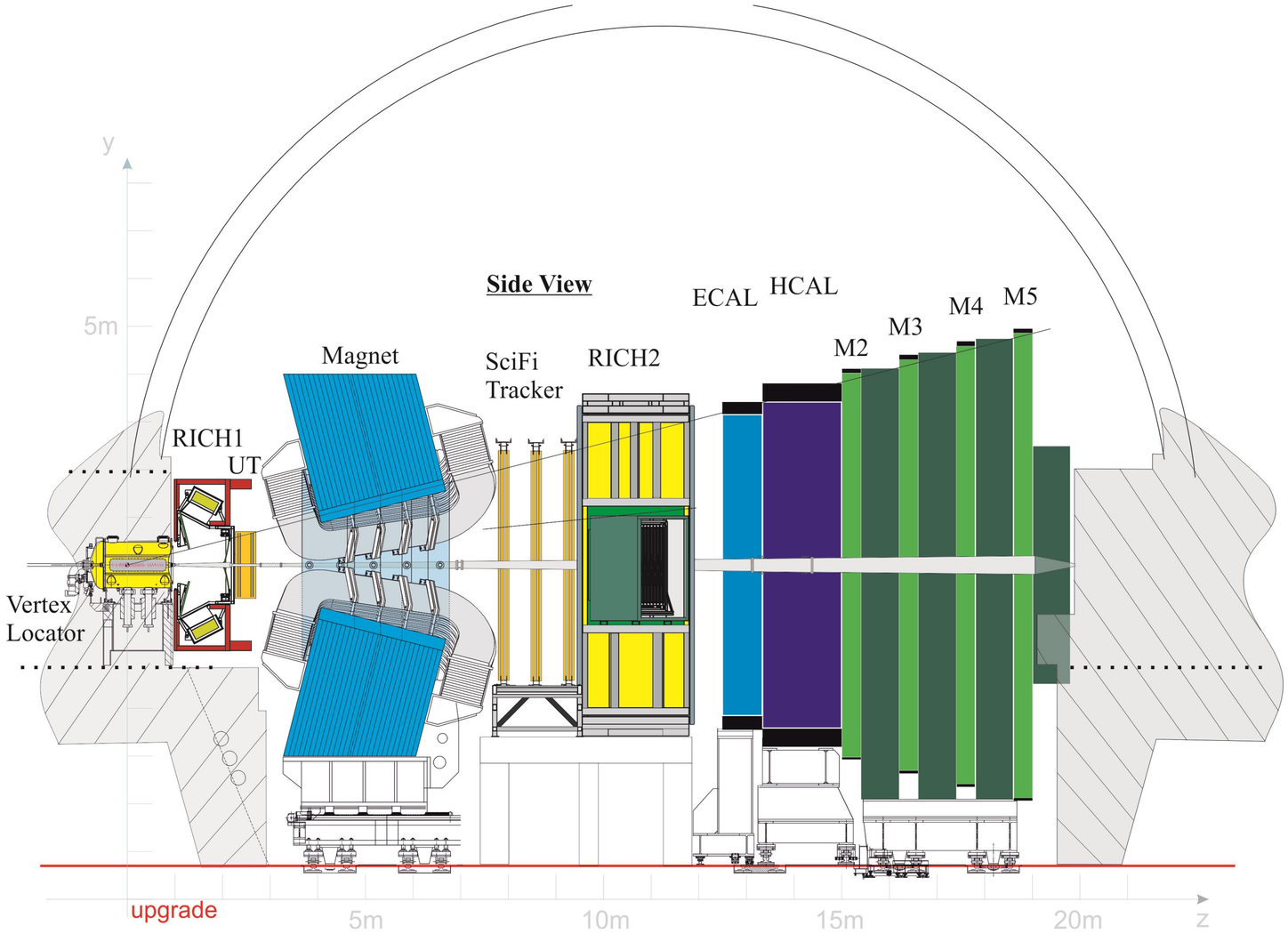


LHCb Real Time Analysis

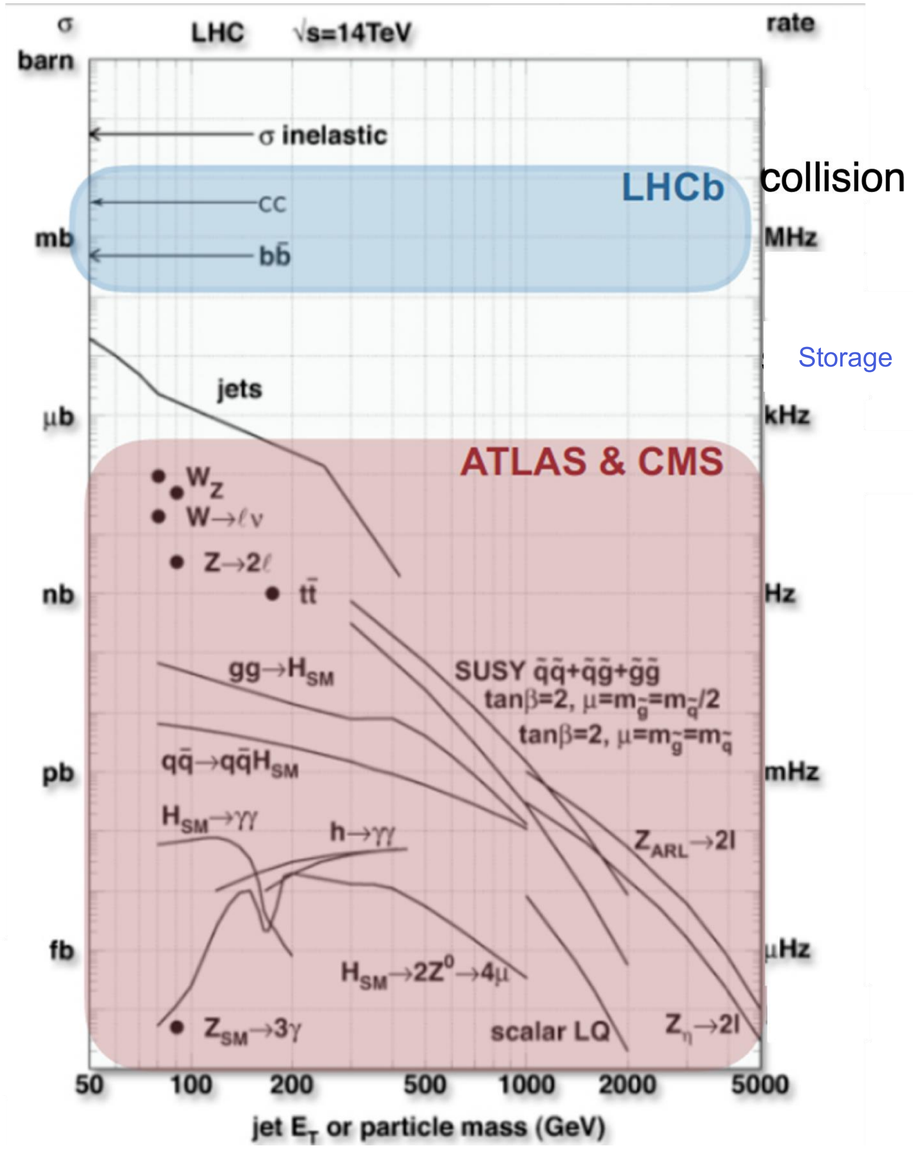
Shanzhen Chen, on behalf of Peilian Li

The LHCb Upgrade I detector

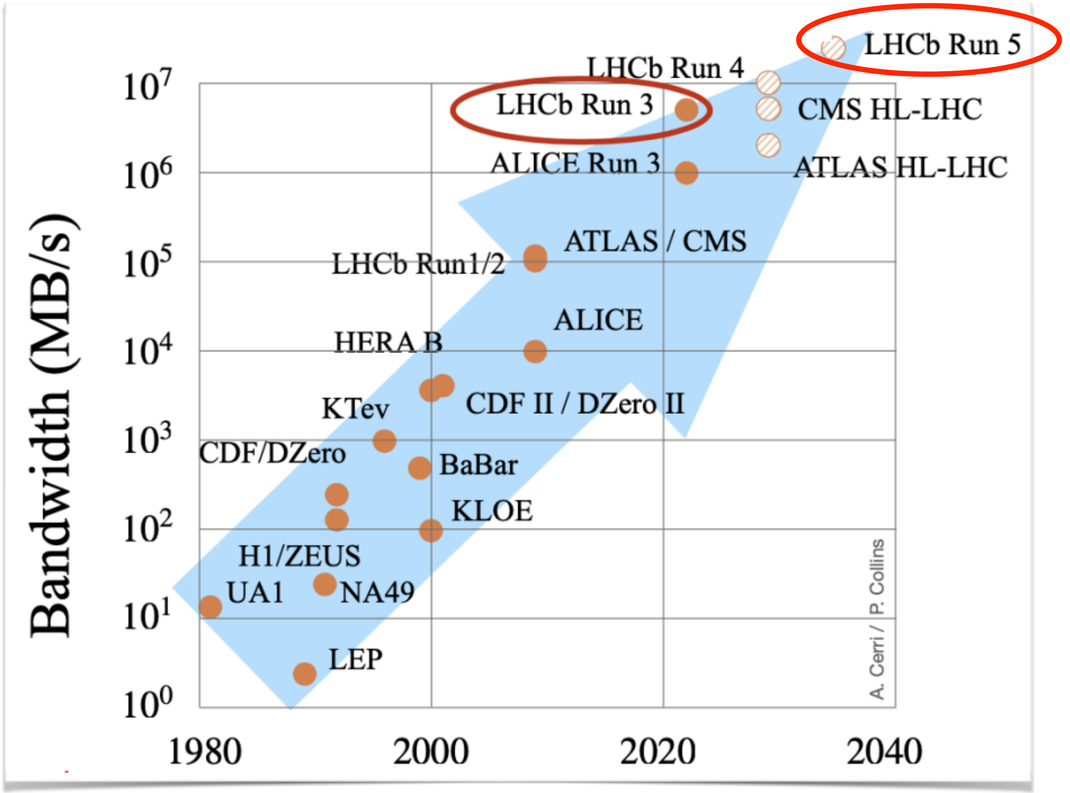
- Dedicated for flavor physics studies, but also serve as a forward general-purpose detector
- Increased instantaneous luminosity 5× from Run 2 to $2\times10^{33}cm^{-2}s^{-1}$
- New tracking detectors
- Improved readout electronics to meet rate requirements
- No hardware trigger



LHCb: a heavy flavour factory



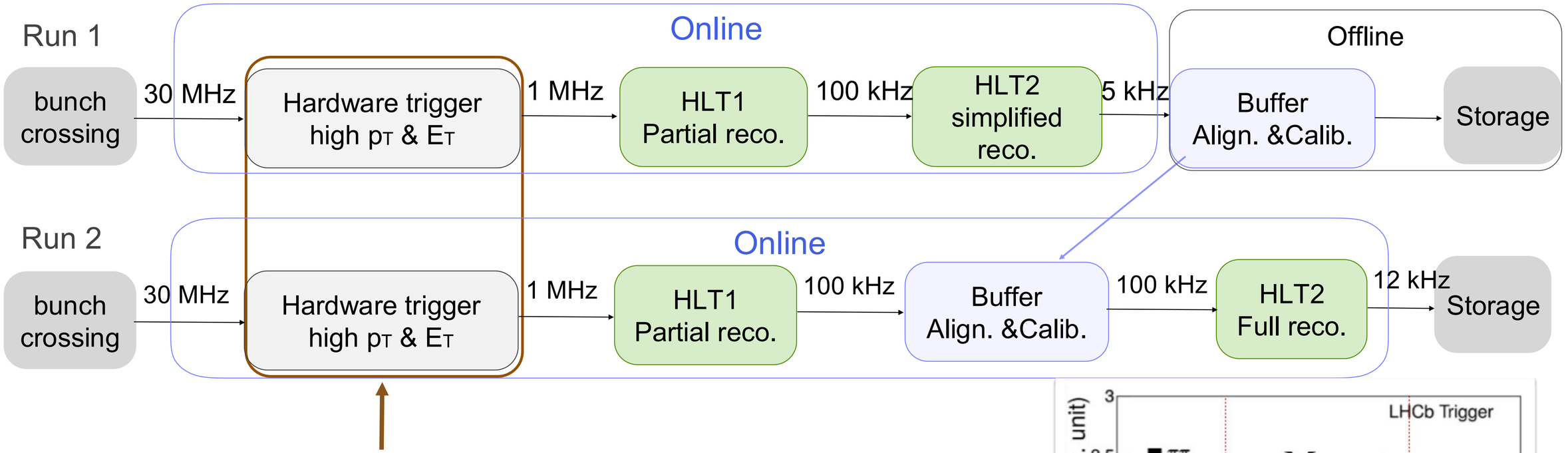
Pioneering in novel trigger strategies!



Signal rate at MHz level

Highest data processing rate of any HEP experiment!

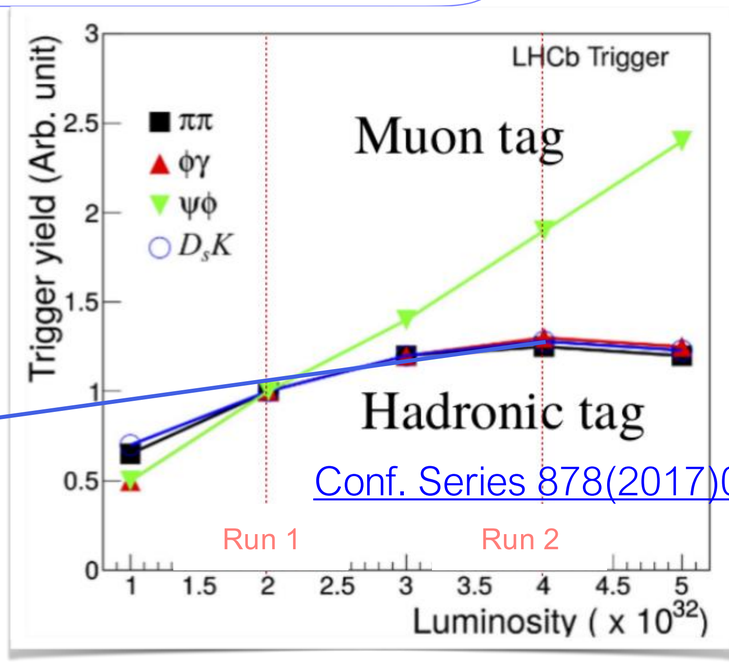
A bit of trigger history



Hardware trigger: 30→1 MHz read-out limits

→ based on muon detector and calorimeters

- Hardware trigger is not an option for Run 3, as rate limit of 1 MHz saturates fully hadronic modes



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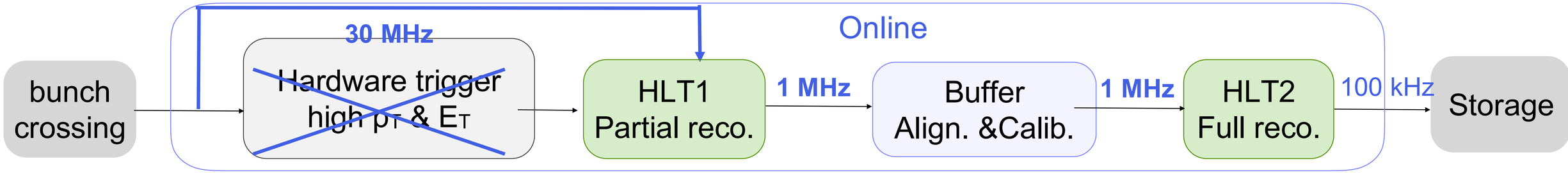
LHCb Run 3 Trigger



Online - Real Time Analysis

Run 1 & 2 trigger:
background rejection

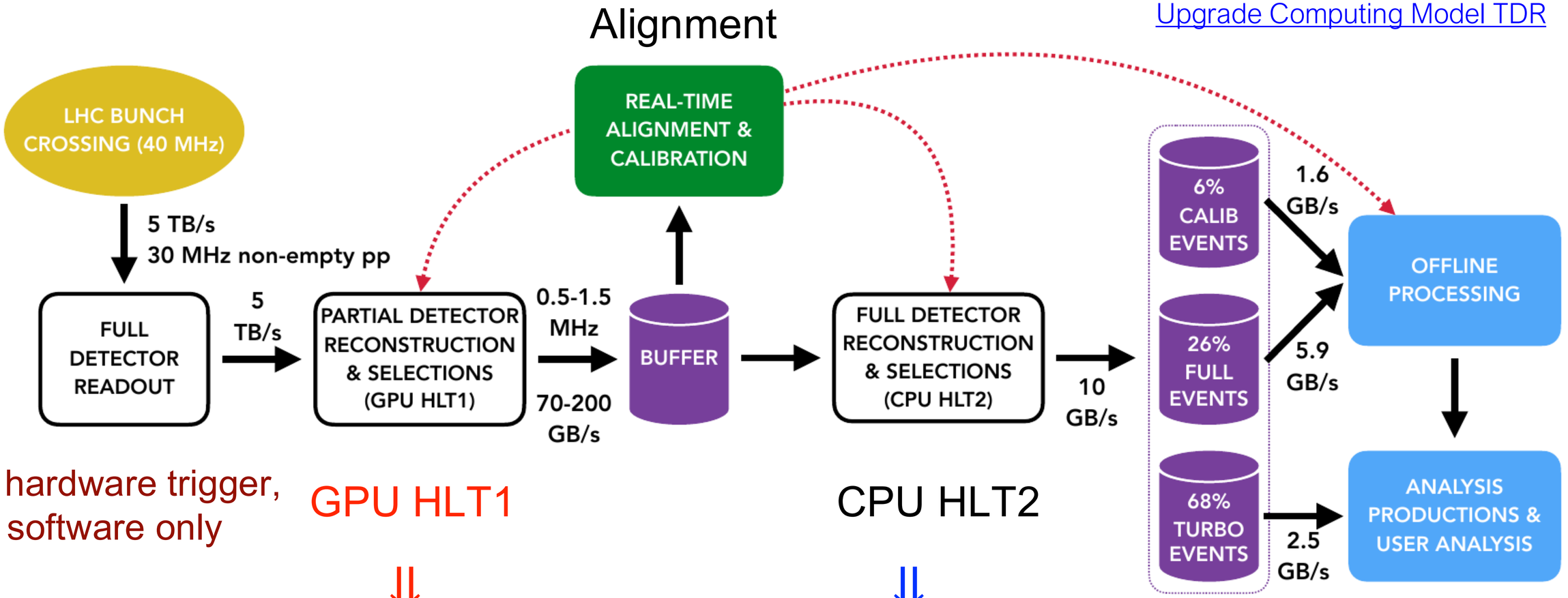
Upgrade trigger:
background rejection & signals classification

LHCb Run 3 Data Flow

All numbers related to the dataflow are taken from the LHCb

[Upgrade Trigger and Online TDR]

[Upgrade Computing Model TDR]



No hardware trigger, software only

GPU HLT1

⇓

First complete **high-throughput GPU Trigger** for a HEP experiment!

CPU HLT2

⇓

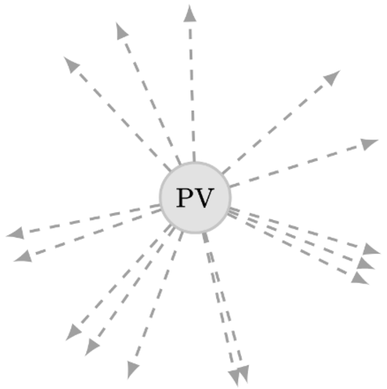
Offline-quality full reconstruction with exclusive selections

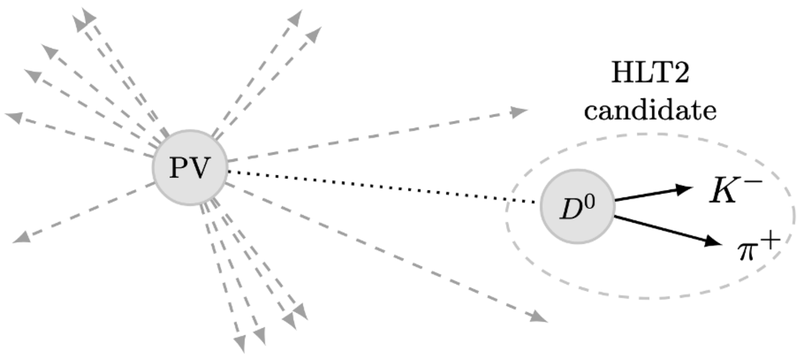
↘

Selective persistence

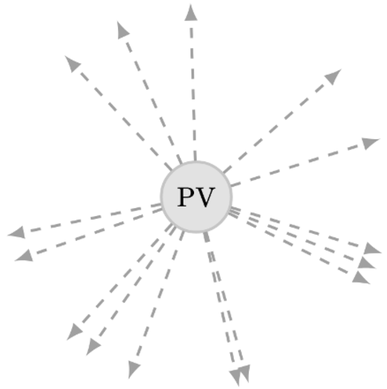
Types of data

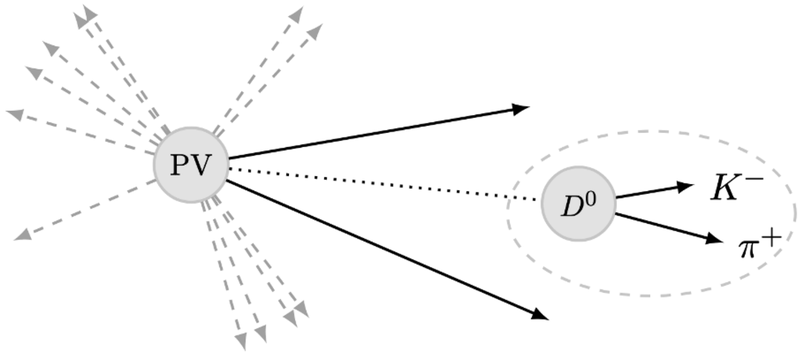
pure TURBO



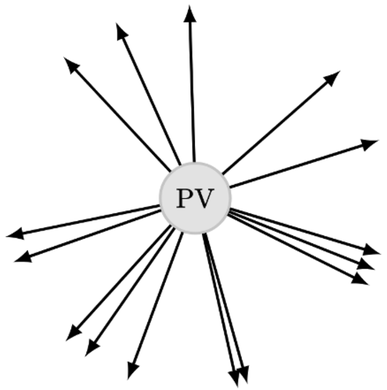


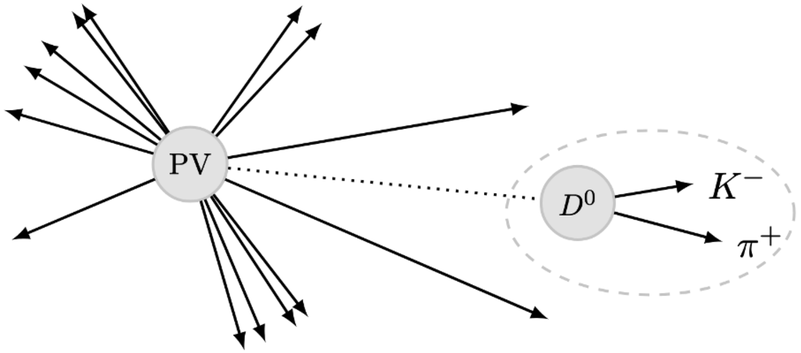
TURBO + selective persistence



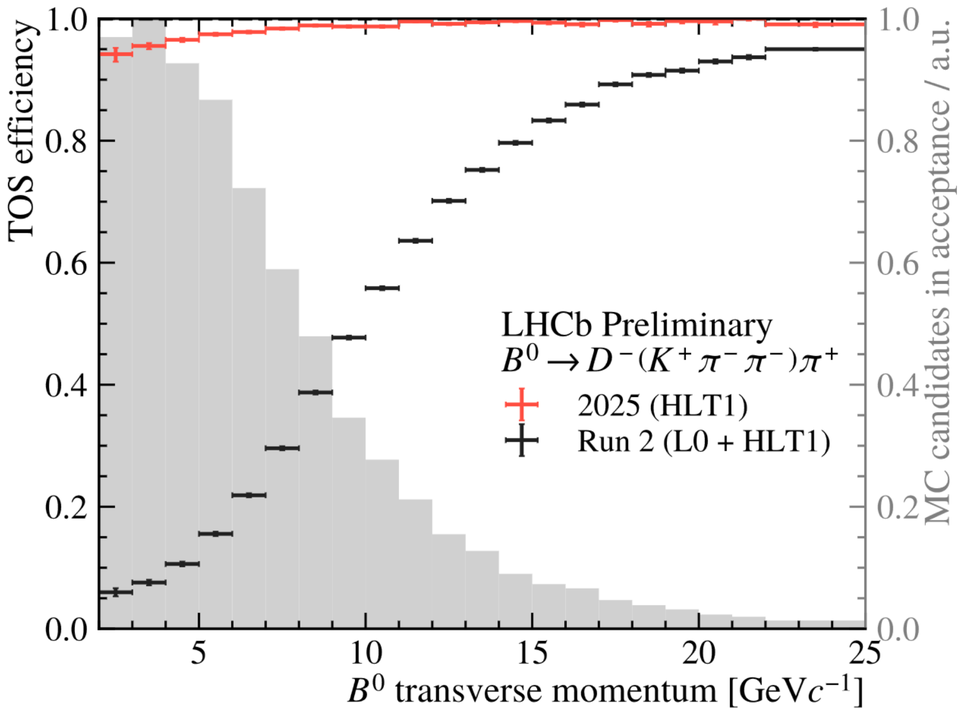


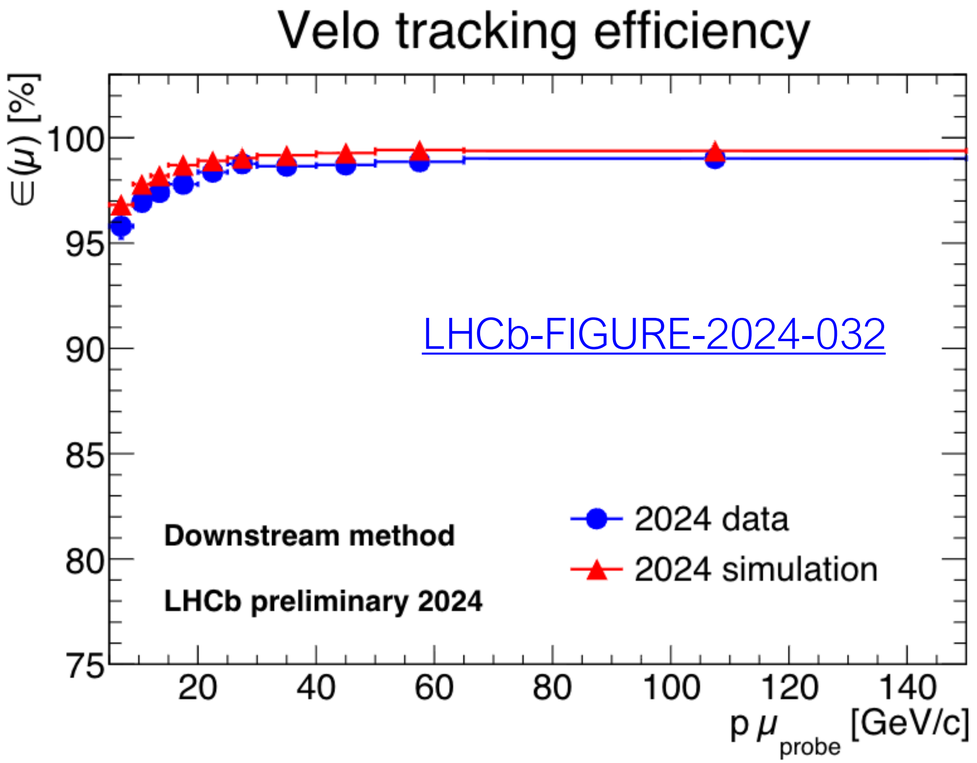
FULL

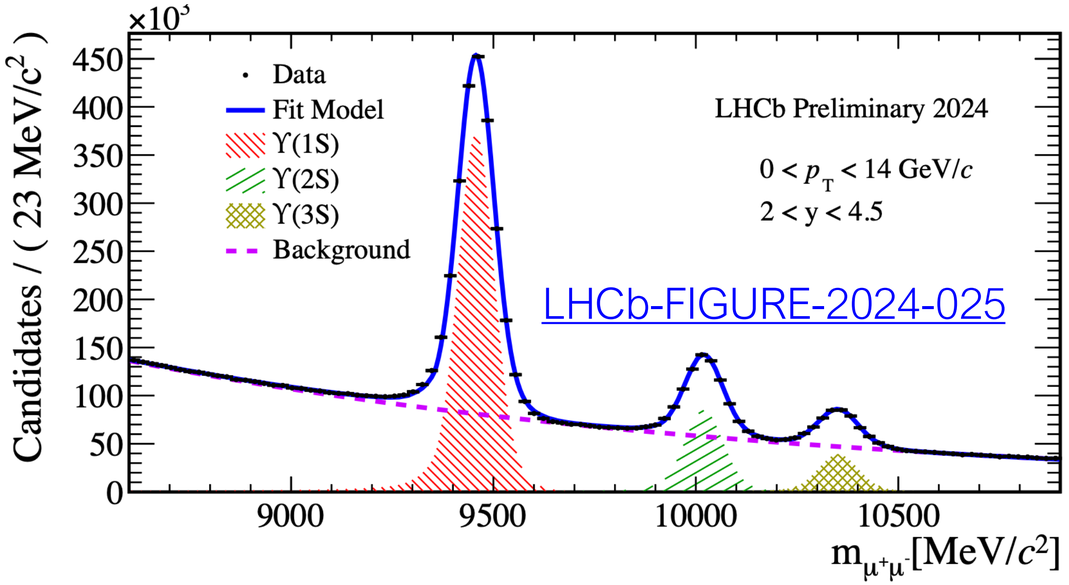




LHCb Run 3 Performance

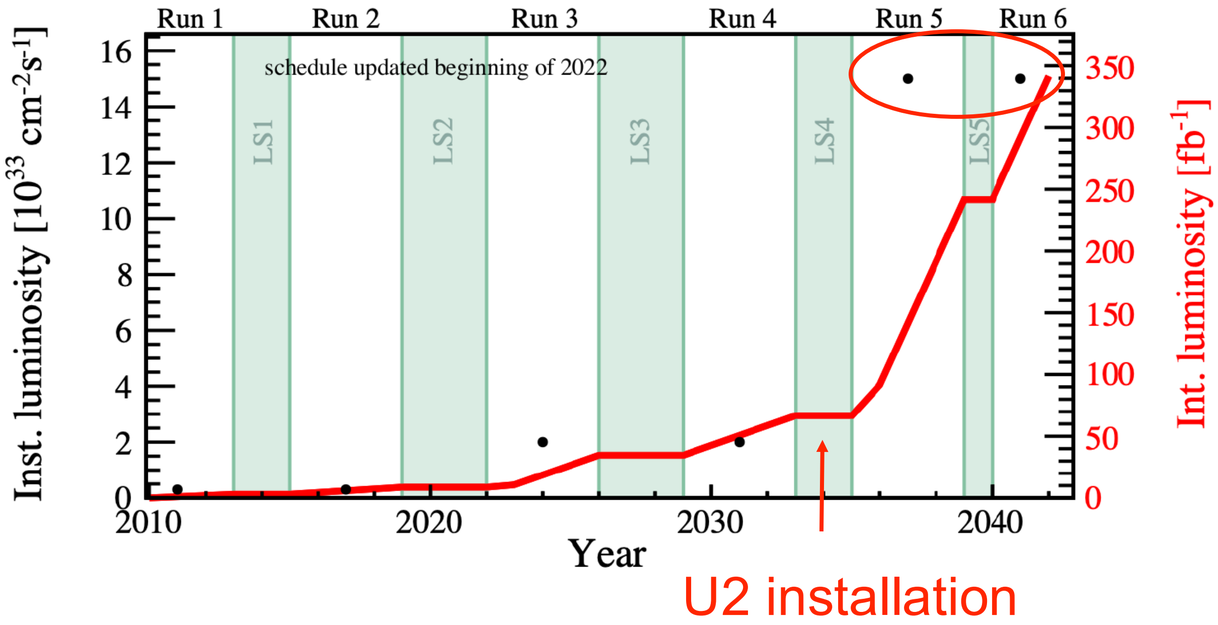




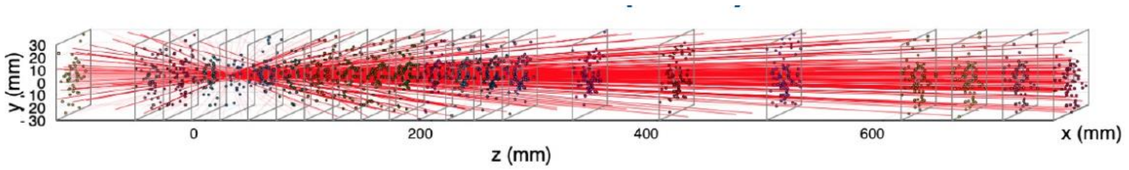


- Significant improvement in HLT1 efficiency (2-4x for hadronic modes)

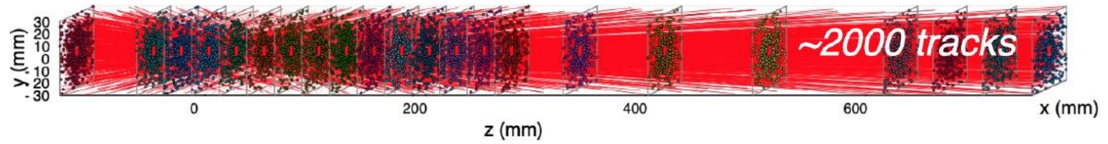
LHCb Upgrade II

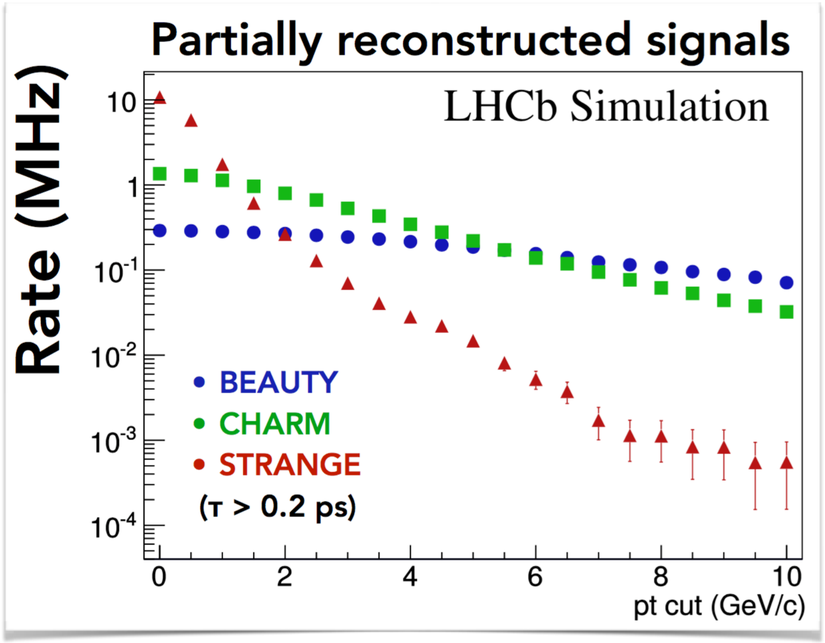


Run 3 pileup ~ 6



U2 pileup ~ 40





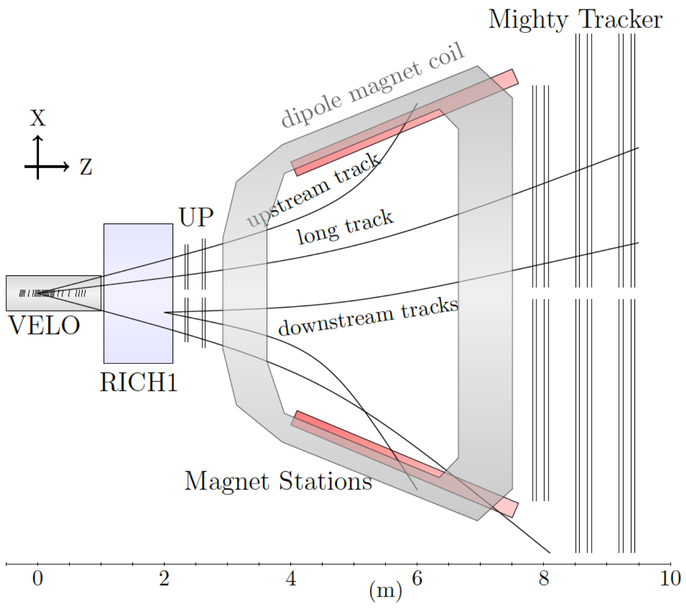
- 5x ~ 7.5x higher luminosity, up to 10^{-34} $cm^{-2}s^{-1}$
- Data rate: from 5 TB/s ⇒ 25 TB/s
- “triggerable” decay in every event
- Larger event size (more PVs + timing info)
- Computing and storage of HLT2 needs scale quadratically [Scoping document, LHCb-TDR-026]

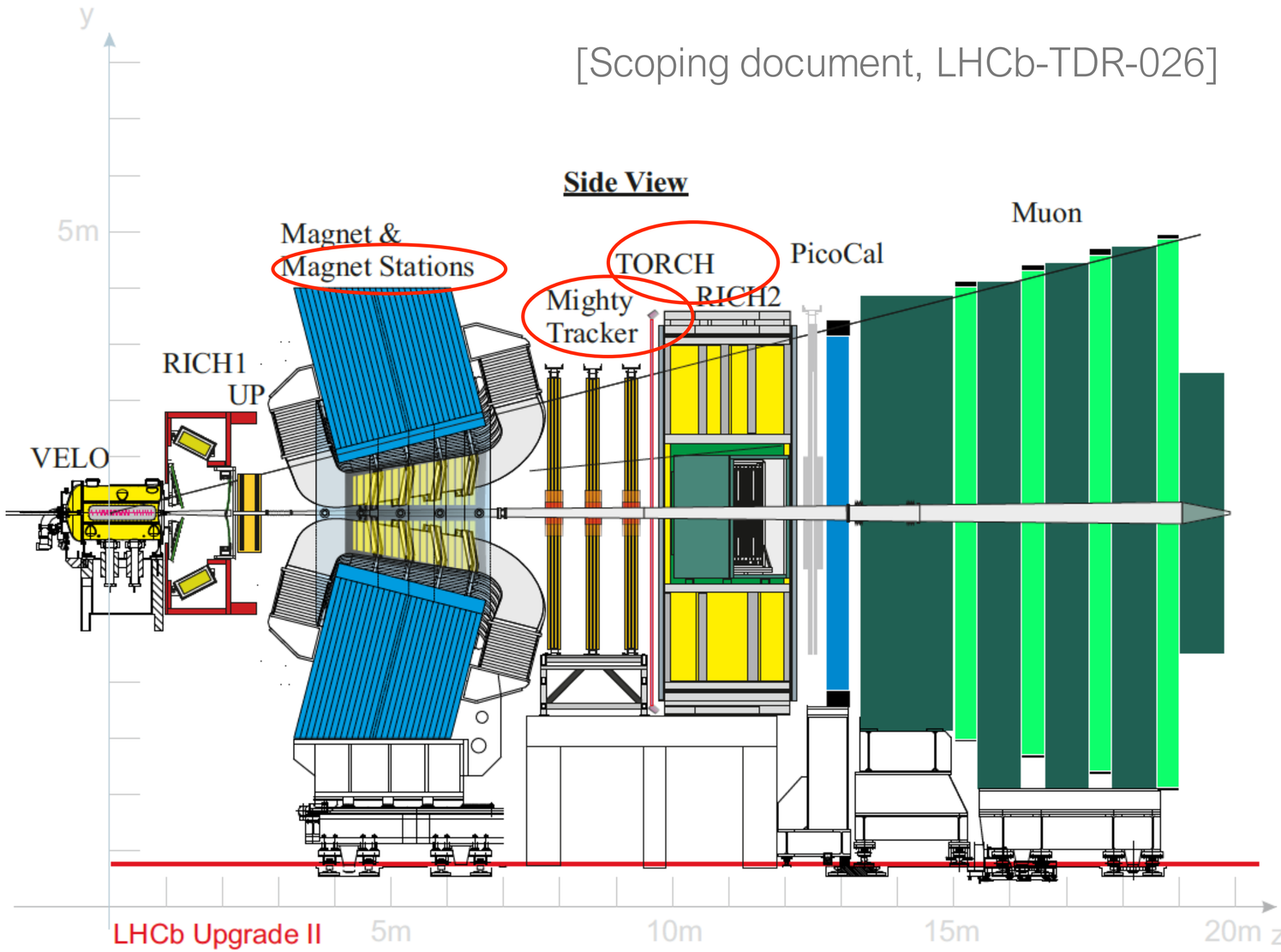
LHCb Upgrade II

[Scoping document, LHCb-TDR-026]

Same layout as Run 3, but with

- Pixels for VELO + UP + Mighty
- TORCH + Magnet Station
- Timing information from VELO, TORCH/RICH and PicoCal





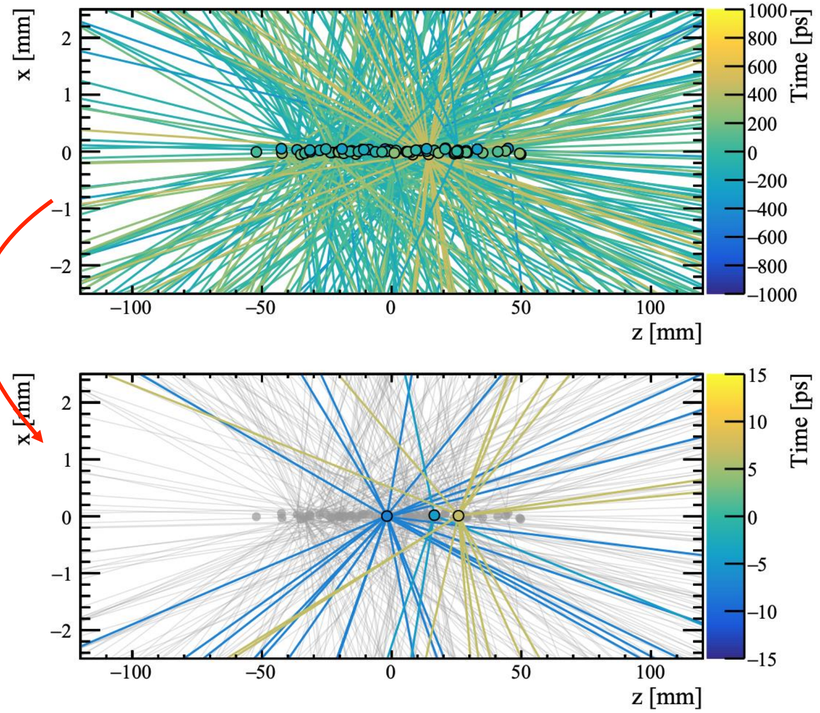
Find more in Fiona's talk and Elena's talk on Thursday

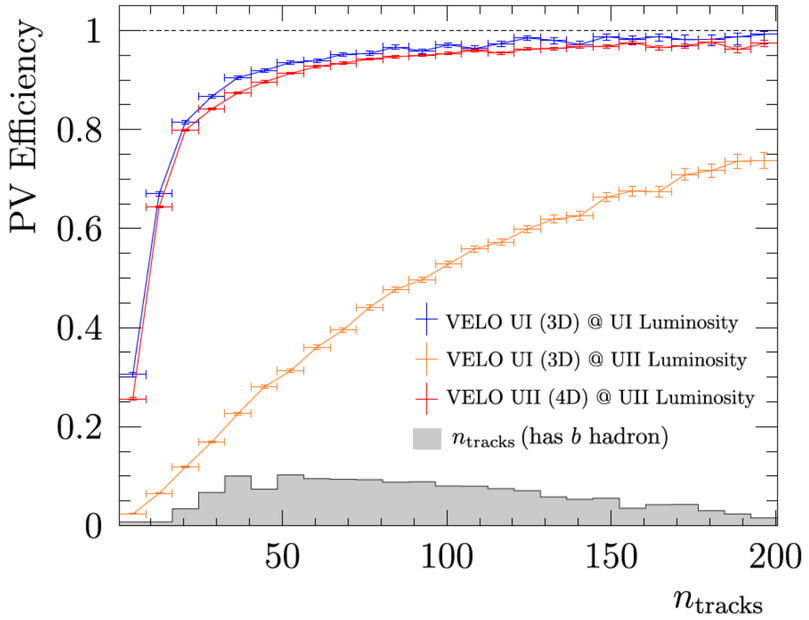
Pile up mitigation with timing

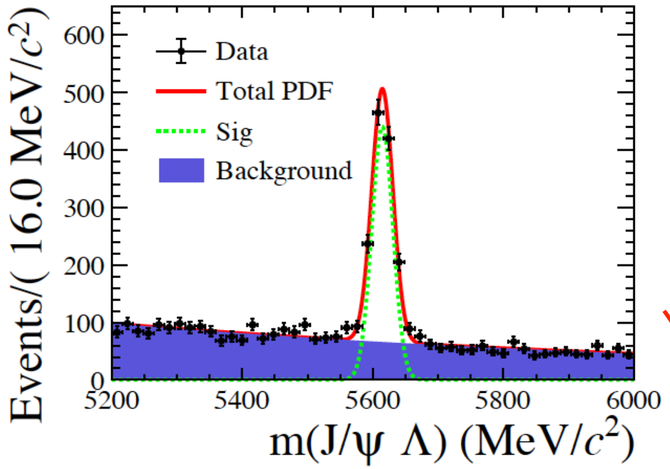
- Timing is necessary for HL-LHC to mitigate the pile-ups
- 4D Tracking and Vertexing, and timing in PID

[Scoping document, LHCb-TDR-026]

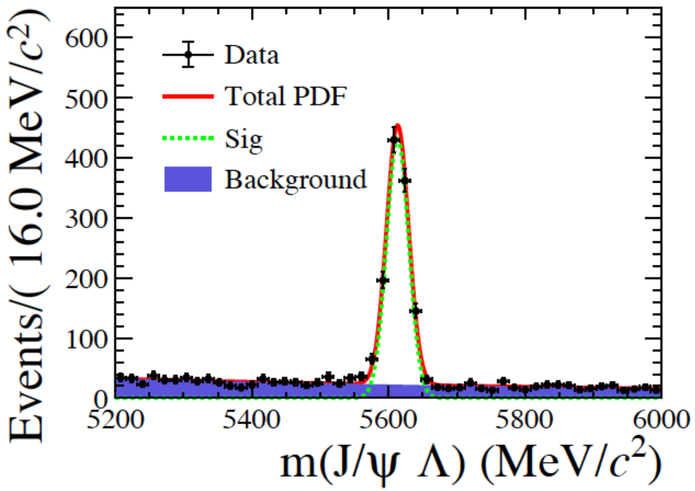
30 ps timing window







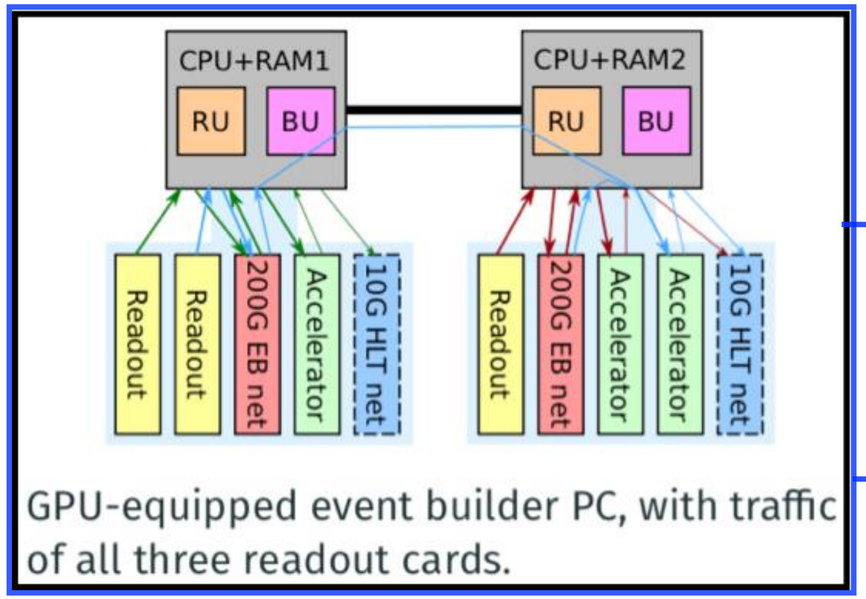
with downstream track timing

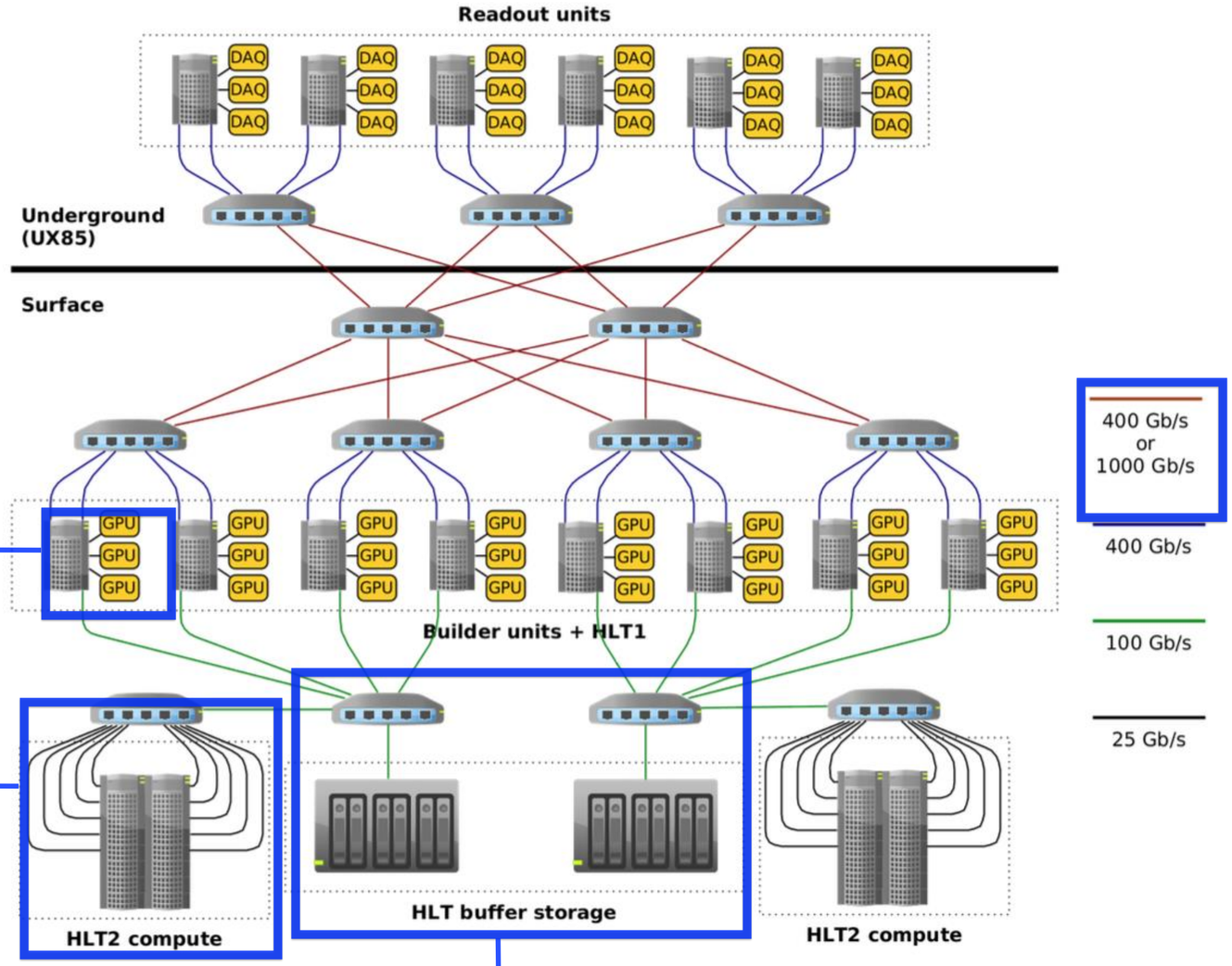


Event-builder architecture

[Framework TDR for the LHCb Upgrade II]

- 5 times capacity of the Run 3 DAQ
- Assume 480 readout-boards at full speed





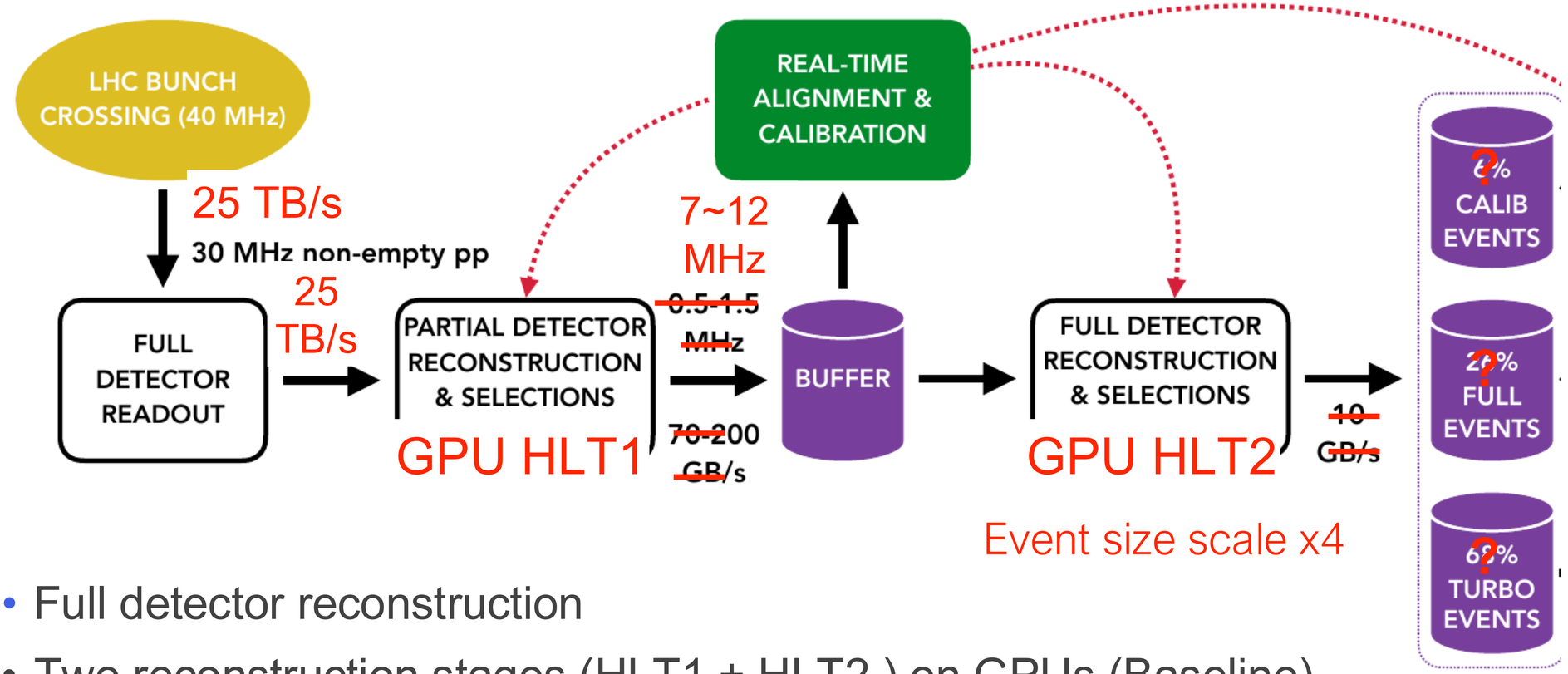
- Full detector reconstruction
- Two reconstruction stages (HLT1 + HLT2) on GPUs (Baseline)
- Disk buffer for alignment & calibration

U2 trigger strategy

All numbers related to the dataflow are taken from the LHCb

[Upgrade Trigger and Online TDR]

[Upgrade Computing Model TDR]



- Full detector reconstruction
- Two reconstruction stages (HLT1 + HLT2) on GPUs (Baseline)
- Clustering & track primitives on FPGAs
- Selective persistency

Summary

- LHCb successfully realised the pure software trigger paradigm in Run 3
  - ✓ Hybrid architecture (GPU+ FPGA +CPU)
  - ✓ Great performance achieved in 2024 data
- Baseline strategy with both HLT1 and HLT2 on GPU for U2
- Various ML / FPGA / IPU developments in progress