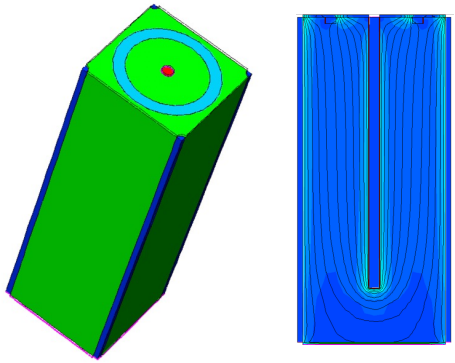
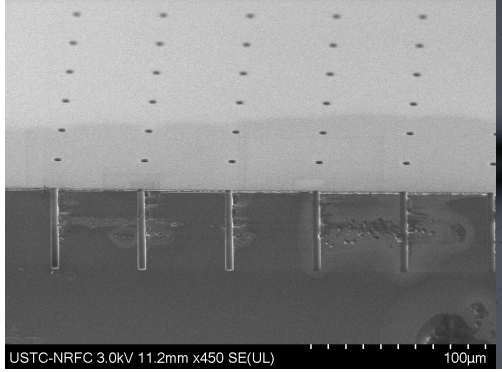
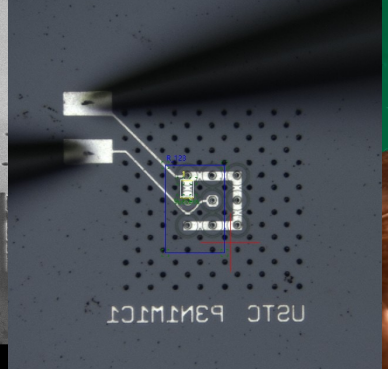
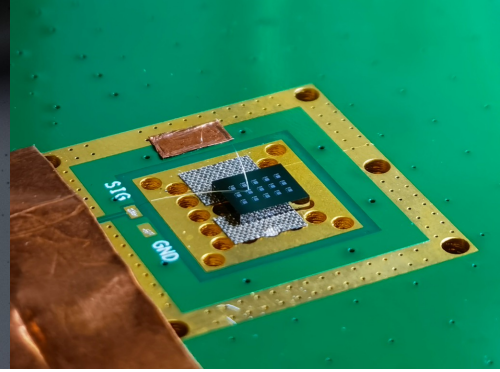



First batch of thin 3D silicon sensors at USTC

Kuo Ma (马 阔)

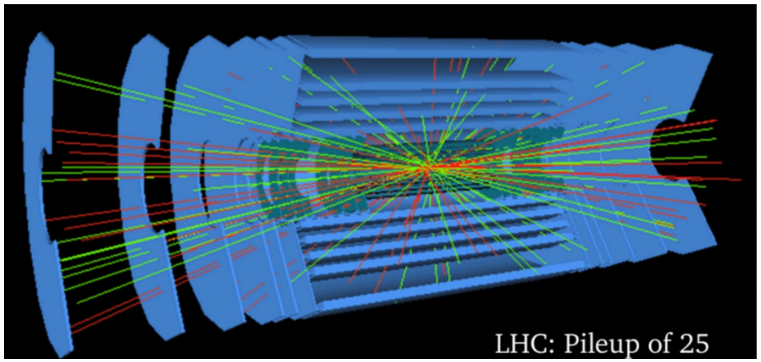
On behalf of the USTC Semiconductor Sensor Group

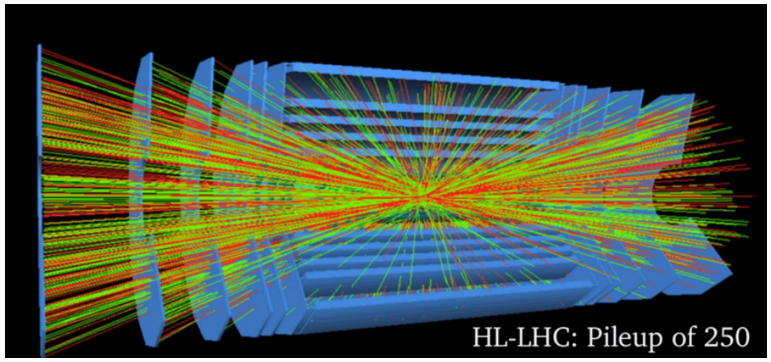
Nov 1st, 2025

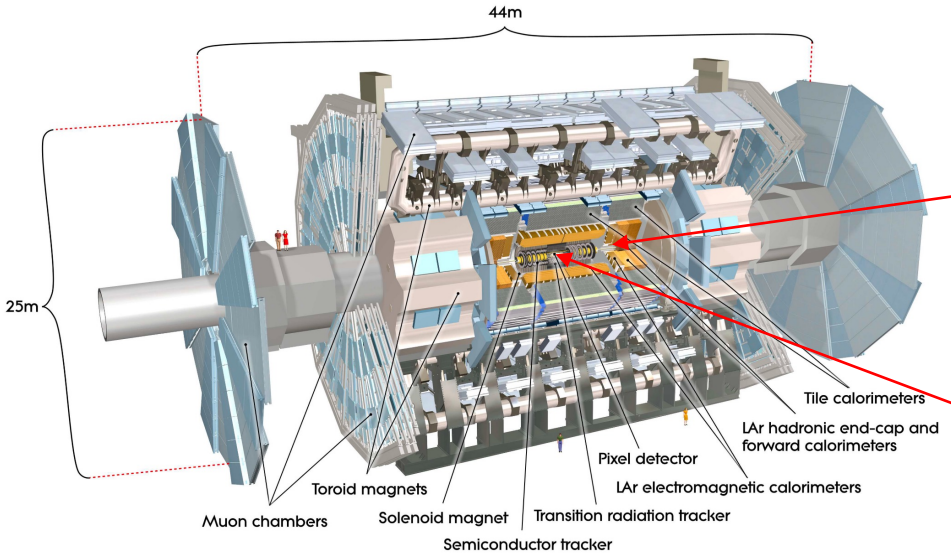
Outline

- Introduction
- The design and simulation
- The layout and fabrication
- The characterizations
- Conclusions

ATLAS Phase2 upgrade







Upgrade of silicon detector:

High Granularity Timing Detector

Forward region ($2.4 < |\eta| < 4.0$)

Precision reconstraction (**30 ps**) with Low Gain Avalanche Detector (LGAD)

Maximum fluence 2.5×10^{15} n_{eq}/cm^2

Details in zhijun's talk

New Inner Tracking Detector (ITk)

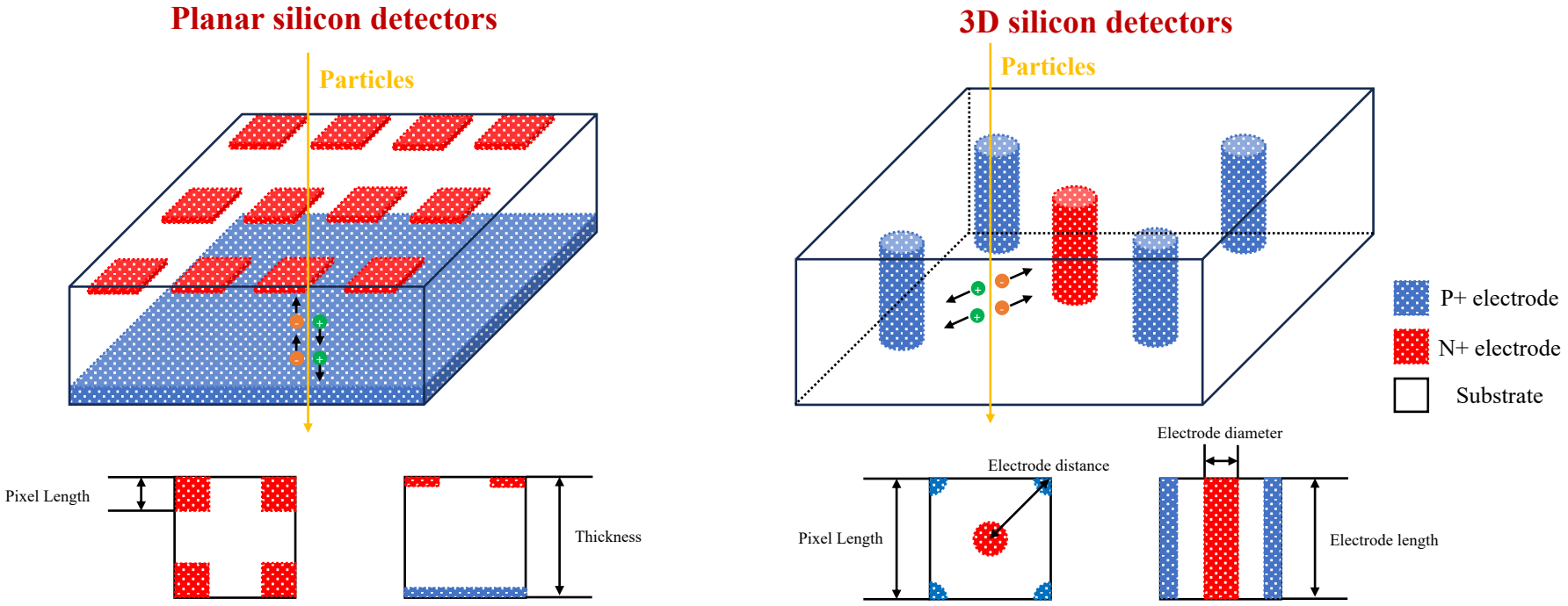
up to $|\eta| = 4.0$

All Silicon (9 layers), **3D sensor**, pixel sensor and strip sensor

Maximum fluence **1.2×10^{16} n_{eq}/cm^2**

Details in xin's talk

Silicon detectors: from planar to 3D



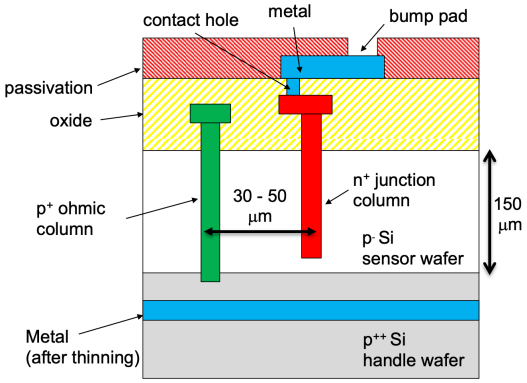
- ➢ Decouple the electrode distance with substrate thickness → Shorten the electrode distance through layout
- The capture probability of carriers decreases due to shorter draft path for carriers → More irradiation tolerant ($> 1\times10^{16}$ n_{eq}/cm^2, 1 MeV equivalent irradiation fluence)
- Lower operation voltage → Lower Power consumption
- Faster signal response but non-uniform spatial response
- Complex processes, such as Deep Reactive Ion Etching (DRIE)

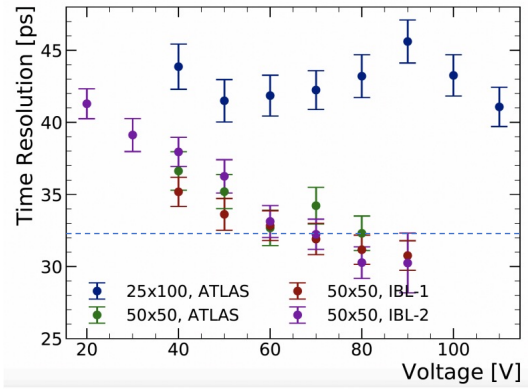
"4D" tracking at extreme environments is important

Details in yanqi's talk

Recent typical 3D silicon detectors

Columnar electrode

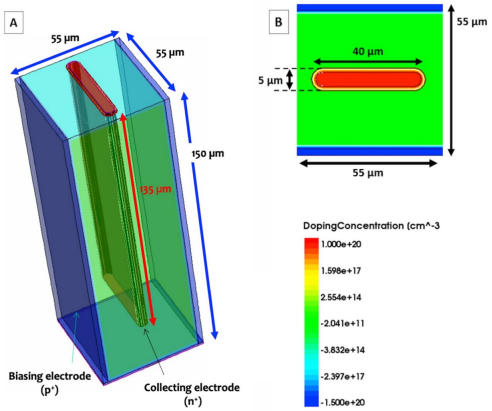


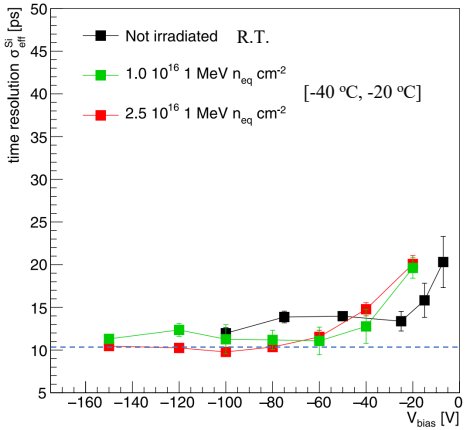


ATLAS ITk project, pixel size
50×50 µm² and 25×100 µm²

Front. Phys. 9:624668 (2021)
L. Diehl and et al. HSTD13, 2023

Trenched electrode

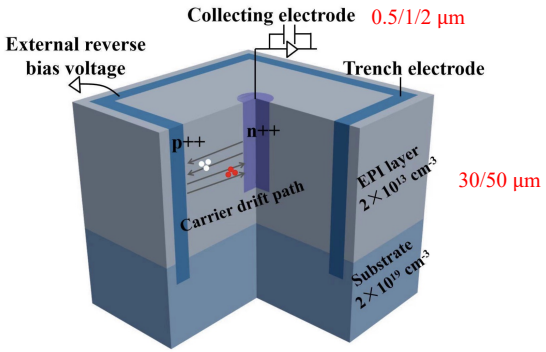


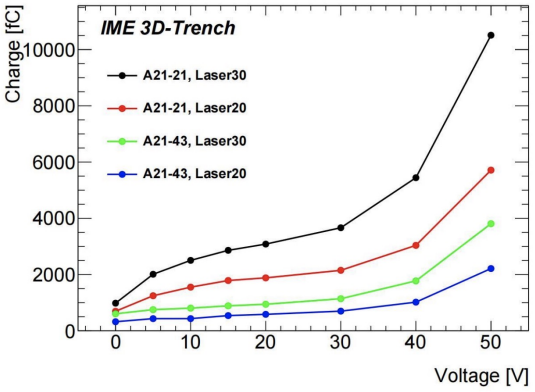


Italy TimeSPOT project,
pixel size 55×55 µm²

JINST 15 (2020)
Front. Phys. 12:1393019(2024)

Trenched-Columnar electrode



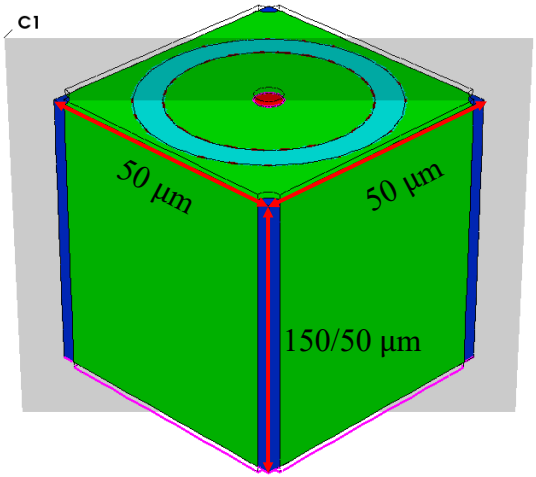


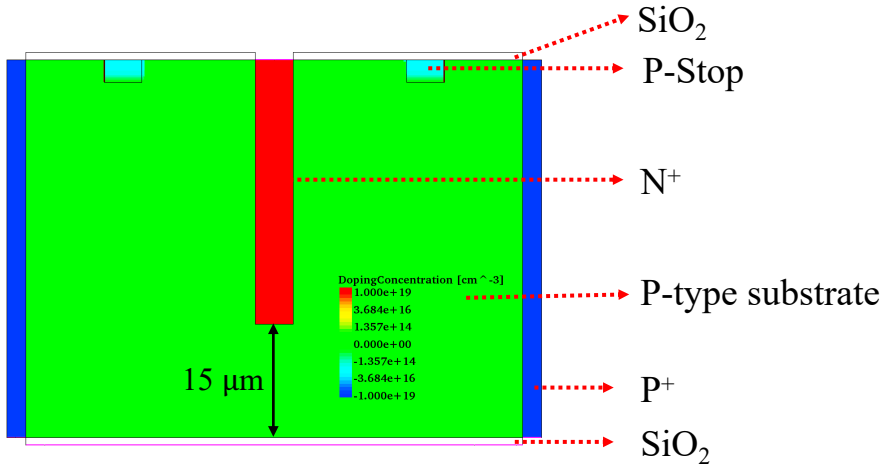
China IMECAS proposal
pixel size 35×35 µm²

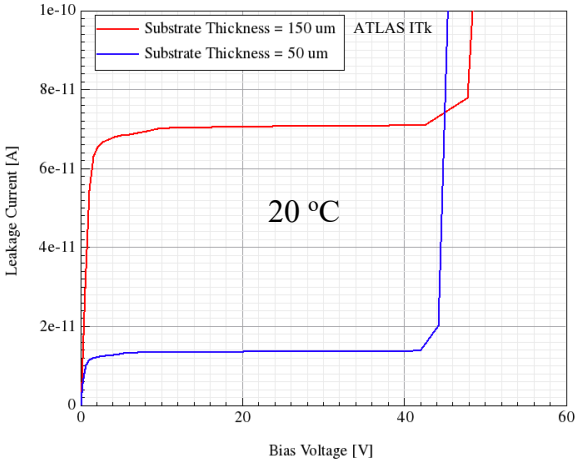
M. Liu and et al, 3th DRD3 Week
G. Kramberger and et al., 3th DRD3 Week

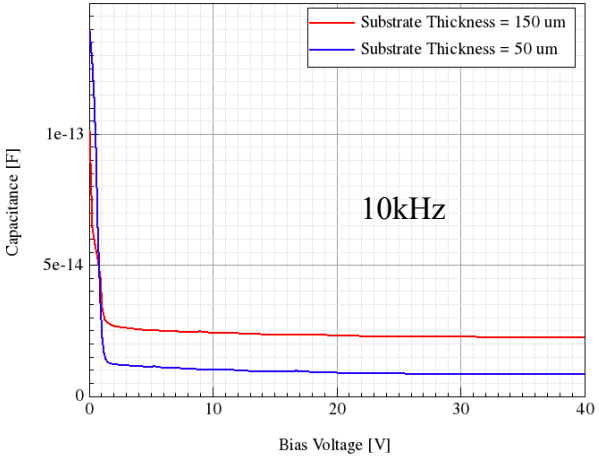
The design and simulation of thin 3D silicon sensors

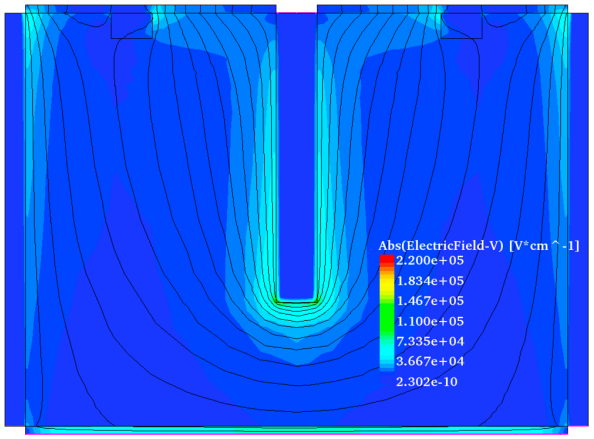
- 3D structure simulation using Sentaurus TCAD:







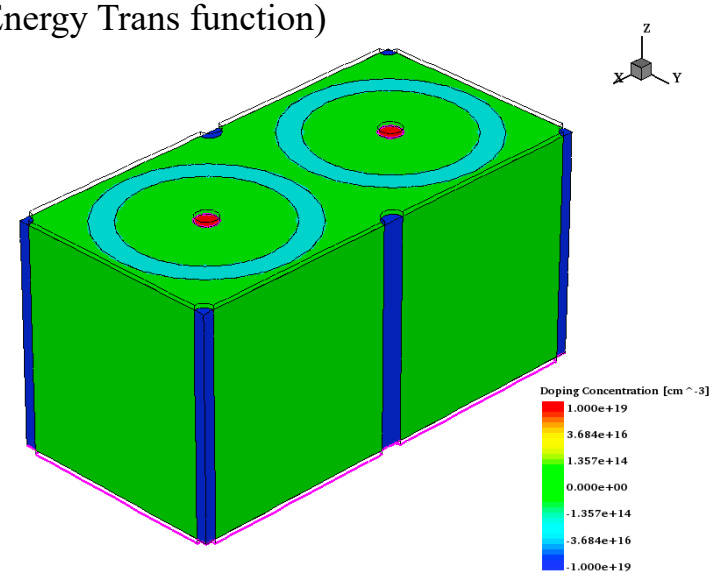


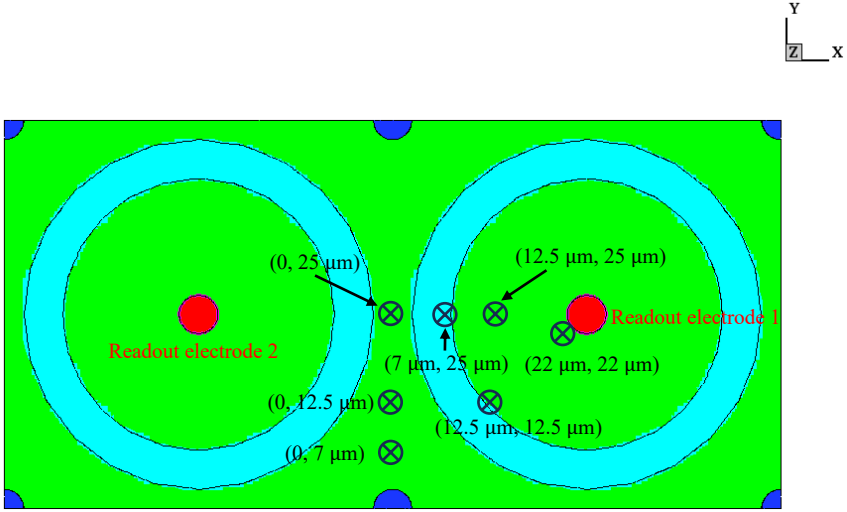


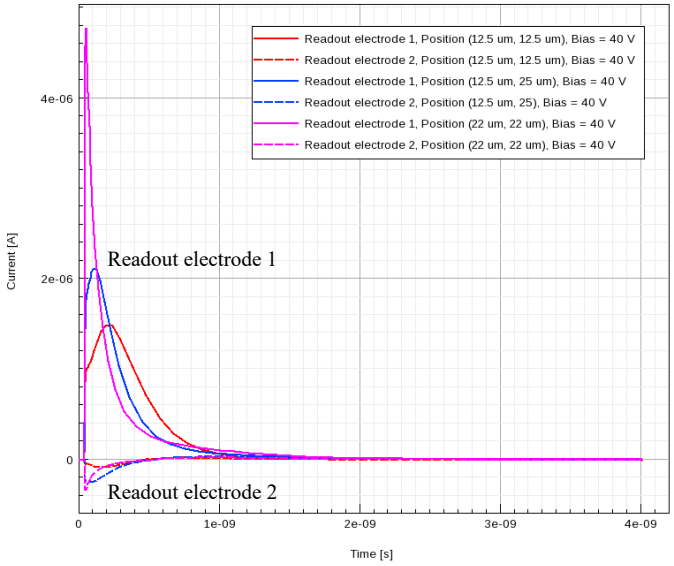
- Simulated two different thickness of substrate.
- The sensor depletes at few volts. And the leakage current after full depletion is in order of several 10^{-11} A.

Transient Current Simulation

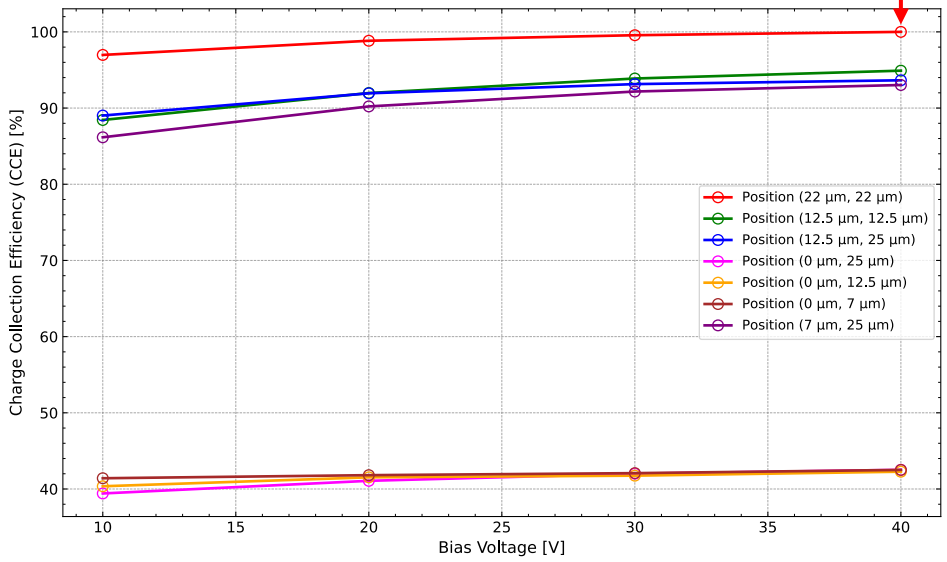
- A minimum ionizing particle (MIP) was simulated with HeavyIon function with LETf = 1.282×10^{-5} pC/μm (Linear Energy Trans function)



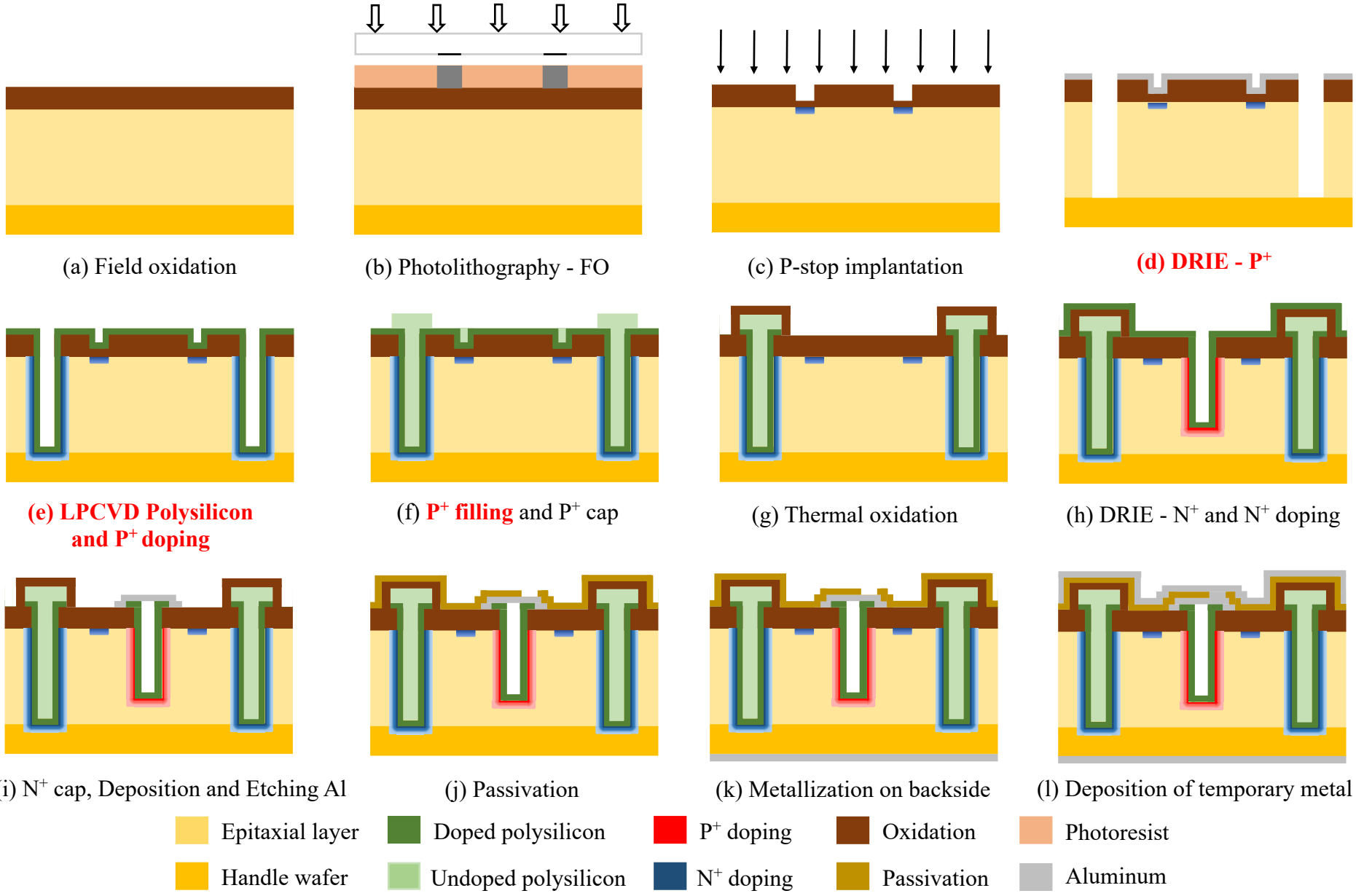




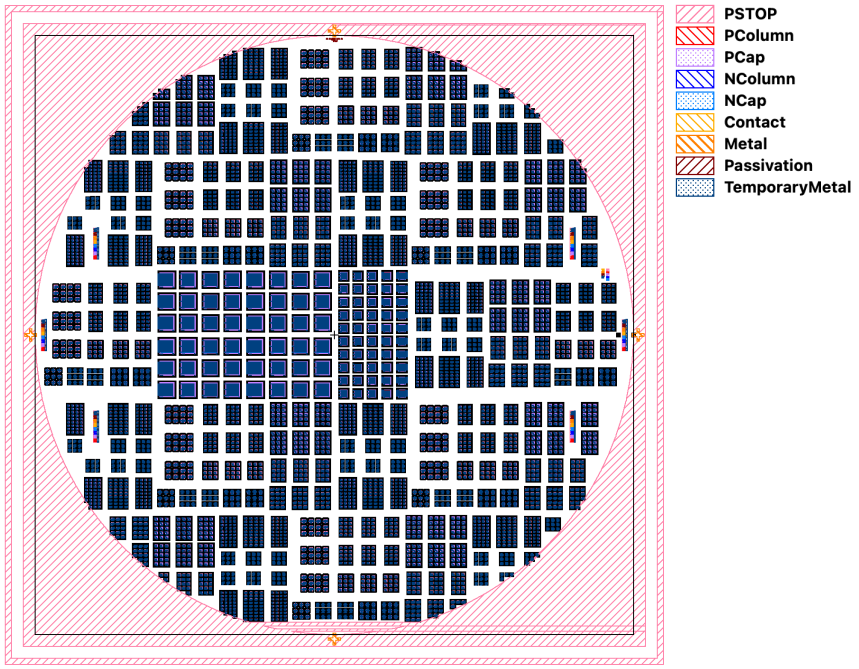
Charge Collection Effiency = 100%

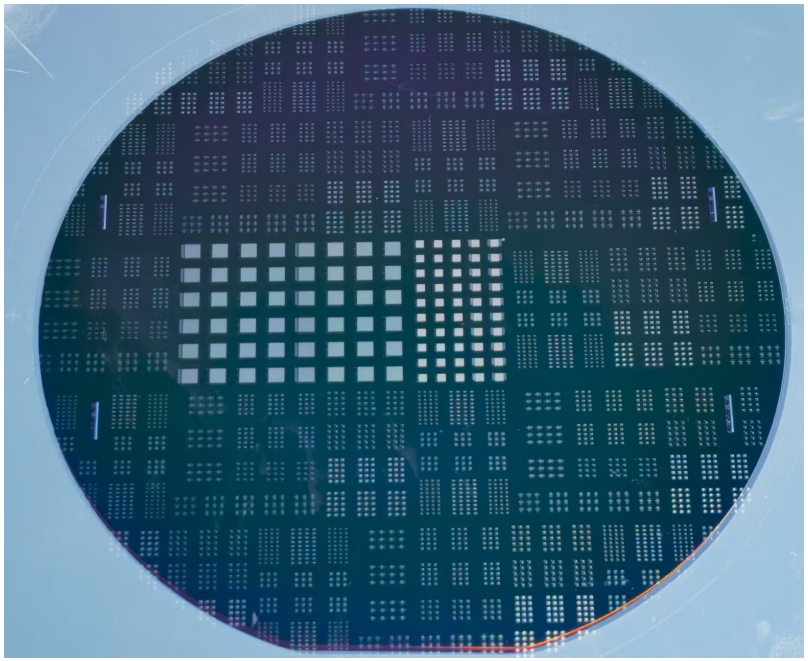


Schematic diagrams of main fabrication steps



The mask and wafer



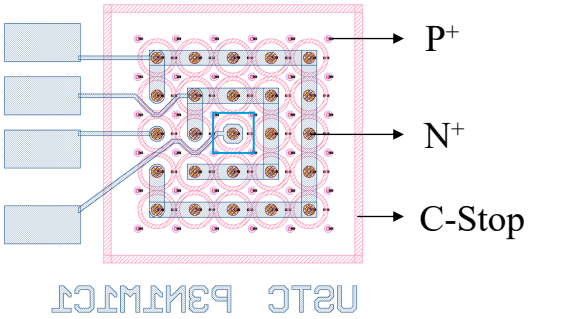


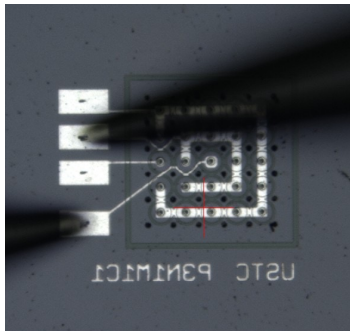
- 5-inch mask with 9 layers
- 6-inch p-type wafer with **50 µm epitaxial layer**
- The sensors are in 4 inch efficient area

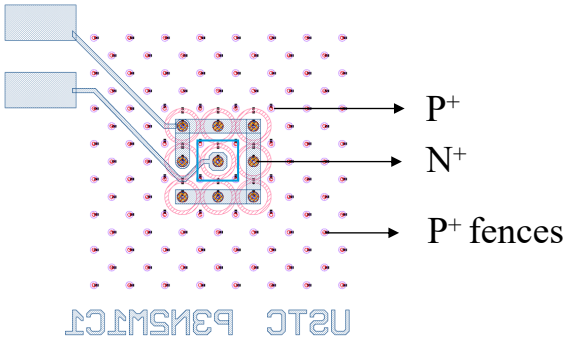
Leakage-Current (I-V) measurements

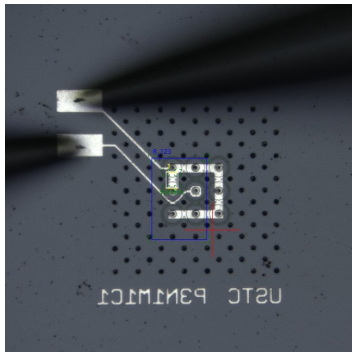
Layout

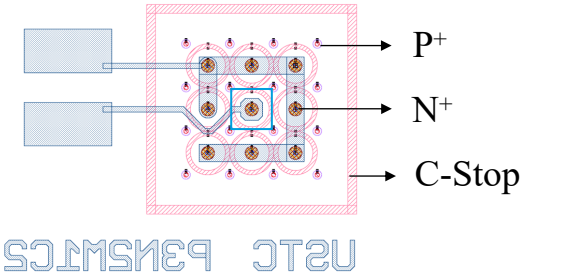
Sensor

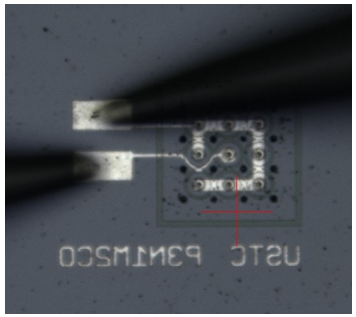


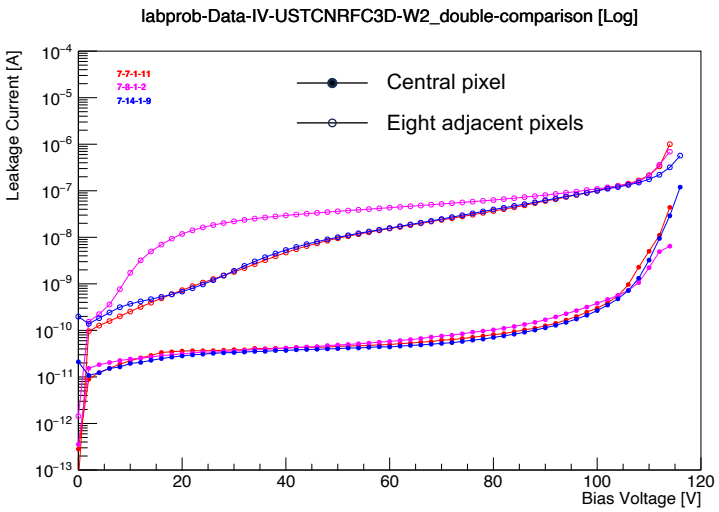






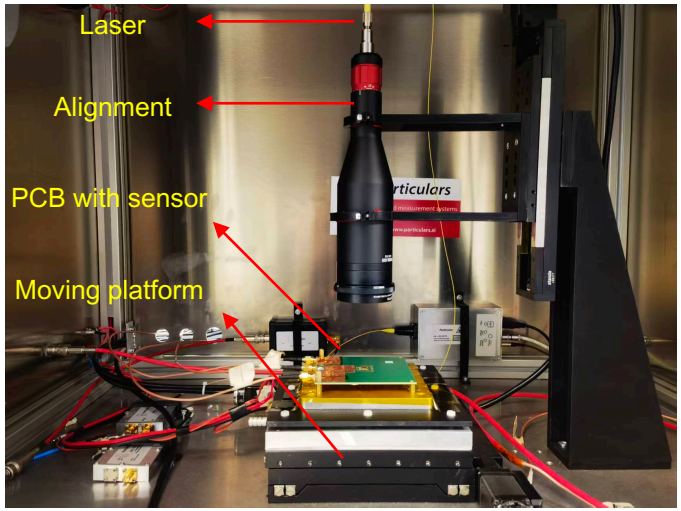


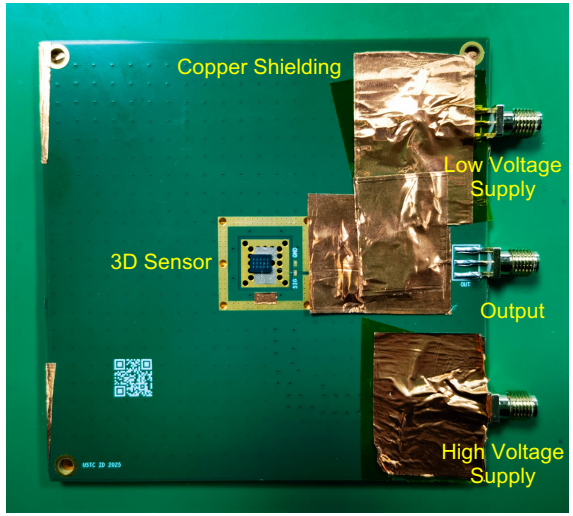




- The sensors deplete in few volts
- The leakage current of normal sensor after full depletion is in order of several 10^{-11} A
- The break down voltage is about 114 V

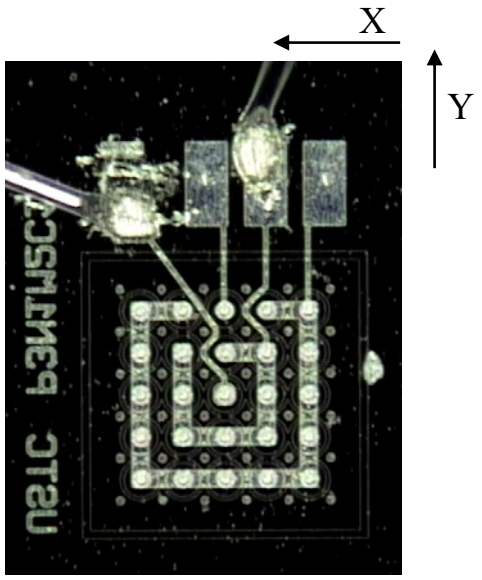
The set-up of Transient Current Technology (TCT)

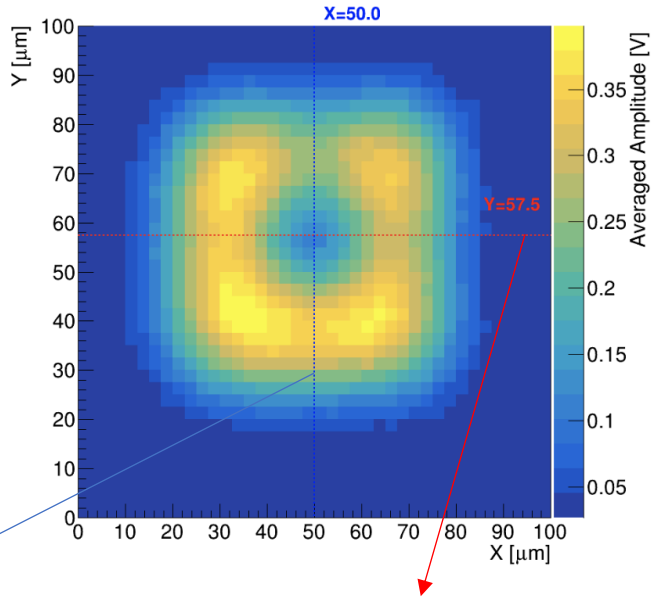


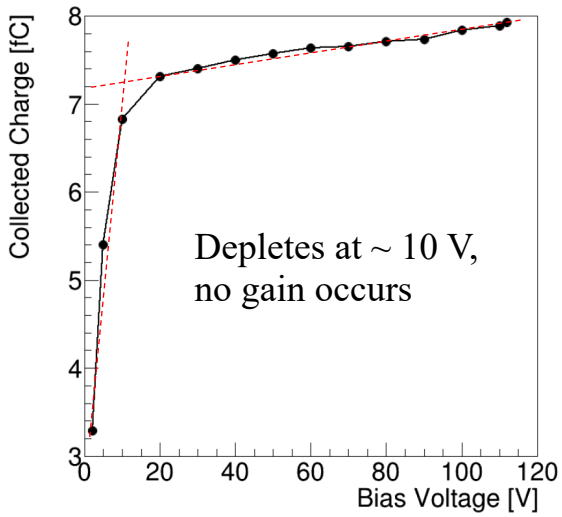


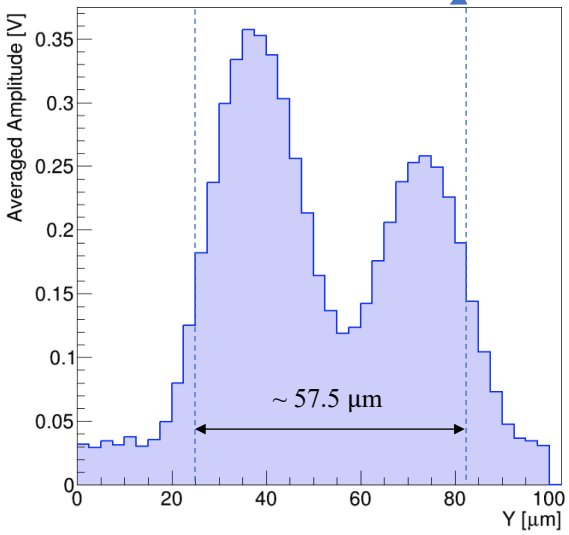
- Tempareture: room temperature
- 3D sensor: the central pixel of 5×5 array with cell size of 50×50 μm^2
- Laser: 1064 nm (infra-red), < 11 μm beam spot (FWHM)
- Trigger: laser sync. signal
- USTC Amplifier board designed for 3D sensor
- Oscilloscope
  - Sampling rate: 40 Gs/s (two channels)
  - Time window: -50 ns ~ 50 ns
  - Full bandwidth

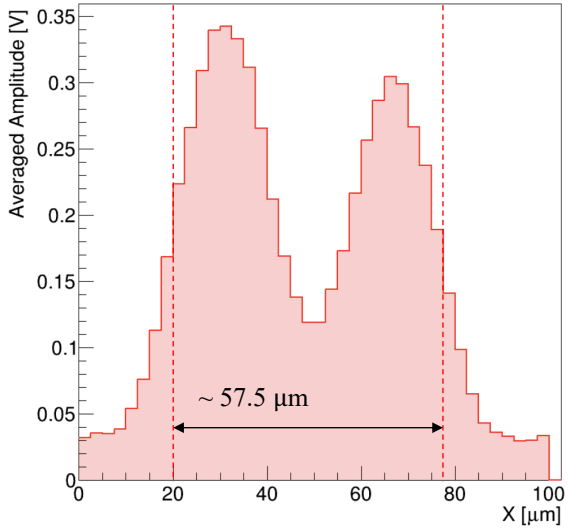
The results of TCT measurements









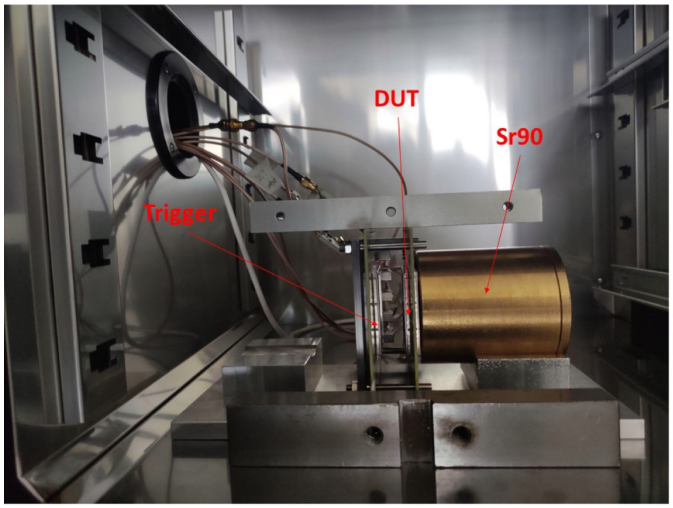


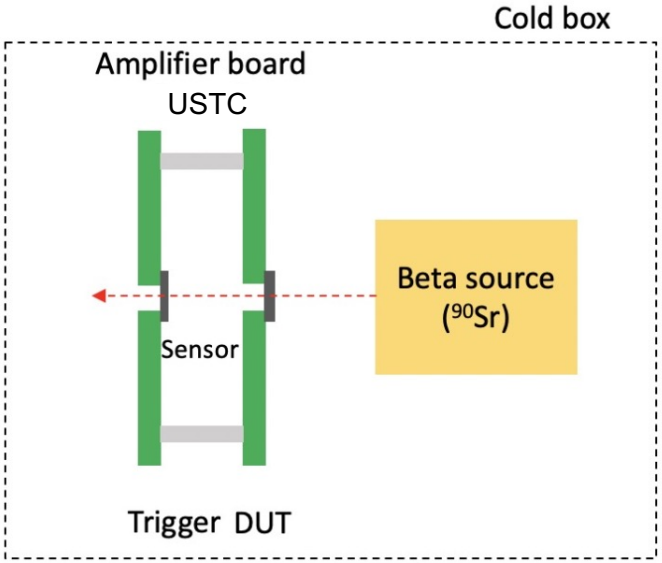
Measured pixel size
(57.5 μm)

≀

Designed pixel size
(50 μm)

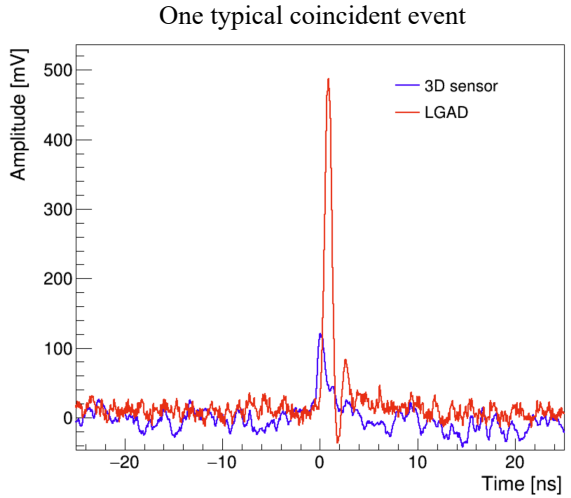
The set-up of β-source measurments

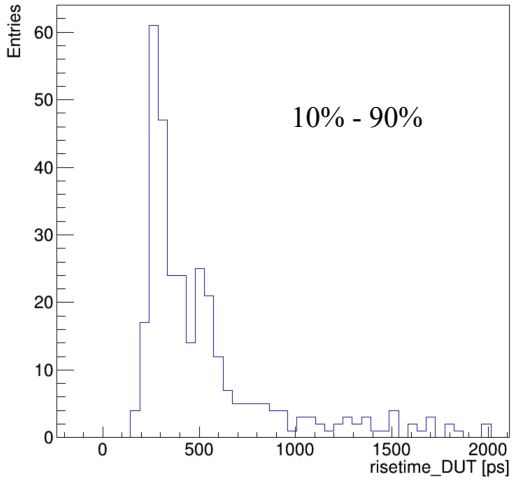


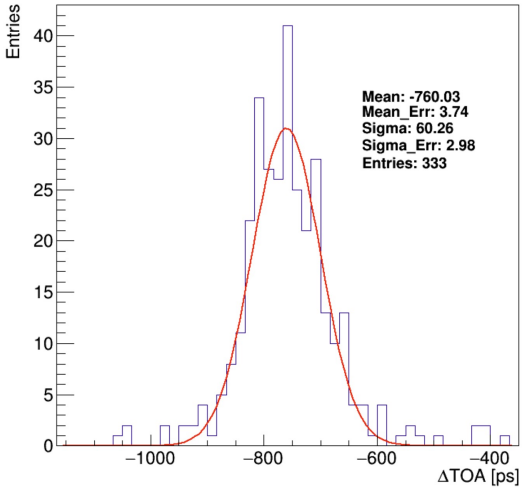


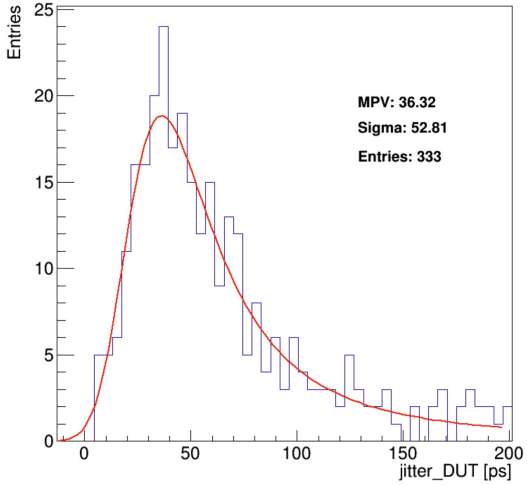
- Temperature: 20 °C
- DUT: USTC 3D pixel sensor, the central pixel of 5×5 array with cell size of 50×50 μm^2
- Reference & Trigger: USTC-IME W17_P4 LGAD, 165V (40.23 ps)
- Oscilloscope:
  - Multi-stage trigger: 35 mV for 3D, 100 mV for LGAD
  - Sample rate: 40 Gs/s
  - Full bandwidth

Time resolution









$$\sigma_{3D} = \sqrt{\Delta TOA^2 - \sigma_{LGAD}^2} \approx 44.86 \text{ ps}\ ,\ \sigma_{Jitter} = \frac{\text{Noise}}{0.8 \cdot \text{Amplitude/Risetime}} \approx 36.32 \text{ ps}$$

Summary

- The 3D silicon sensors with pixel size of 50×50 μm^2, and active thickness of 50 μm have been fabricated.

- The 3D silicon sensors with pixel of 50×50 μm^2 have been characterized:

  - The IV measurements shows the break down voltage is about 114 V.

  - Using TCT measurements, the depletion voltage is around 10 V and the measured pixel size is about 57.5 μm.

  - The time resolution is 44.86 ± 4 ps (20 ^oC, 110V) tested by the β-source.

Acknowledgment

- The fabrication of sensors were carried out at the USTC Center for Micro and Nanoscale Research and Fabrication and Suzhou Institute of Nano-Tech and Nano-Bionics.
- The solid phosphorus diffusion wafers were supplied freely by VivioGrowth Technology.
- The characterization of sensors were carried out at the USTC Platform for Semiconductor Detectors R&D and System Integration.
- We are grateful for all staff who participated in this work.

中国科学技术大学微纳研究与制造中心

USTC Center for Micro- and Nanoscale Research and Fabrication

新成科技

VIVIOGROWTH TECHNOLOGY

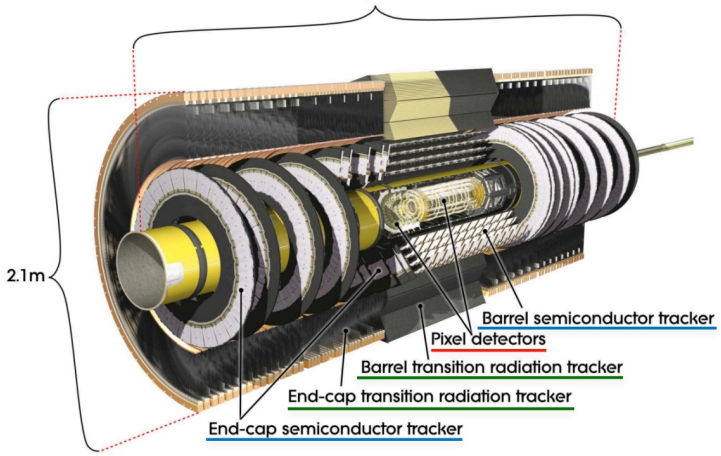
中国科学院苏州纳米技术与纳米仿生研究所

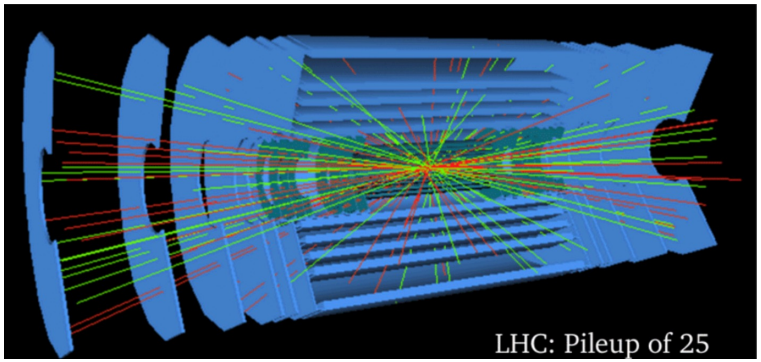
Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO), Chinese Academy of Sciences

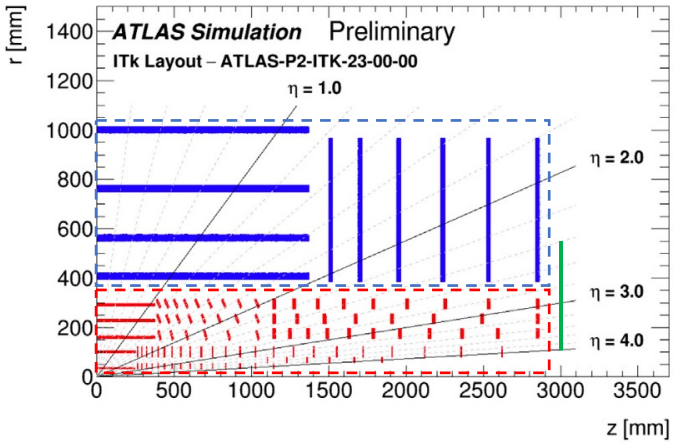
Thanks for your attention!

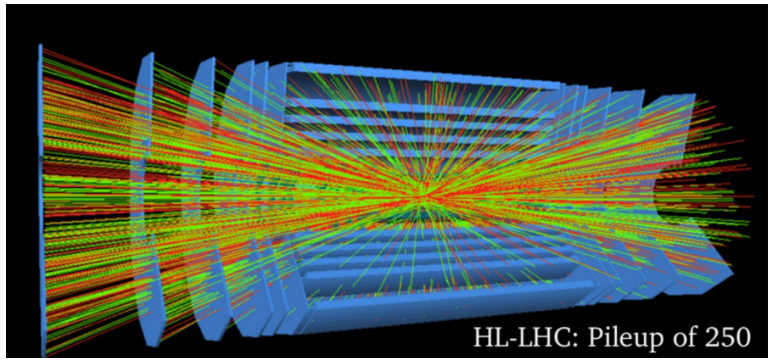
Back up

Inner detector and the upgrade



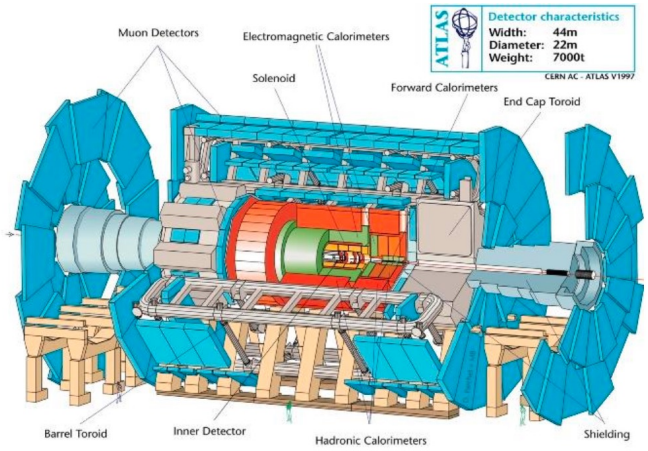




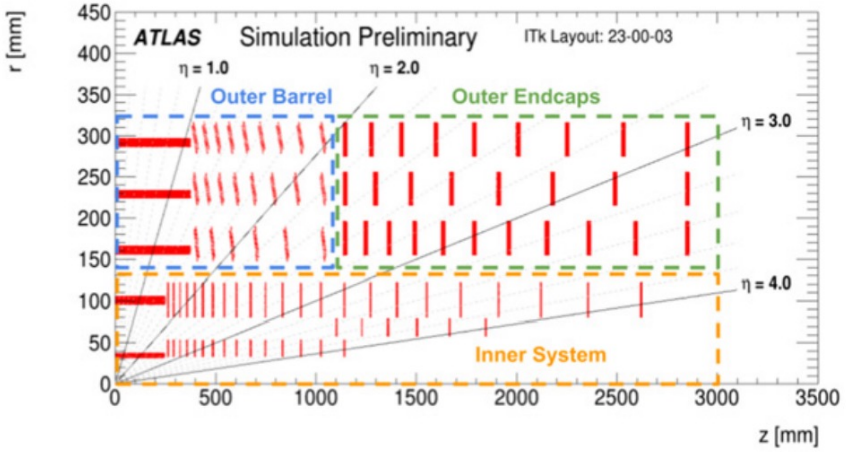


- With high pile up and hard radiation environment:
  - Full inner detector replacement → **Full silicon tracker, I**nner **T**racker (ITk)
  - A timing detector at the end-cap will be added → **H**igh **G**ranularity **T**iming **D**etector (HGTD)

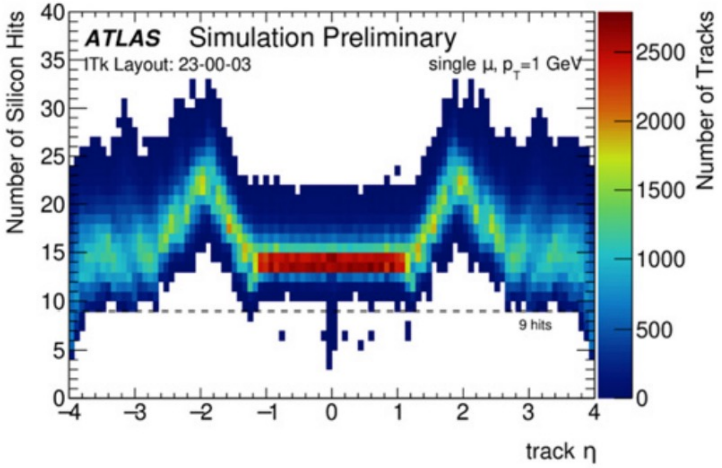
Inner Tracking (ITk)



- Challenges of High-Luminosity LHC (HL-LHC):
  - Radiation levels: $\sim 2 \times 10^{16}\ n_{eq}/cm^2$ for innermost pixel layers
  - High hit-rate capability (up to 200 events per bunch-crossing)
- Sensors requirements:
  - Small pixels: 50×50 and $25 \times 125\ \mu m^2$
  - Thinner active region ($\sim 150\ \mu m$)
  - Narrower electrodes ($\sim 5\ \mu m$)



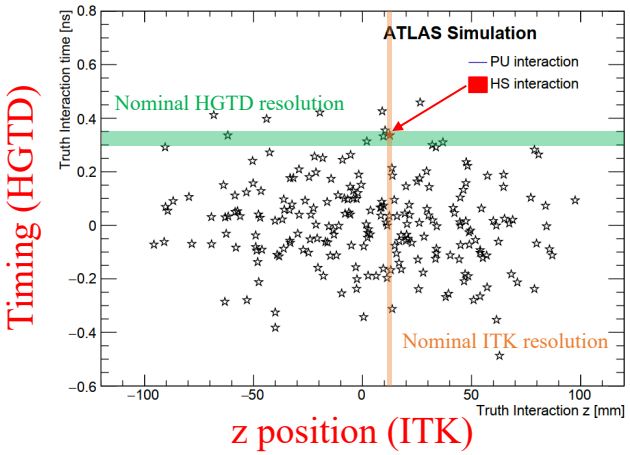
- One quadrant of the ITk pixel system

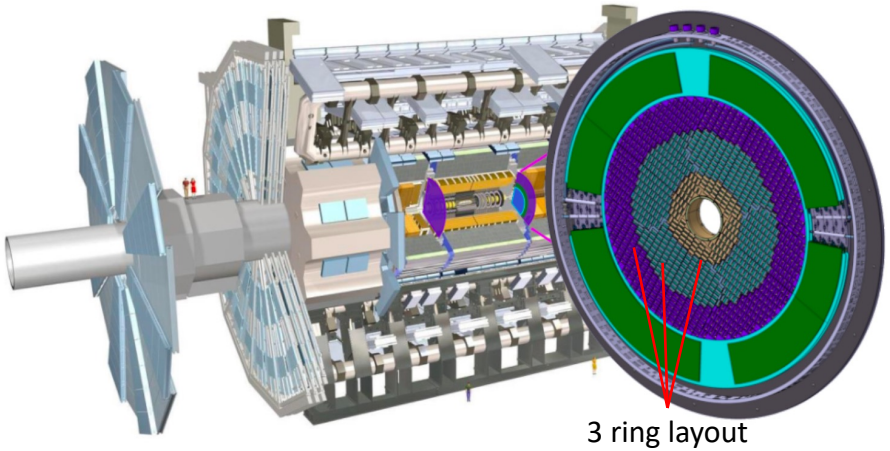


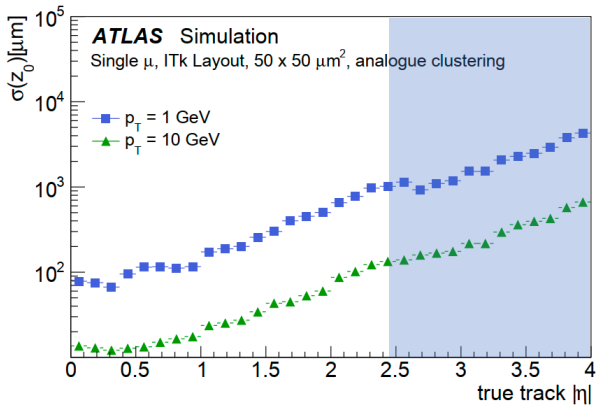
- Simulated hits in silicon pixel layers of the ITk [1]

ATLAS **H**igh **G**ranularity **T**iming **D**etector (HGTD)

- To measure high-precision time of charged particles in the forward region ($2.4 < |\eta| < 4.0$) while with ~1 mm position resolution, complementing the ITk







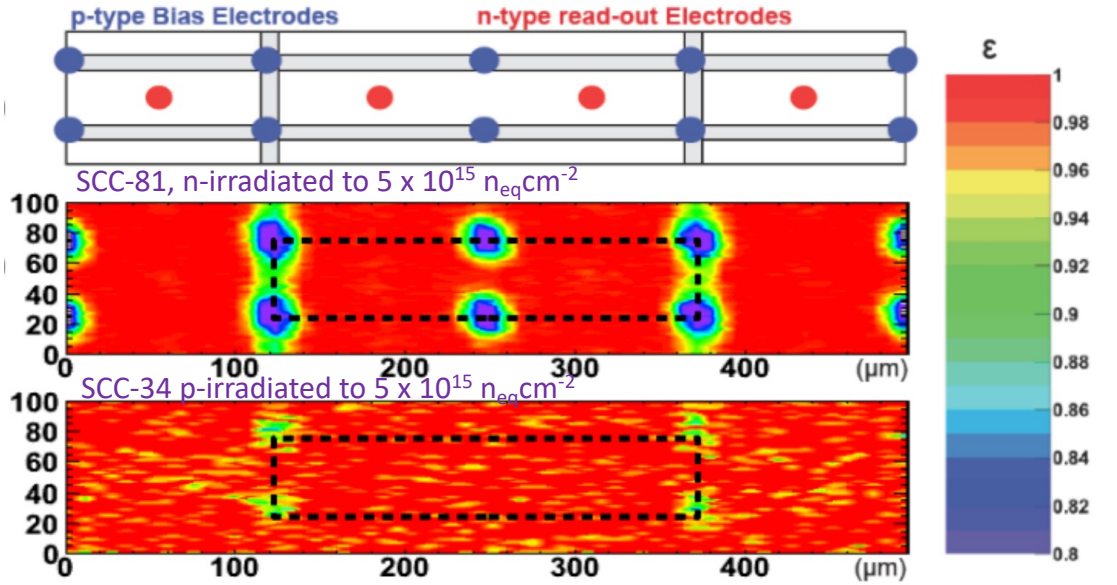
HGTD requirements:

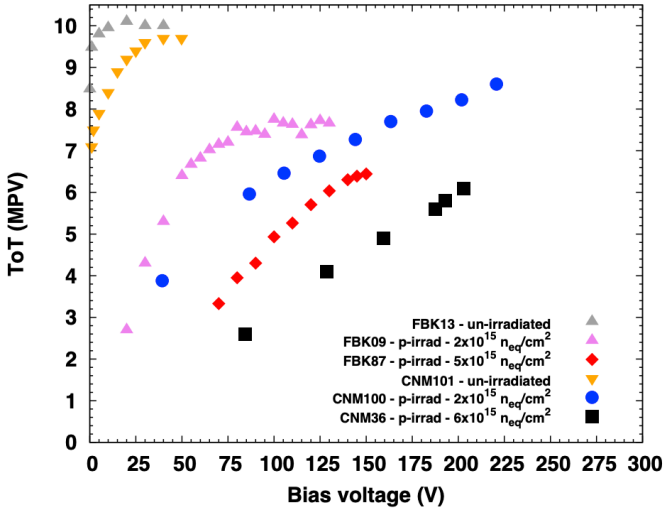
- Withstand intense radiation environment
  - Maximum fluence: 2.5E15 n_{eq}/cm^2
  - Total Ionising Dose (TID): 2 MGy
- Collected charge per hit > 4 fC
- Timing resolution: 35 ps (start), 70 ps (end) per hit / 30 ps (start), 50 ps (end) per track
- Hit efficiency of 97% (95%) at the start (end)

Main Milestone: ATLAS IBL 3D pixels sensors

- Double-sided 3D sensors supplied by CNM and FBK
- Excellent performance up to > 5 x 10^{15} n_{eq} cm^{-2}

Cell efficiency maps (120 GeV pions, CERN – SPS)





SCC-81, normal incident, HV = 160 V, Threshold = 1500 e^-: Eff = 97.46%

SCC-34, 15° incident, HV = 160 V, Threshold = 1500 e^-: Eff = 98.85%

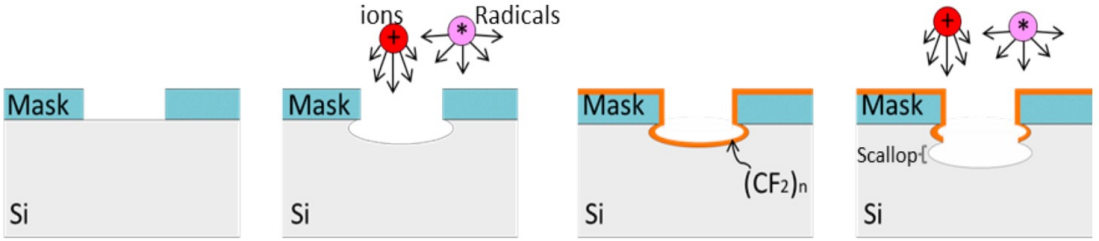
ATLAS IBL, JINST 7 (2012) P11010

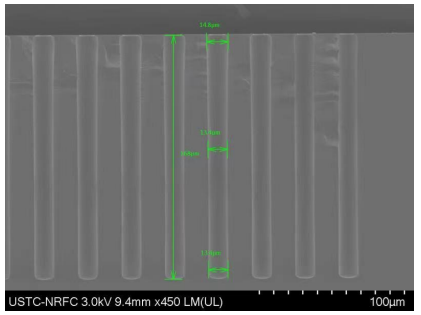
The ToT-collection charge corrention is not shown in this plot.

S. Grinstein. A. Micelli.

The key technology: Deep Silicon Etching

- Deep Reactive Ion Etching (DRIE): Bosch, alternating etch cycles (SF_6) and passivation cycles (C_4F_8)





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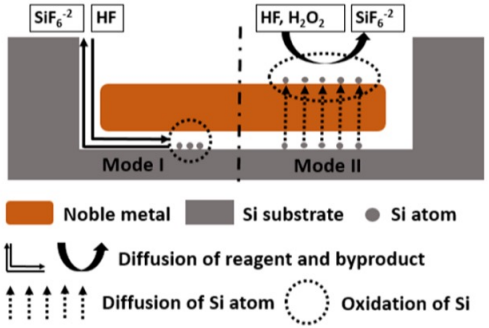
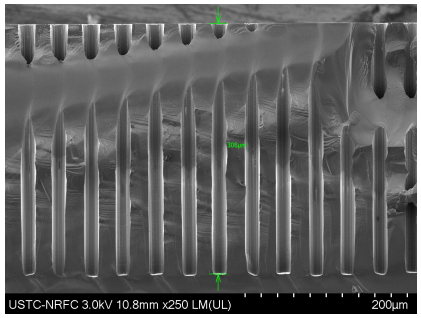
- Metal-Assisted Chemical Etching [A. Nur'aini, et al. ACS 7 (2022)]

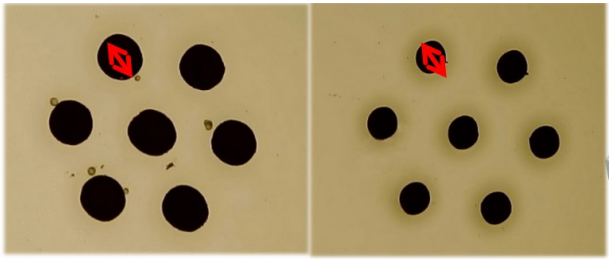




- Fairly high aspect ratio (15:1)
- obvious defect in the side walls
- The irregular bottoms
- The thickness/kind of noble metal and the solution ratio should be selected very carefully

- Laser Etching [X Shi, SiC high timing resolution detector, 2023]

Hole	Diameter（μm）
Entrance	103
Exit	81



- More defects can cause high leakage current in silicon detectors

Experimental conditions

中国科学技术大学微纳研究与制造中心
USTC Center for Micro- and Nanoscale Research and Fabrication
NANO · USTC

中国科学院苏州纳米技术与纳米仿生研究所
Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO), Chinese Academy of Sciences

- The 6-inch experimental fabrication line is available in USTC **N**anoscale **R**esearch and **F**abrication **C**enter and **S**uzhou **I**nstitute of **Na**no-Tech and **Na**n**o**-Bionics (SINANO)

Estrelas 100 - DRIE

Plasma System100 ICP180 - Dry etching Al

PlasmaPro NGP 80 - Dry etching SiO_2

SKT6, etc - Wet etching

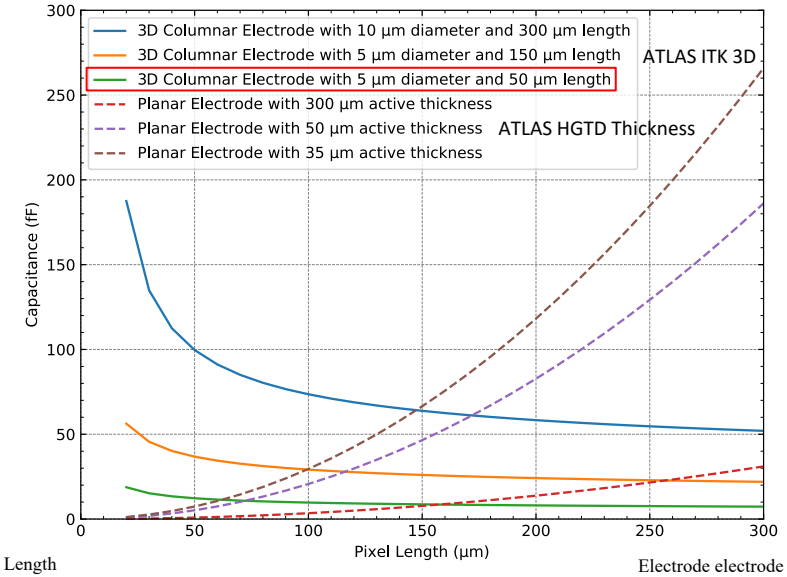
Tystar mini-tytan 3600 - Deposition/Diffusion

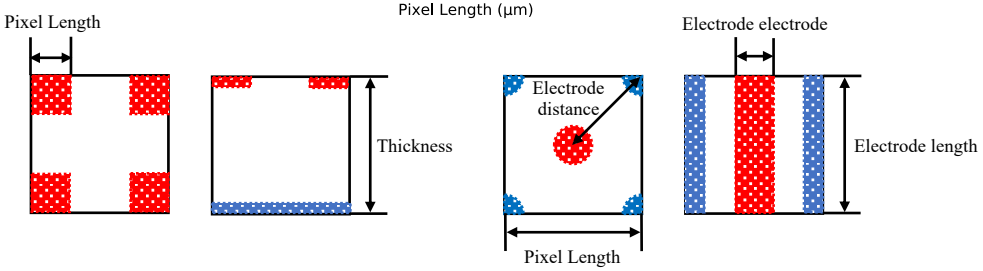
RCH5600 - Oxidation/Passivation

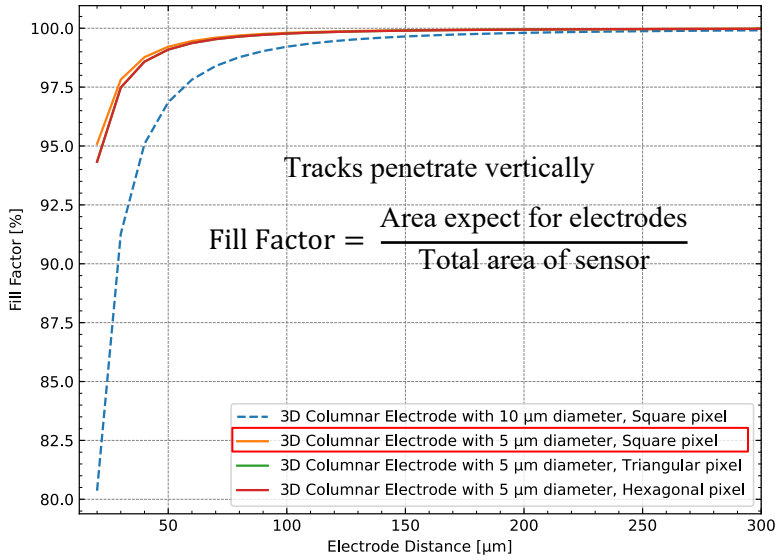
MABA6 - Photolithography

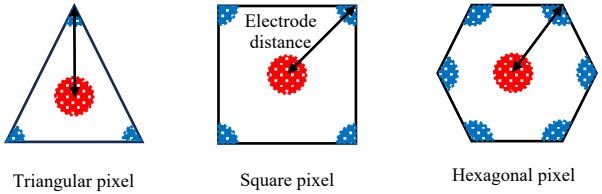
NV-GSD-HE - Boron implantation

Capacitance and Fill Factor









- Capacitance is the main noise source. The smaller diameter and shorter length of electrode is benefit for small pixel cell.
- The larger fill factor means less insensitive area。The smaller diameter of electrode can also make the fill factor larger and the square pixel has larger fill factor compared with other common shape.
- Also considering the experimental conditions, we focus the development of 3D silicon sensors with **square pixel of 50 μm × 50 μm**, **electrode diameter of 5 μm** and **length of 50 μm in the first batch**.

USTC Amplifier Board