Comprehensive Full-Power Testing of Demonstrator System for the High Granularity Timing Detector

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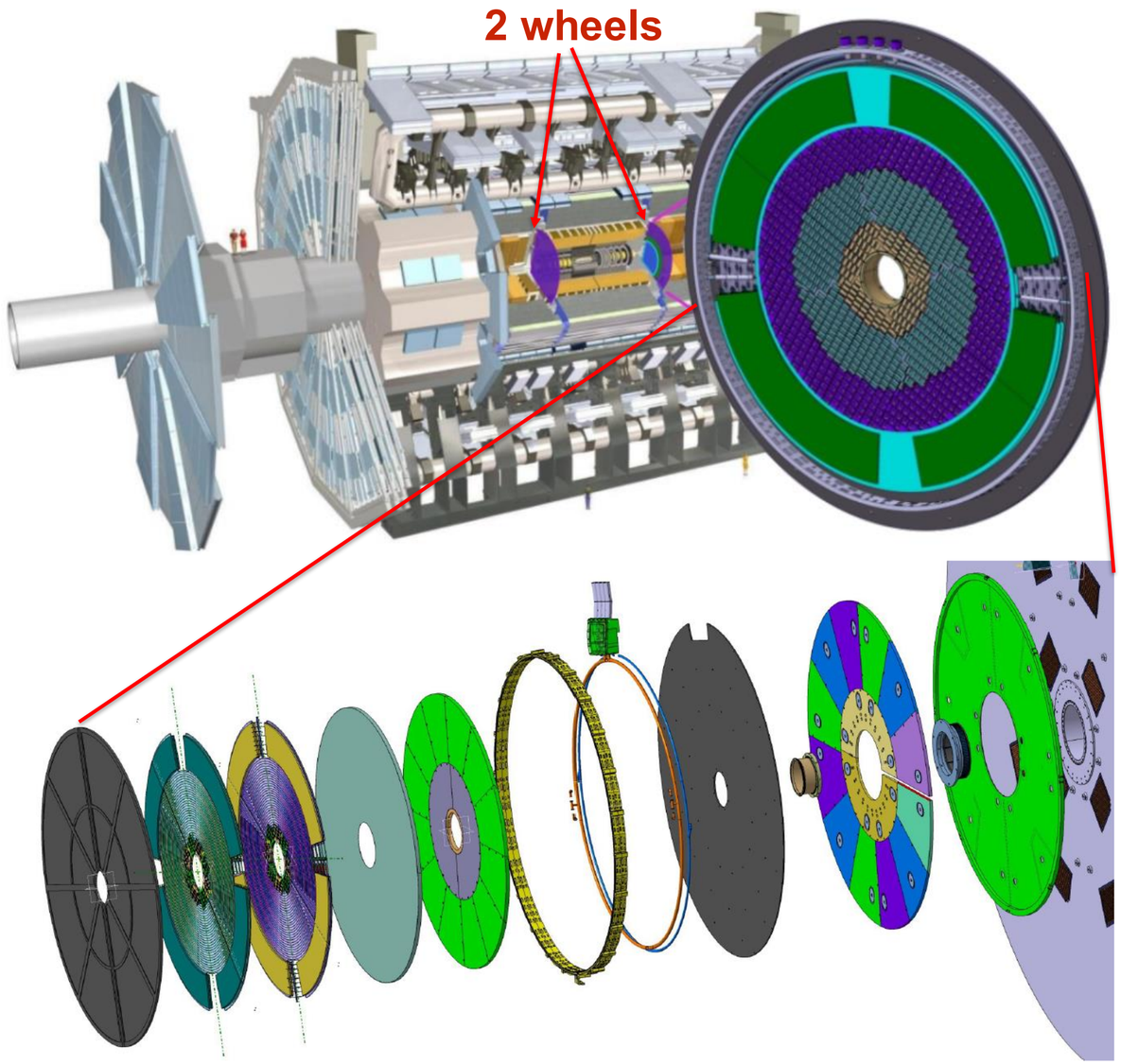
The High Granularity Timing Detector



- Pixel detector with coarse spatial resolution but **precision timing**

Time resolution target

σ_t ~ 50-70 ps/hit, 30-50 ps/track up to 4000 fb^{-1}

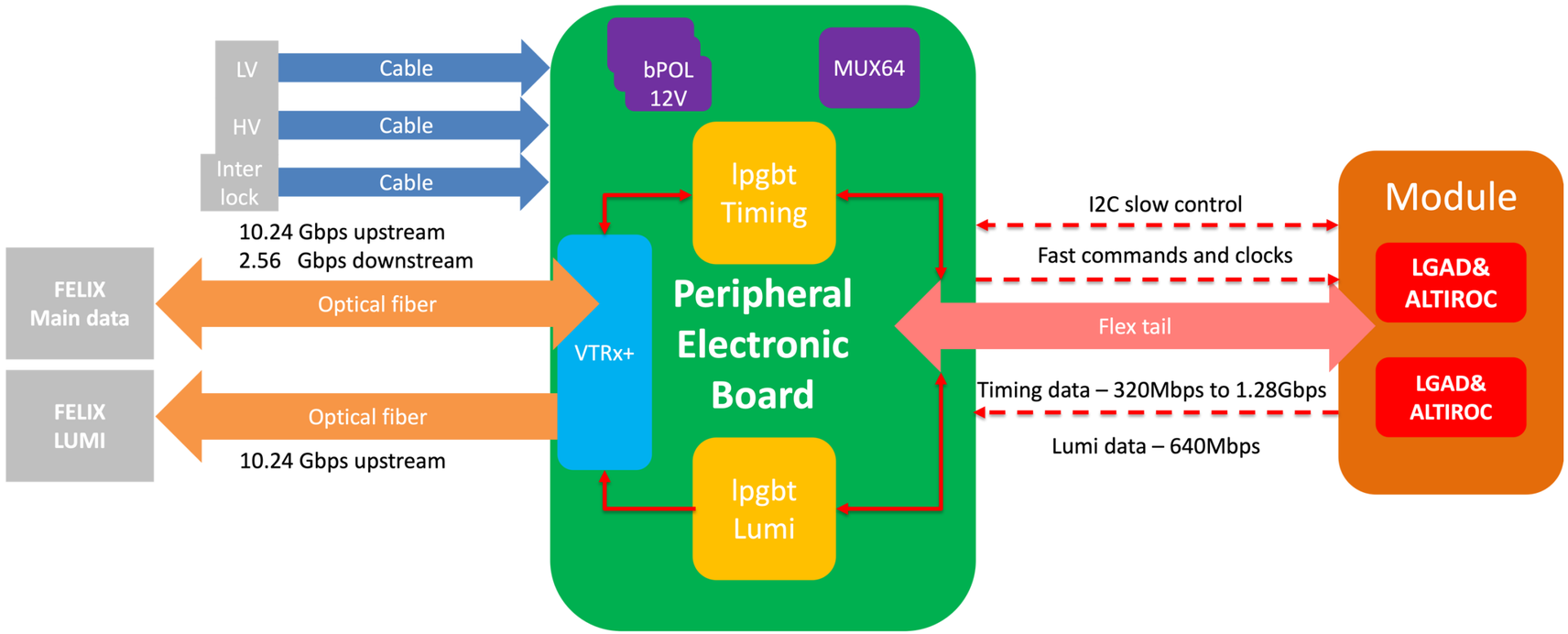
Luminosity measurement

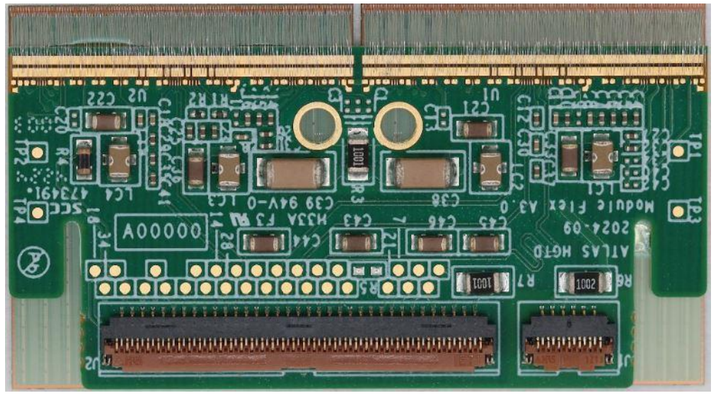
bunch-by-bunch

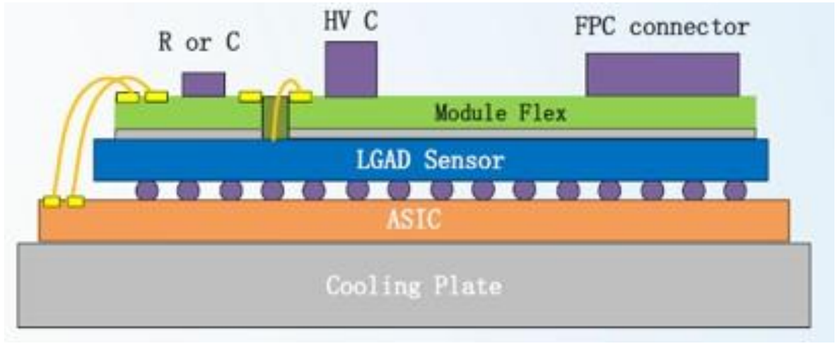
- Active region
  - Position in Z from IP: $\pm$ 3.5 m
  - Pseudorapidity coverage: 2.4 <|η|< 4.0
  - Radial extension: 12 cm < R < 64 cm

- 8032 modules with 2 ASICs and 2 sensors
- 6.4m^2 active area and 3.6M channels
- Up to 2.5×10^{15} n_{eq}/cm^2 , 2 MGy TID

Demonstrator

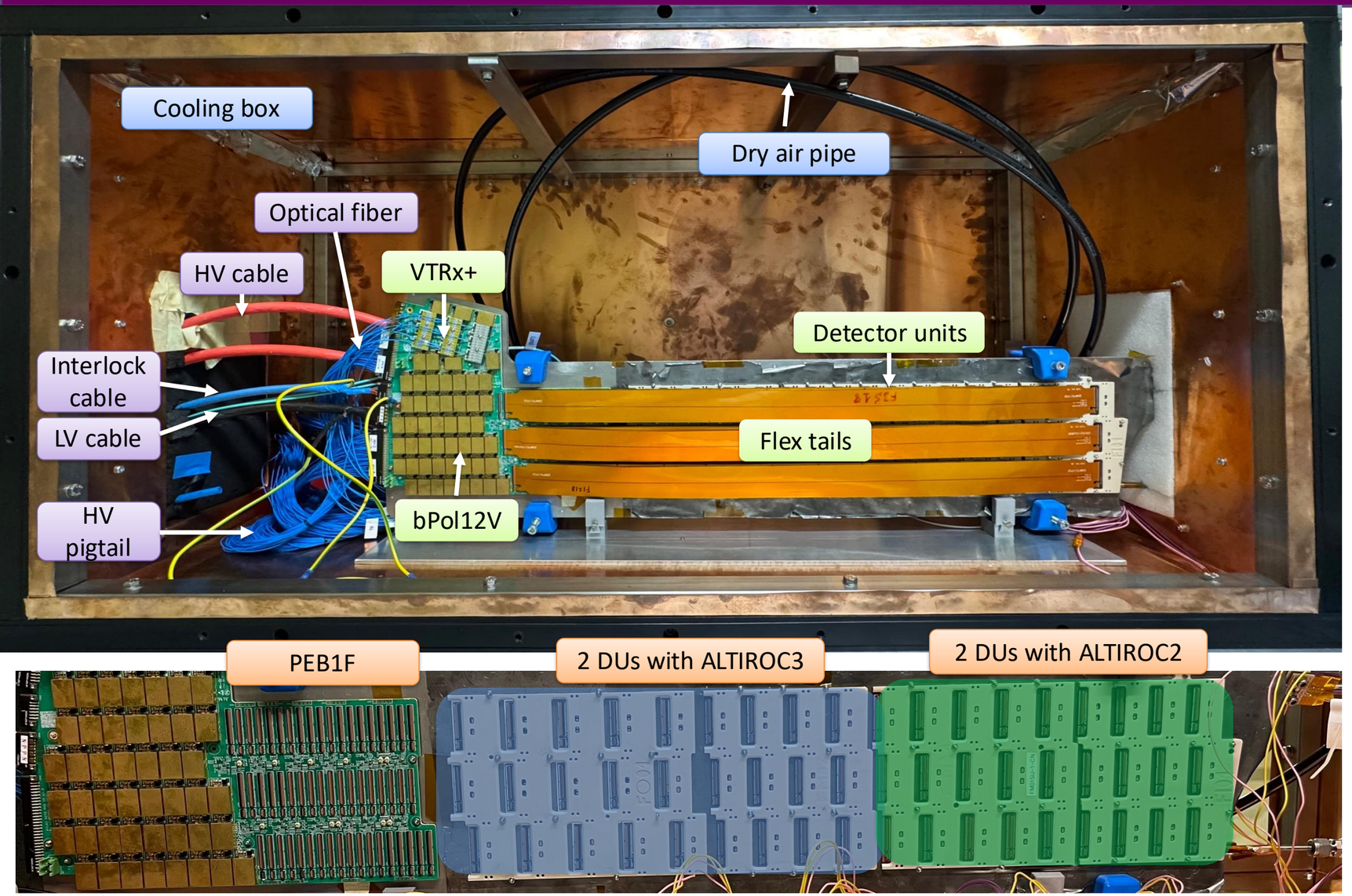






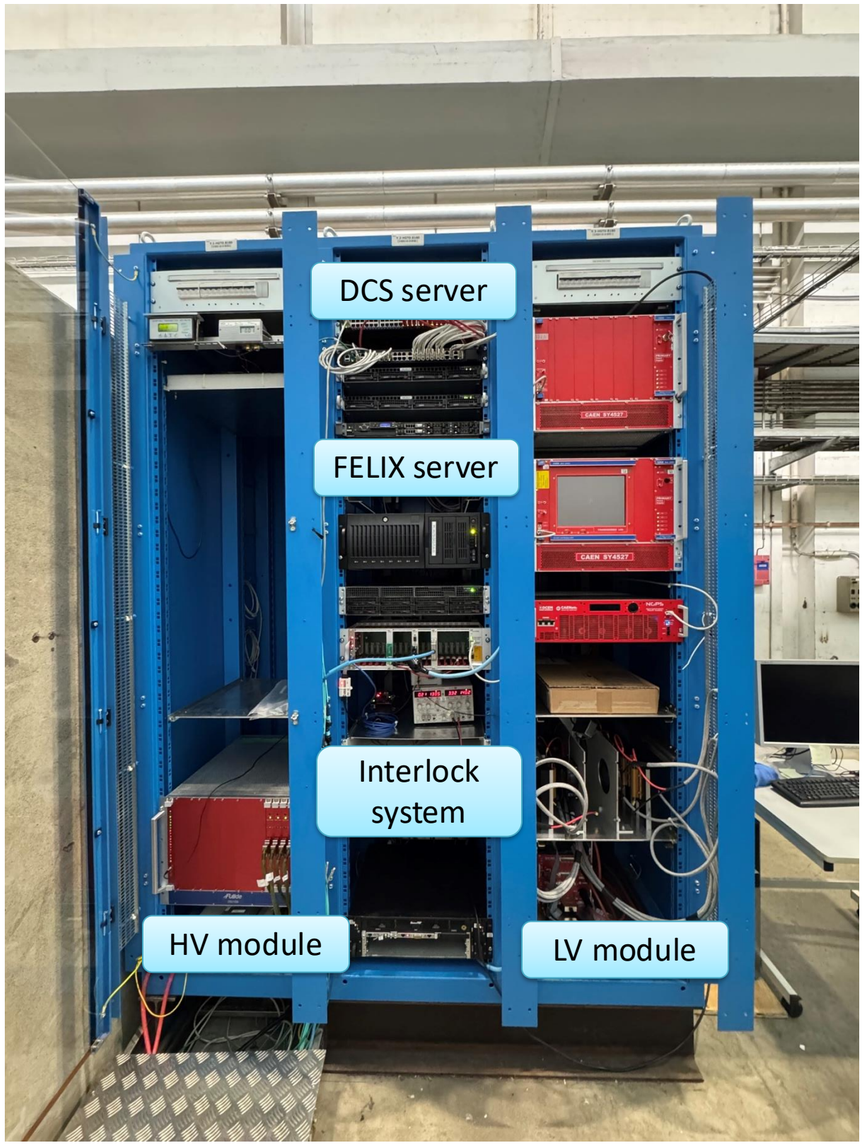
- Represent one slice of detector
  - A prototype system incorporating all key components of the HGTD project
- FELIX
  - A Readout system of the ATLAS experiment
- Peripheral Electronic Board (PEB)
  - Components: low-power GigaBit Transmission chip (lpGBT), Versatile Link + Transceiver (VTRx+), 12 V to 1.2 V DC-DC converters (bPOL12V), etc.
- Module
  - Consist 2 ALTIROC and 2 LGAD
  - Module flex on the top

Demonstrator



- Peripheral Electronic Board (PEB) 1F:
  - Connects up to 55 ALTIROC modules
- Four Detector Units (DU):
  - Several modules make up a DU
  - 27 ALTIROC2 and 27 ALTIROC3 modules individually
- Minimum slice of the detector to have full test

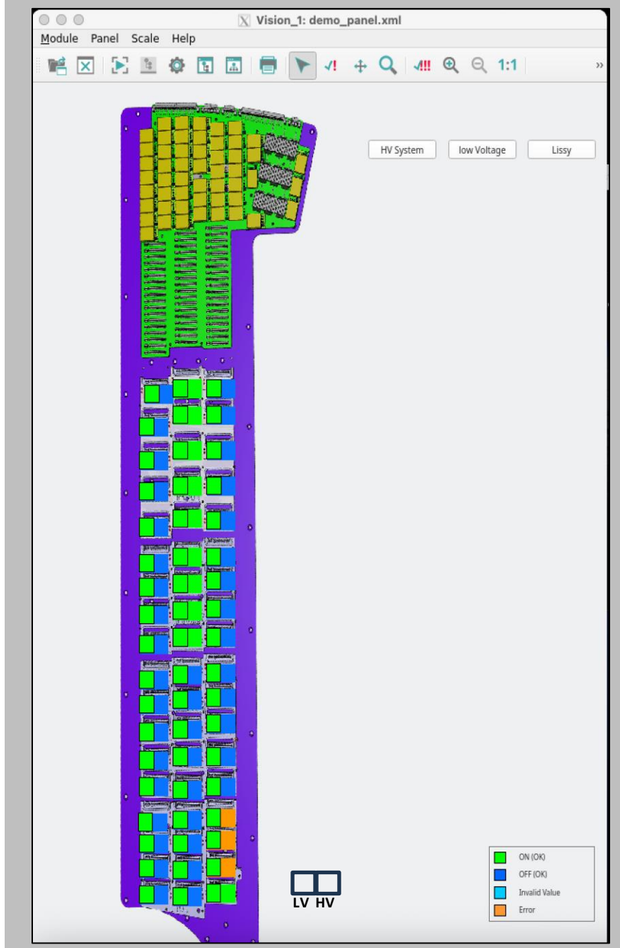
Demonstrator



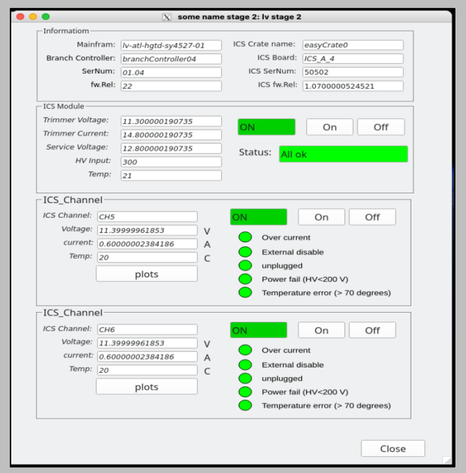
- LV module: connect to pre-production HGTD LV system (BRIC modules from CAEN)
- 4 HV modules connecting to the PEB
- Interlock system has been integrated and tested successfully
- FELIX server used for data taking
- Detector Control System (DCS) used for controlling and monitoring LV, HV and Interlock

DCS panel

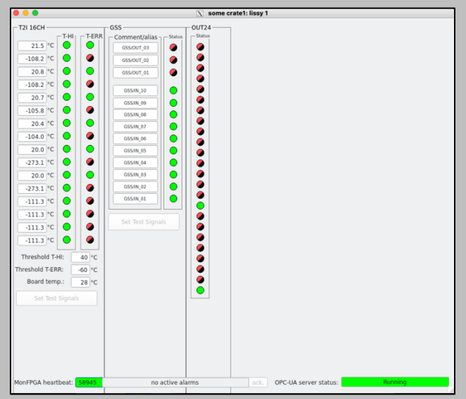
Main DCS panel



Low voltage



Lissy



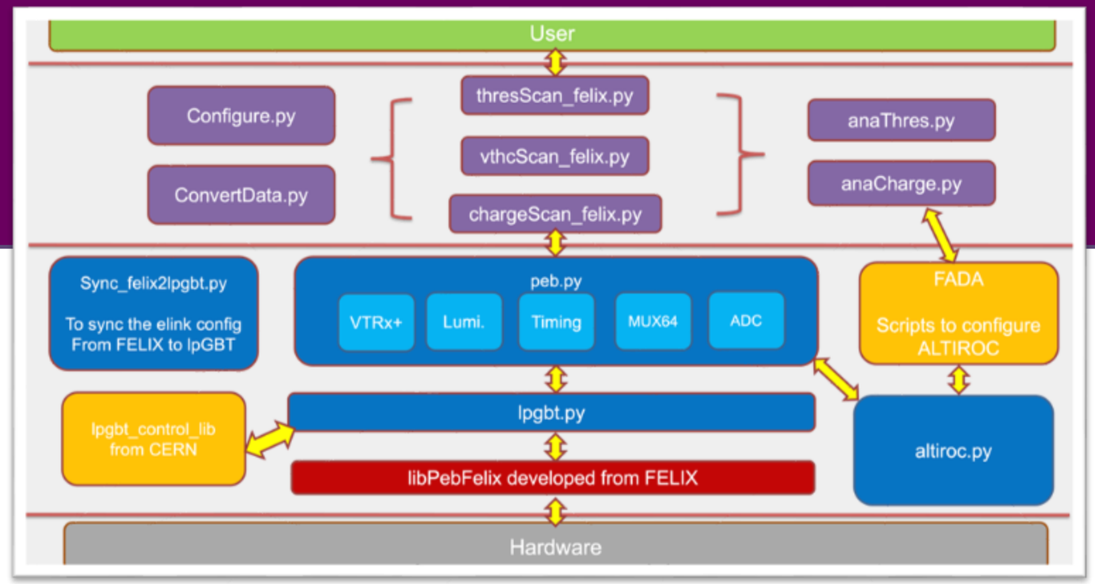
HV System

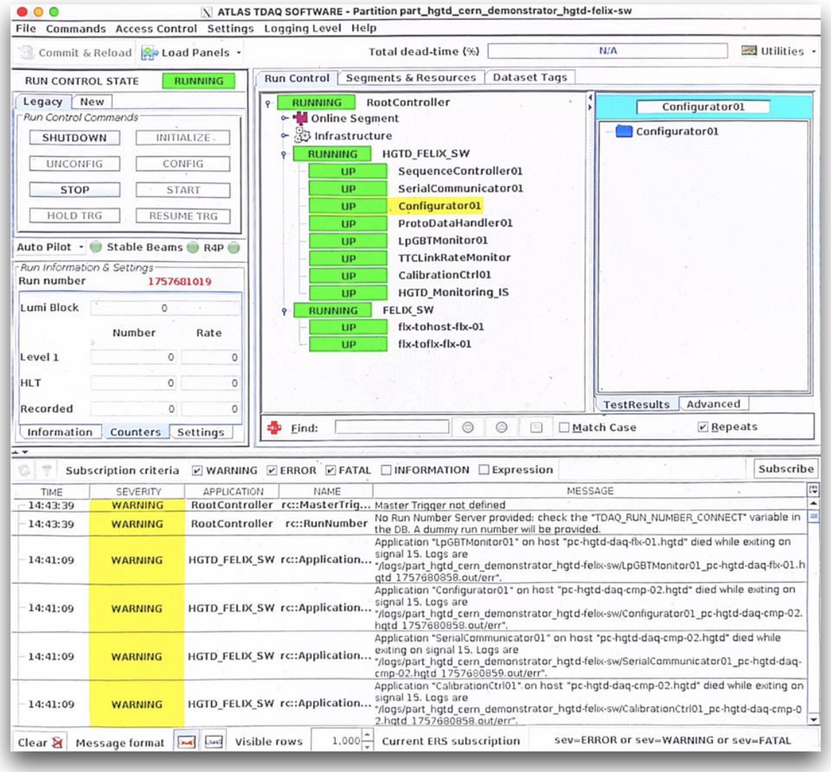
- Use DCS panel to control LV, HV and Interlock
- LV:
  - 2 LV channels for demonstrator
- HV:
  - Individual channel for each ALTIROC module
- Interlock:
  - PEB1F has 6 ALTIROC modules connected to interlock
- All collected information saved into database for future reference

Software

- Script template
  - Python-based scripts used for temporary tests
  - Will be replaced by Standard Trigger and Data Acquisition (TDAQ) system

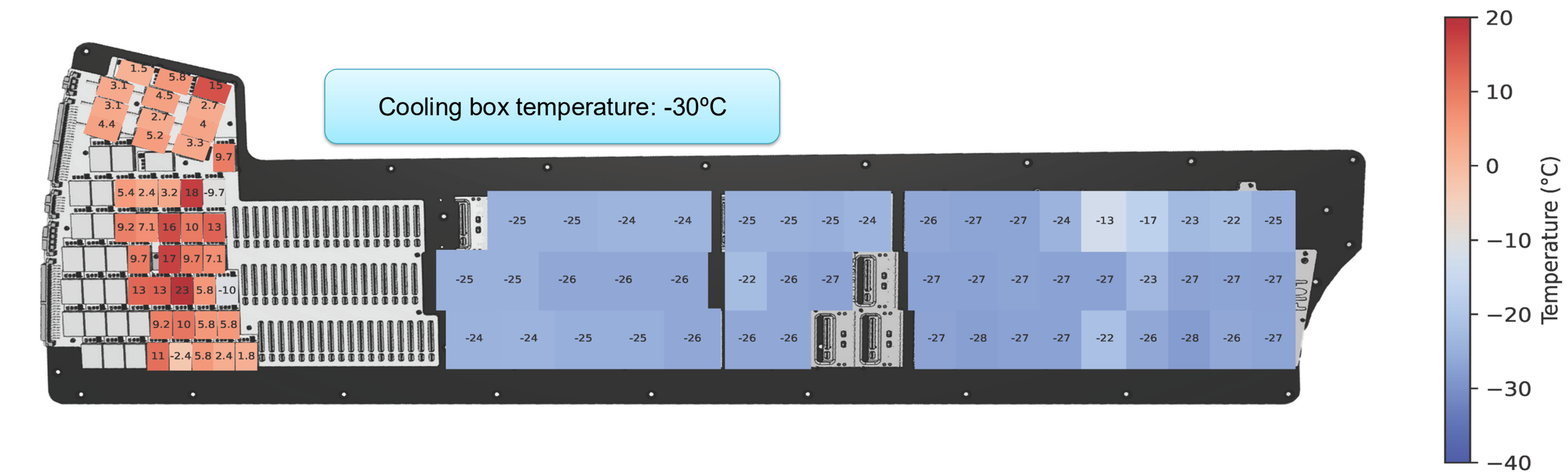
- TDAQ software
  - Still work in progress
  - Use partition to monitor the status of TDAQ system
  - Use web-based Grafana to monitor the status of demonstrator





Temperature measurement

- Temperature on the whole demonstrator measured via NTCs sensors or internal sensors



- Left side: VTRx+ and bPOL12V, some bPOLs cannot be monitored due to limited number of read-out channels → higher temperature due to self heating
- Right side: NTC on each module flex, some of them are broken

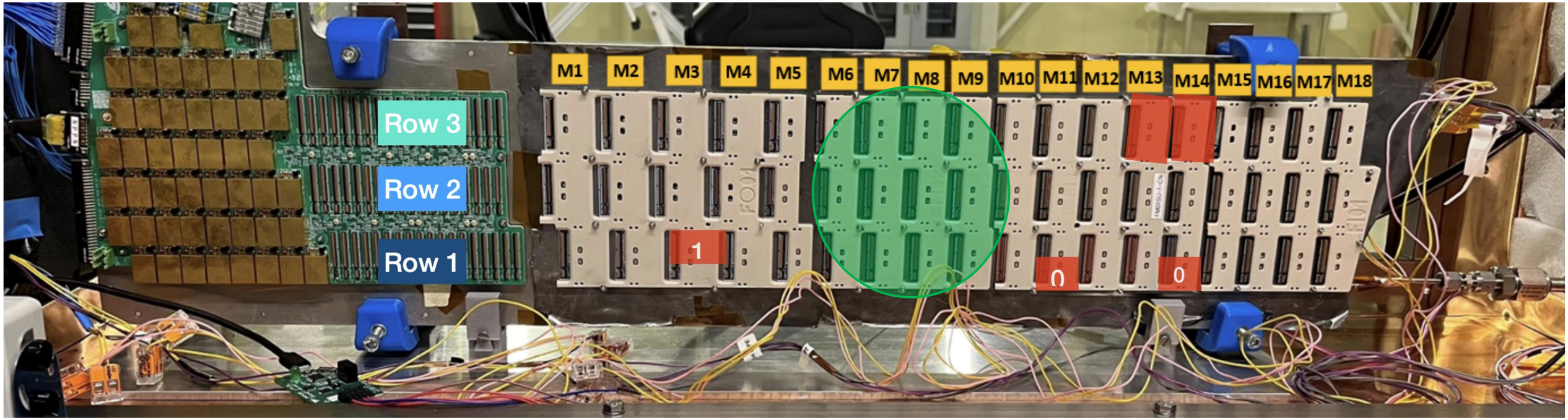
Comprehensive tests on modules

- A full chain for testing modules on demonstrator:

I2C test	Make sure ASIC is working
Vth scan	Find an average value for Voltage threshold (can be used for bump connection check)
Vthc scan	Find specific Voltage threshold for each pixel with a dedicated value of charge injected
Charge scan	Measure hit efficiency, TOA and TOT
Delay/Width scan	Measure TOA/TOT LSB

Results – I2C connection

- 101/108 ALTIROCs pass I2C connection test
- The best DU (in green circle) has all ALTIROC3s working and produces good results



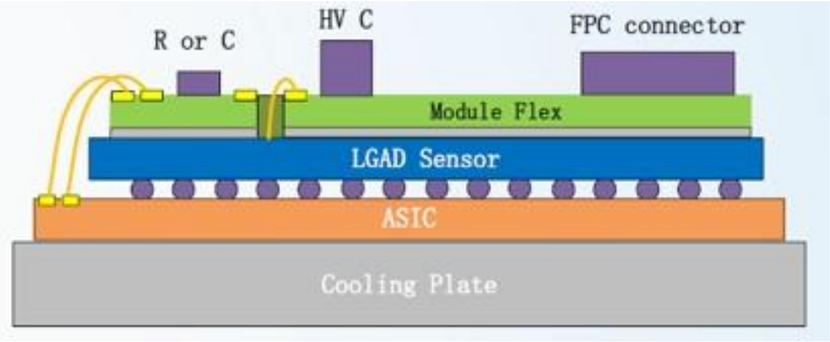
- Red boxes indicate the ALTIROCs fail the I2C connection test

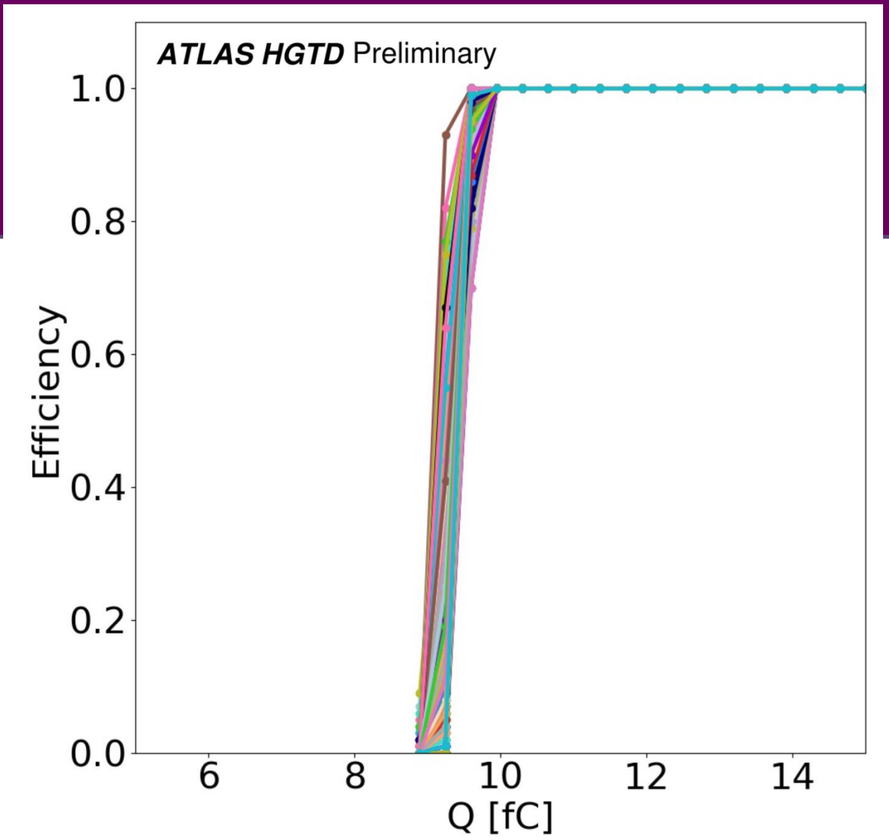
Hit efficiency of one ALTIROC

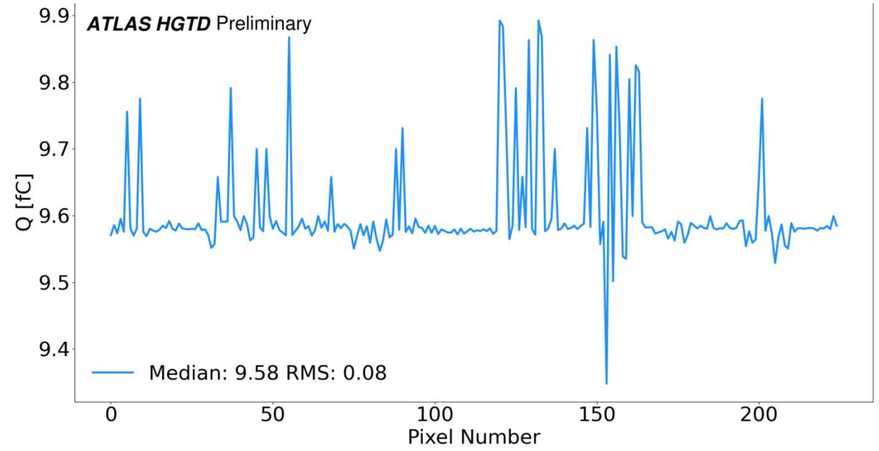
➢ Hit efficiency plot:

- Measured at -30ºC on module Row3M8C0 without HV
- Data transfer speed: 320Mbps
- Using Vthc value produced with Injected Q=9.6fC
- Pixels found a threshold at Q = 9.58 fC

- With expected median value and low RMS, this ALTIROC shows a good hit efficiency





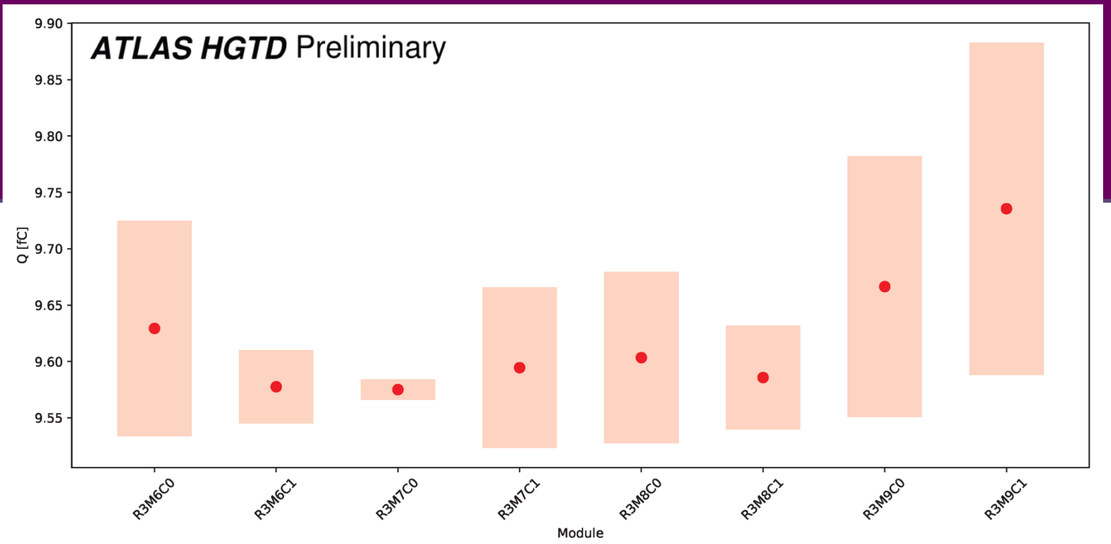


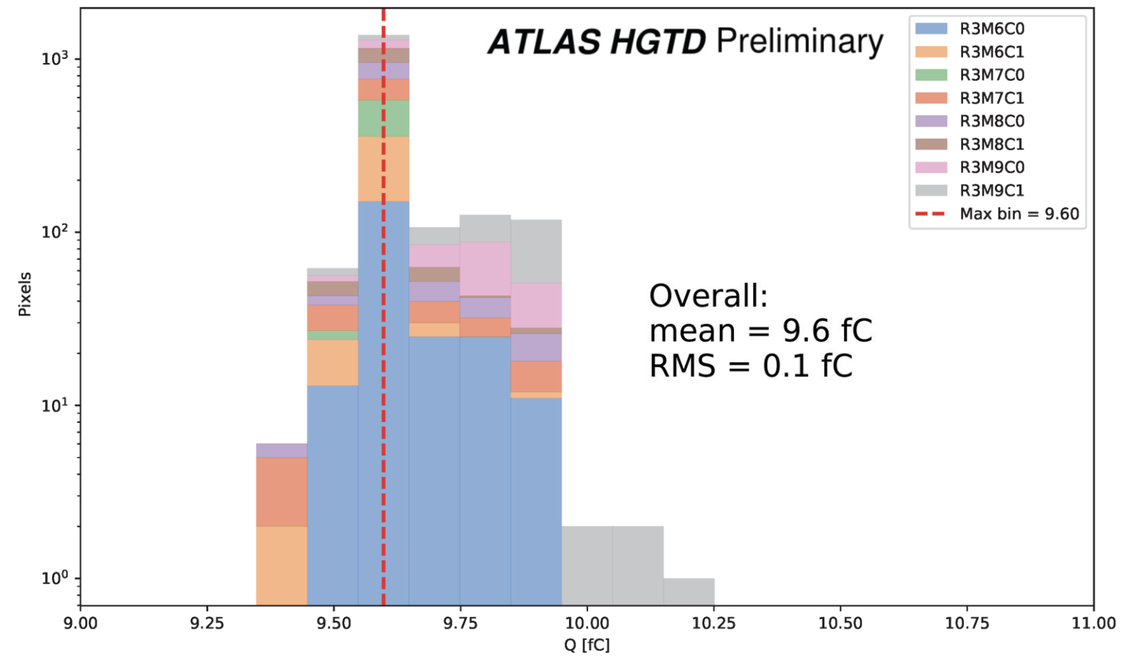
Hit efficiency of several modules

- Hit efficiency for **multiple modules**

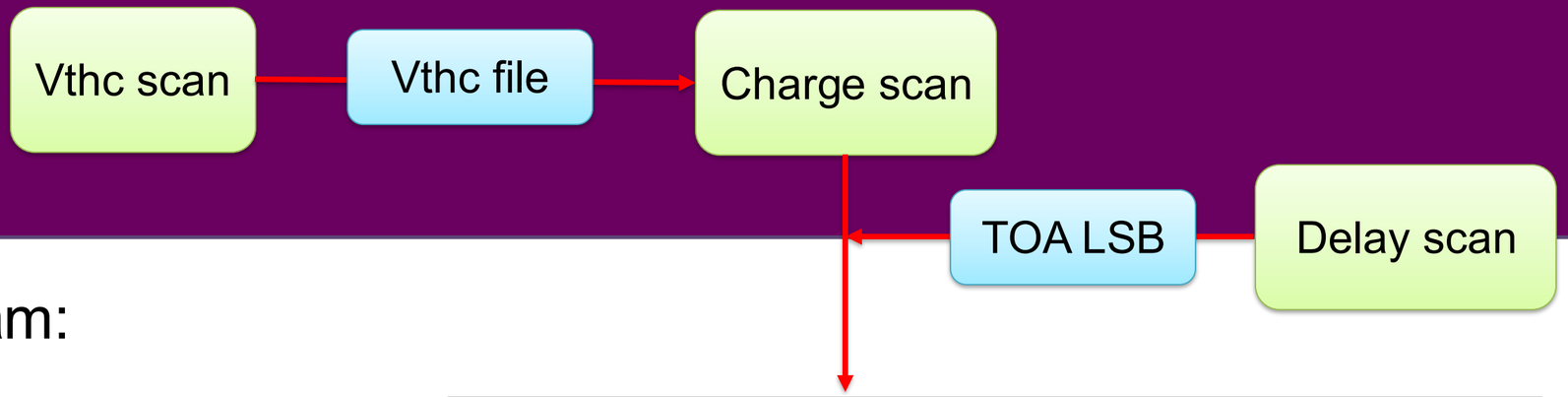
- Measured at -30ºC on Row3 without HV
- Data transfer speed: 320Mbps
- Most ASICs have a median value around 9.6fC
- Still slightly differ from one to one

- Stacked histogram shows 9.6fC still the central value, with acceptable RMS



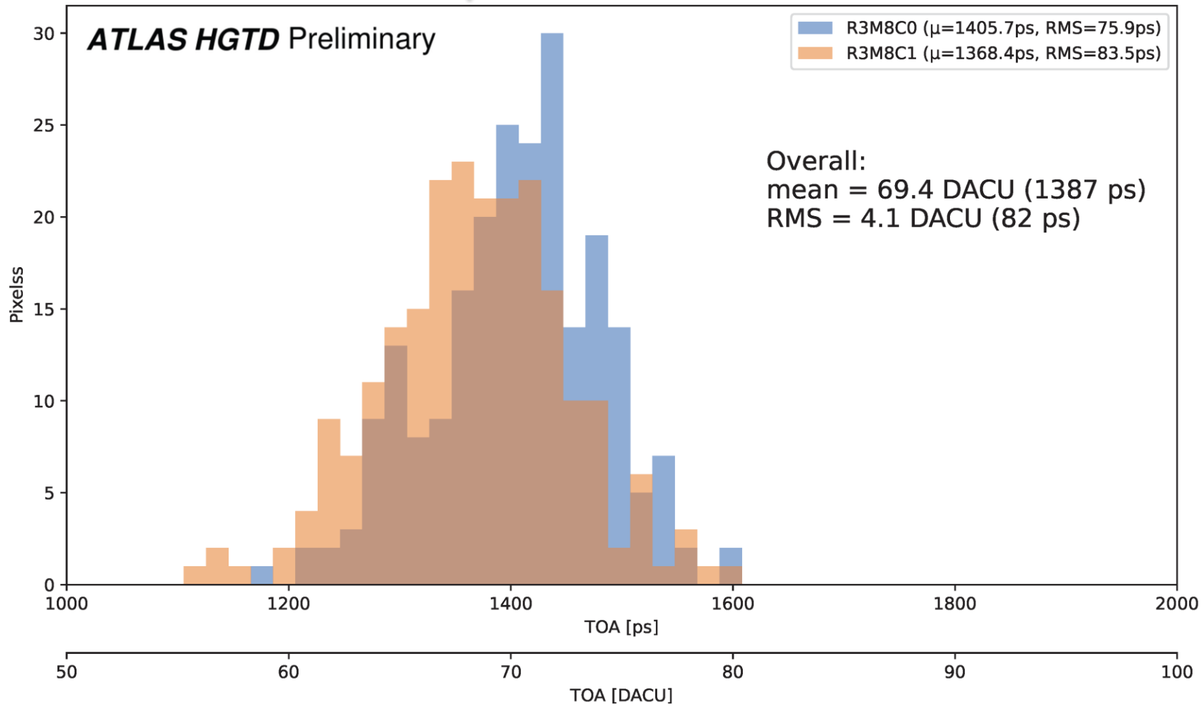


TOA



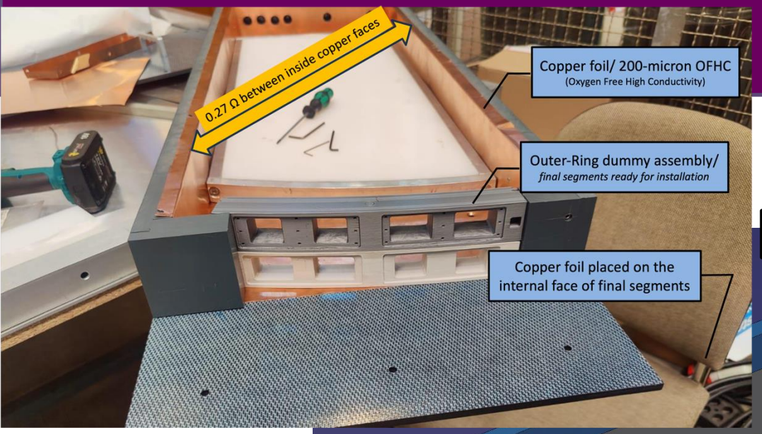
➢ Time of Arrival (TOA) histogram:

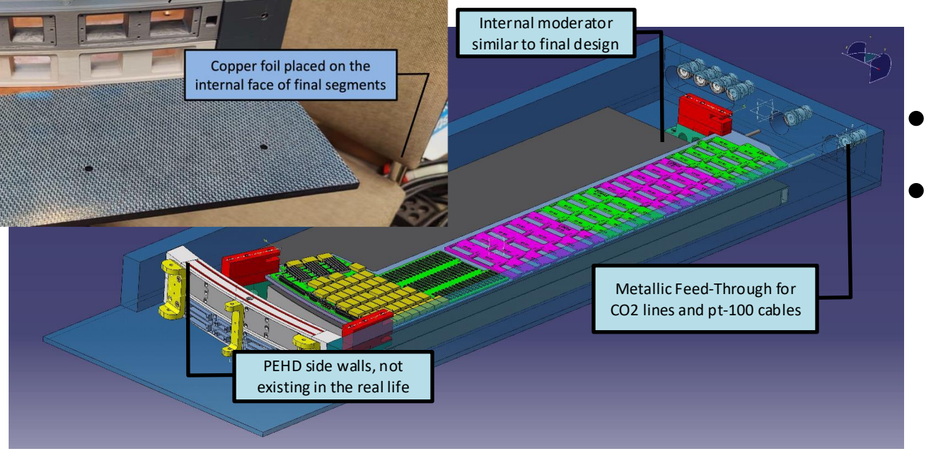
- Measured at -30ºC on Row3M8 without HV
- Data transfer speed: 320Mbps
- TOA LSB measured via DelayScan is around 20 ps
- Two ALTIROCs on the module show good agreement in TOA distribution, with an acceptable mean value at 1387ps



- 82 ps RMS
  - Skew of clock distribution system
  - Skew of used calibration pulse which is distributed to all the pixels through a clock tree (±75 ps by design)

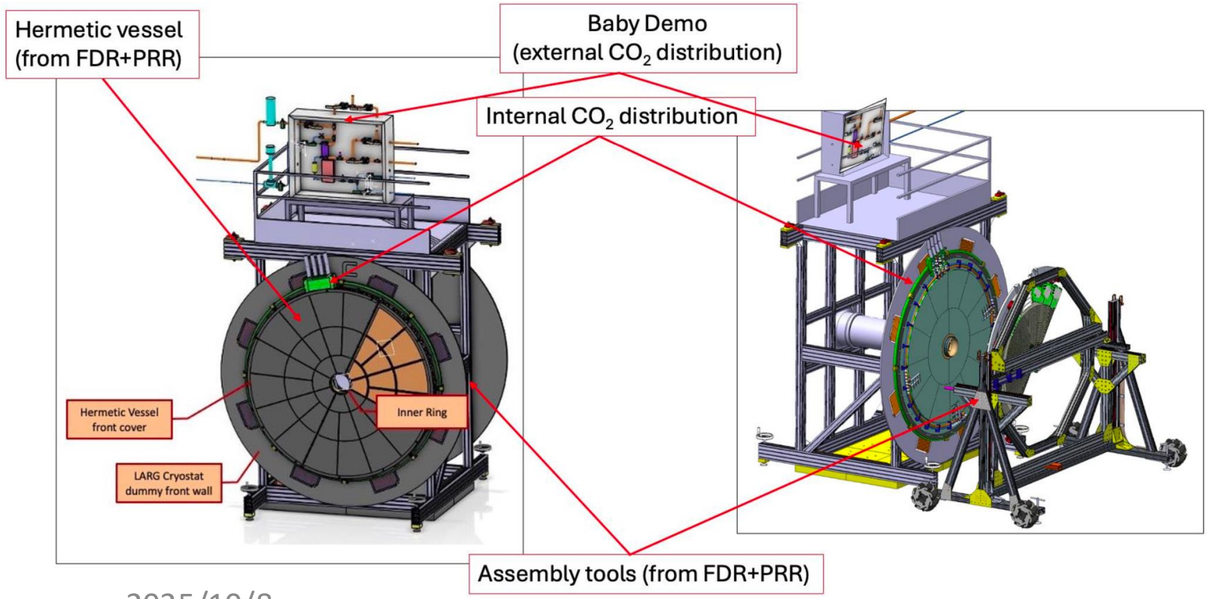
Towards the future





➢ Second generation box:

- New cooling box, new PEB and ALTIROCA DUs
- Expect to be in place by the end of this year



➢ Module-0:

- A quarter of back side of HGTD wheel
- Demonstrate that HGTD individual items are ready to pass to the production phase
- Integrate and test 3% of the HGTD active components

Summary

- A comprehensive full-power testing has been carried out on HGTD demonstrator
- The full read-out chain has been tested successfully
- DCS also successfully used to monitor and control demonstrator operation
- A brand-new ATLAS standard DAQ is in progress and already in good shape and will replace the current python scripts
- Various measurements have been carried out on demonstrator
  - Temperatures on the whole demonstrator are reasonable
  - ALTIROCs show hit efficiency and noise as expected
  - ALTIROCs show expected TOA distribution and RMS within one module

Thank you!

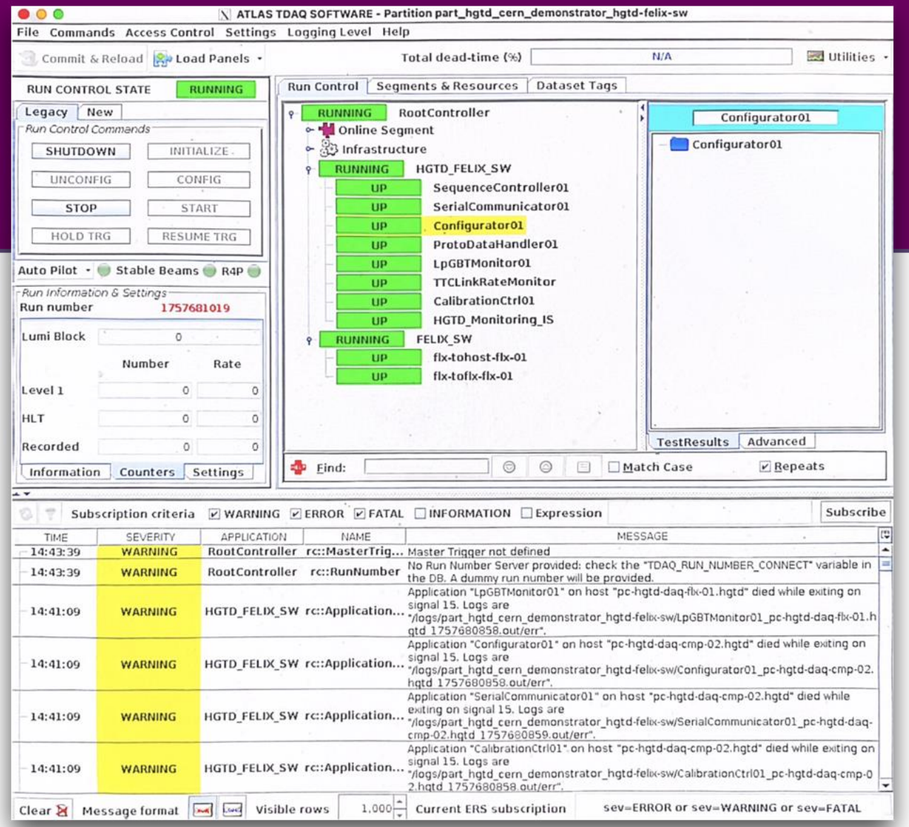
Backup

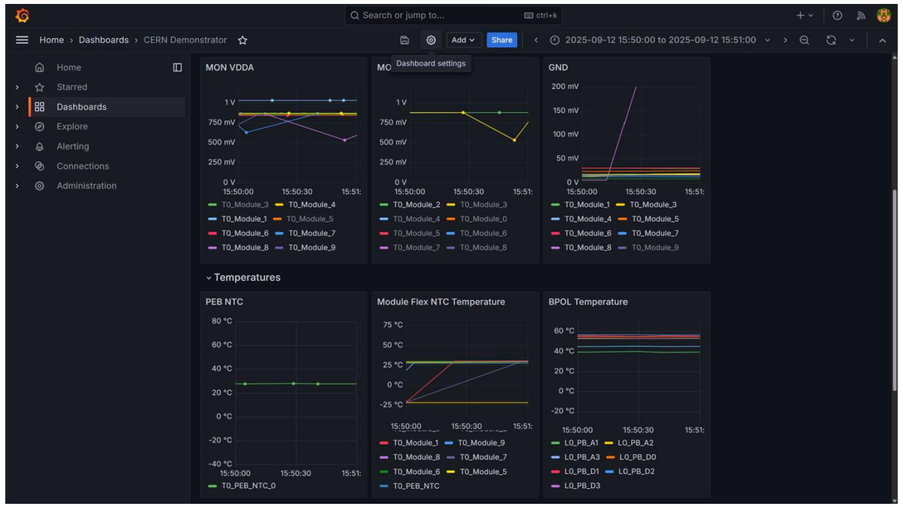
Software – HGTD_FELIX_SW

- Software: still work in progress

- Use partition to monitor the status of TDAQ system
- Shows different component of this software

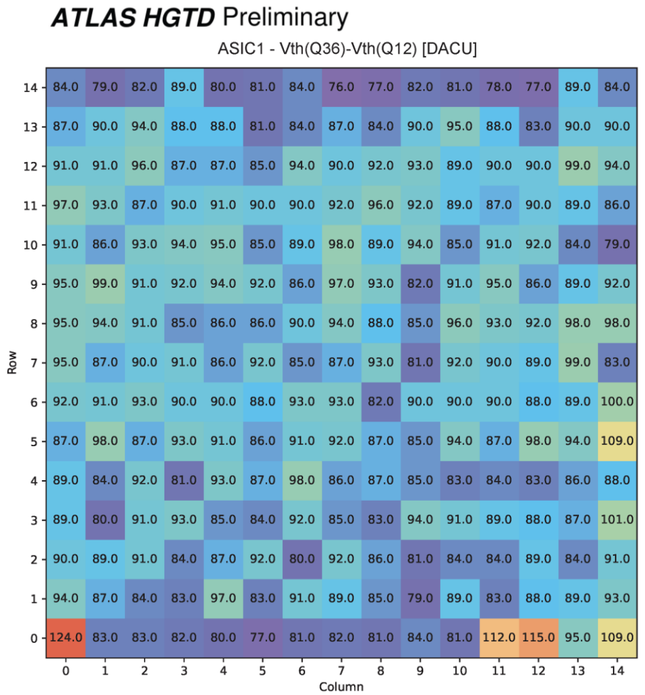
- Use web-based Grafana to monitor the status of demonstrator
- Monitoring VDDA, VDDD and GND for each ALTIROC as well as all the temperature information

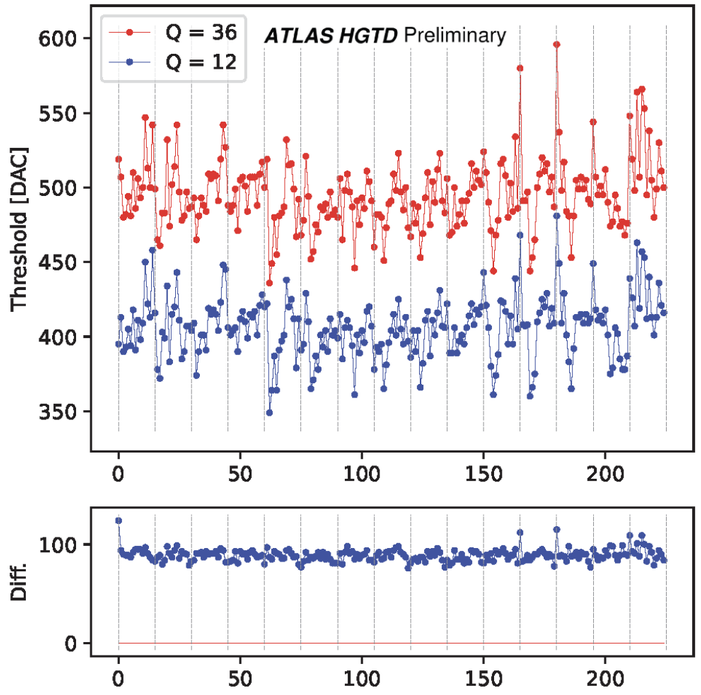




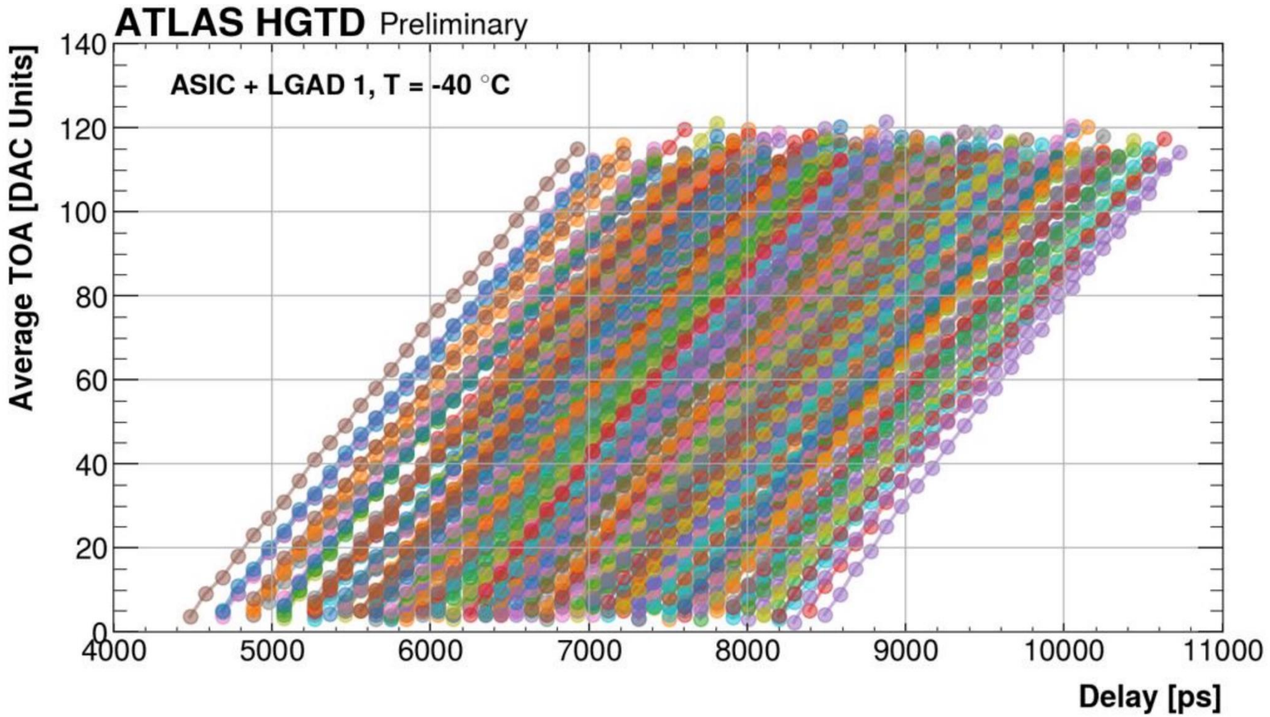
Results – bump connection

ASIC bump connection plot produced with demonstrator cooled down to -30° C. High voltage is applied. ASIC number Row1Module1ASIC1. The method used to check the bump connection relies on the difference between the voltage threshold value for two different injected charges (in this example 36 DACU=15 fC and 12 DACU=5 fC). Pixels with disconnected bumps are expected to have a higher difference due to the lower input capacitance. The number in the pixels map and the histograms represents this difference. To be noted that pixel (0,0) is not connected by design and it can be used as reference. This example shows that, in addition to pixel (0,0) , pixel (0,11) and (0,12) are clearly disconnected while pixel (5,14) and (0,14) might be (and should be cross-checked with a different method).





TOA LSB



Average Time Of Arrival (TOA) measured with the TDC as a function of the programmable delay using direct injection of a digital discriminator pulse at the input of the TDCs. Each curve belong to one single channel of the matrix. The TOA bin (LSB) is extracted from the linear fit