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Progress on ACTS-based 4D tracking and a design of timing pixel digital chip

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At the future collider High-Luminosity LHC (HL-LHC), the average number of the simultaneous pp interactions per event, or pile-up (μ), will rise to as much as 200. Resolving the pile-ups using time measurement has already been investigated during LHC Phase-Il Upgrade, e.g. the ATLAS High Granularity Timing Detector (HGTD), which will be placed outside the ATLAS Phase-Il Inner Tracker (ITk) endcap region. Meanwhile, the possibility of replacing the inner barrel layers of the ATLAS ITk with 4D pixel detector after Run 4 is foreseen as well. In the first part of the report, we will introduce the implementation of 4D tracking based on the common tracking software (ACTS) workflow. The performance of 4D tracking, e.g. efficiency and resolution, will also be discussed. In the second part, we will present a digital readout chip architecture for 4D pixel detectors, which is designed to overcome a significant increase in data rates resulting from high-precise time of arrival (ToA) information.

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