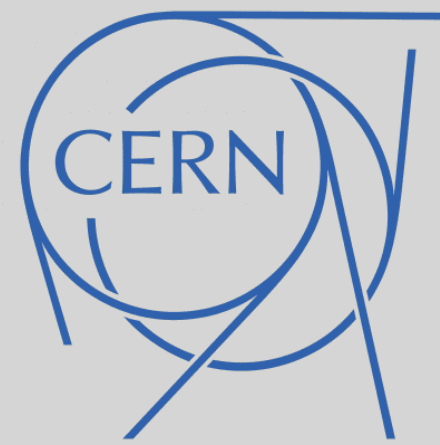




# Status and performance of ALICE FoCal pixel layers

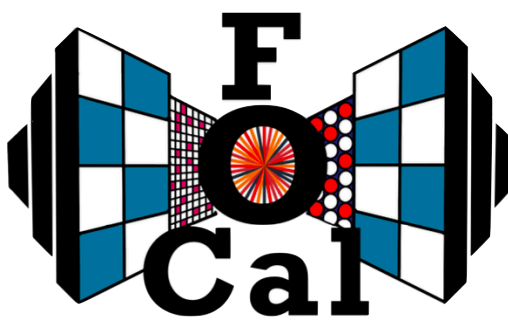
Jie Yi (CCNU)

CLHCP 2025

31/10/2025



# Contents



**Introduction of FoCal**

**FoCal-E pixel layer simulation based on SystemC**

**Data Link**

**Busy Violation**

**Exploring Options to Reduce BUSY Violations**

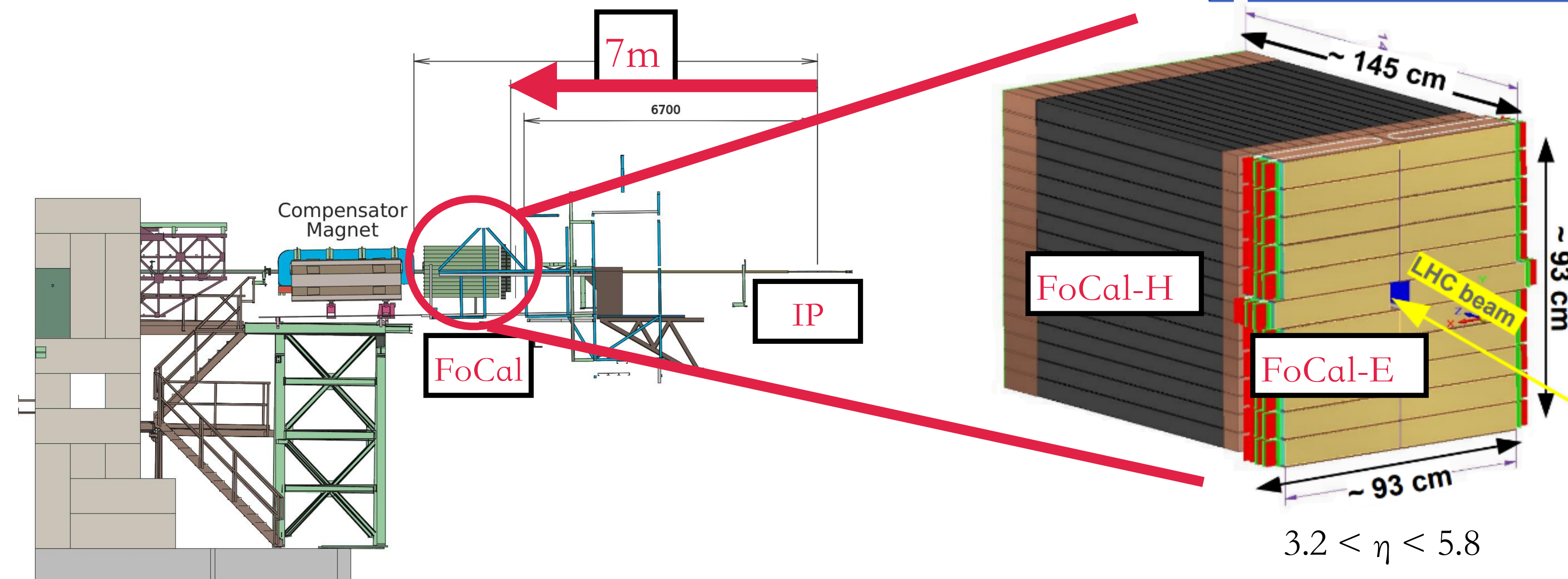
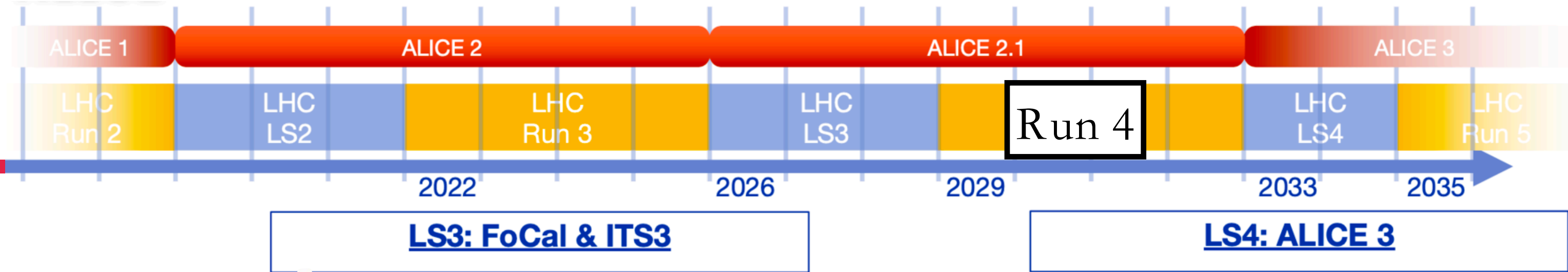
**Regional Trigger**

**Pixel layer module production test**

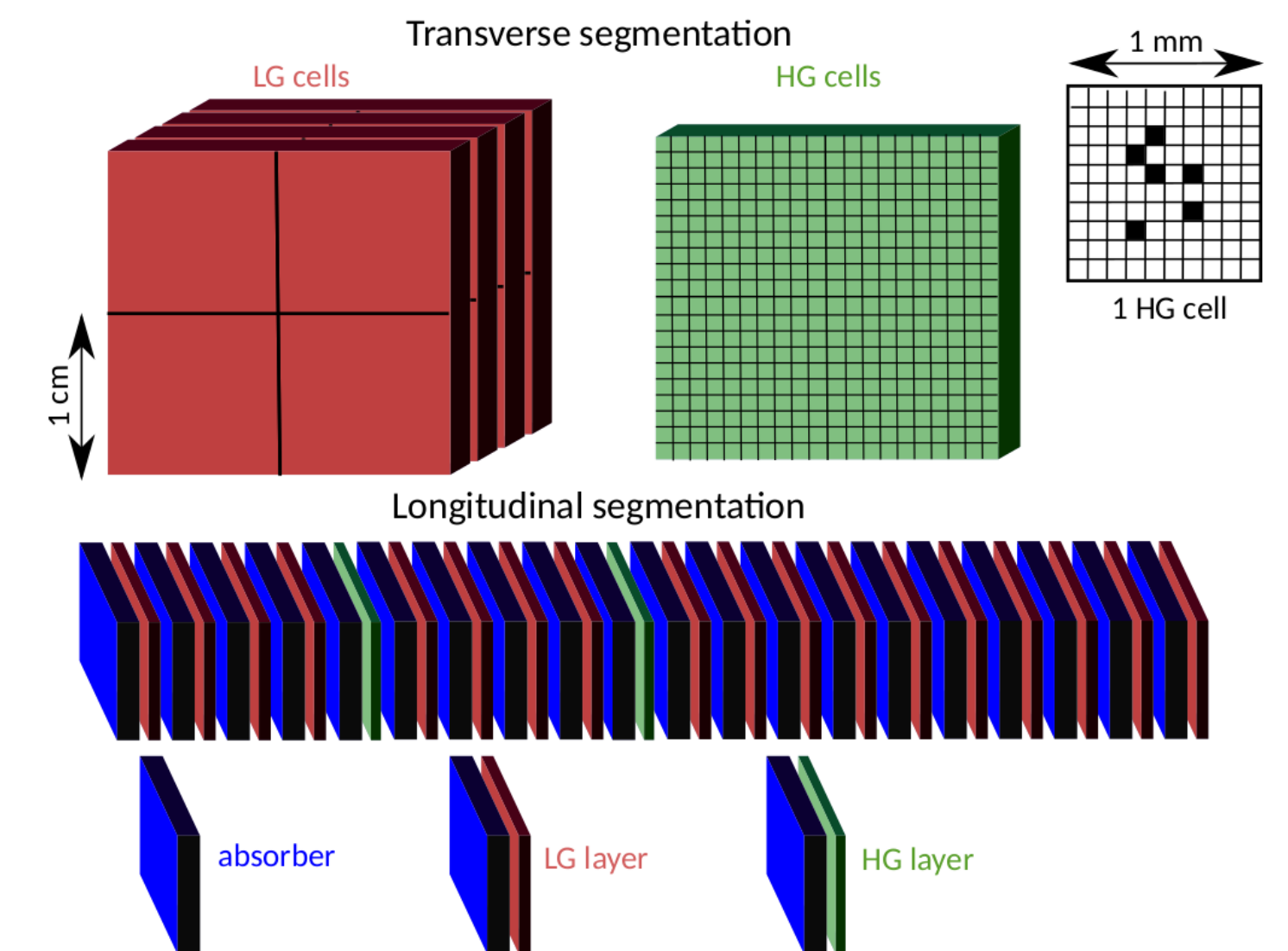




# Overview



- During the LHC LS3 period, ALICE will add a **new** calorimeter detector (**Forward Calorimeter**, FoCal)
  - The TDR was approved by the LHCC in March 2024
- Public Notes & Paper:
- TDR ([CERN-LHCC-2024-004](#))
  - Letter of Intent ([CERN-LHCC-2020-009](#))



## •FoCal-E

- Highly-granular, longitudinally-segmented **silicon-tungsten** (Si+W) electromagnetic calorimeter.
- 18 pad layers ( $1 \times 1 \text{ cm}^2$ ) + 2 pixel layers ( $29.24 \times 26.88 \mu\text{m}^2$ ).
- Designed for detecting **direct photons** and **neutral pions**.

## •FoCal-H

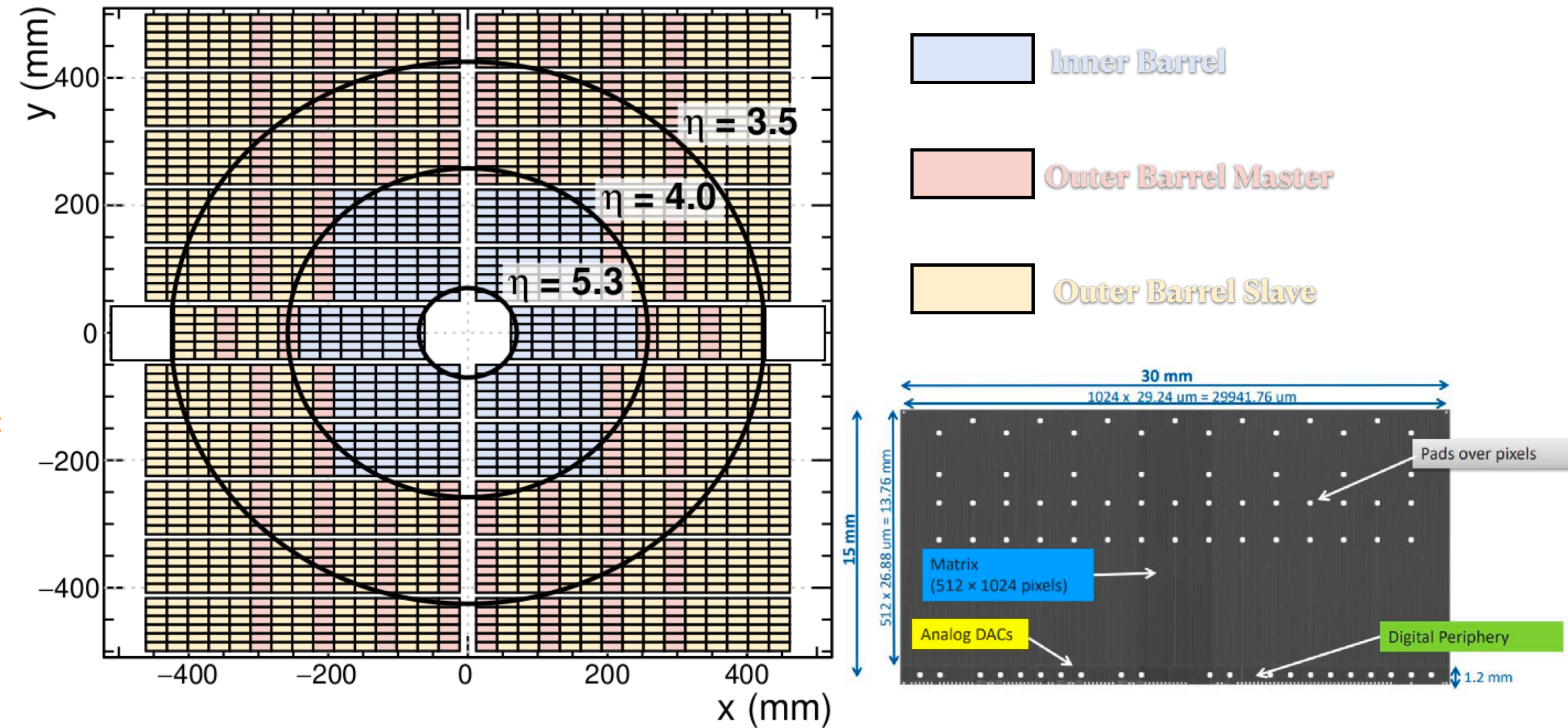
- A metal-scintillator sampling calorimeter ( $0.6 \times 0.6 \text{ cm}^2$ ).
- Constructed from copper grooved plates filled with scintillating fibers.



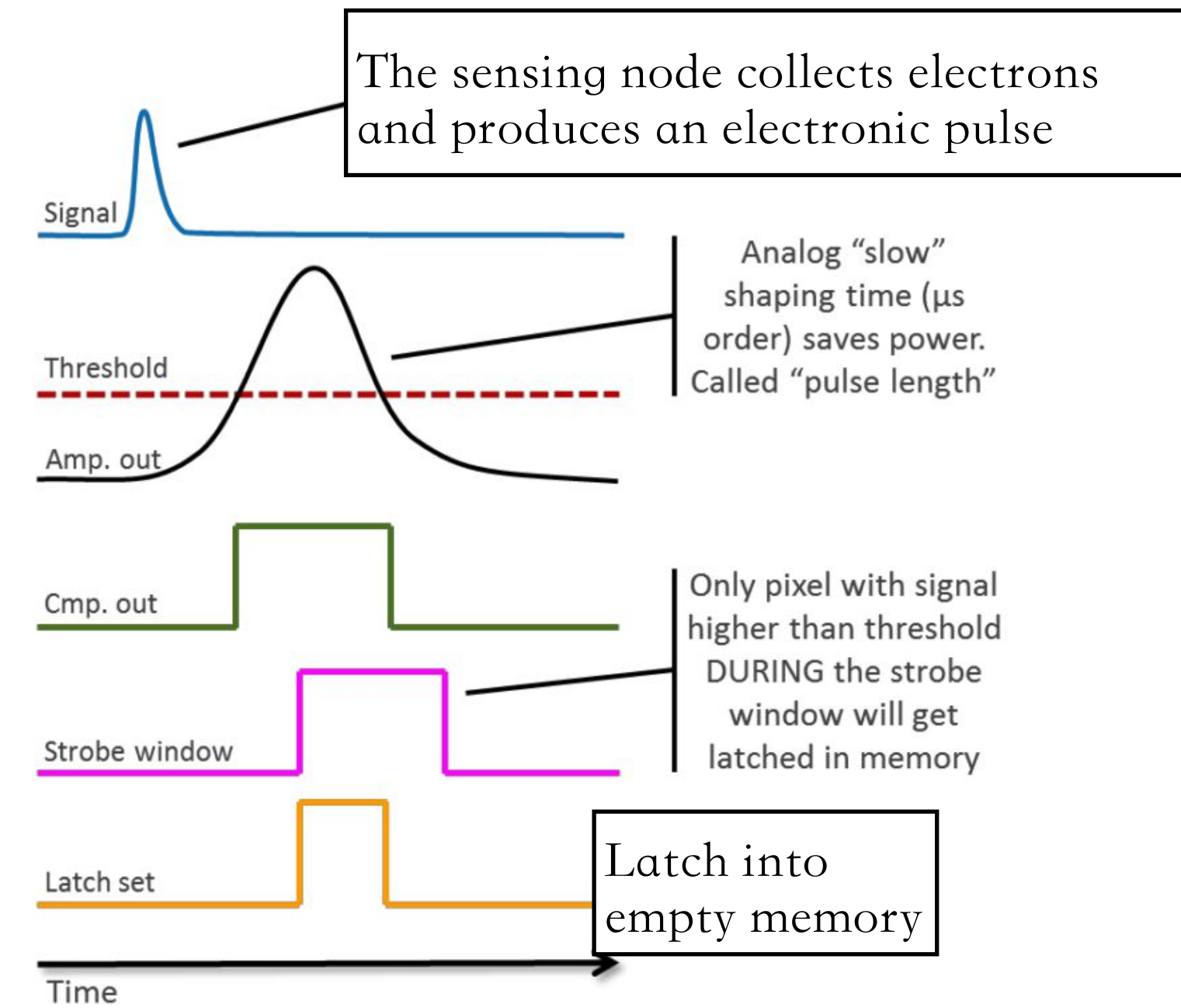
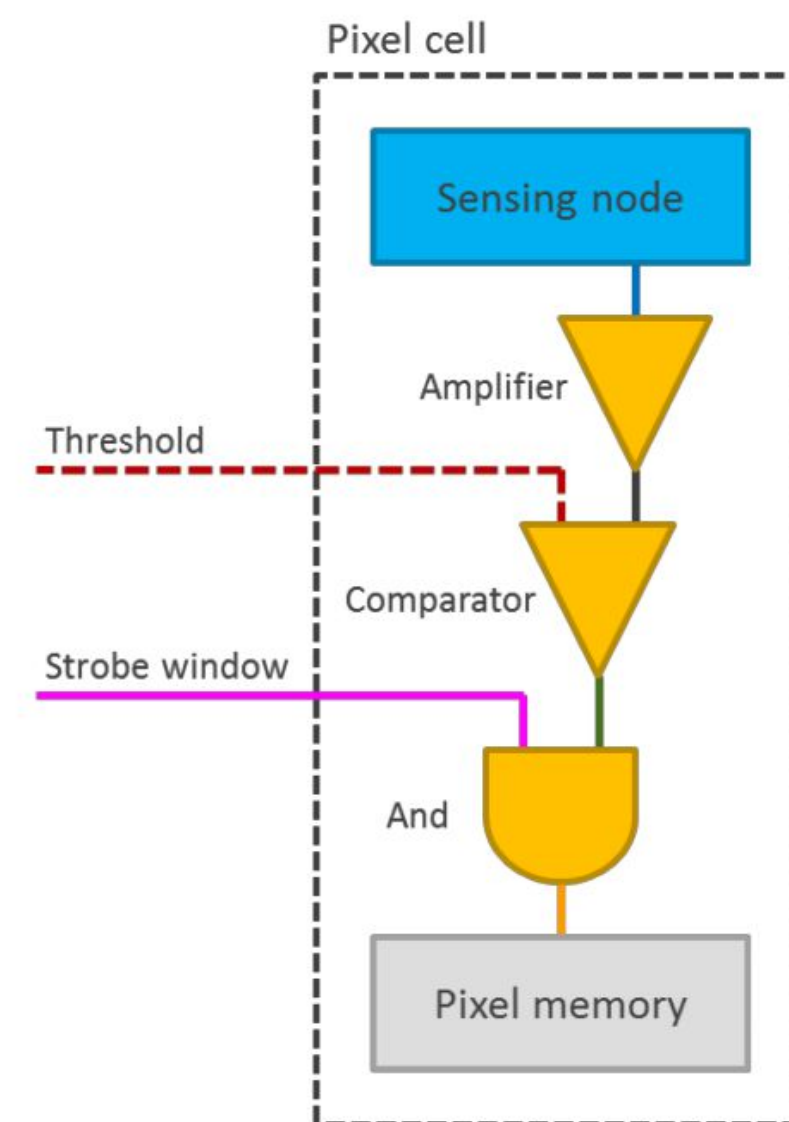
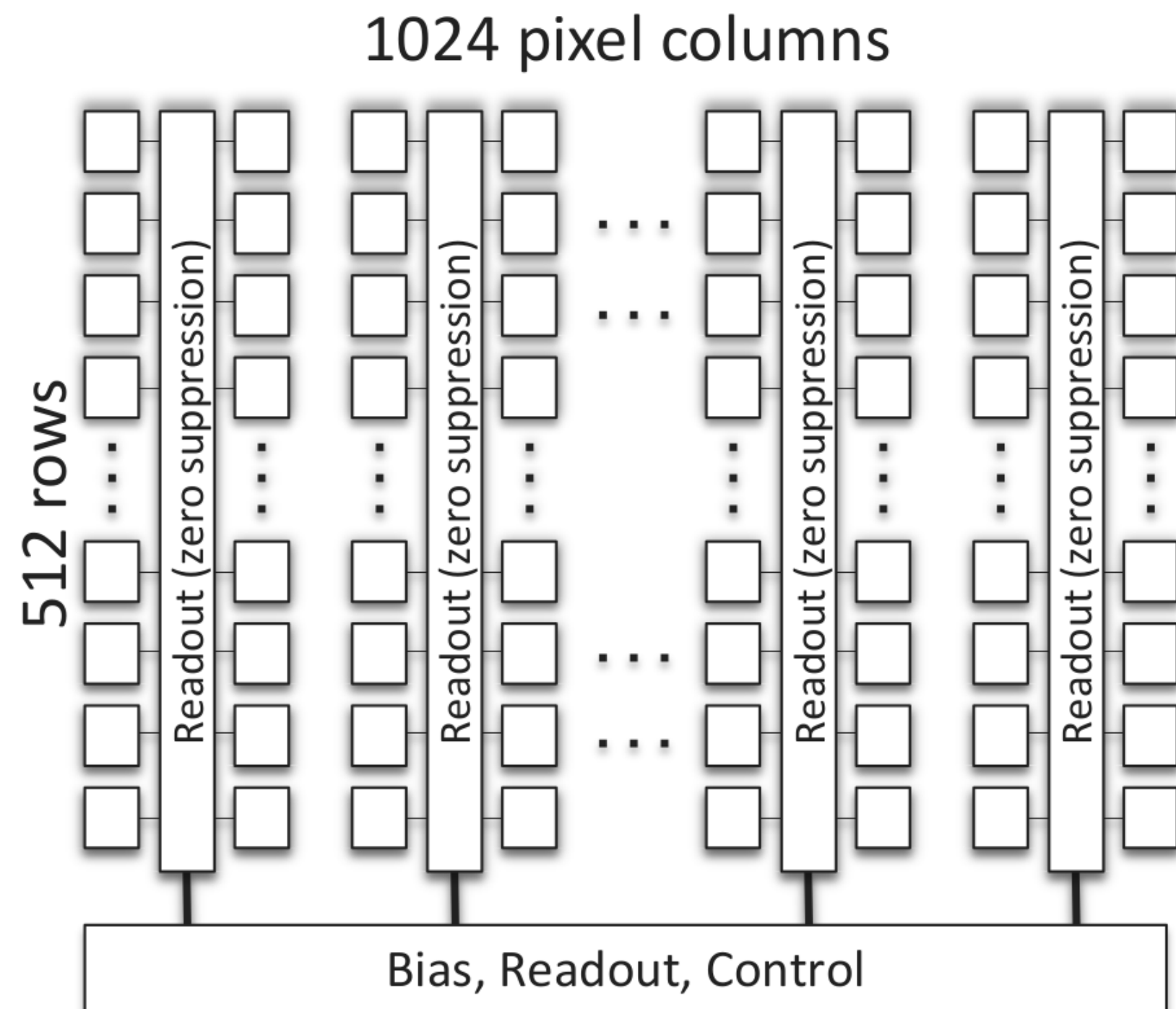
Blue: IB mode

Red: OB master mode

Yellow: OB slave mode



- The pixel layer consists of 22 modules, each containing 6 chip strings.
- The chip strings are divided into Inner and Outer Strings.
- Each string has 15 ALPIDE silicon pixel chips, with a total of 1980 ALPIDE chips per layer.
- Pseudo-rapidity coverage:  $3.2 < \eta < 5.8$ , with full coverage from  $3.5 < \eta < 5.3$ .



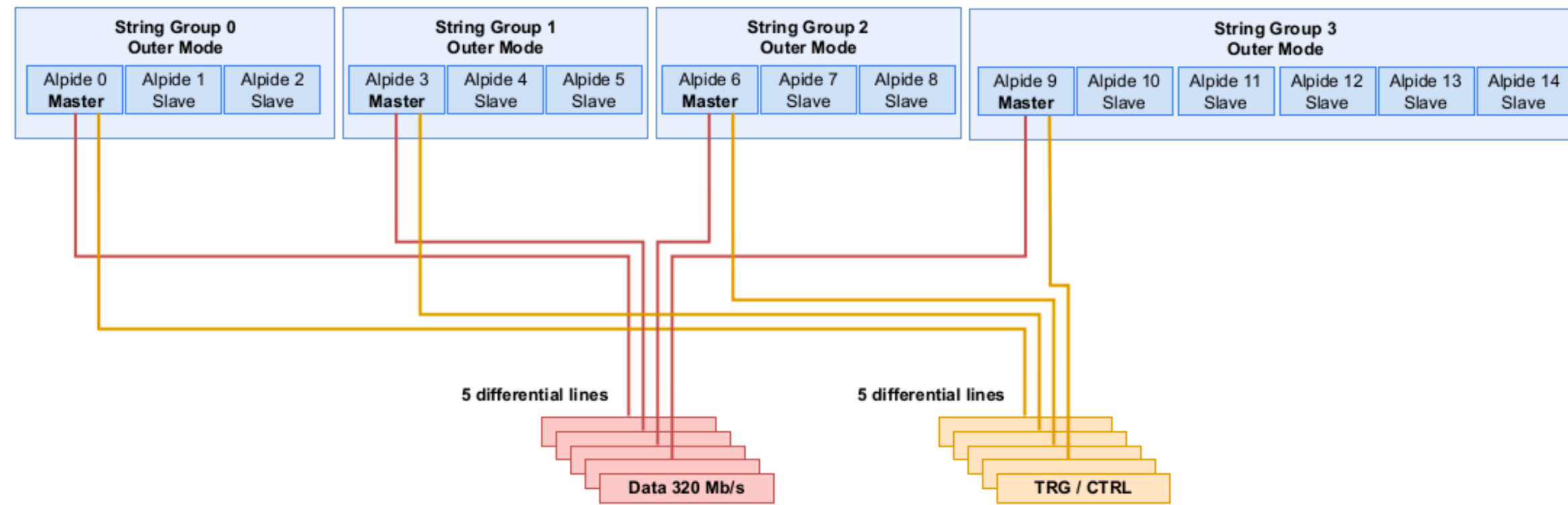
- The pixel matrix is divided into 32 readout regions, each read out in parallel.
- Each pixel equipped with three pixel memories.
- Each region contains 16 pixel double columns and 512 pixel rows
- The pixel memory are connected to the three partitions of the MEB.

The matrix readout duration  $\Delta t_{matrix} = N_{region,max} \times 50 \text{ ns}$

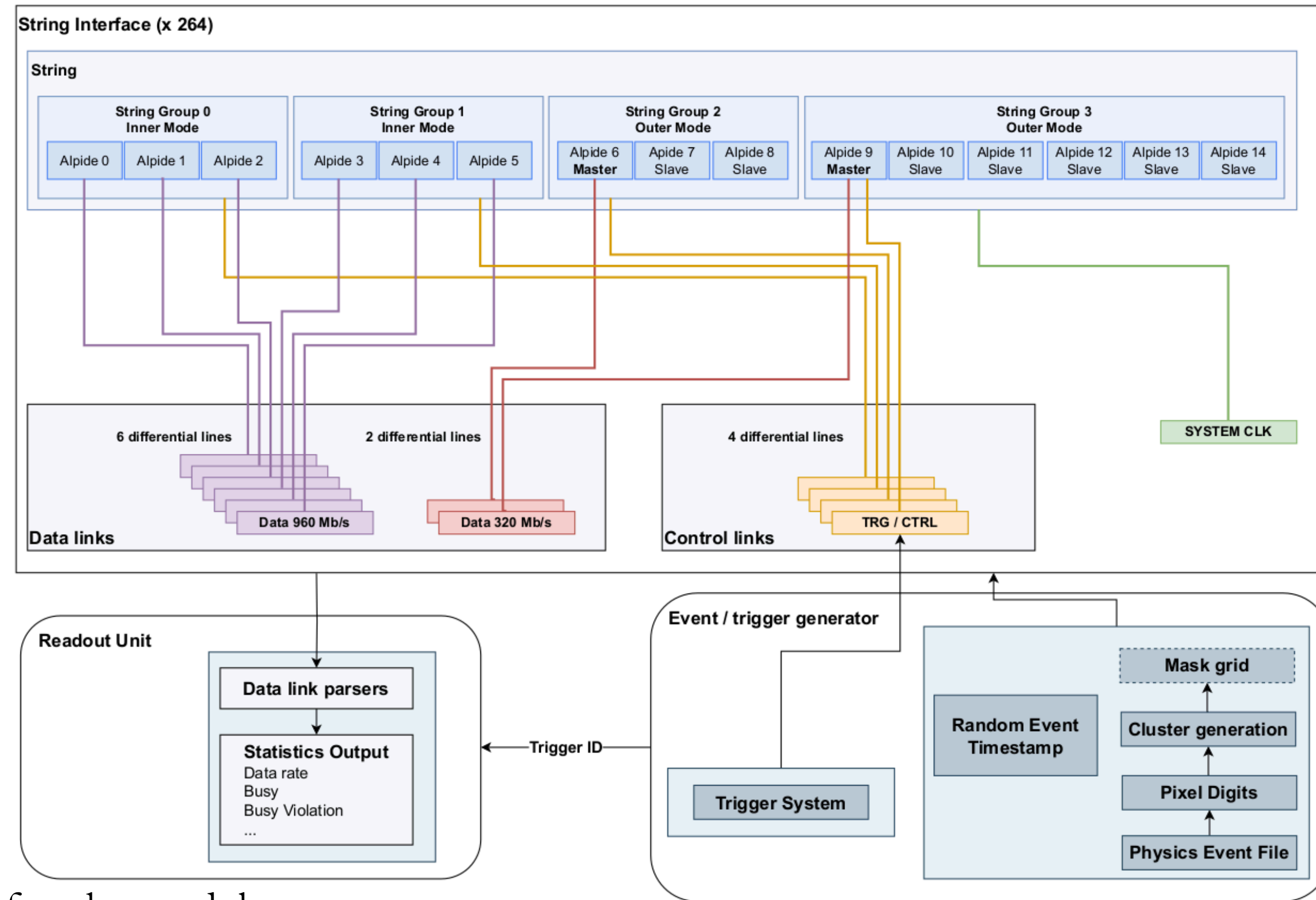


- SystemC is a C++ library used for hardware description
- ‘SC\_METHOD’ can handle operations that need to be executed in parallel

Outer string, 15 alpides



Schematic overview on the functionalities of the FoCal-E Pixel Simulation Framework



- Simulate the ALPIDE chip string, providing input and output interfaces for the model.
- In the Pixel Digits, particle xyz coordinates are converted into chip pixel row and column numbers.
- Cluster generation simulates the realistic pixel cluster.



System Trigger Method

Continuous Mode

Trigger mode

Continuous setting

Default trigger frequency  $f_{\text{trg}} = 100 \text{ kHz}$

Default timeframe  $\Delta t_{\text{frame}} = 10 \mu\text{s}$

Inactive strobe time  $\Delta t_{\text{strobe, inactive}} = 1 \mu\text{s}$

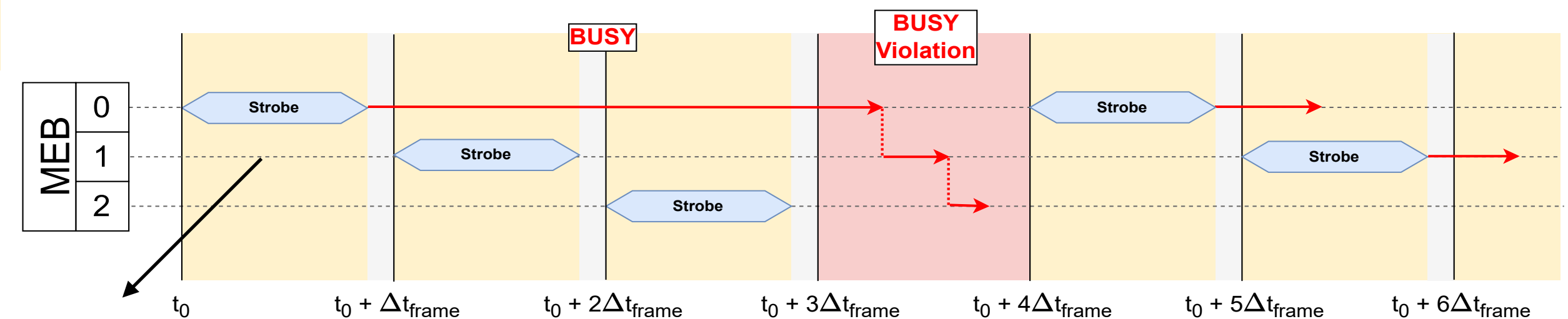
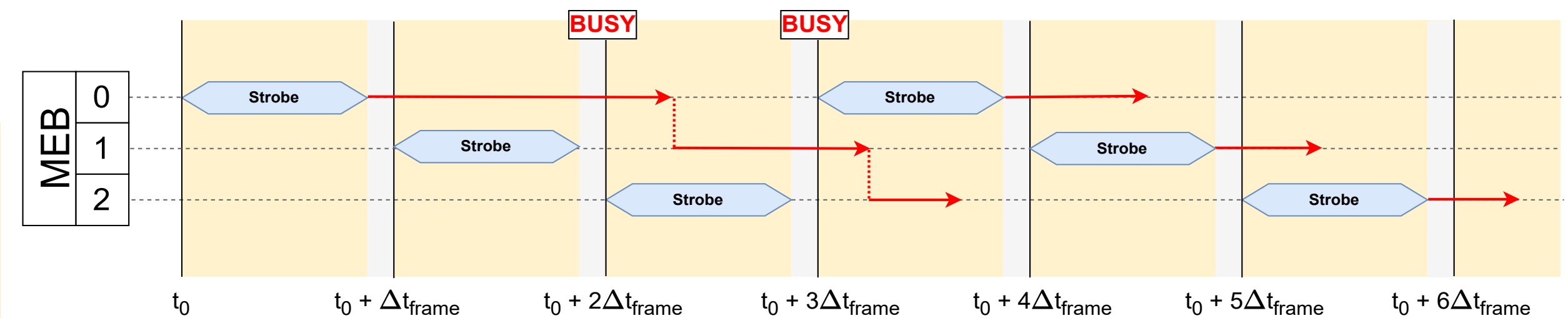
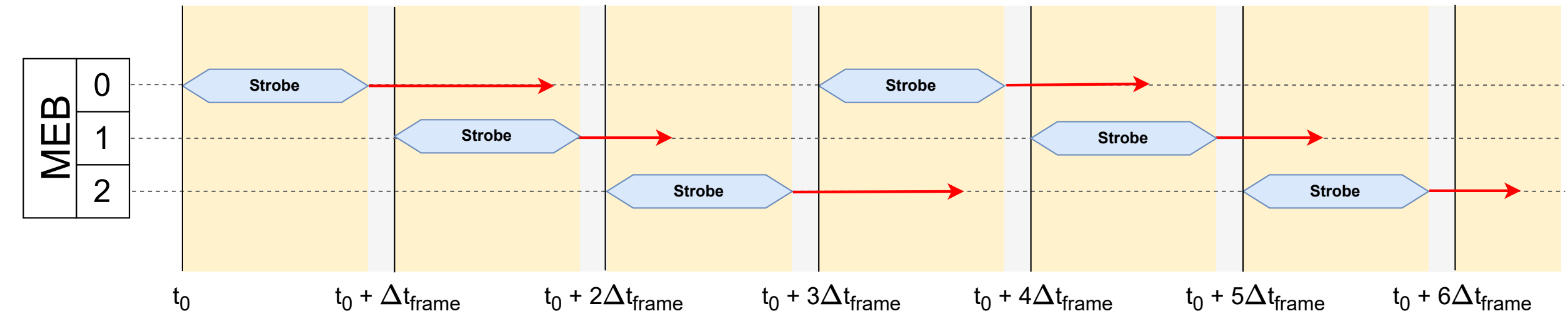
Impact of Busy Violations:

The chip will **skip** the trigger.

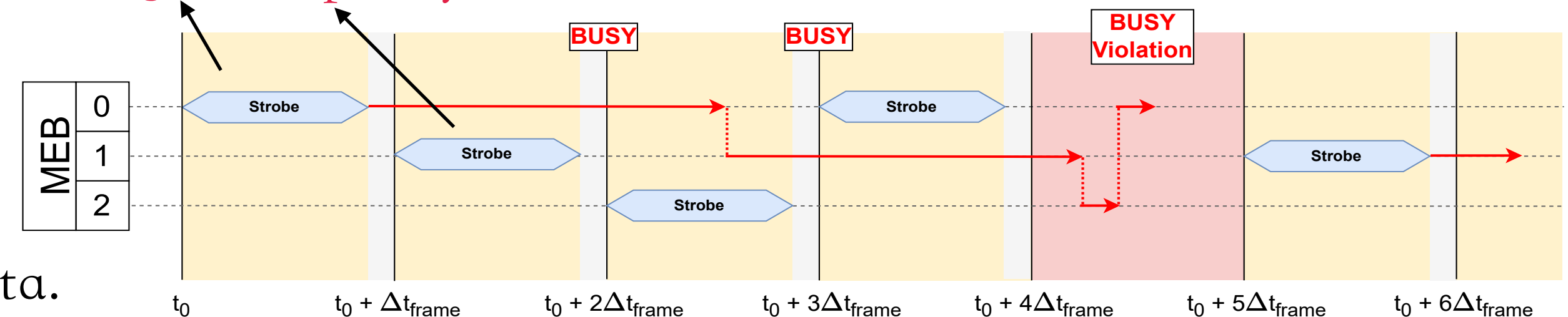
The pixel hit will be completely **lost**.

Once a slot in the MEB is freed,

the chip is again ready to receive triggers and take data.



Include high occupancy events



$$N_{\text{event}} = 45000 \quad \Delta t_{\text{frame}} = 10 \mu\text{s} \quad n_{\text{cl.size}} = 4$$

$$f_{\text{event}} = 1\text{MHz} \quad \Delta t_{\text{strobe,inactive}} = 1 \mu\text{s} \quad \sigma_{\text{cl.size}} = 1.4$$

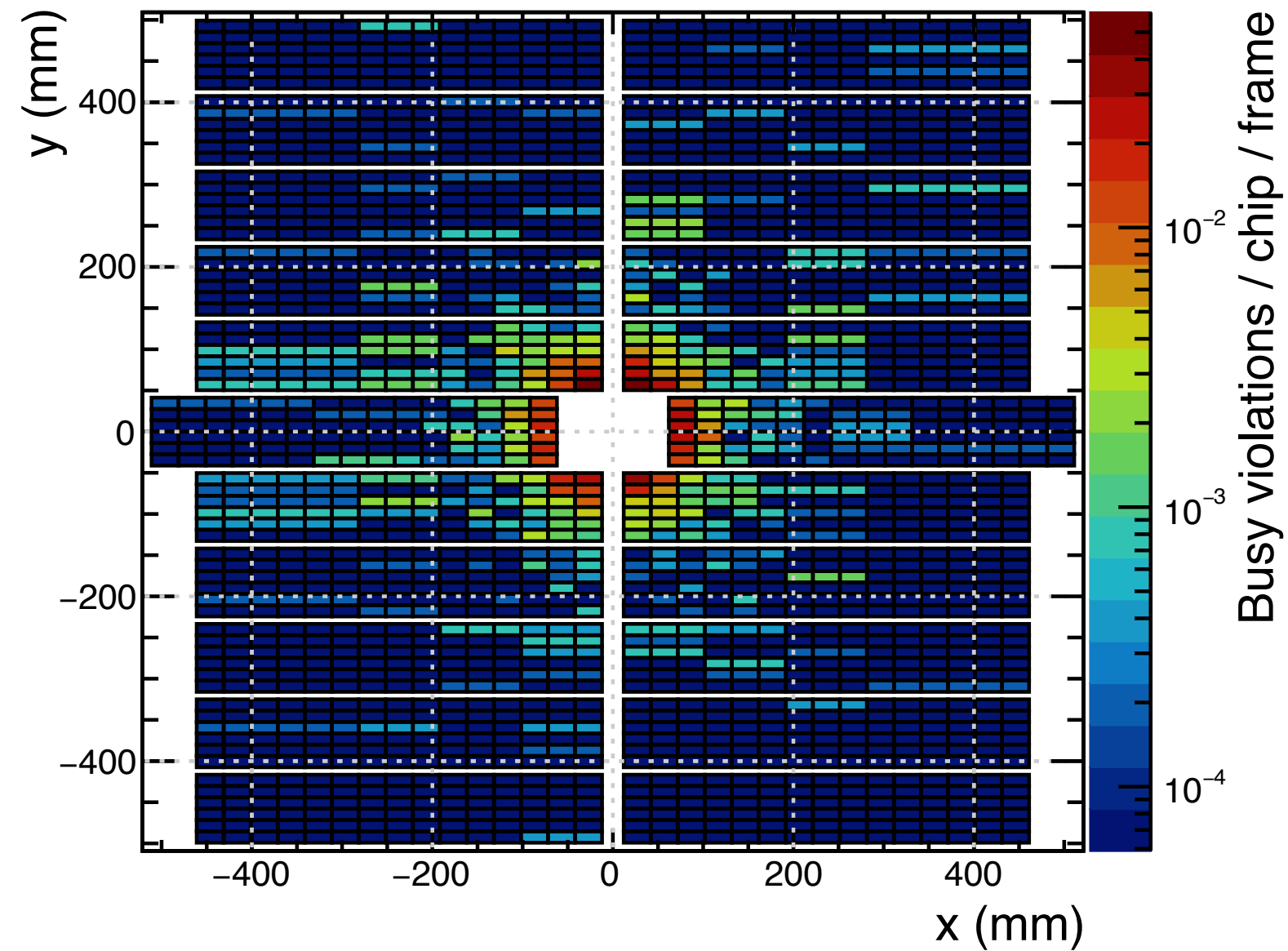
BUSY Violation Rate:

$$r_{\text{BUSYV}}(\text{chip}) = \frac{N_{\text{BUSYV,chip}}}{N_{\text{readout}}}$$

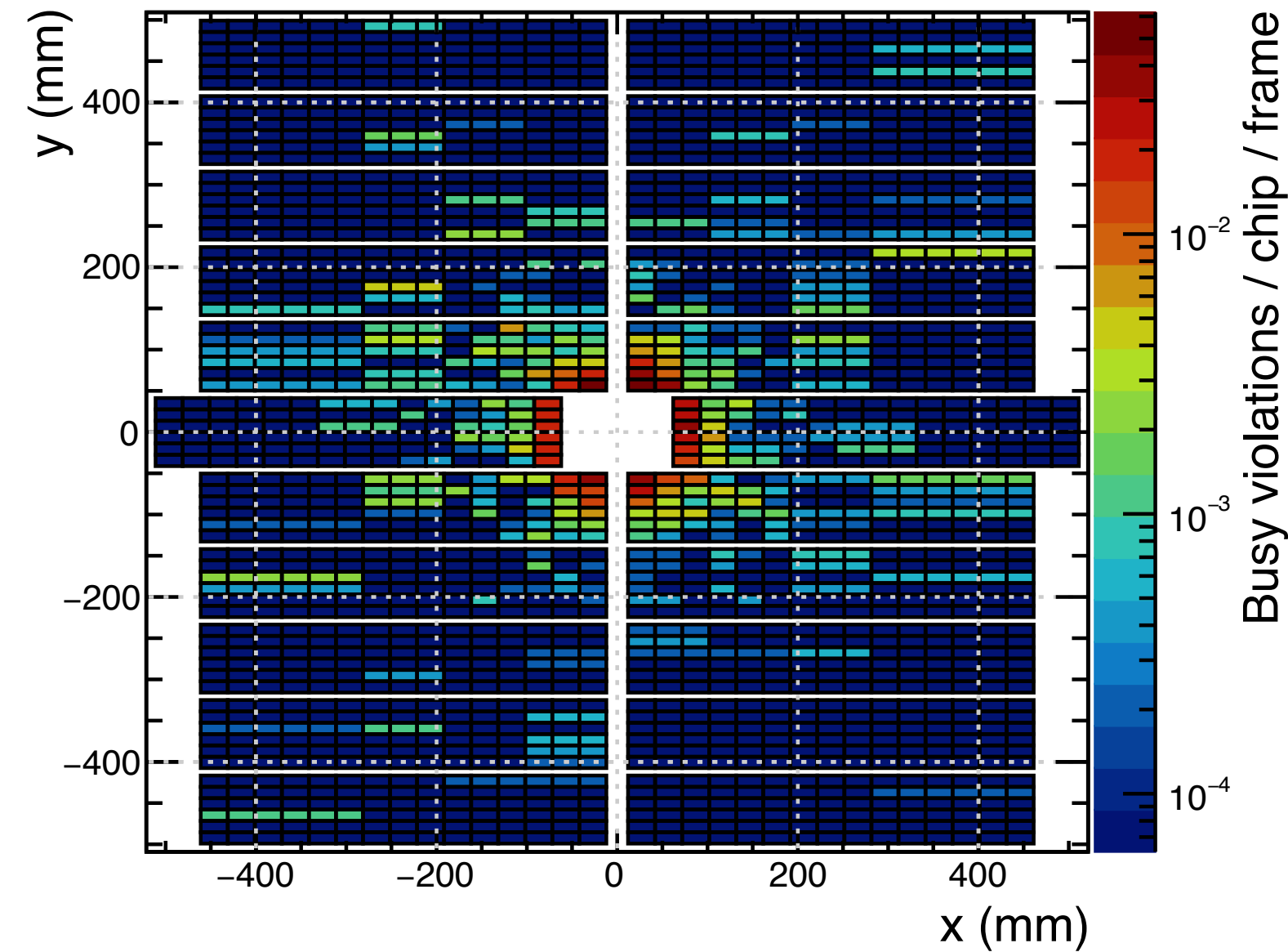
$N_{\text{BUSYV,chip}}$  : Number of dead frame

$N_{\text{readout}}$  : Total number of readout frames

FoCal Pixel Busy Violations Plane 5



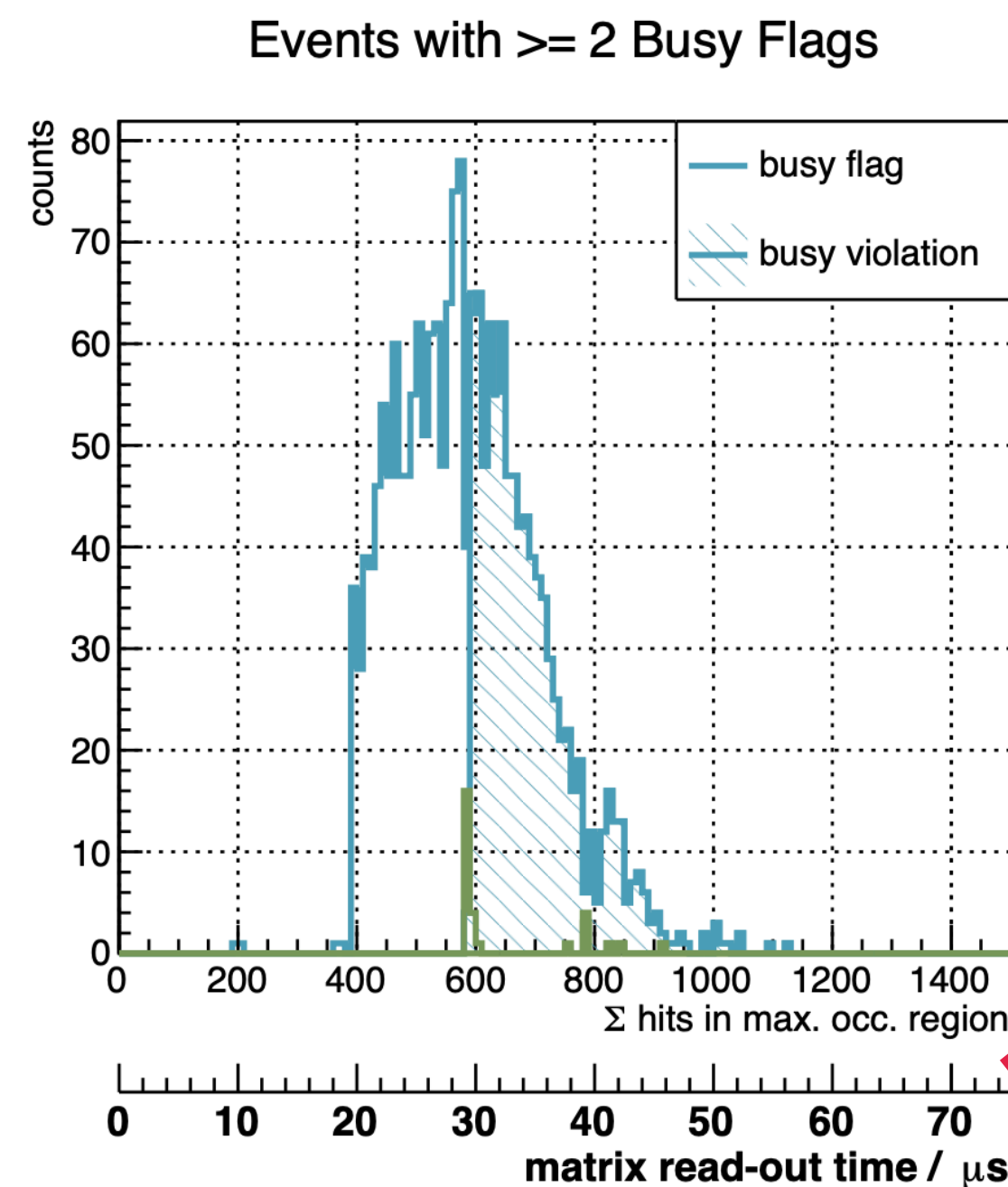
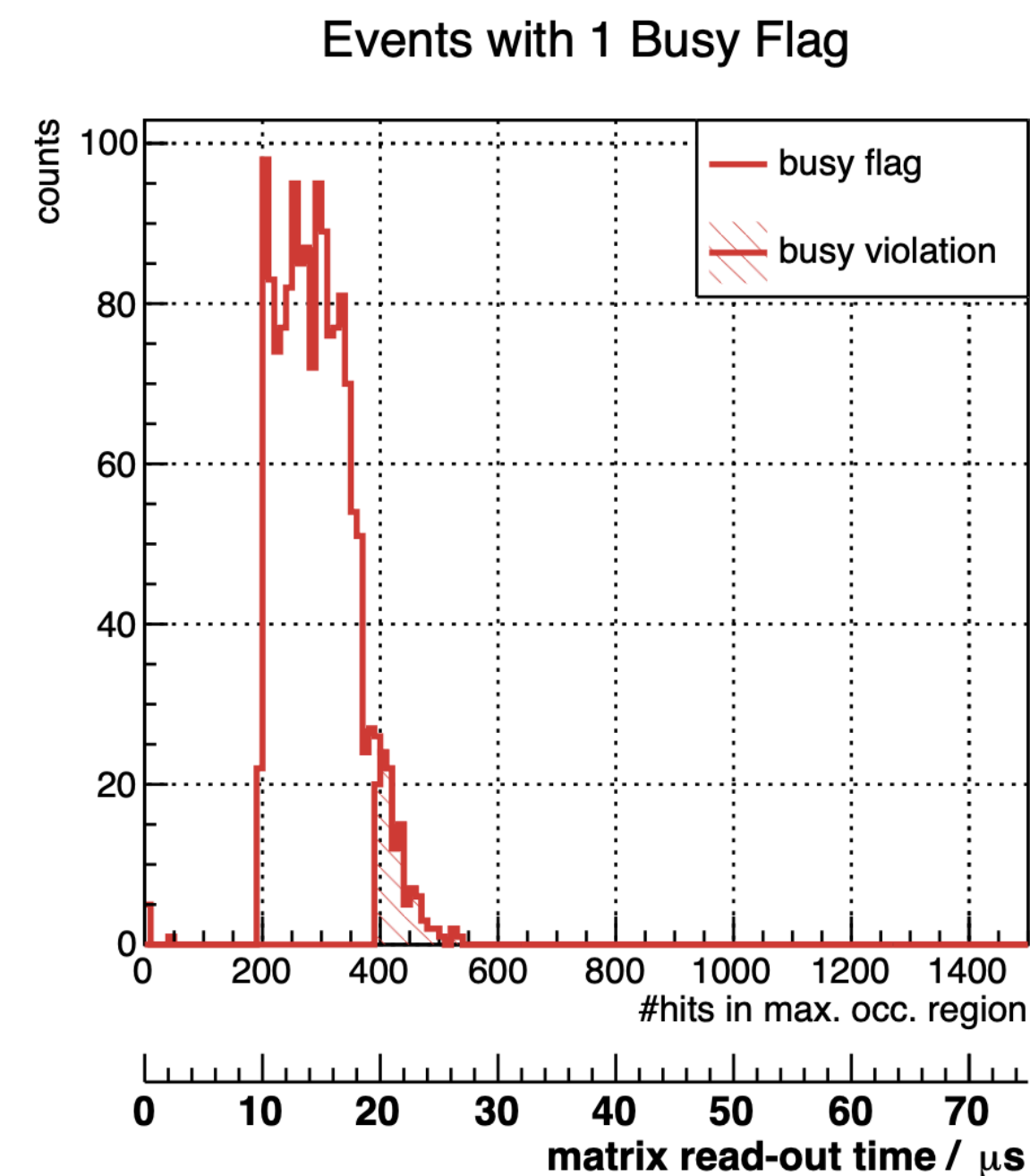
FoCal Pixel Busy Violations Plane 10



- The BUSYV rate is around 5%-6% for the innermost chips
- The BUSYV rate decreases sharply as the radius increases.



The bottleneck is regional read-out; **high local occupancy** (most-occupied region) drives BUSY and violations.



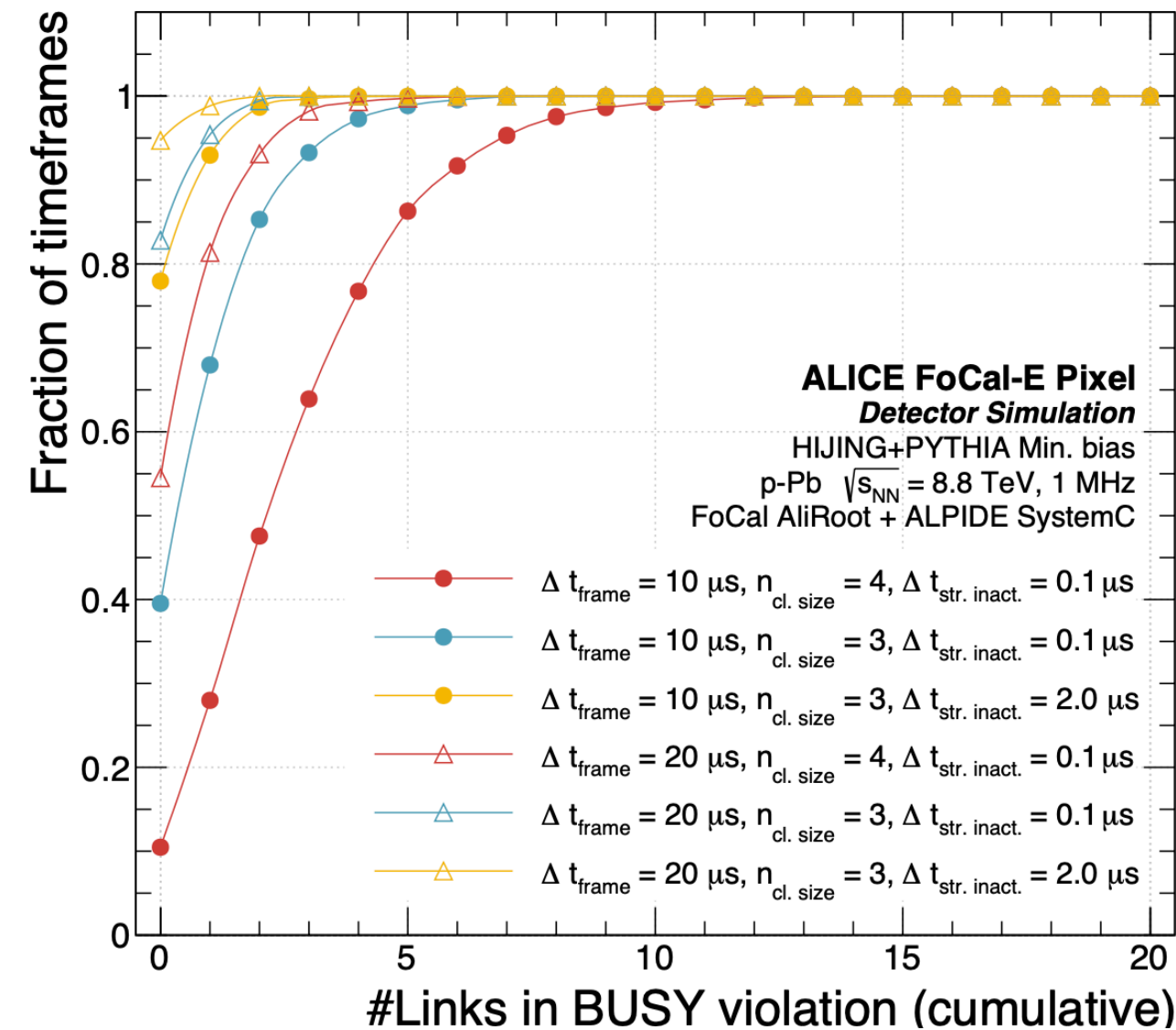
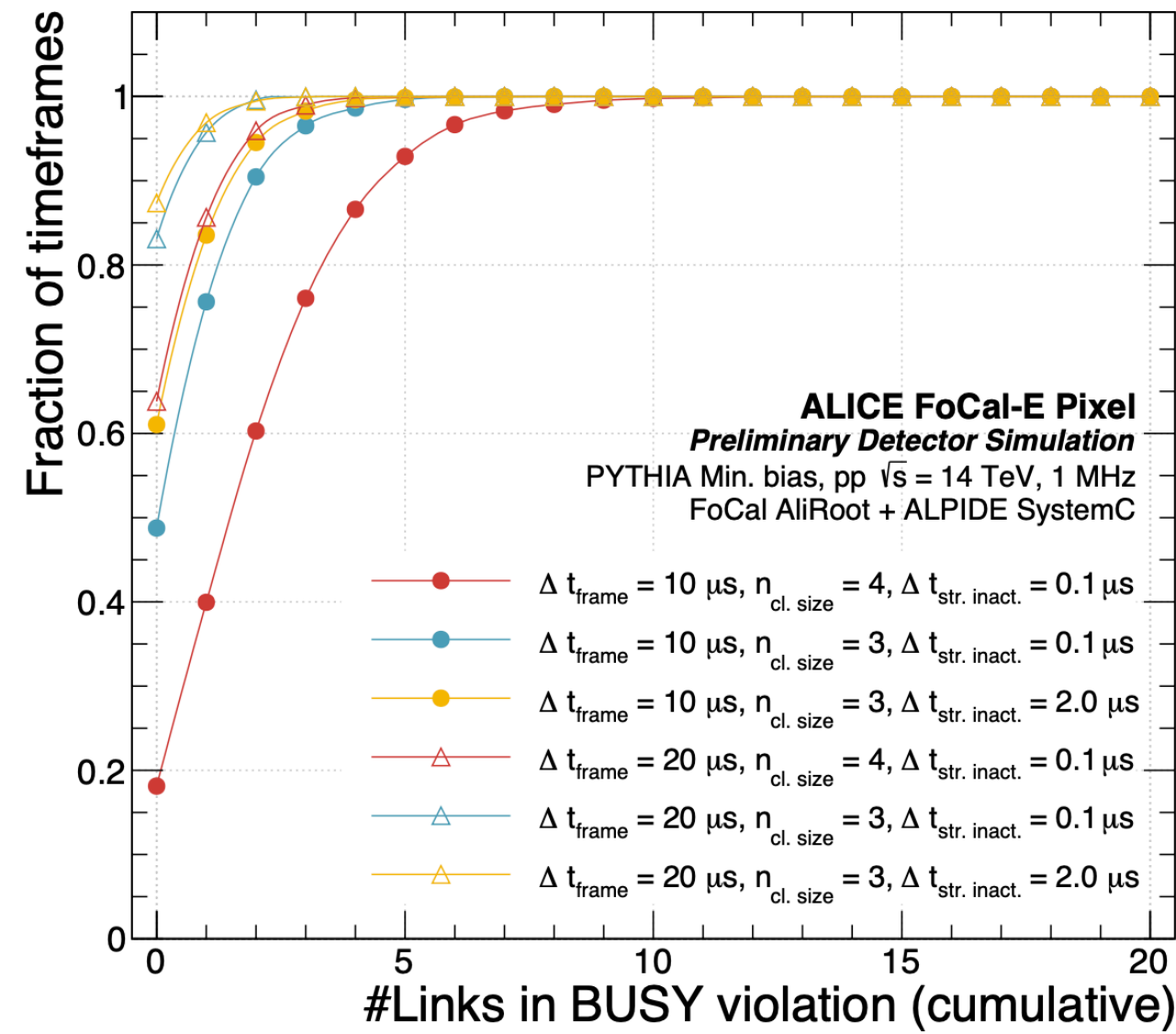
$$N_{\text{event}} = 45000 \quad \Delta t_{\text{frame}} = 10 \mu\text{s} \quad n_{\text{cl.size}} = 4$$

$$f_{\text{event}} = 1 \text{ MHz} \quad \Delta t_{\text{strobe,inactive}} = 1 \mu\text{s} \quad \sigma_{\text{cl.size}} = 1.4$$

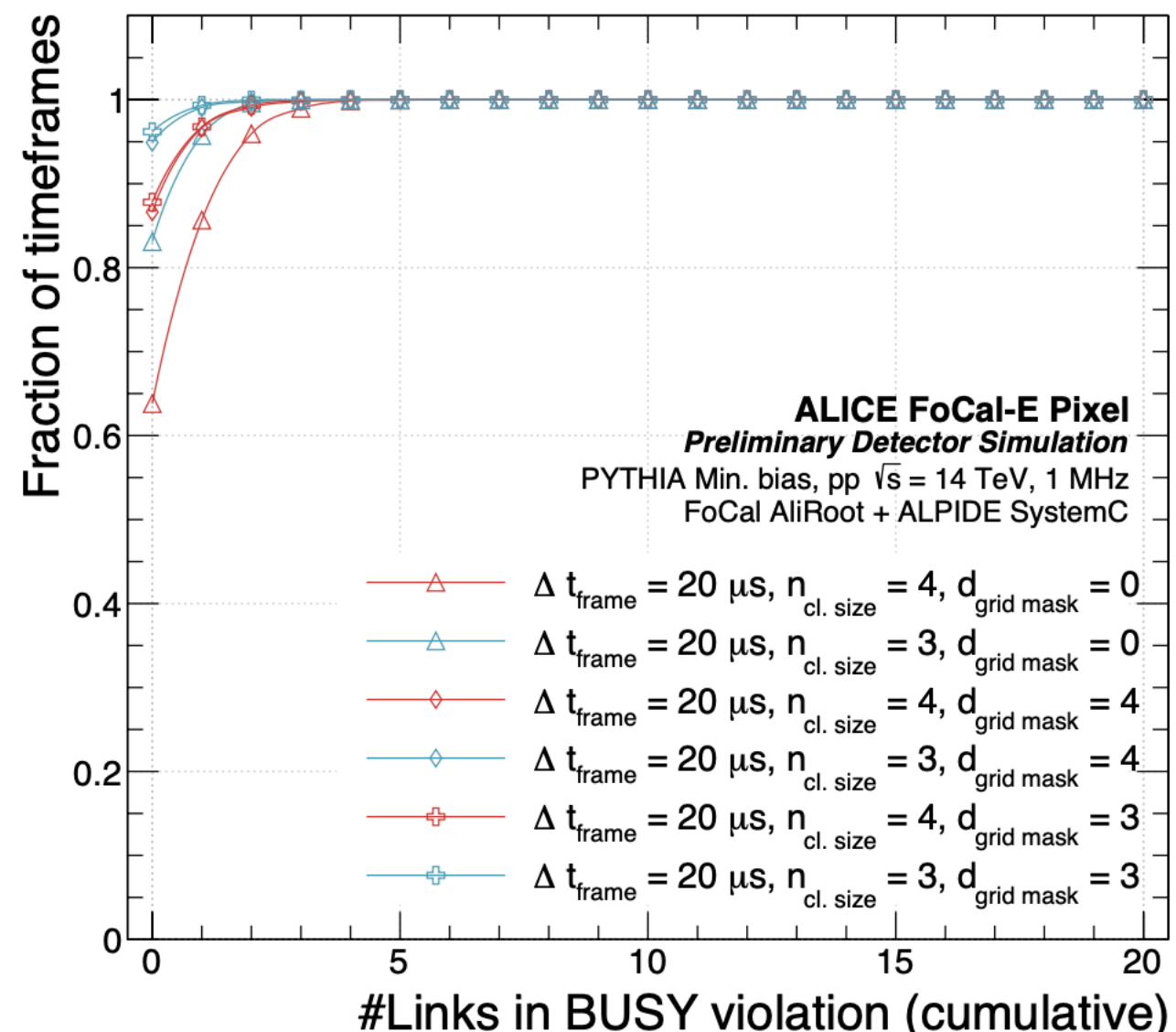
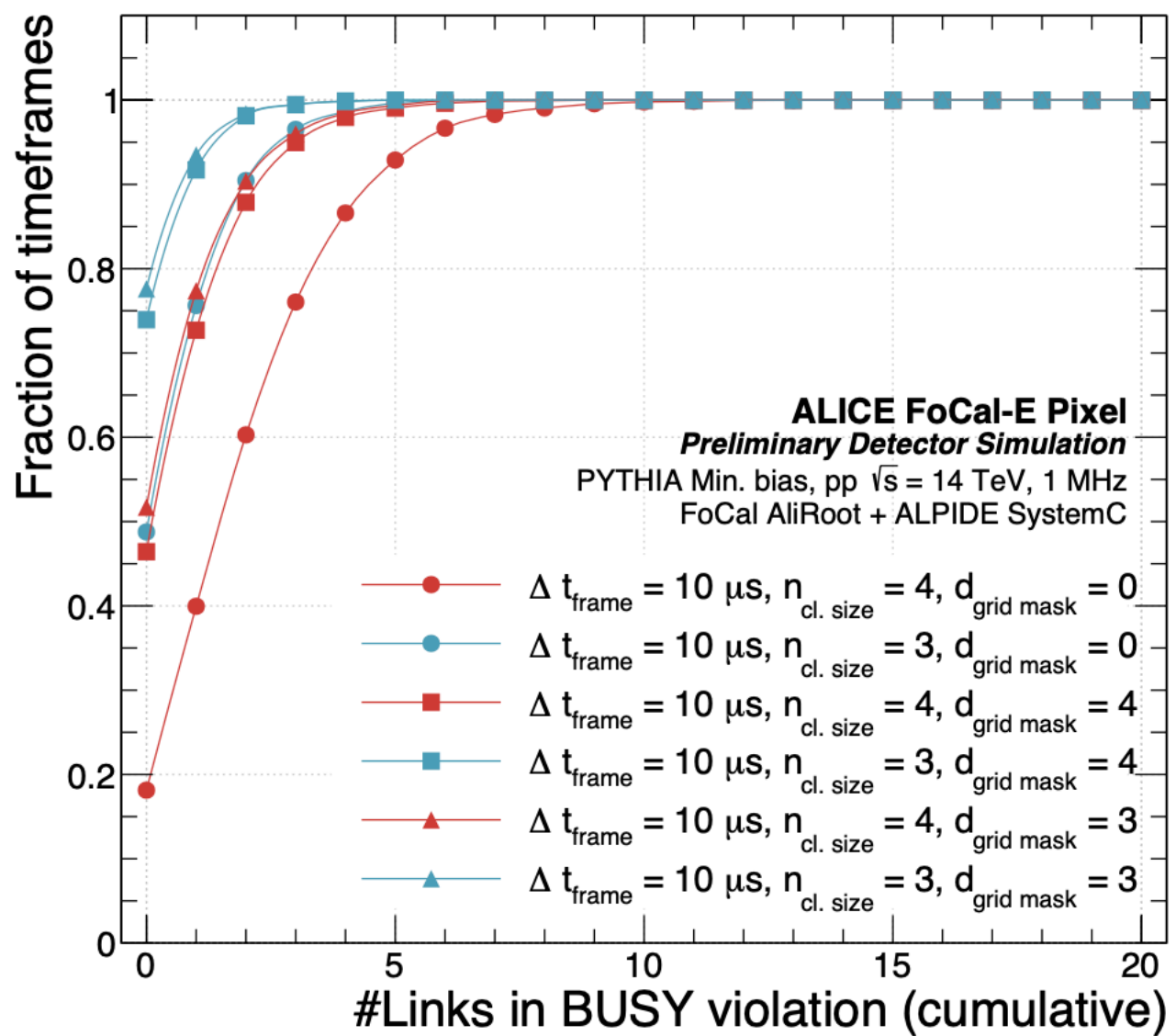
- A **BUSY flag** appears when the matrix read-out time exceeds the frame length ( $\Delta t_{\text{frame}} \approx 10 \mu\text{s}$ ).
- Left panel** (Events with 1 **BUSY flag**): single-frame phase. **BUSY** starts around  $\sim 200$  hits ( $\approx 10 \mu\text{s}$ ); BUSY violation emerges around  $\sim 400$  hits ( $\approx 20 \mu\text{s}$ ).
- Right panel** (Events with  $\geq 2$  **BUSY flags**): two-frame phase. Occupancy is spread over two frames; violations shift to higher totals, appearing around  $\sim 600$  hits ( $\approx 30 \mu\text{s}$ ).

BUSY/violation thresholds scale with the most-occupied region:  
 $\sim 200 \rightarrow \text{BUSY}$ ,  $\sim 400$  (1-frame) /  $\sim 600$  (2-frame)  $\rightarrow$  violation.

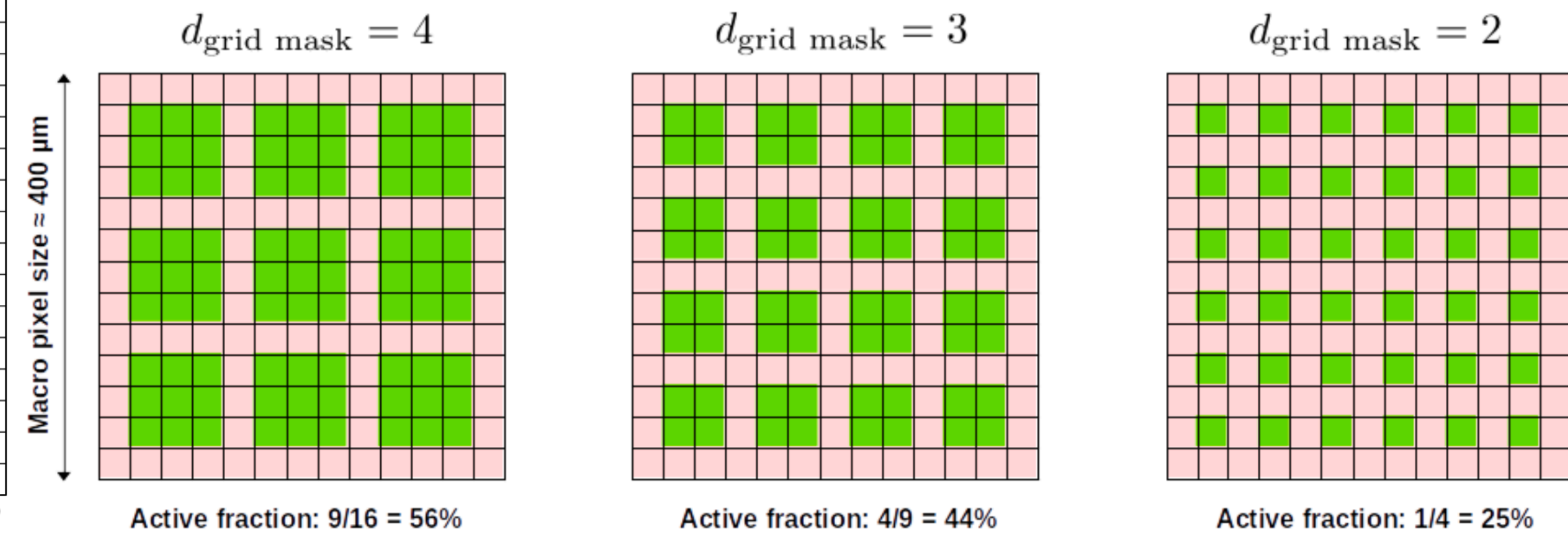
Dual x-axis: top = hits in the most-occupied region; bottom = equivalent matrix read-out time ( $\approx 50 \text{ ns per hit}$ ).



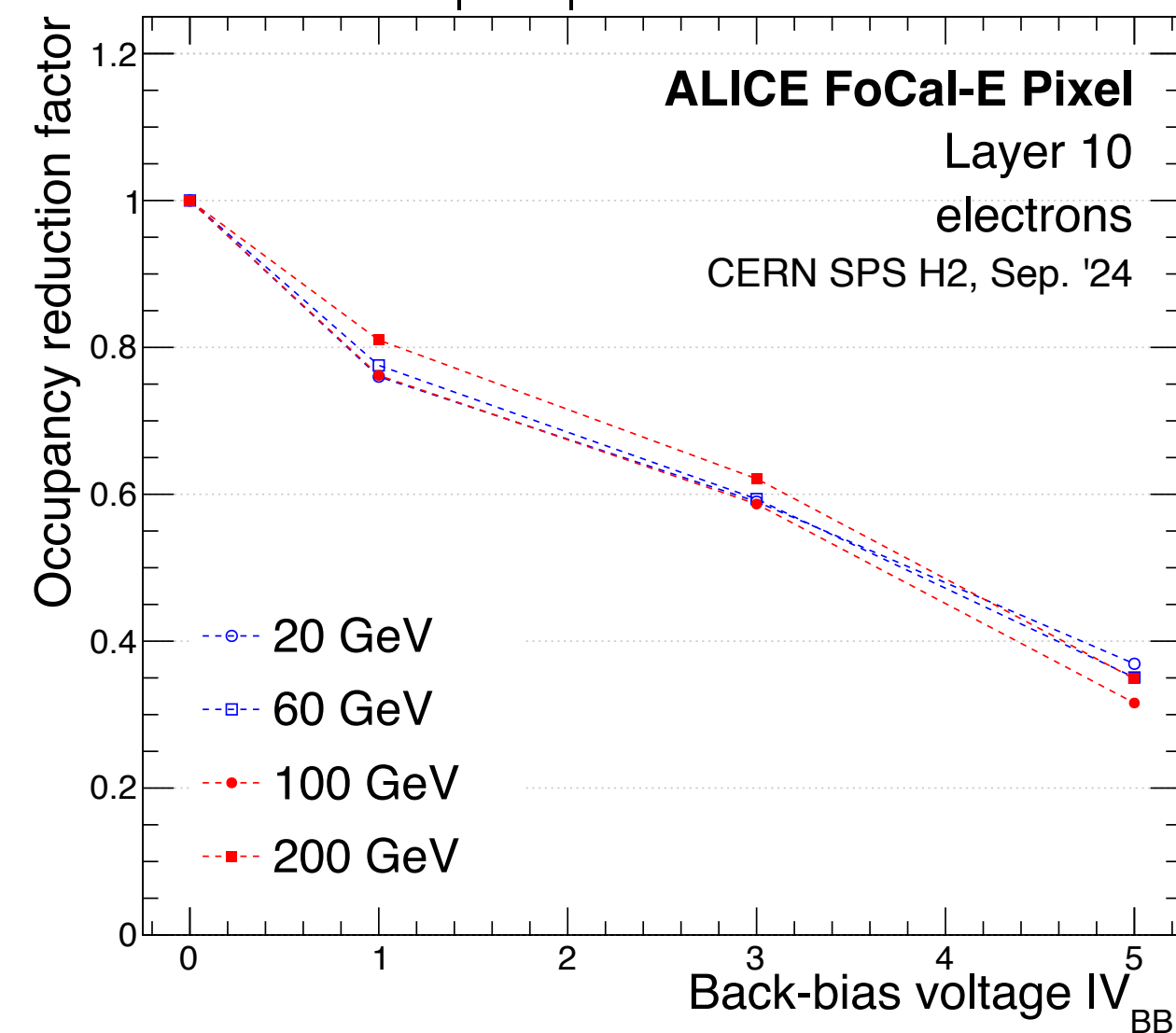
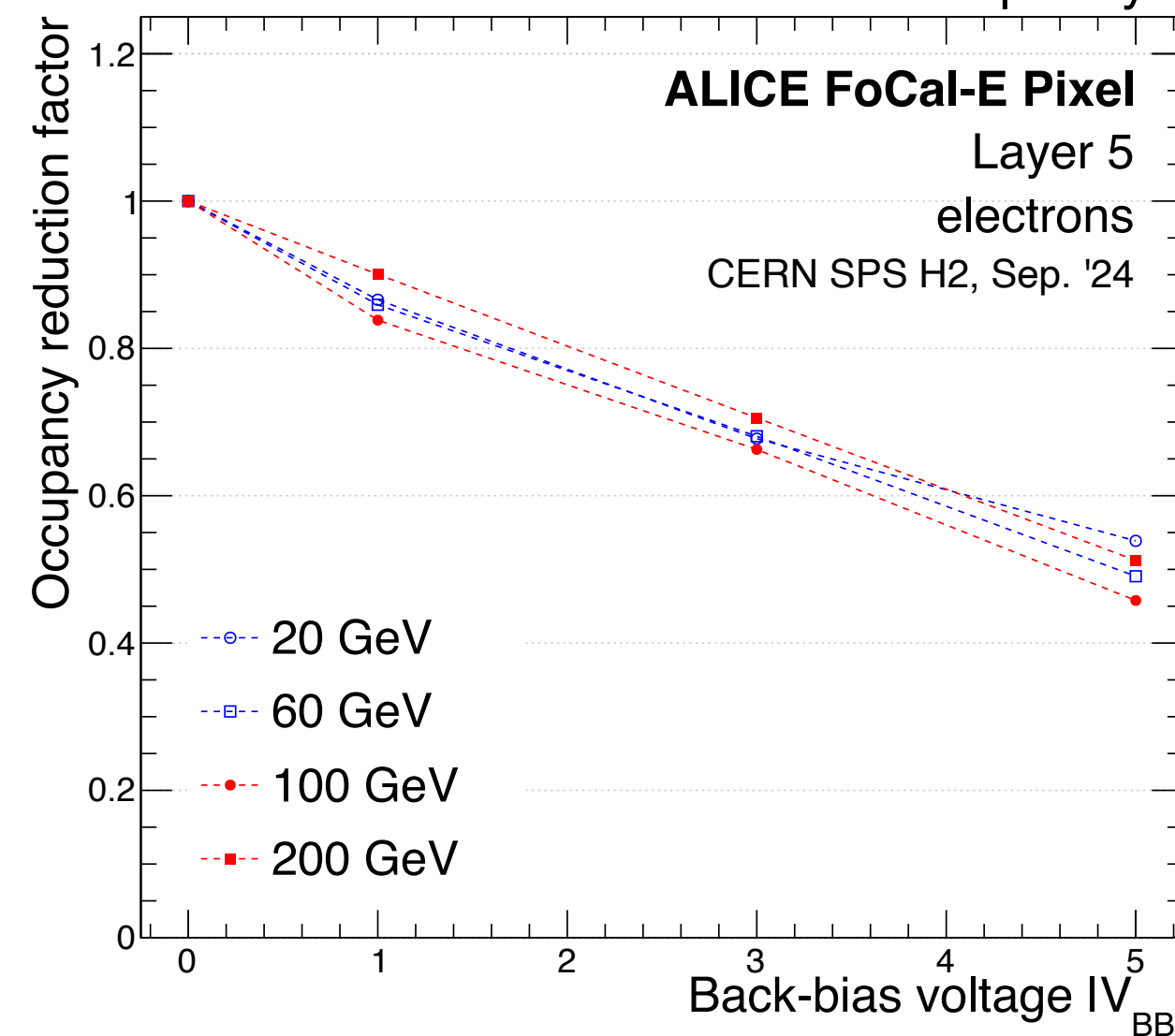
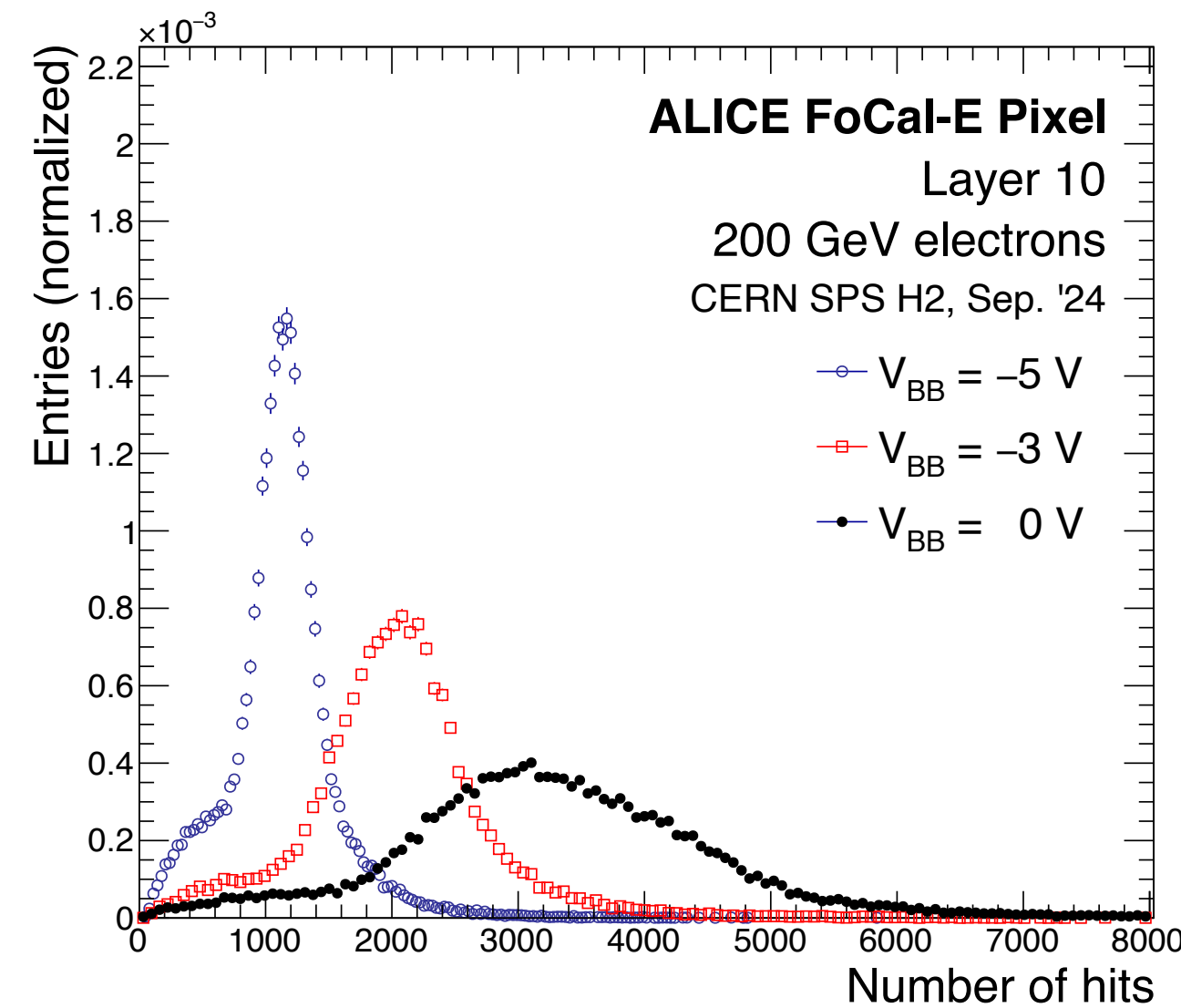
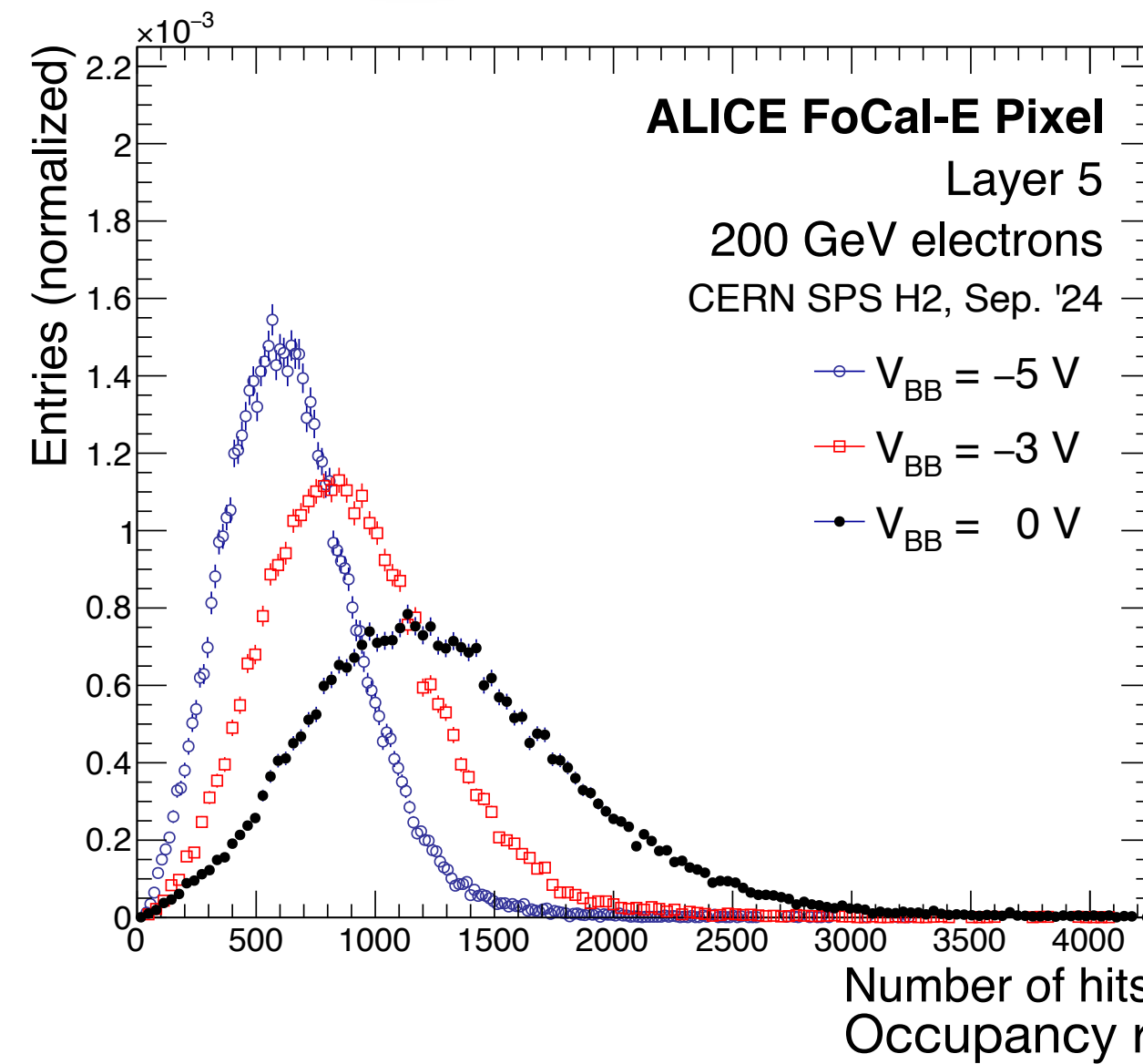
Longer **frames** and a  $\mu\text{s}$ -level **strobe-inactive** make the curves close to 1.0, sharply reducing violations.



Smaller **clusters** and **grid-masking** further suppress violations







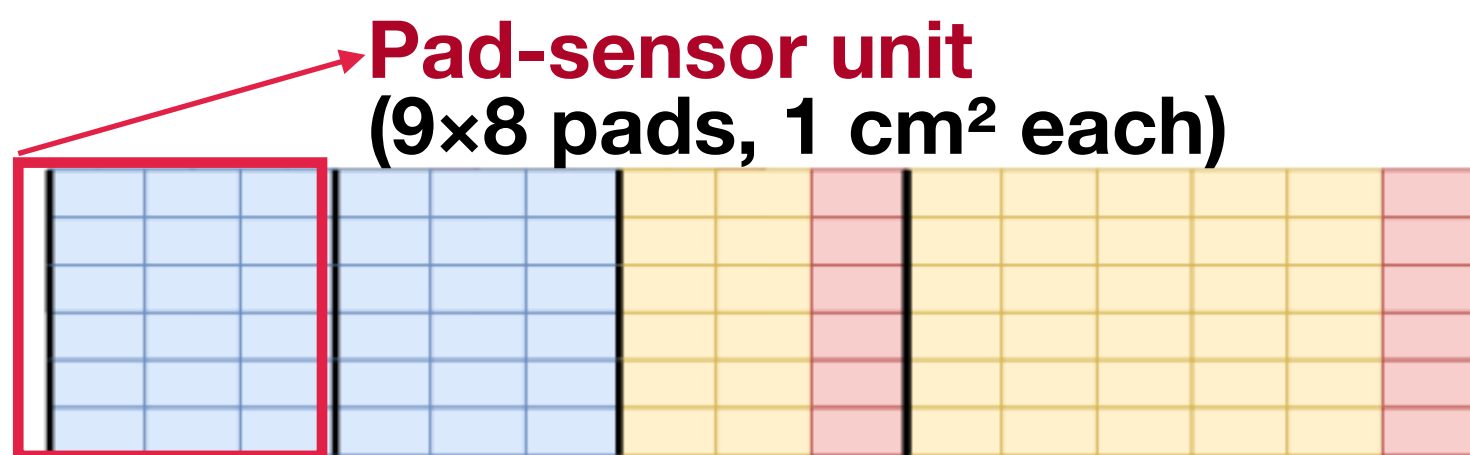
## How to **reduce** the cluster size ?

Increasing reverse **back-bias** deepens the depletion region and strengthens the electric field, speeding charge collection and reducing lateral diffusion—so pixel clusters get tighter.

Occupancy-reduction factor:  $R = \frac{\text{Occupancy at } |V_{BB}|}{\text{Occupancy at } 0\text{ V}}$

As **back-bias** increases, the **normalized hit** counts decrease and the **occupancy-reduction factor** decreases in both layers (meaning stronger reduction), with Layer 5 showing a slightly larger improvement than Layer 10.

Apply a few-volt **back-bias** to shrink cluster size and occupancy, thereby suppressing BUSY and BUSY-violation; then combine with longer frames, strobe-inactive, and grid-masking for best results.



(a) IB/OB pixel module-layer

Each **pad-sensor unit** can be seen as an ROI whose **deposited-energy** sum is monitored.

Threshold Triggering (**pad layer 4**, before pixel layer 5):

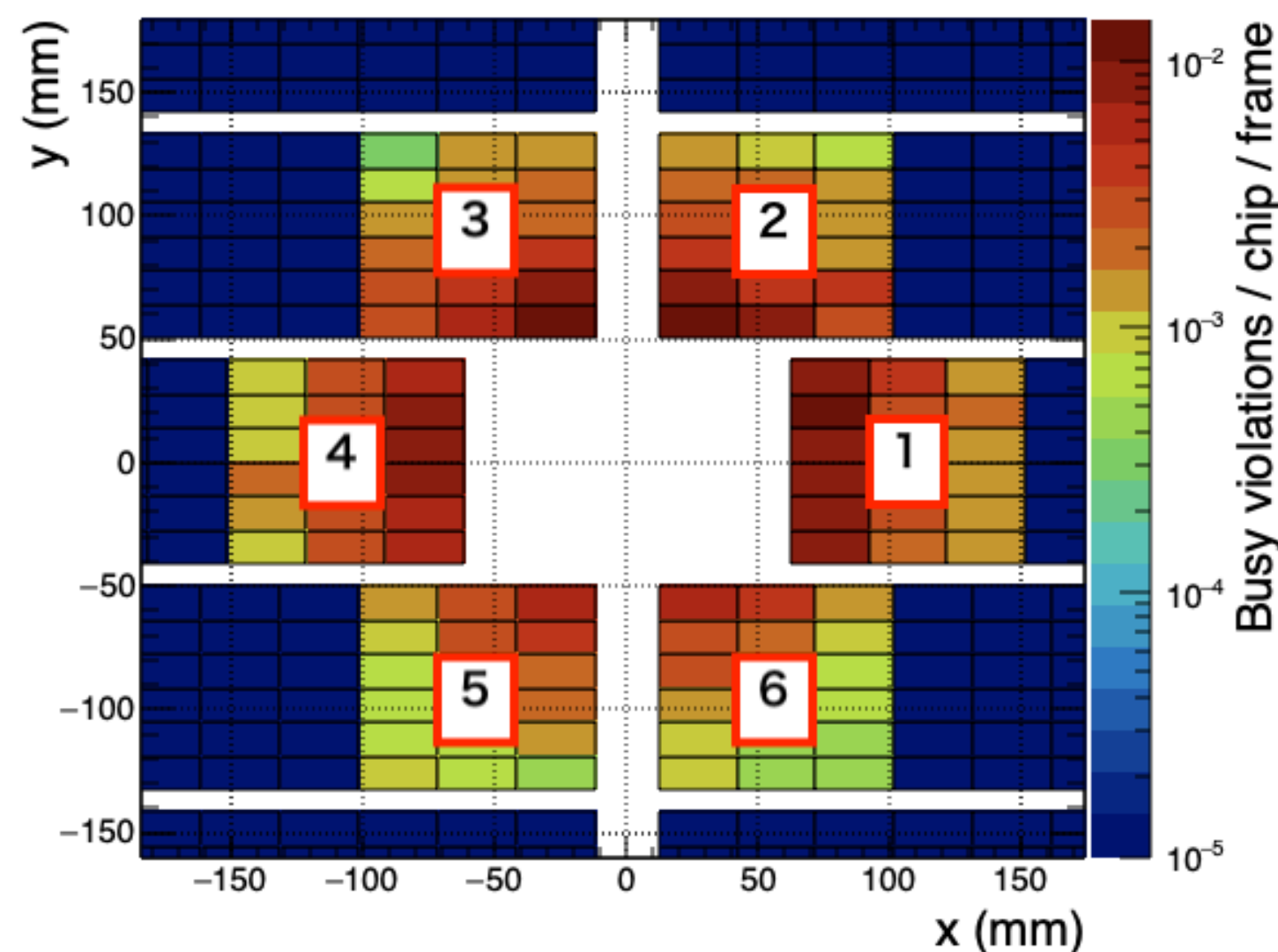
- o Pad-trigger primitives are aggregated on the Concentrator board and compared to **thresholds**.
- o If a threshold is passed, the **Concentrator** → **CRU/RU** forwards a regional enable to the control links of the **overlapping ALPIDE regions** (only those areas are activated).

Triggers are sent only to the overlapping areas between the **pad sensor unit** and the **ALPIDE** sensors

Now, Triggers are **only** sent to ALPIDE near the beam pipe; other channels are disabled.

Regional-trigger zones near the beam-pipe gap (color scale shows BUSY Violation rate at a 10 MeV threshold).

FoCal Pixel Busy Violations Plane 5



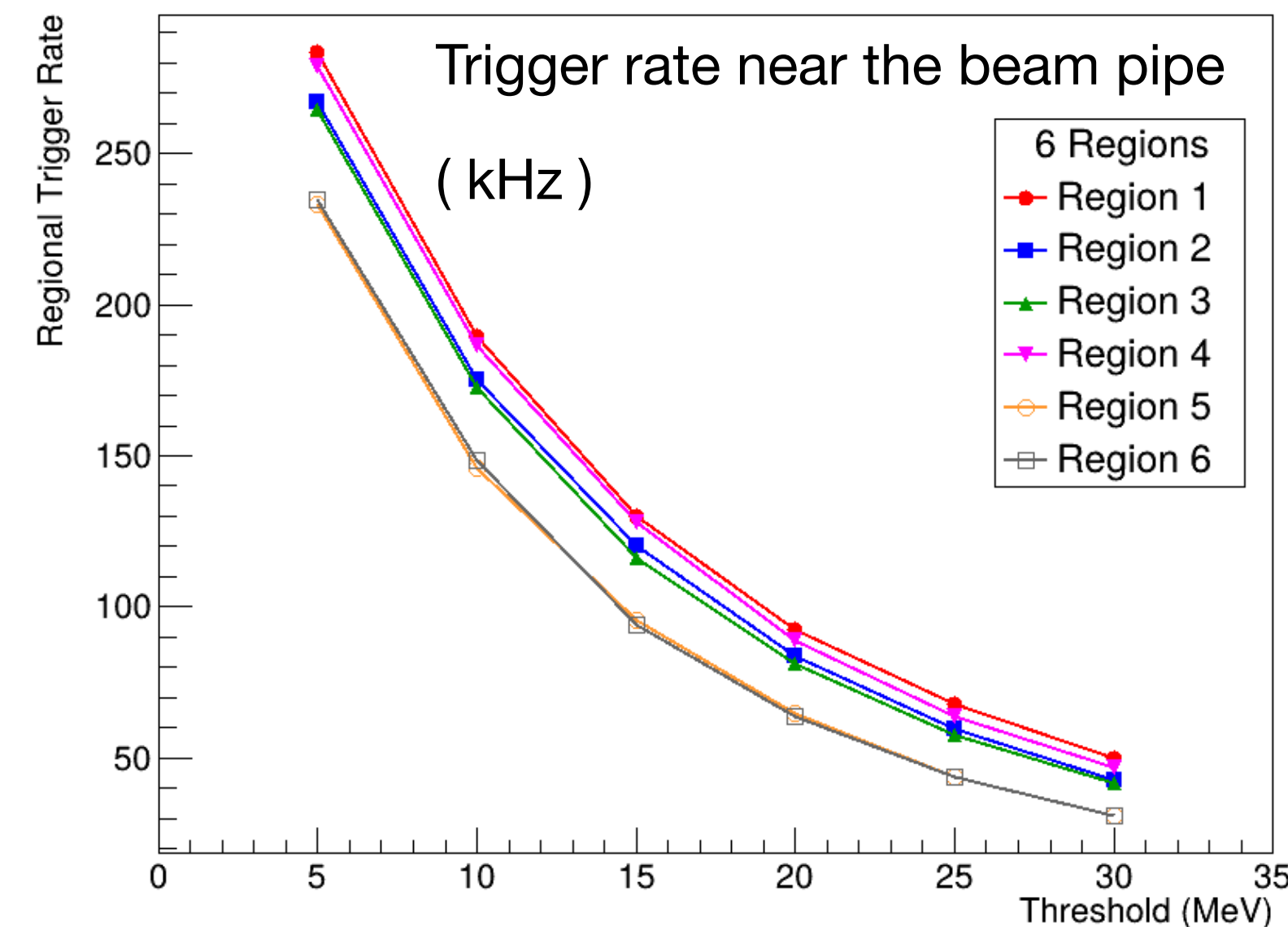
BUSY Violation Rate:

$$r_{\text{BUSYV}}(\text{chip}) = \frac{N_{\text{BUSYV,chip}}}{N_{\text{readout}}}$$

$N_{\text{BUSYV,chip}}$  : Number of dead frame

$N_{\text{readout}}$  : Total number of readout frames

TriggerRate vs Threshold





1 MHz Event Rate

200 ns Strobe Window ( including 50 ns inactive time)

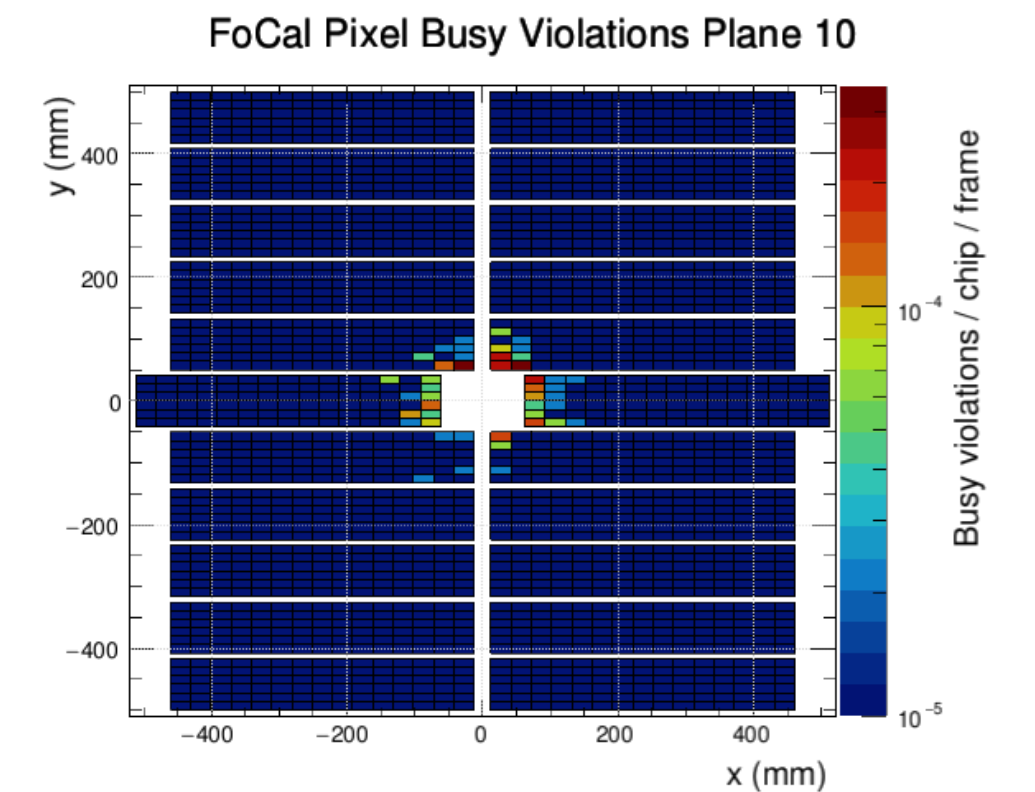
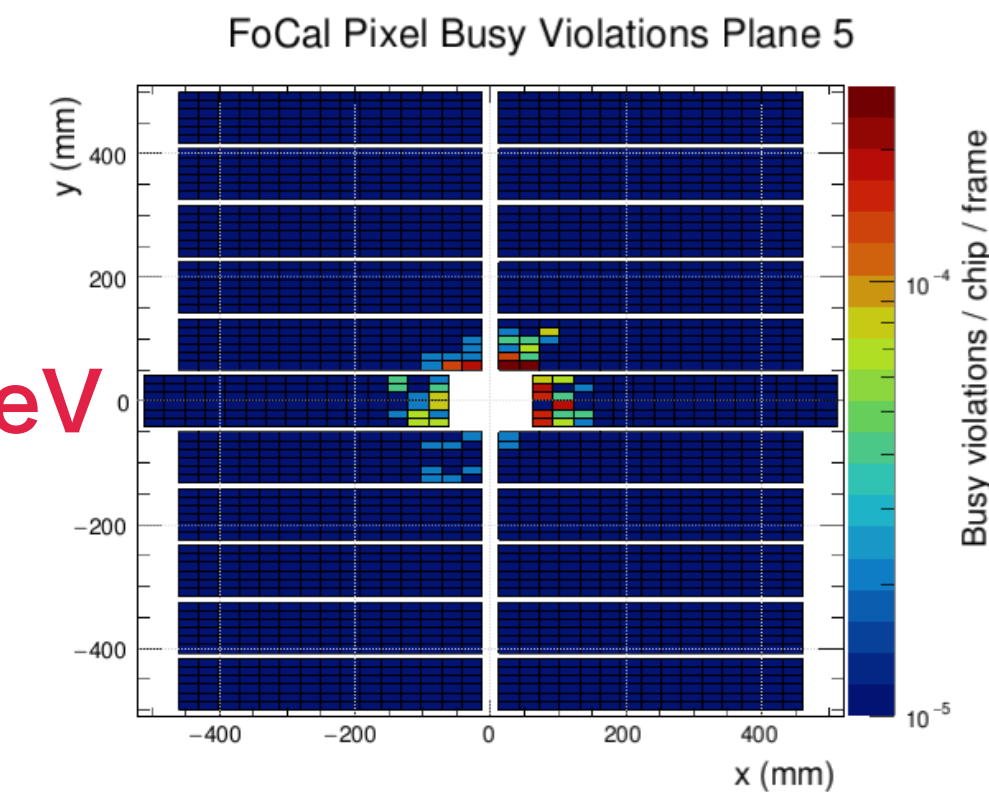
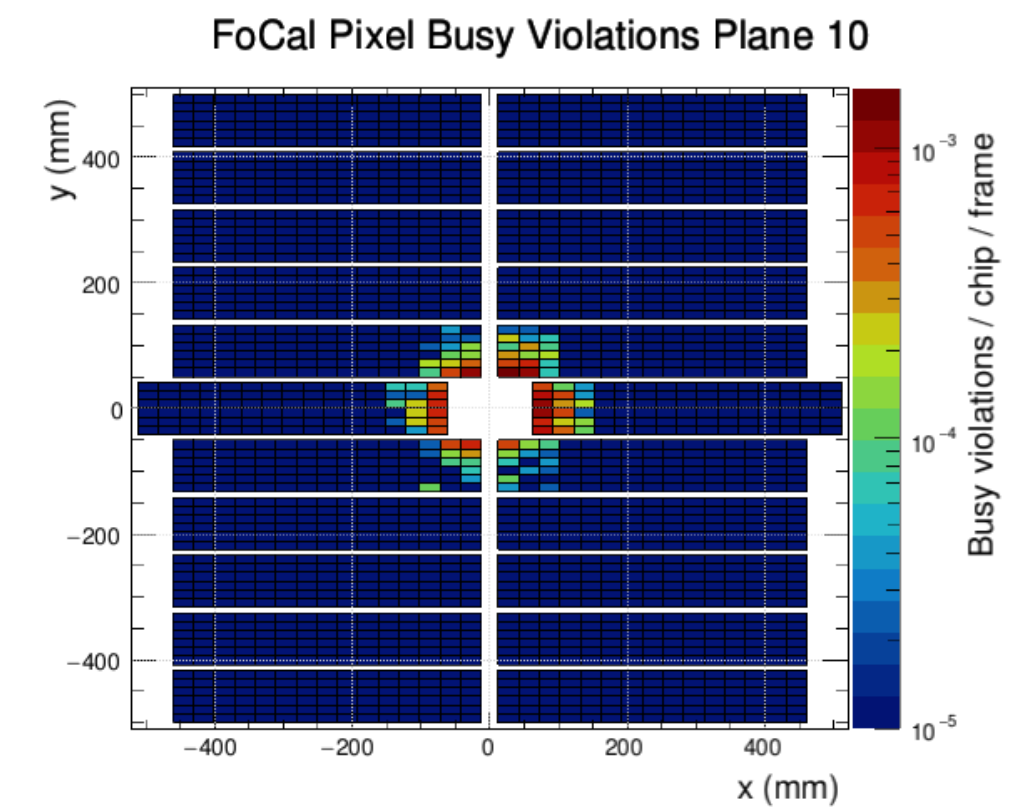
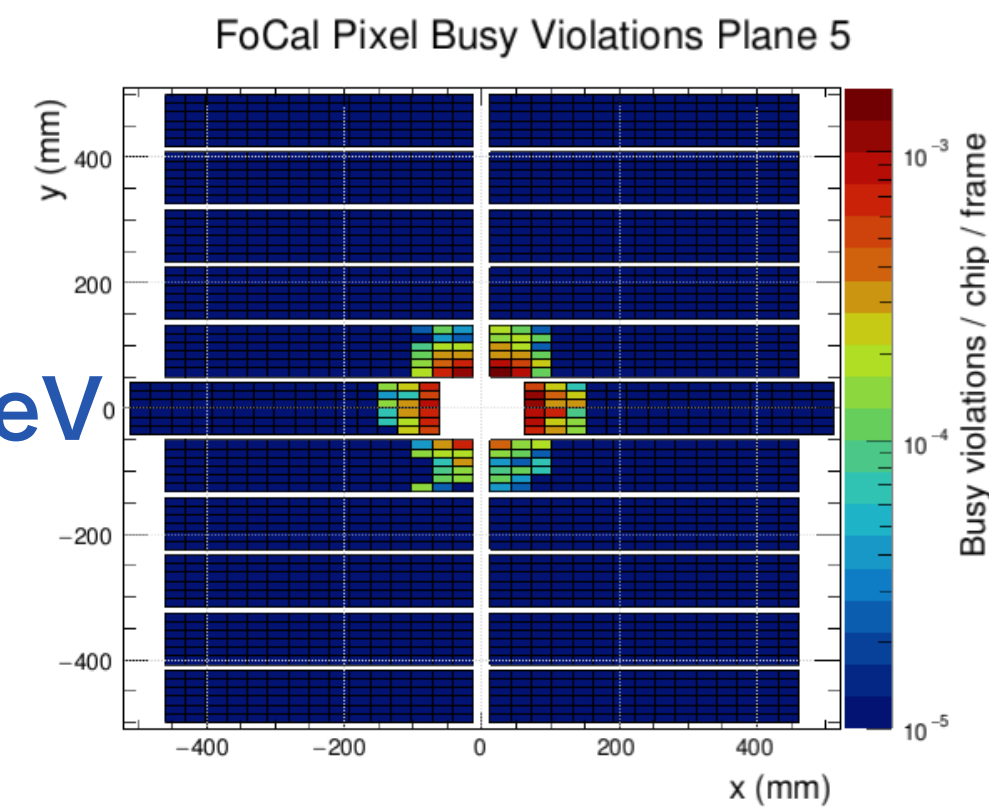
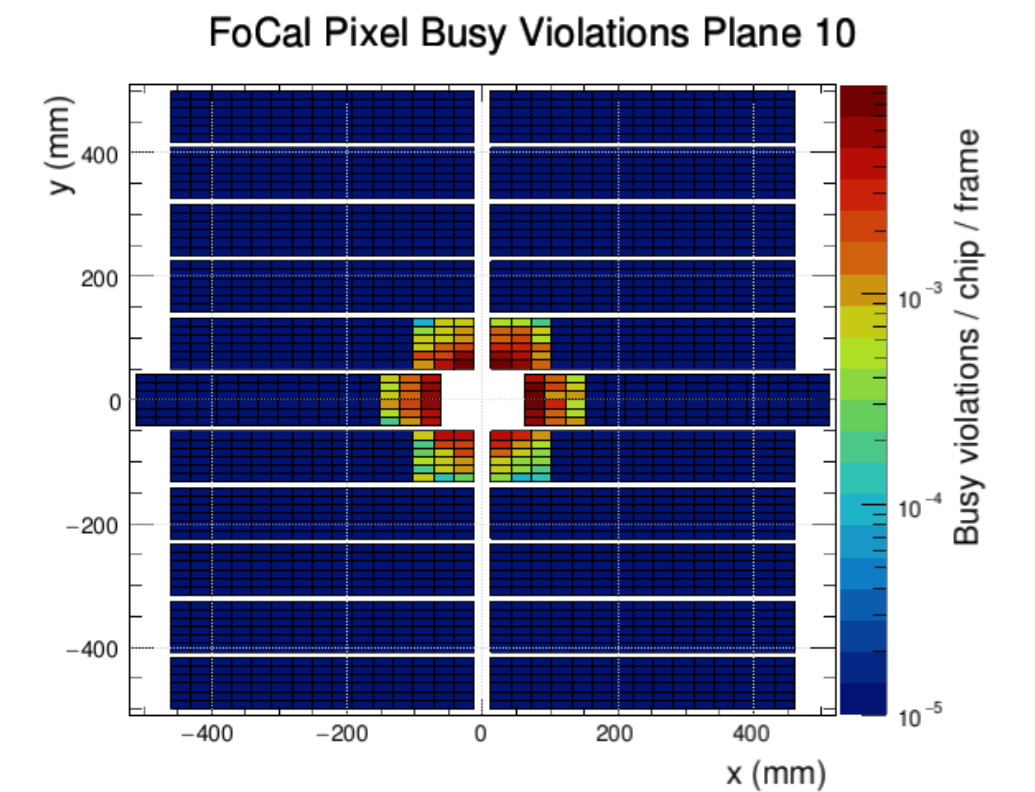
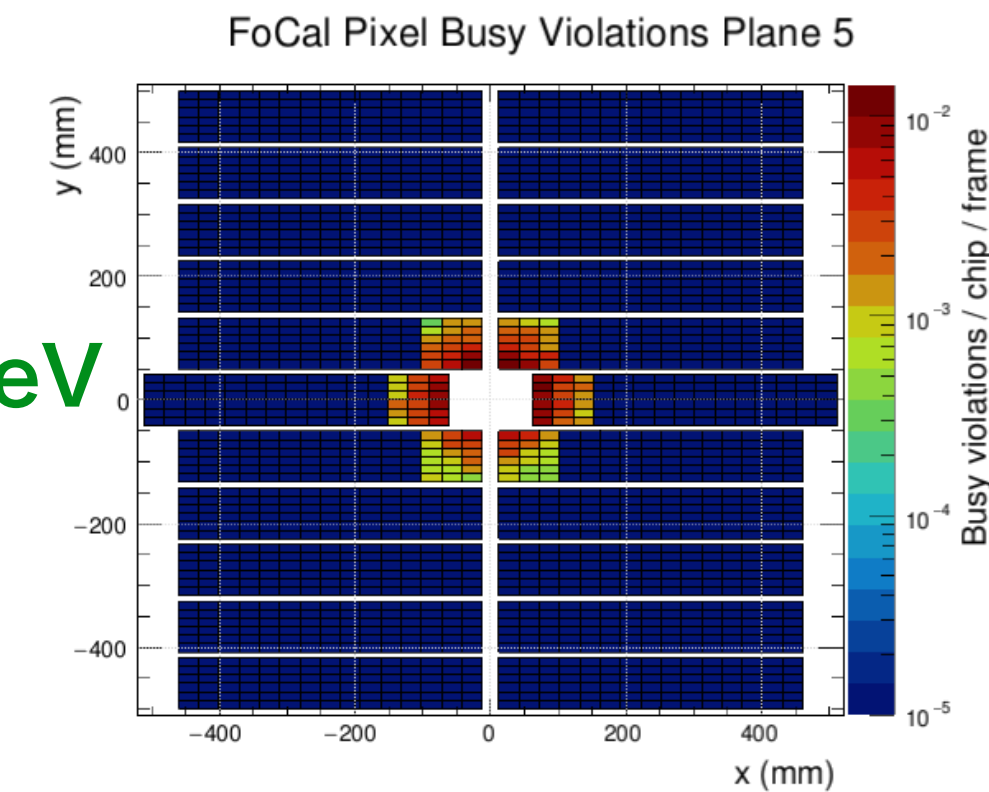
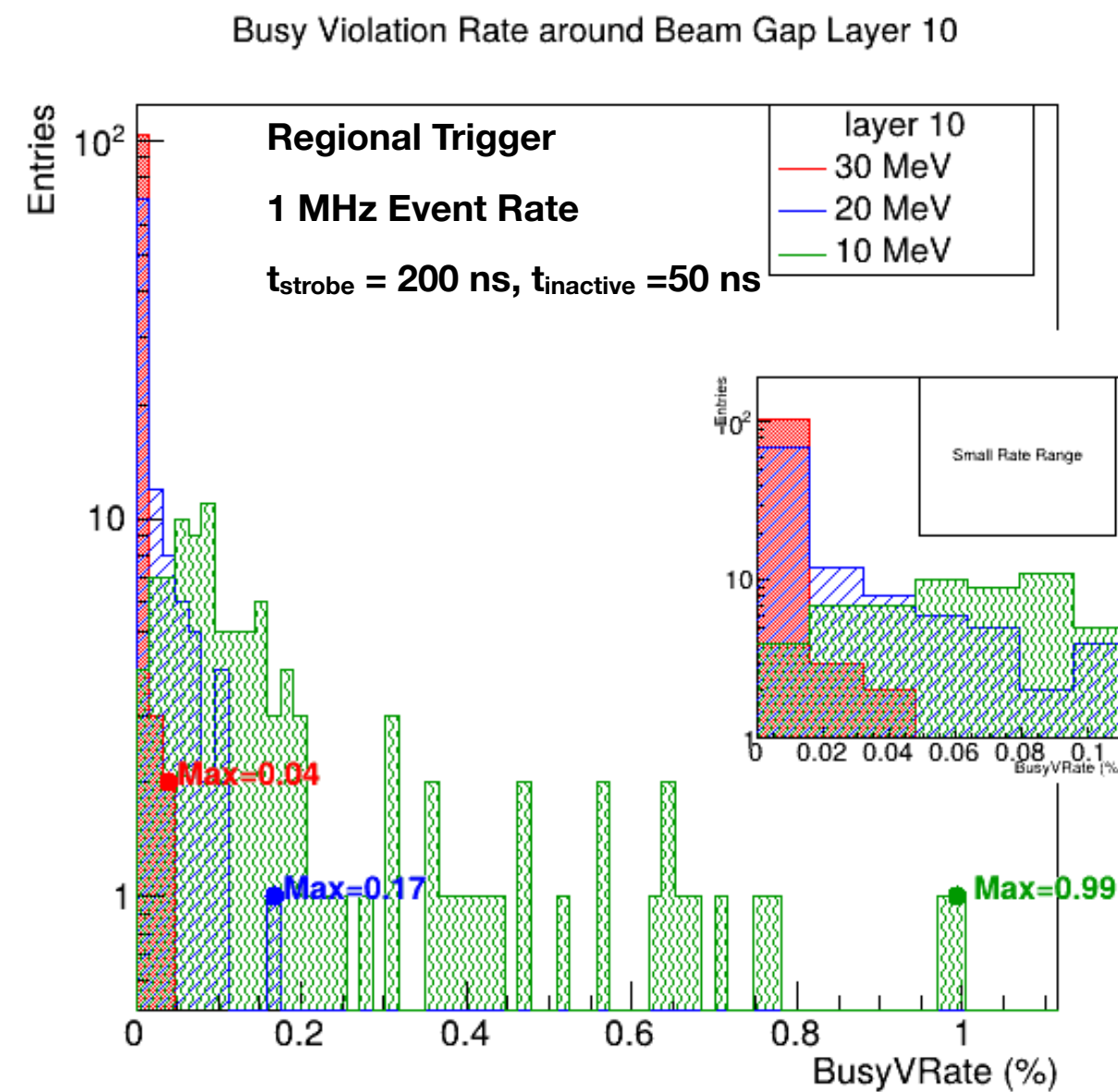
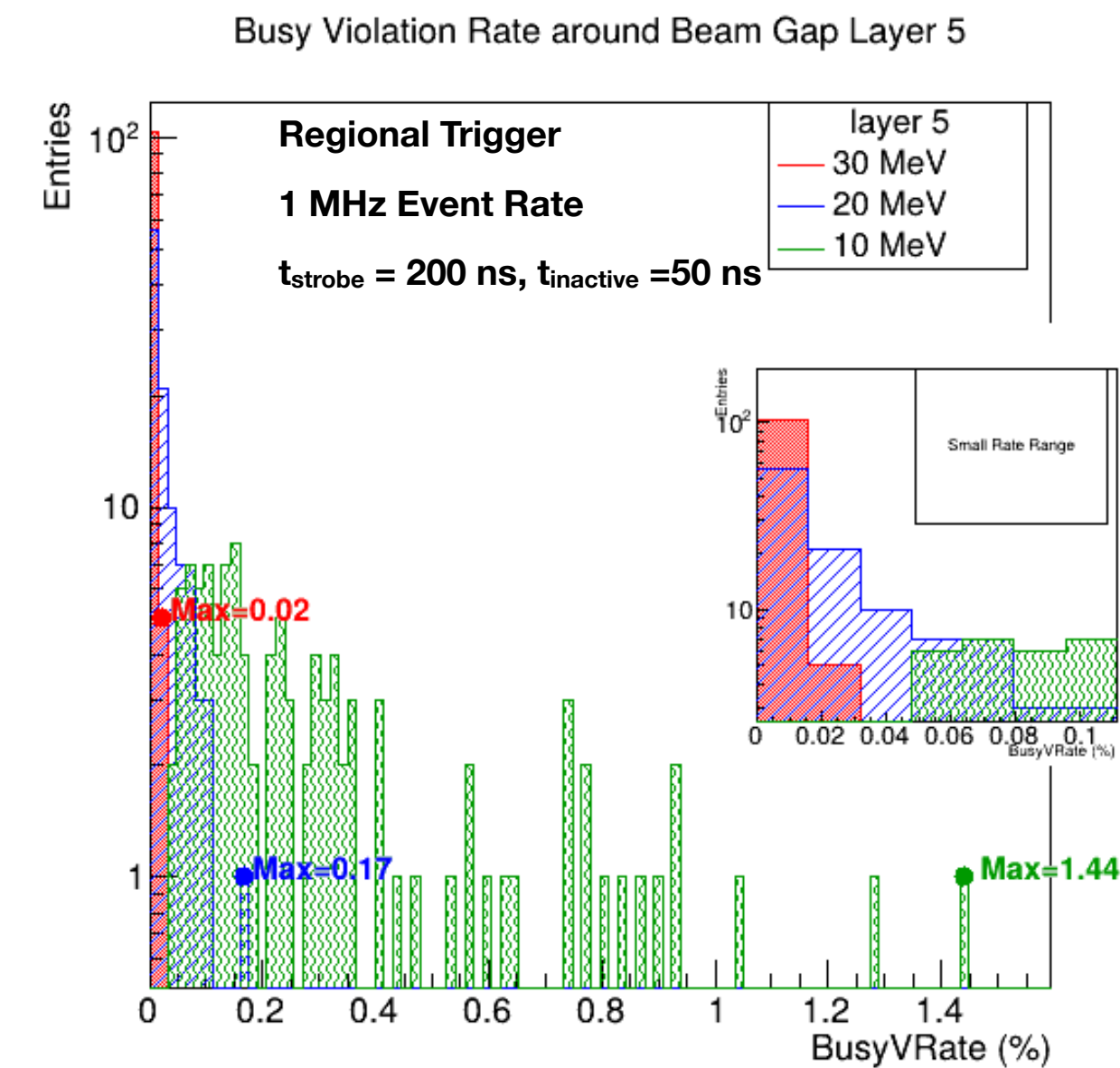
Using 45000 events

Energy Threshold : 10 MeV, 20 MeV, 30 MeV

10 MeV

20 MeV

30 MeV



Raising the threshold from 10 MeV to 30 MeV further **decreases** the BUSY violations down to about **0.04%**, greatly minimizing dead frames



## ALPIDE Chip Production Test

Test Platform: Production Test Box (PTB) or VCU118  
Provides **power** distribution, **slow control**, and **data readout**.

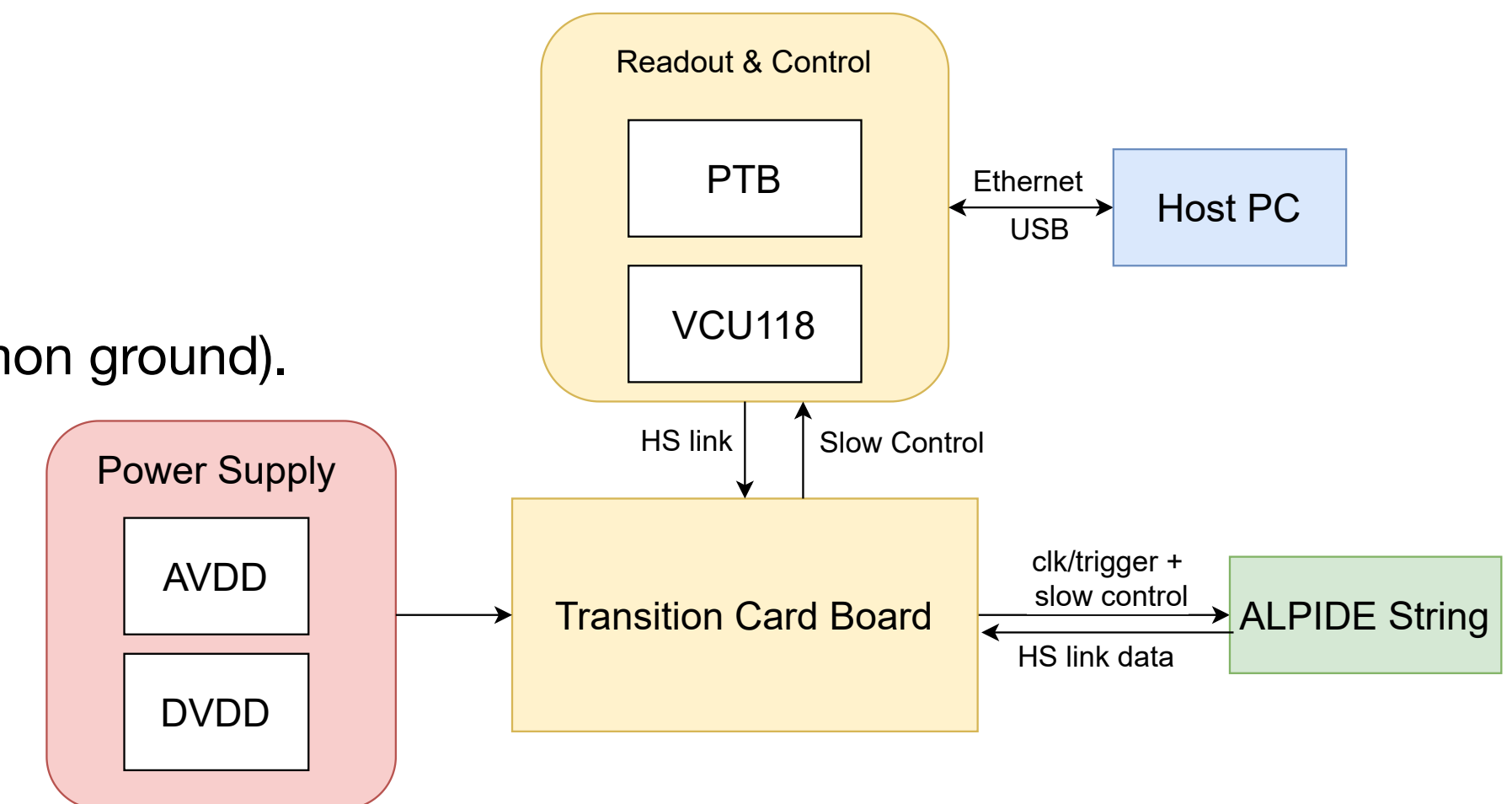
Test Module: Four ALPIDE module ( Top1, Top2, Bottom1, Bottom2 )

Each module consists of **3 strings**, and each string contains **9 ALPIDE** chips (total 27 chips per module).

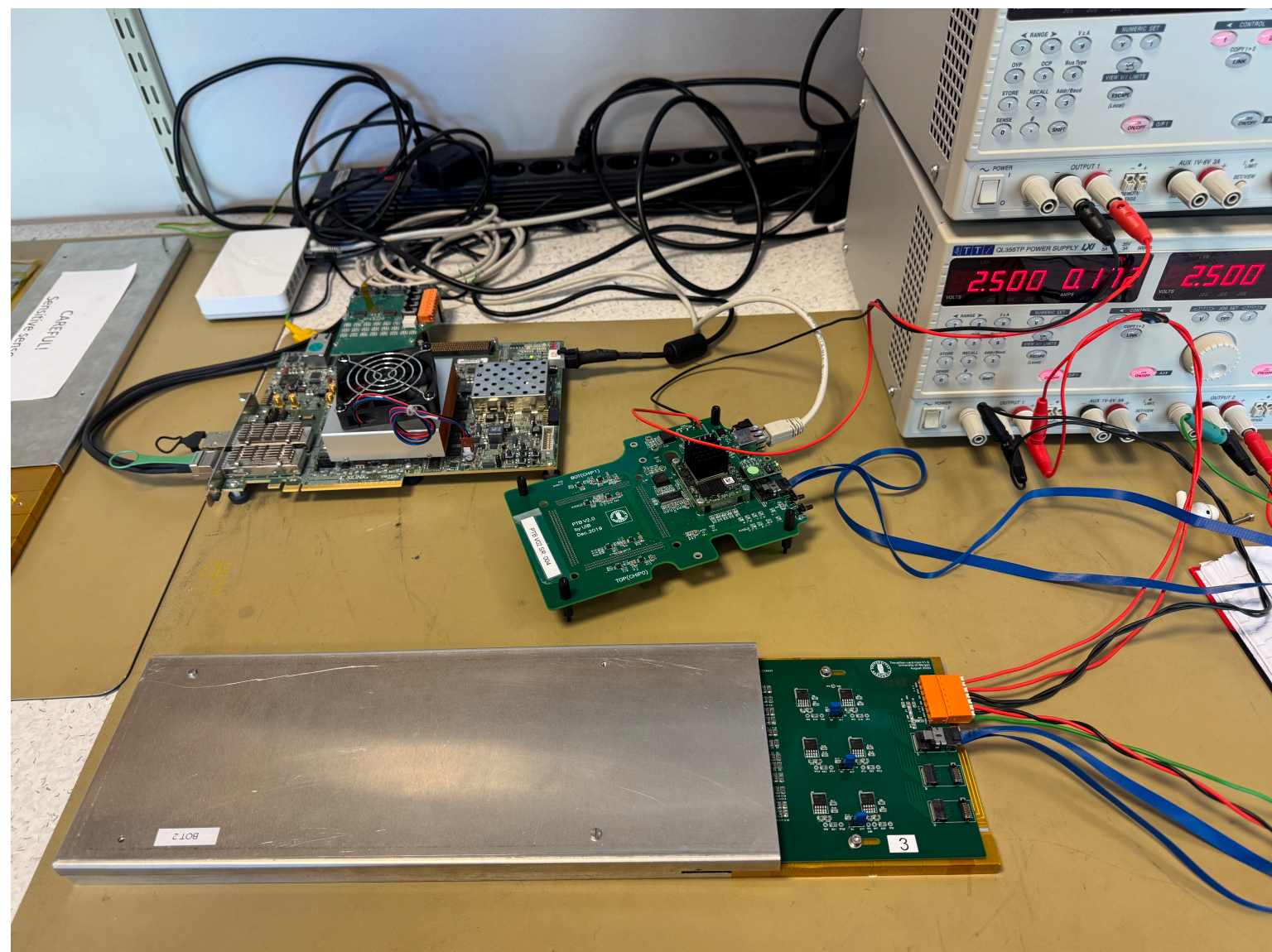
Power Supply: Programmable DC power supplies providing **AVDD (analog)** and **DVDD (digital)** rails (common ground).

Control Software: Automated Python test suite (**complete\_test\_suite.py**)  
Used for register checks, analog/digital/threshold scans, and FIFO verification.

### ALPIDE Test - Hardware Connections



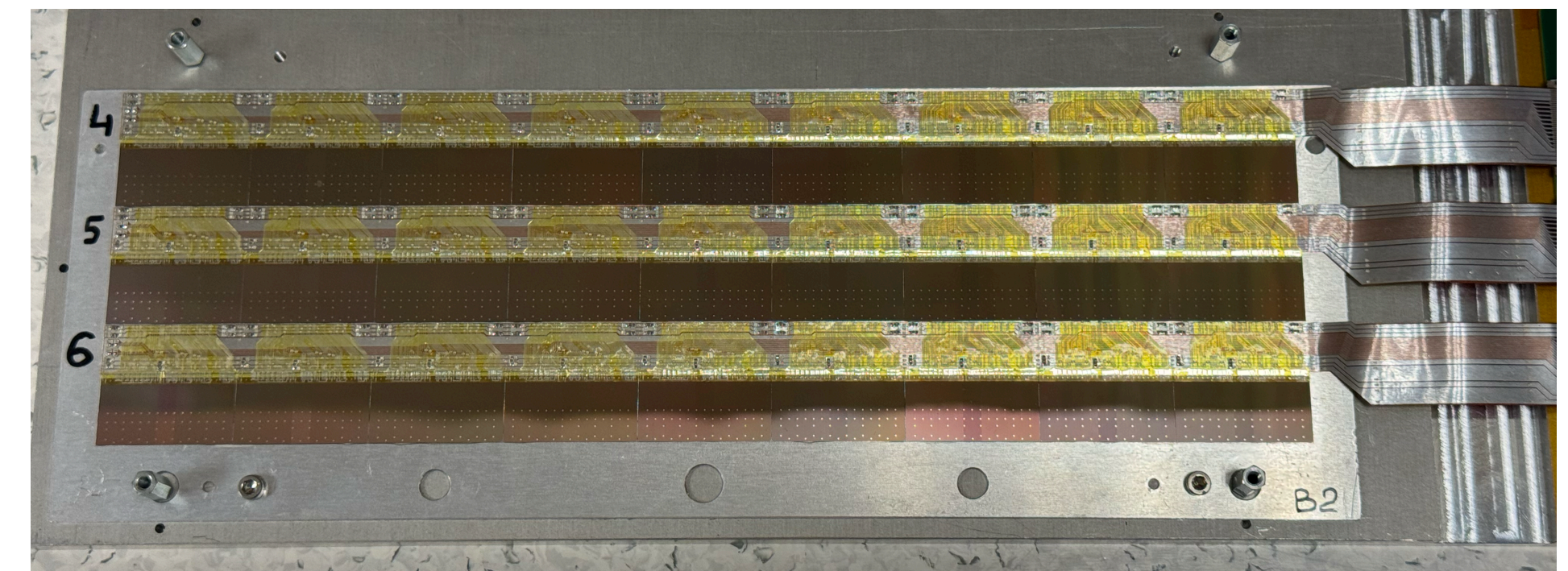
### Setup procedure for the ALPIDE chip



### Test List:

- Register test
- HS test
- Analog scan
- Digital scan
- Threshold scan
- FIFO test

### Bottom-2 module

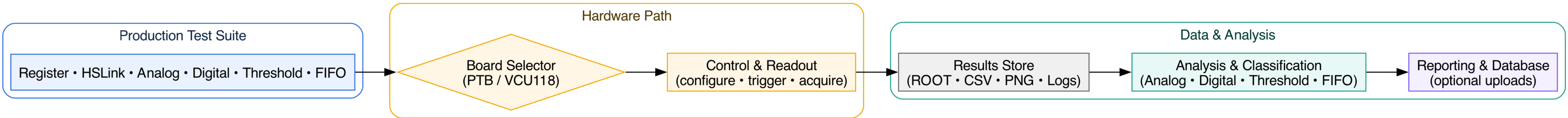






# ALPIDE Chip Testing Architecture

ALPIDE Production Test – Overview (Grouped)



**hardware\_health\_check.py** (Pre-test validation)

- Basic Level: connectivity, register integrity, communication health
- Extended Level: add pattern testing
- Stress Level: add register cycling stress tests.

**complete\_test\_suite.py** (Master Orchestrator)

- registertest.py (3 seconds)
- hslink.py (45 seconds)
- auto\_run\_analogscan.sh (2 hours)
  - analogscan.py
  - pixel\_stats.py
- digitalscan.py (30 minutes)
- auto\_run\_thresholdscan.sh (2 hours)
  - thresholdscan.py
  - threshold\_stats.py
- auto\_run\_fifotest.py (1 hour)
  - fifo.py
  - sweep\_delay\_test.py
- alpide\_fifo\_diagnostic.py (NEW option - 5-15 minutes)
  - SEU Monitoring
  - Manchester Encoding Comparison
  - Communication Stress Testing

Layered Automation Approach:

- **Level 1:** Individual test scripts (registertest.py, hslink.py, etc.)
- **Level 2:** Test-specific automation scripts (auto\_run\_\*.sh/py)
- **Level 3:** Complete test suite orchestration (complete\_test\_suite.py)
- **Special:** System health validation (hardware\_health\_check.py)

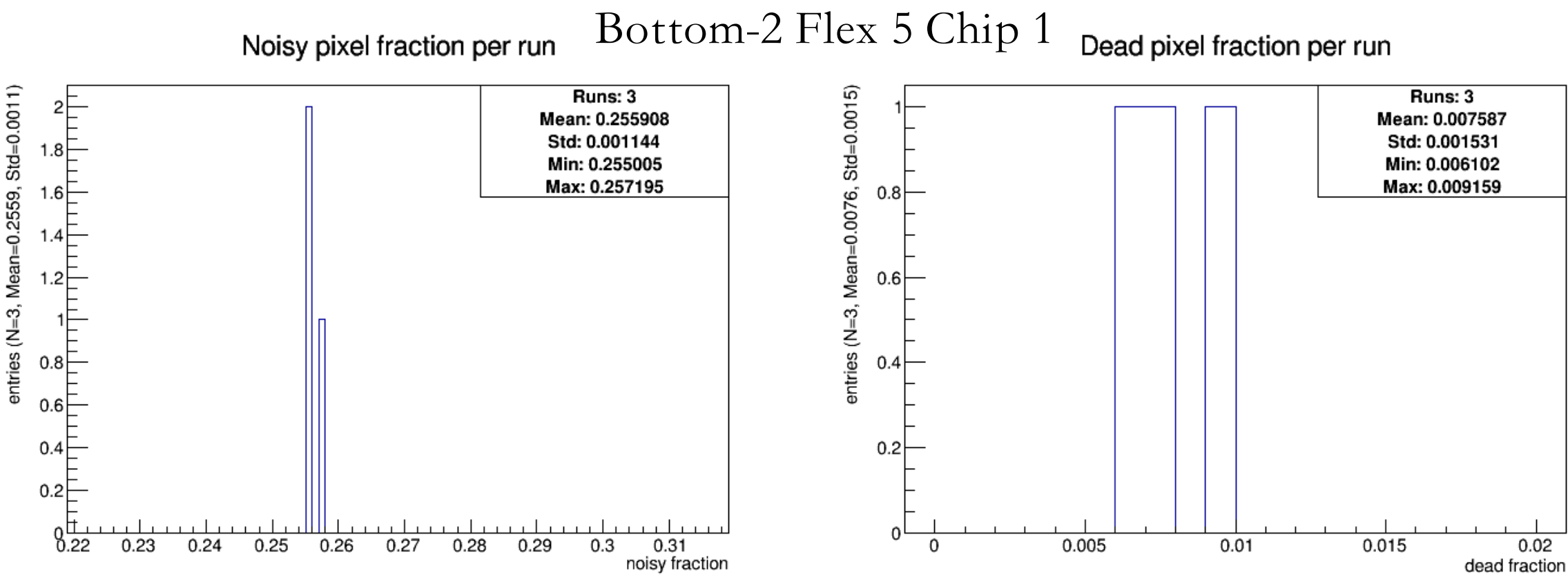
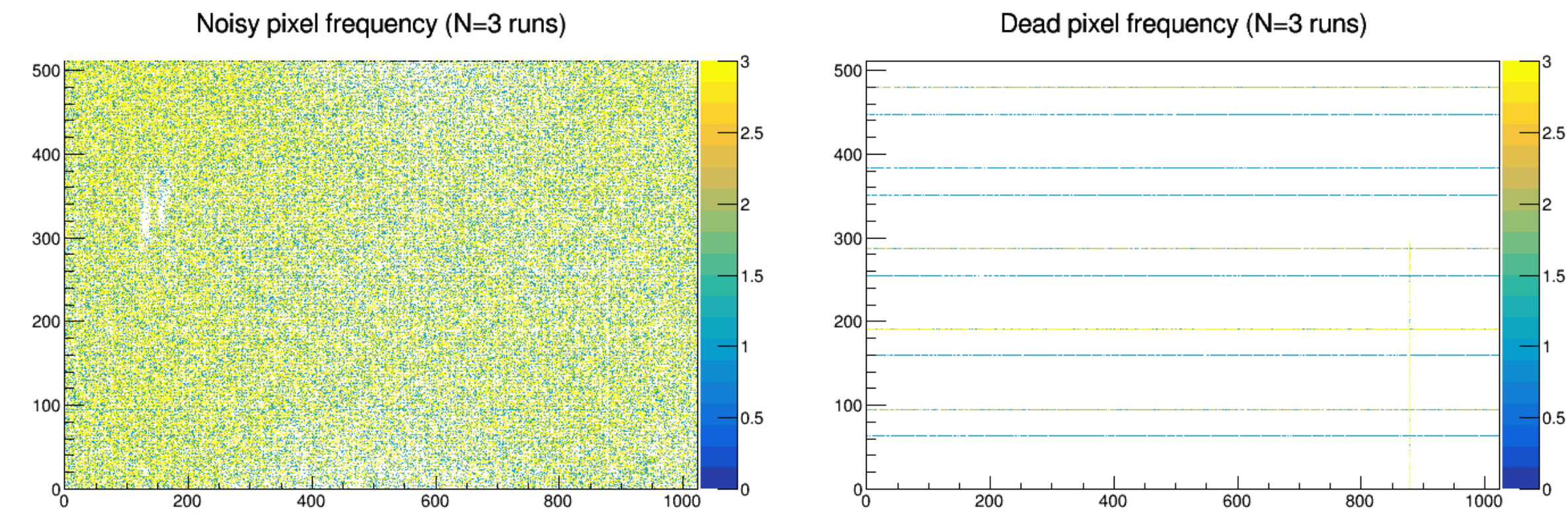
```
bash-4.4$ python complete_test_suite.py --test-name TEST_v5 --board PTB --module BOTTOM2-c8 --string S4 --chips=8 --only-test analog
2025-08-27 16:49:41,188 - INFO - ALPIDE Complete Test Suite Started
2025-08-27 16:49:41,188 - INFO - Test Name: TEST_v5
2025-08-27 16:49:41,188 - INFO - Results Directory: /ssdwork/jiyi41006/src/production_tests/results/TEST_v5
2025-08-27 16:49:41,188 - INFO - Board: PTB, Module: BOTTOM2-c8, String: S4
2025-08-27 16:49:41,188 - INFO - Chips: 8, FIFO Iterations: 20
2025-08-27 16:49:41,188 - INFO - Only Tests: {'analog'}
2025-08-27 16:49:41,188 - INFO - =====
2025-08-27 16:49:41,188 - INFO - STARTING COMPLETE ALPIDE TEST SUITE
2025-08-27 16:49:41,188 - INFO - =====
2025-08-27 16:49:41,188 - INFO - ❌ Skipping Register Test (not in --only-test list)
2025-08-27 16:49:41,188 - INFO - ❌ Skipping High-Speed Link Test (not in --only-test list)
2025-08-27 16:49:41,188 - INFO - =====
2025-08-27 16:49:41,188 - INFO - RUNNING: Analog Scan
2025-08-27 16:49:41,188 - INFO - =====
2025-08-27 16:49:41,188 - INFO - Starting: Analog Scan (3 runs)
2025-08-27 16:49:41,188 - INFO - Command: bash auto_run_analogscan.sh --module BOTTOM2-c8 --string S4 --chips 8 --runs 3
2025-08-27 16:49:41,188 - INFO - 🔄 Showing real-time output for Analog Scan (3 runs)
2025-08-27 16:49:41,188 - INFO - =====
```

Overall, **complete\_test\_suite.py** and **hardware\_health\_check.py** serve as the main controllers of all tests.



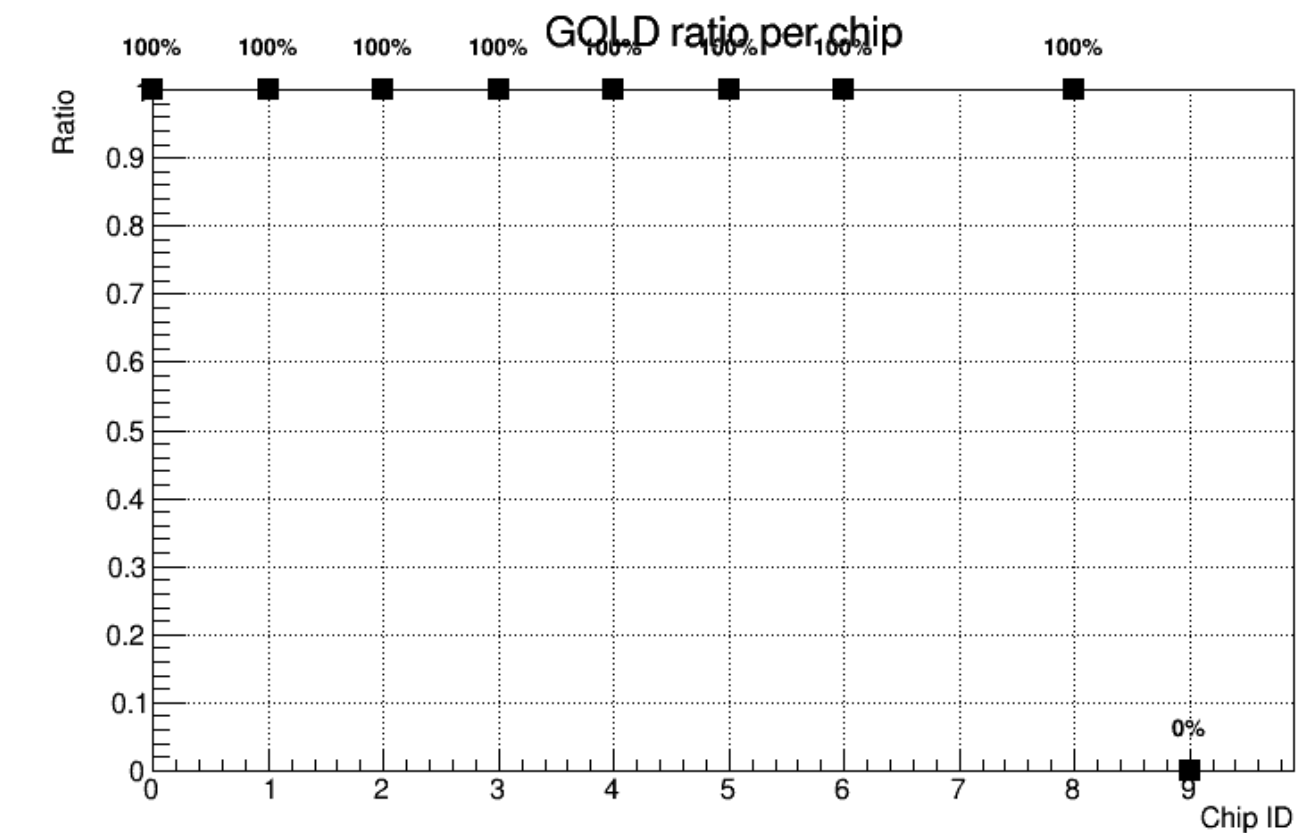
## Analog Scan:

- Analog Scan measures pixel activity under injected charge and classifies each chip based on **noisy** and **dead** pixel counts.
- The script builds ROOT histograms per column/row, exports CSV summaries, and applies production grading rules.



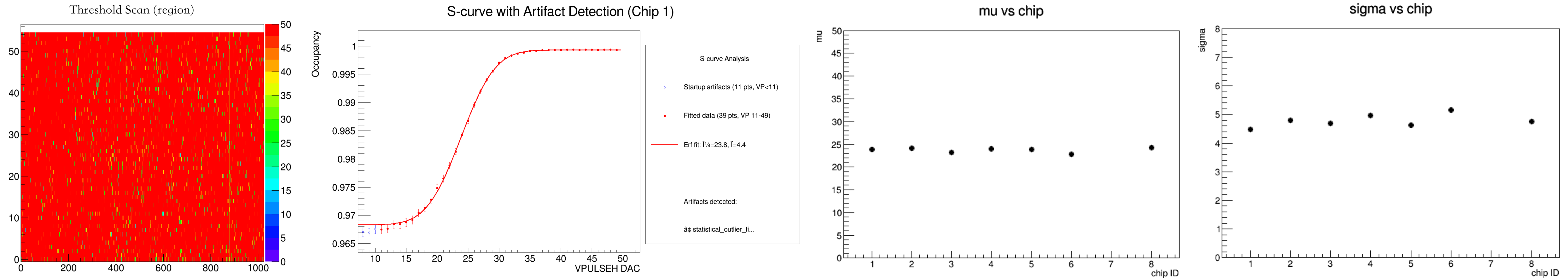
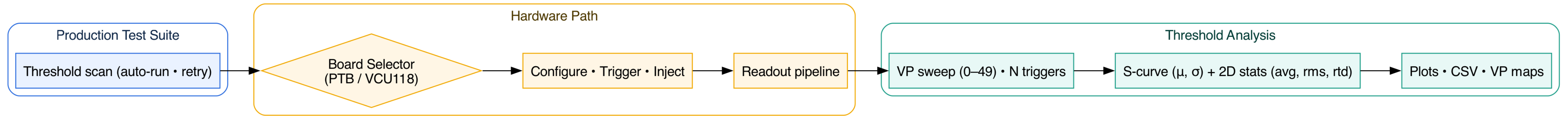
## FIFO Test:

- FIFO Test verifies the ALPIDE offload memory by writing deterministic patterns and reading them back either per-address (SINGLE mode) or per-region (REGION mode).
- Performs repeated runs, collects logs/CSVs, and aggregates **GOLD** ratios per chip for production statistics.





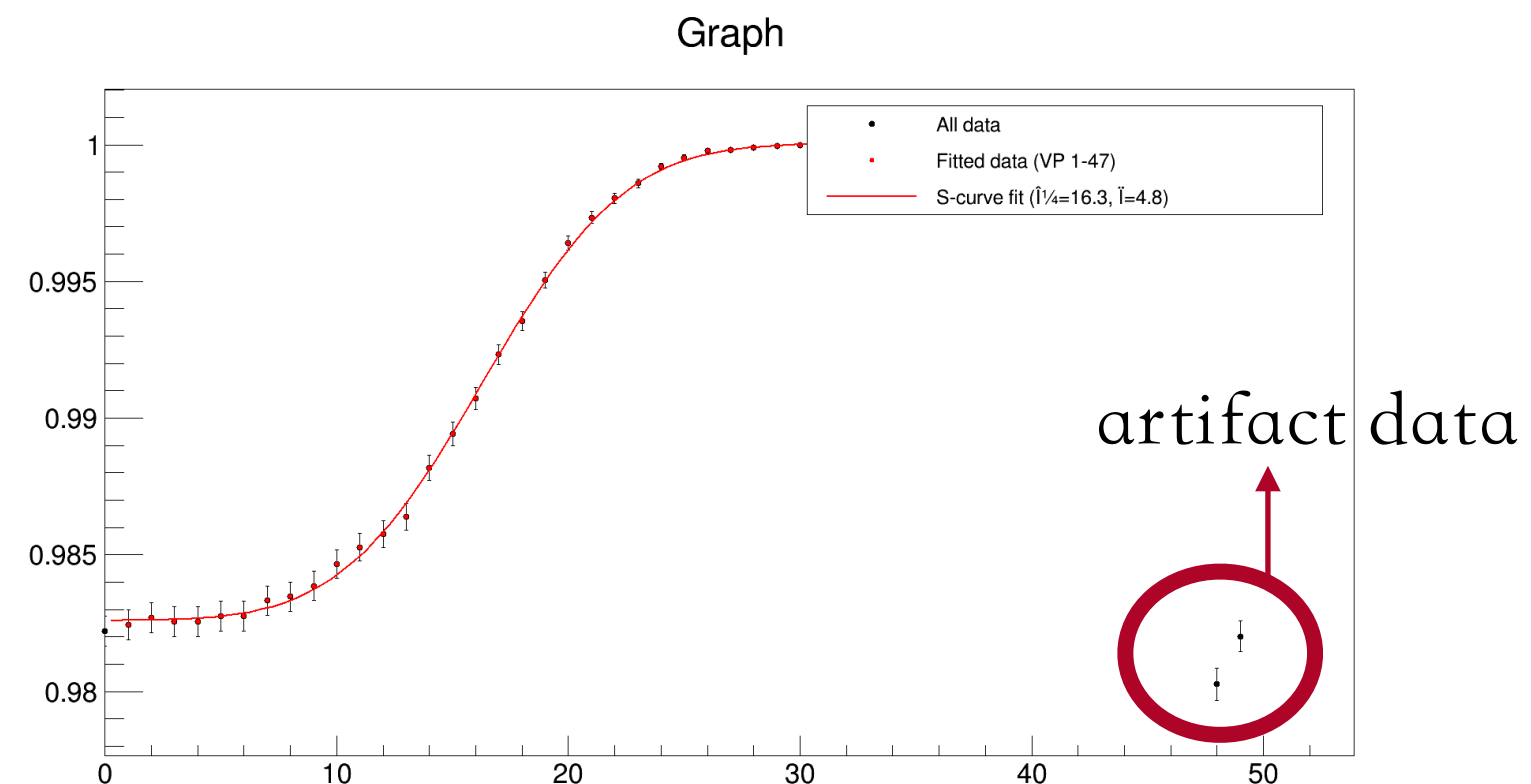
ALPIDE Threshold Test – Overview (Grouped)



Since the tests are performed in a laboratory environment, various external factors can affect the measurements.

In the lab, the **S-curves** sometimes produces **artifact data** that cause the fit to fail. To address this, an additional **artifact detection** mechanism was implemented in the data processing to ensure result stability.

The chips should be **in the dark room** in order to test the threshold scan.



Add an extra card box to cover the whole module

Aluminium cover was **not sufficient** to shield the chip from ambient light, which caused the noise signals.





## BUSY Violation :

- The overall BUSY violation rate is low (with a maximum of 5%-6%).
- The bottleneck is regional read-out.
- Regional trigger decreases the BUSY violations down to about 0.04%

## Options to Reduce BUSY Violations:

- Combine longer frames, strobe-inactive extension, back-bias, grid-masking, and regional trigger to reduce BUSY and BUSY-violation rates.
- Together these optimizations keep  $\geq 95-99\%$  of timeframes within 0–1 BUSY-violating links, even under high-occupancy conditions near the beam-pipe gap.

## Pixel layer module production test:

- Execute automated register, HSLink, analog, digital, threshold, and FIFO tests on PTB/VCU118.
- Implemented an additional artifact detection mechanism to ensure result stability.
- Tests are progressing in an orderly manner, and the modules evaluated so far exhibit good overall health and stable performance.

In simulation, FoCal ALPIDE chips perform well, and we identified several effective strategies to reduce BUSY violations.

In hardware, the modules tested to date show correspondingly solid performance.