Performances of the hybrid of LGAD and LATIC

Li Zhuang

2025.10.28

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

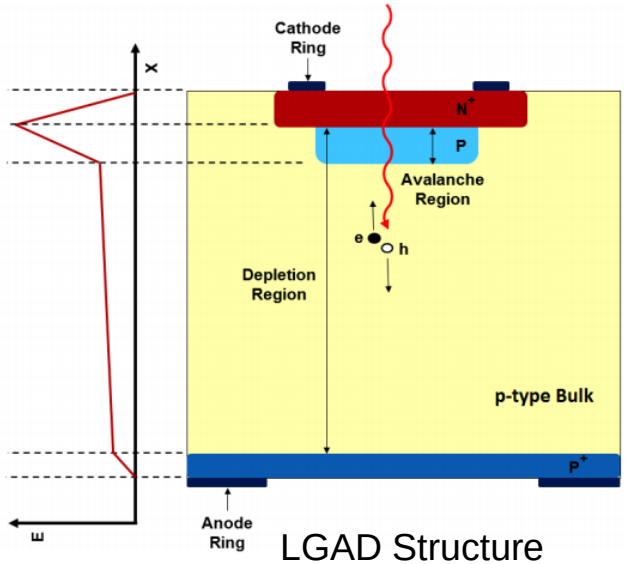
MODERN PHYSICS DEPARTMENT

Outline

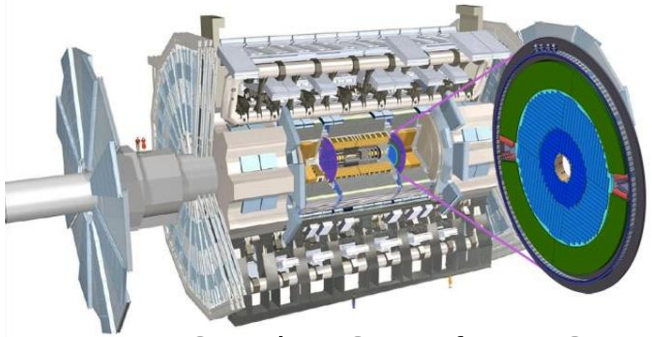
- Background
- LATIC Structure and Electronic Performance
- Flip Chip Bonding of LGAD and LATIC
- Hybrid Test
- Summary

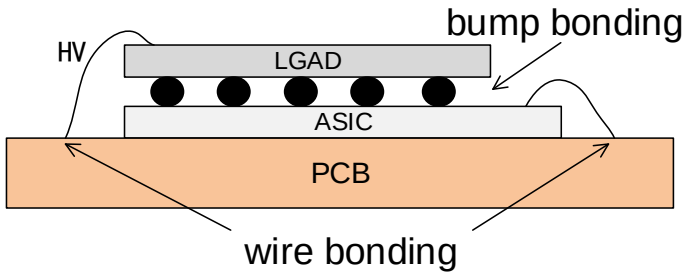
Background: LGAD and The Electronic Readout

- LGAD: Low Gain Avalanche Detector
  - Structure: n-in-p silicon detectors containing an extra highly-doped p-layer.
  - Used for dealing with pill-up through its high time resolution and high spatial granularity.
- Electronic characteristics:
  - Rise time： ~ 500 ps
  - Signal duration: ~1 ns
  - Charge: 10fC
  - Detector capacitance: ~ 4 pF
- Readout requirements:
  - Flip-chip bonding the sensor with the front-end readout chip.
  - High speed and low-noise preamplifier and discriminator.
  - High precision TDC.

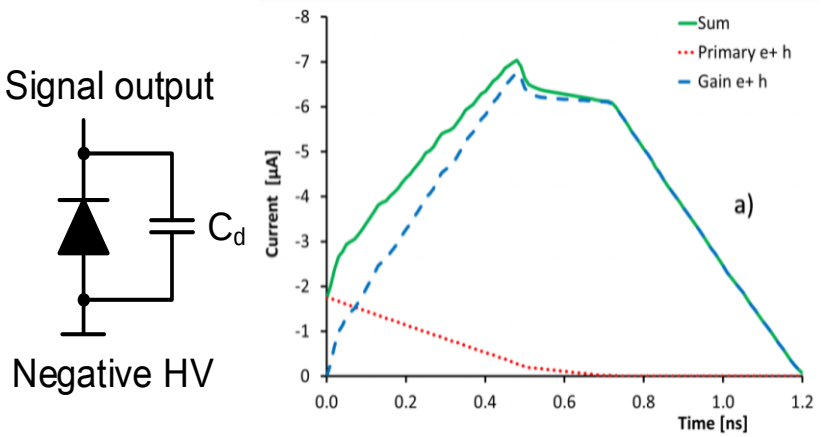


LGAD Structure


LGAD in HGTD of ATLAS



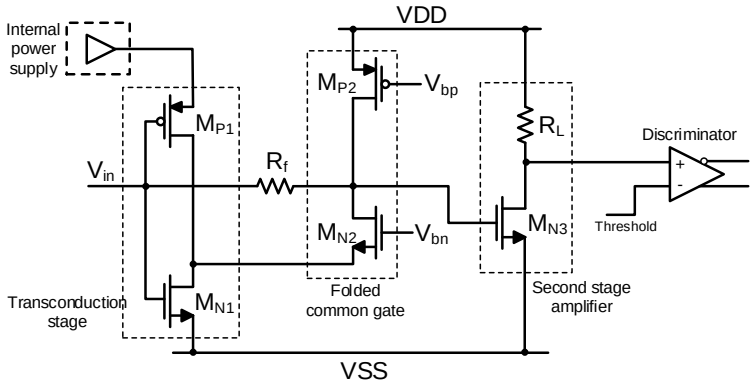
Hybrid of LGAD and the front-end readout ASIC



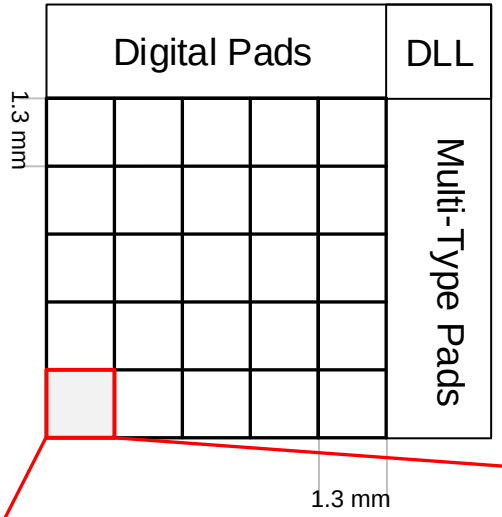
LGAD electronic model and signal

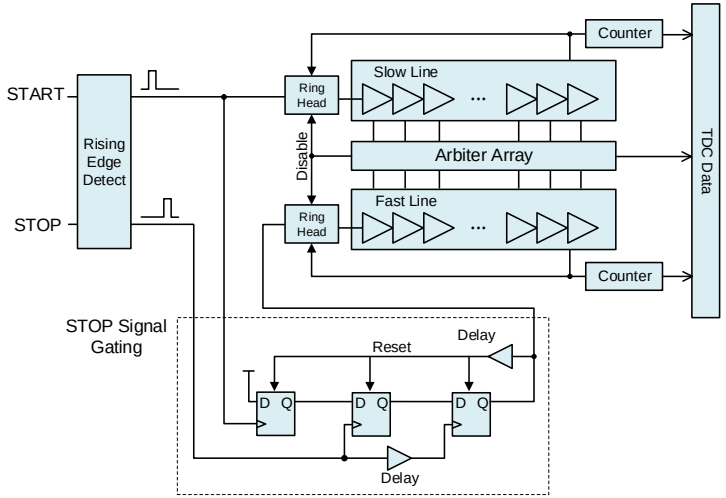
LATIC: LGAD Readout Prototype ASIC Designed at USTC

- LATIC: LGAD Amplification and Timing IC
- 25 channels, 1.3 mm pitch
- Pre-Amplifier:
  - CMOS cascode pre-amplifier.
    - for lower noise and better time performance.
- TDC:
  - Dual-ring vernier TDC
    - for fine binsize and large measurement range.

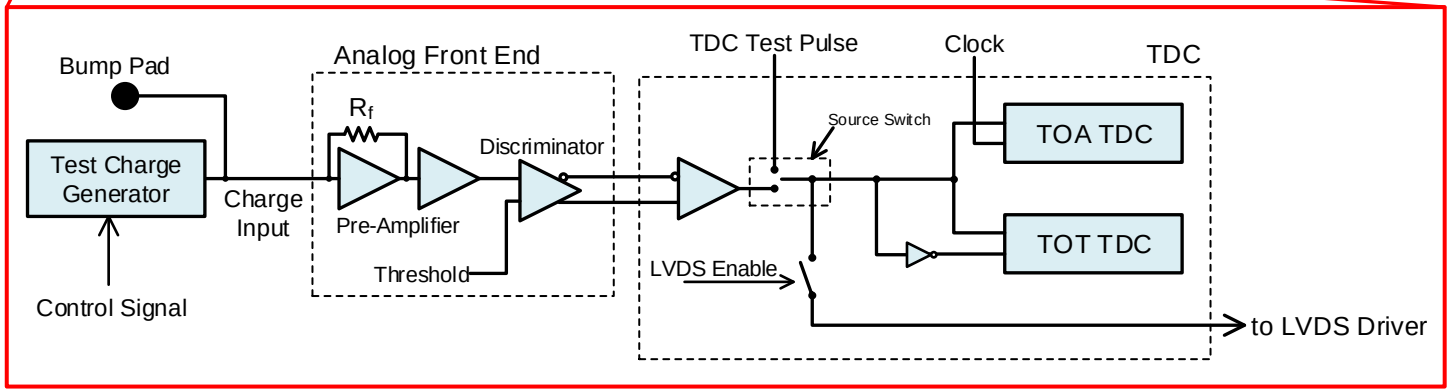


CMOS Cascode Pre-Amplifier





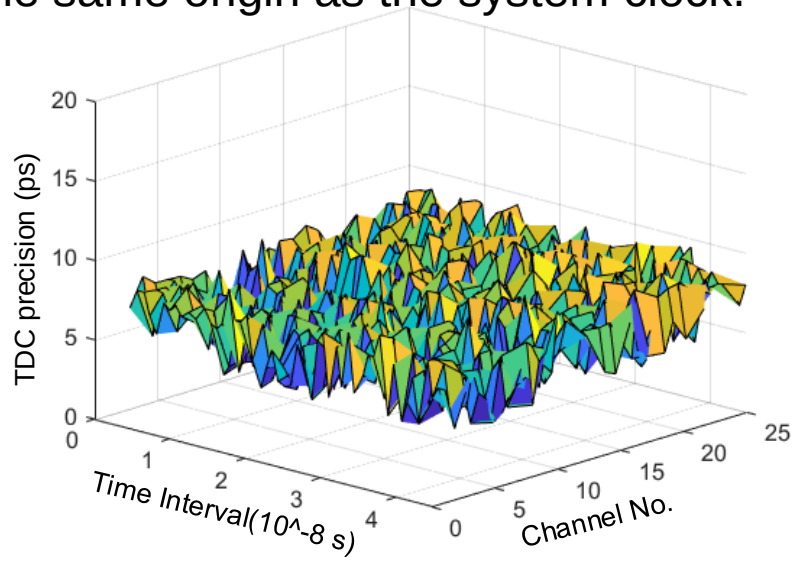
Dual-ring Vernier TDC

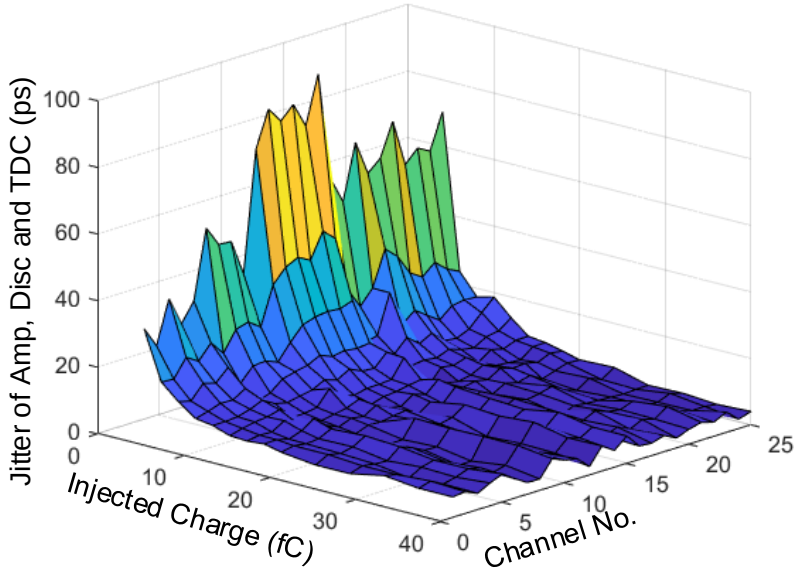


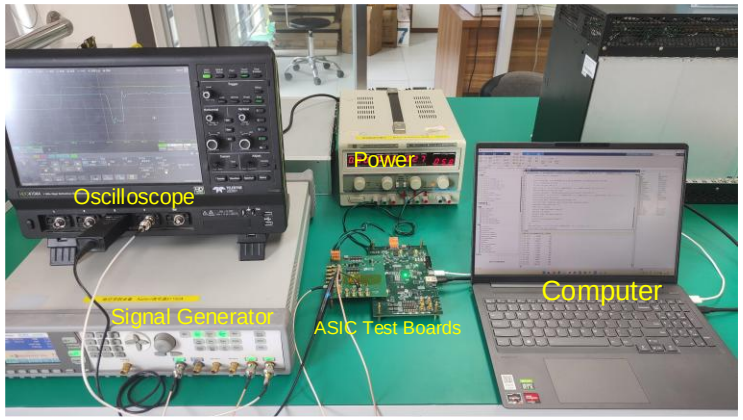
[1] Chen H , Li Z , Cai Y ,et al. Design of high-precision time measurement prototype ASIC for the LGAD readout[J].Nuclear Instruments and Methods in Physics Research, Section A. Accelerators, Spectrometers, Detectors and Associated Equipment, 2024:1064.DOI:10.1016/j.nima.2024.169302.

LATIC electronic performance

- TDC test:
  - Inject external TDC test signal of the same origin as the system clock.
  - TDC precision: <10 ps
  - Non-Linearity: INL<1 DNL<2
- Full-chip test:
  - Generate test signals within the chip.
  - 4 pF dummy capacitor.
  - Jitter: <20 ps at 10 fC input charge





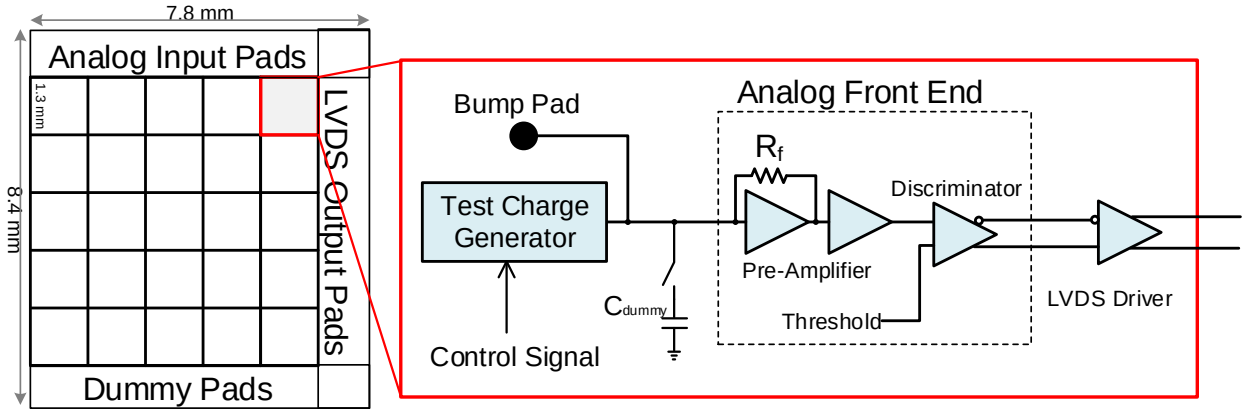


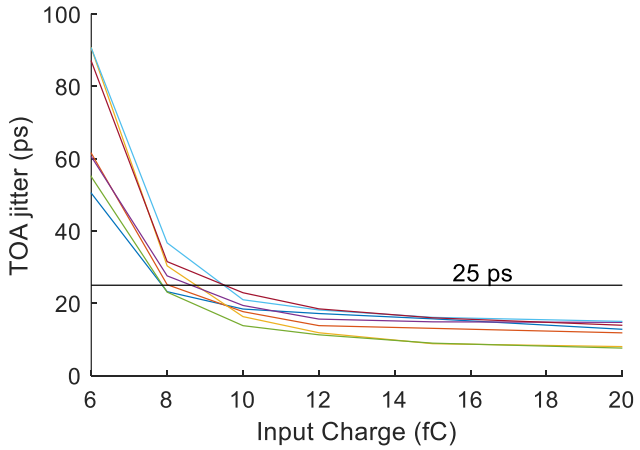
key design parameters of LGAD readout ASICs.

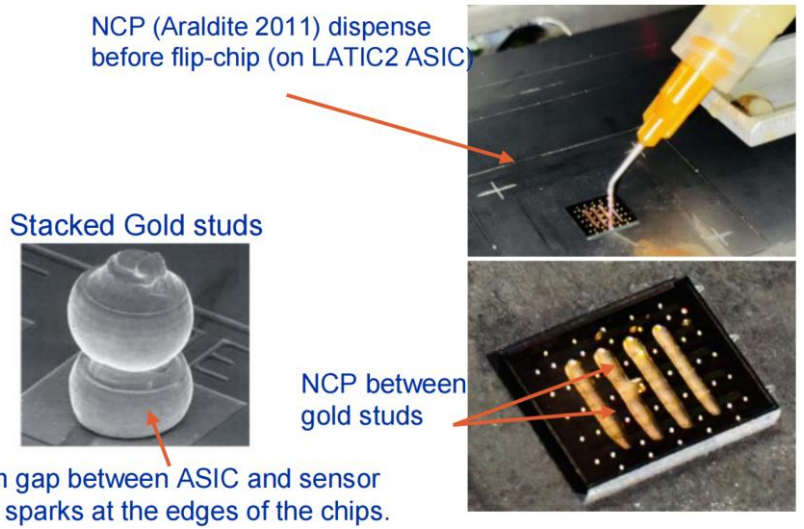
ASIC	ALTIROC0	ALTIROC1	ETROC0	ETROC1	LATIC0	LATIC1
Technology	130 nm	130 nm	65 nm	65 nm	180 nm	130 nm
LGAD pad size	1.3 × 1.3 mm^2	1.3 × 1.3 mm^2	1.3 × 1.3 mm^2	1.3 × 1.3 mm^2	1.3 × 1.3 mm^2	1.3 × 1.3 mm^2
Channel number	8	5 × 5	1	5 × 5 (4 × 4 with full chain)	8 / 5 × 5	5 × 5
Integrated TDC	no	yes	no	yes	no	yes
σ_{TOA} @	27 ps	<25 ps	<16 ps	~42 ps beam test with sensor	<20 ps	<20 ps
Charge	10 fC	10 fC	15 fC sensor cap.		10 fC	10 fC
Capacitance	3.3 pF	4 pF			6 pF	4 pF

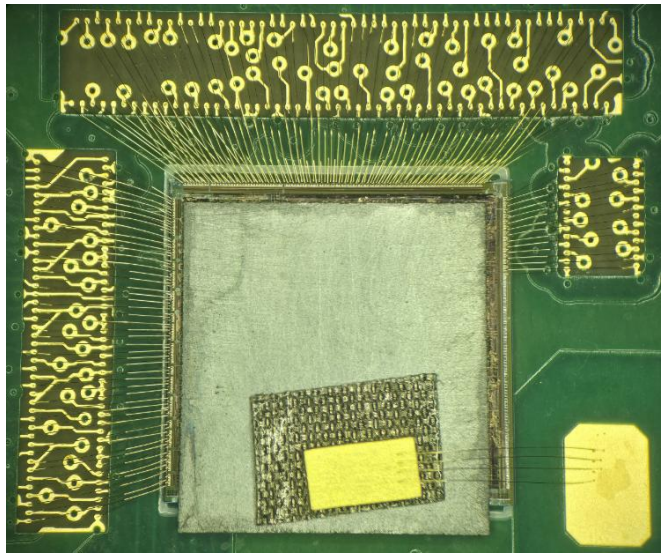
Flip-Chip Bonding of LGAD and LATIC

- LGAD sensor: USTC IME sensor
- ASIC: LATICv2
  - Mid version, discriminator LVDS out, no TDC.
  - jitter < 25 ps @10 fC
- 5x5 pixels, 1.3mm square pitch
- Flip-Chip processing:
  - Deposition of double gold studs on LATIC2 ASICs
  - Argon plasma cleaning for both ASICs and sensors
  - Applying Araldite 2011 glue on ASIC in 4 lines between gold studs
  - Align ASIC and sensor, thermo-compression bonding





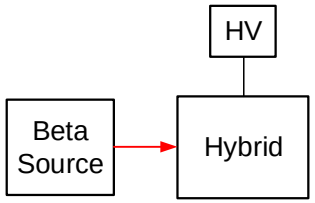


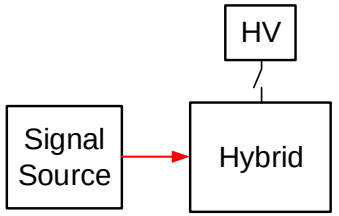


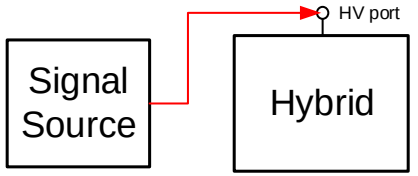
·Thanks to CERN (Dominik Dannheim) and Geneva U. (Mateus Vicente) and their teams for helping with flip chip bonding.

Hybrid Test: Connectivity

- Test method: the connectivity was tested using the different methods, and the results were consistent.







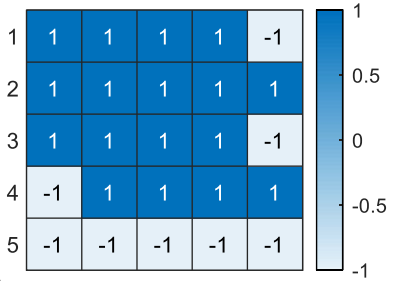
- Result:
  - Partial channels are connected.
  - Some channels have abnormal functions. (Possible short circuit caused by bump bonding)
  - The connectivity changes over time.(Temperature and humidity changes)

Paths and circuits under the solder pads should be avoided.

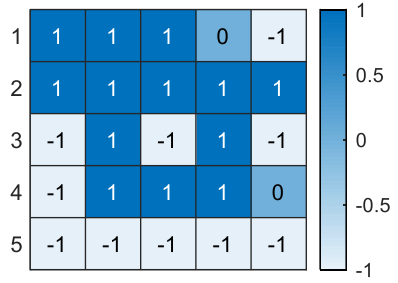
-1	: abnormal
0	: unconnected
1	: connected

Hybrid1：

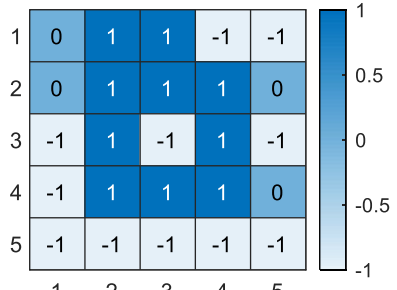
June



July

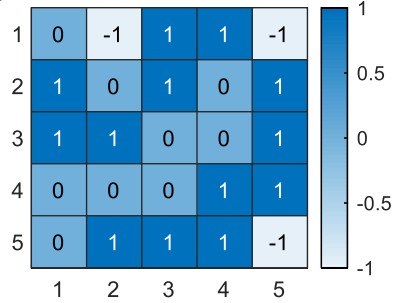


August

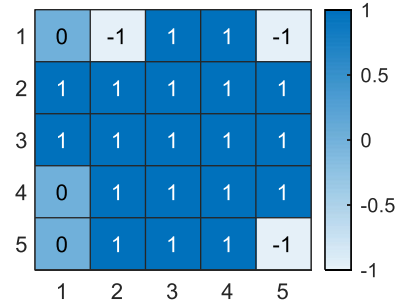


Hybrid2：

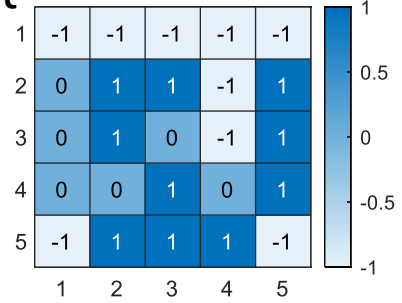
June



July

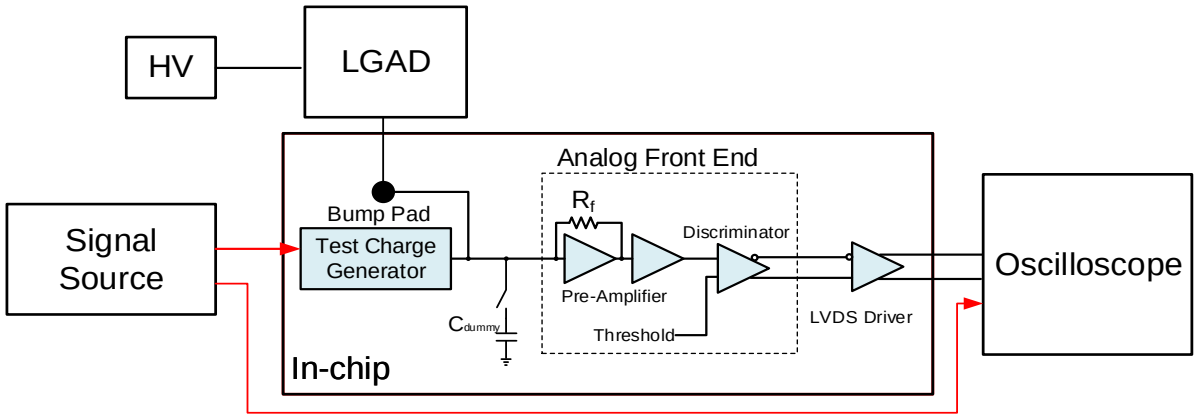


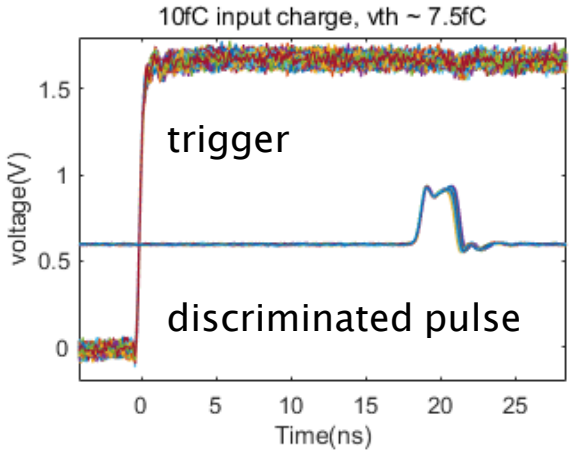
August

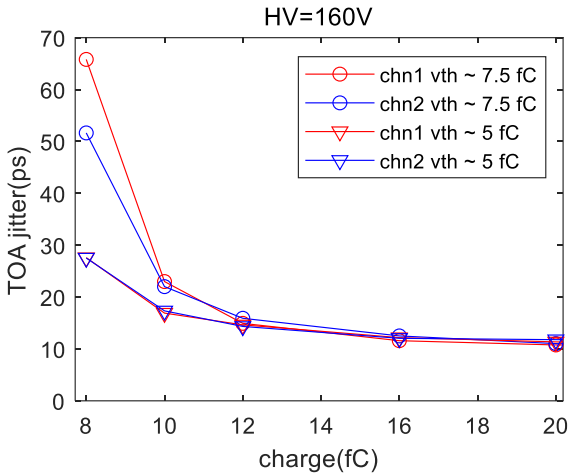


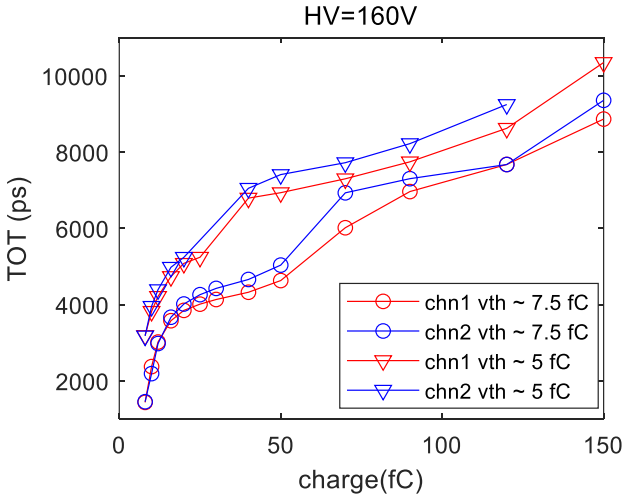
Hybrid Test: Electronic Test

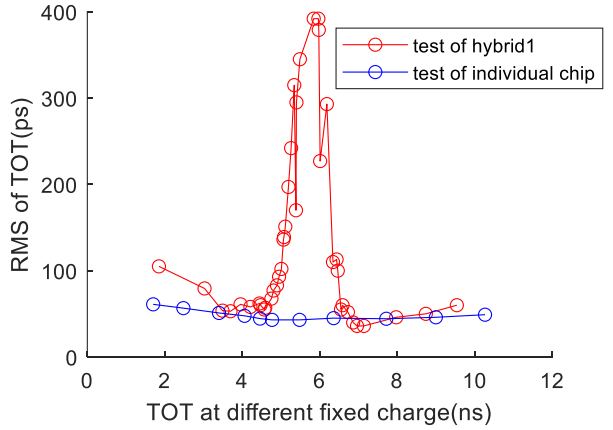
- Test conditions: HV 160 V; Room temperature.
- TOA jitter < 25 ps at 10 fC input charge.
- The linearity of TOT with charge is not good, TOT jitter increases in the 5ns ~ 7ns interval.
  - Due to layout design error, failure to isolate digital ground and analog ground.





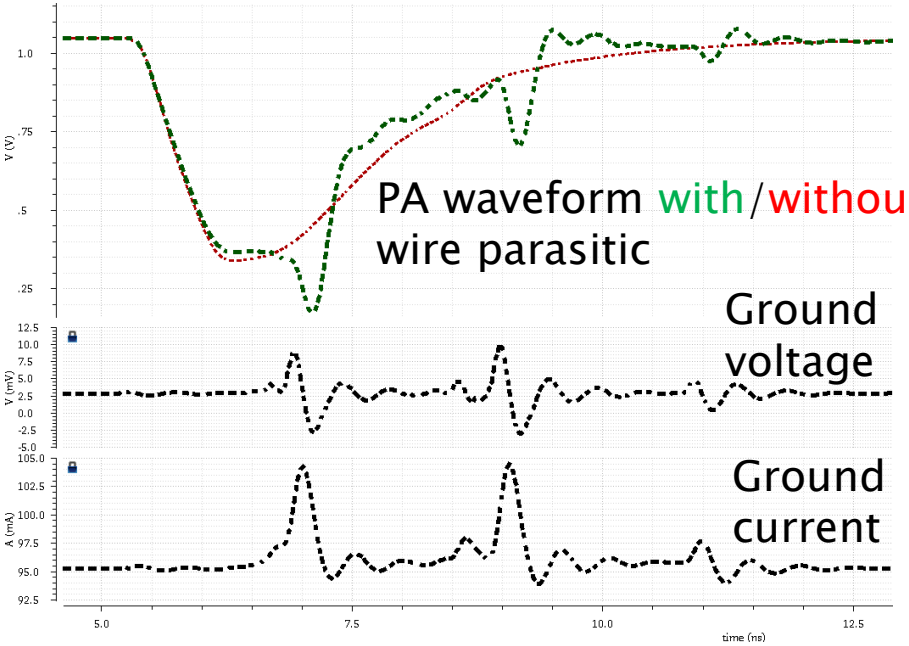


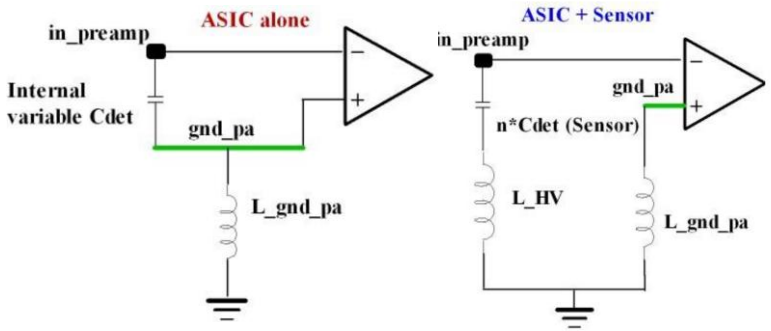


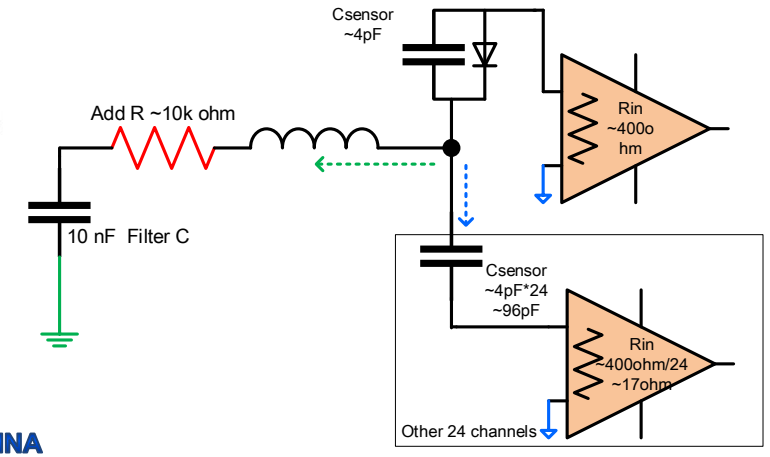


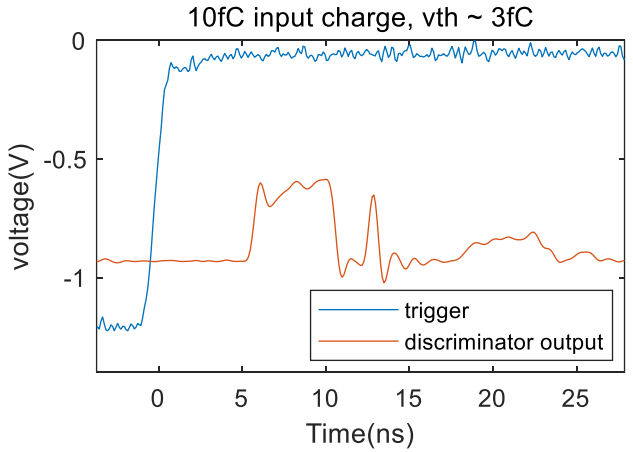
Hybrid Test: Electronic Test

- **Why bad TOT jitter?**
  - The voltage fluctuation of in-chip ground caused by transmission buffer and bonding parasitic(mainly inductance).
- Simulation verification:
  - Simulate with the wire bonding parasitic using 0.1 nH and 30m ohm.
- Test verification：
  - Turn down the threshold and multiple pulses occurrence at the trailing edge of the waveform.（Not seen in ASIC individual test）
- Possible solutions:
  - In testing: Add a high-voltage decouple resistor to achieve better consistency between the high voltage and the in-chip ground. (not good effect for small channel number)
  - In ASIC design: Isolate the ground between the pre-amplifier and other circuits.



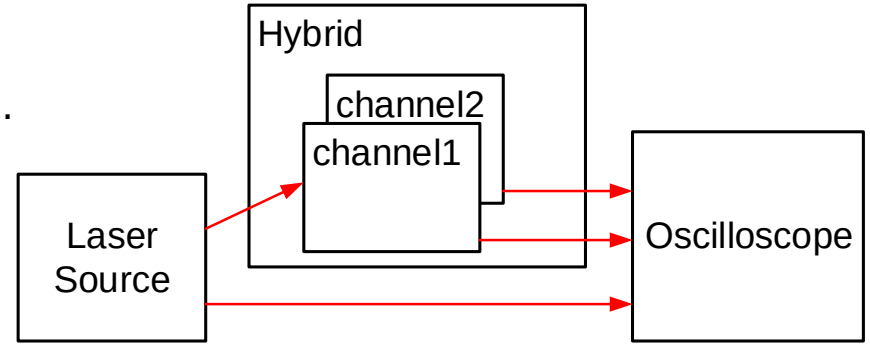


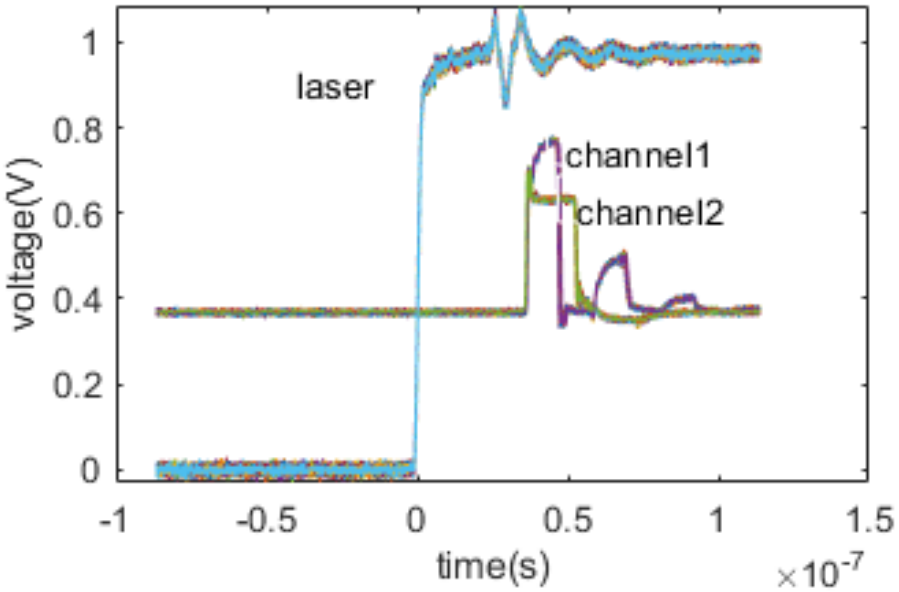


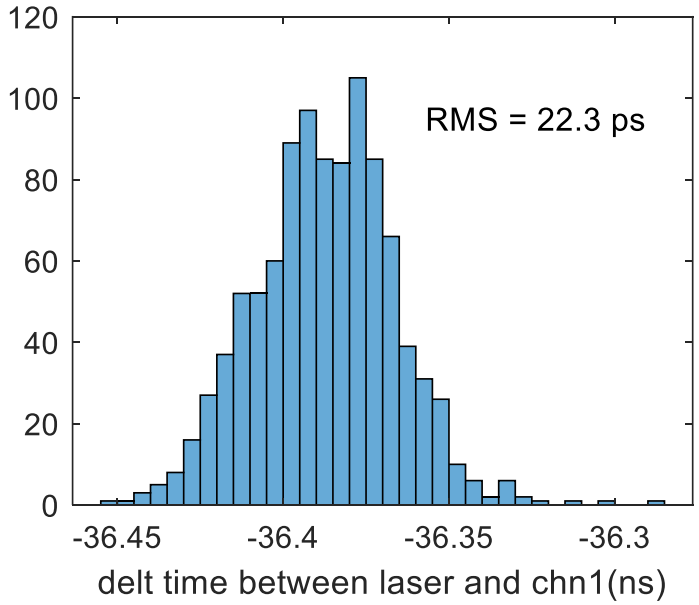


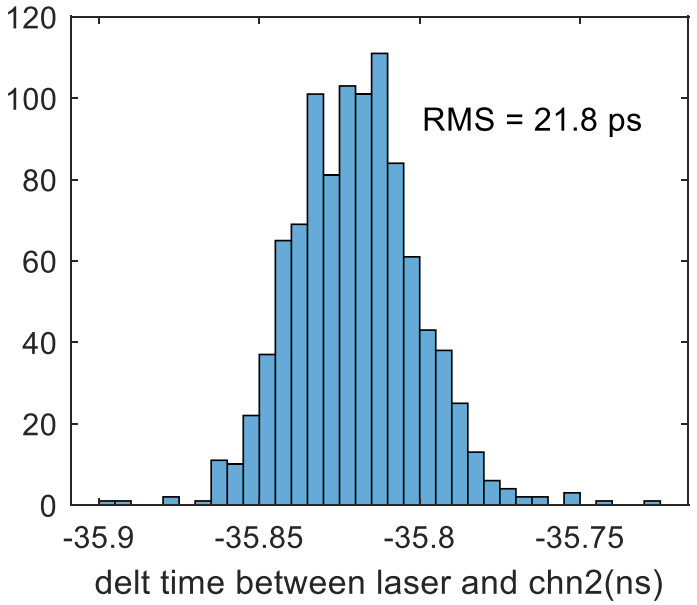
Hybrid Test: Laser Test

- Test method:
  - Irradiate the sensor with laser on both channel 1 and channel 2.
  - Measure the discriminated pulse and the laser synchronous electrical signal.
- Test result:
  - The time difference jitter between laser and channel1: 22.3 ps
  - The time difference jitter between laser and channel2: 21.8 ps



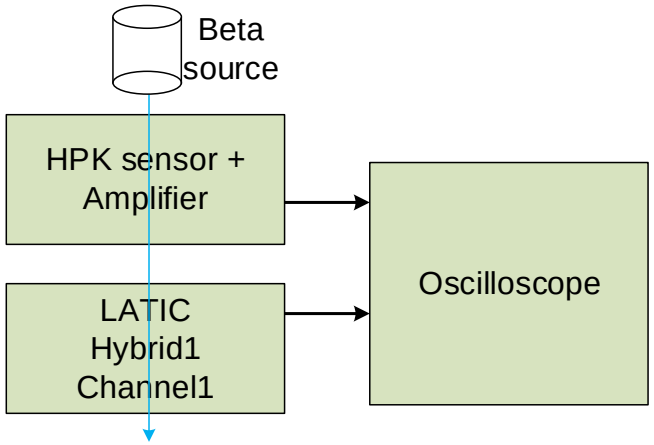


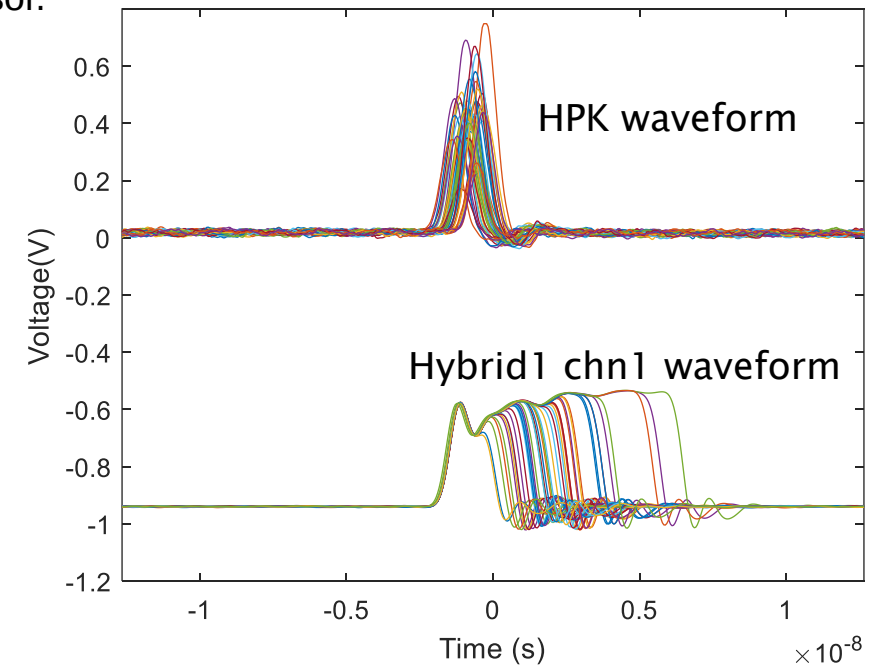


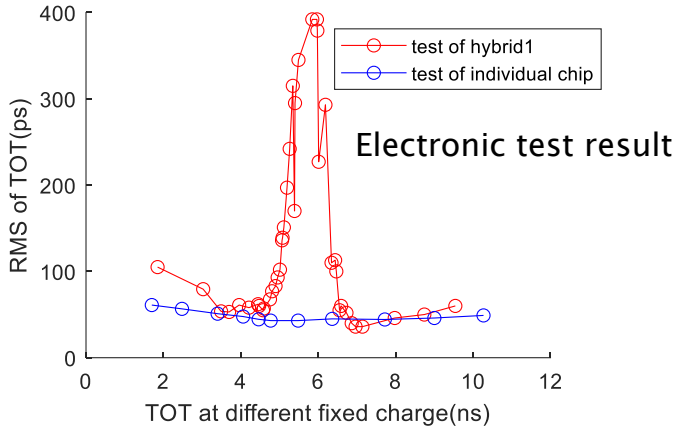


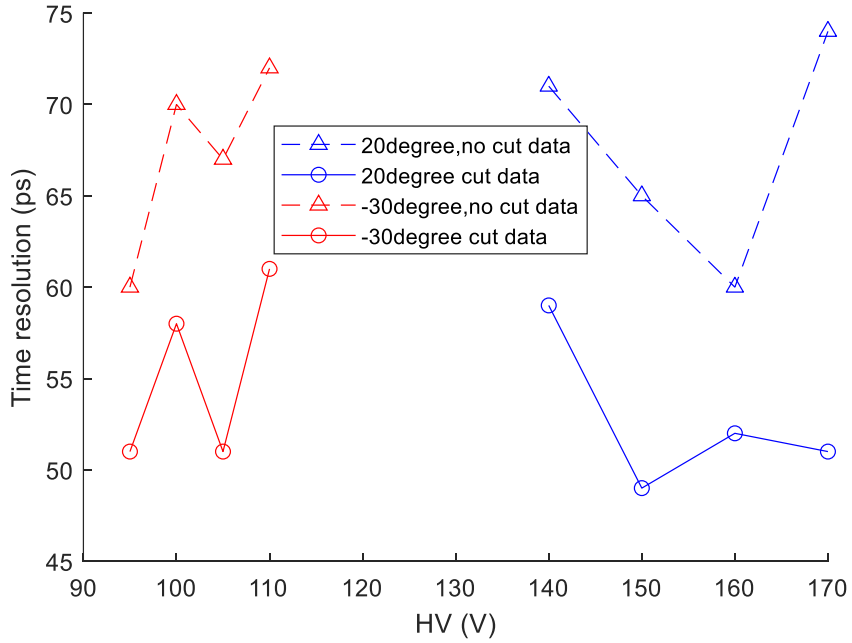
Beta source test using oscilloscope

- Test setup:
  - Use a calibrated single channel HPK sensor as the time reference.
  - Use a ^{90}Sr beta source to irradiate the HPK sensor and the hybrid.
  - Measure the amplified HPK sensor and the hybrid waveform with an oscilloscope.
- Data process:
  - Using TOT to correct time walk of TOA.
  - Cut the data with TOT larger than 5ns (~20%).
  - Subtract the time jitter of HPK sensor.



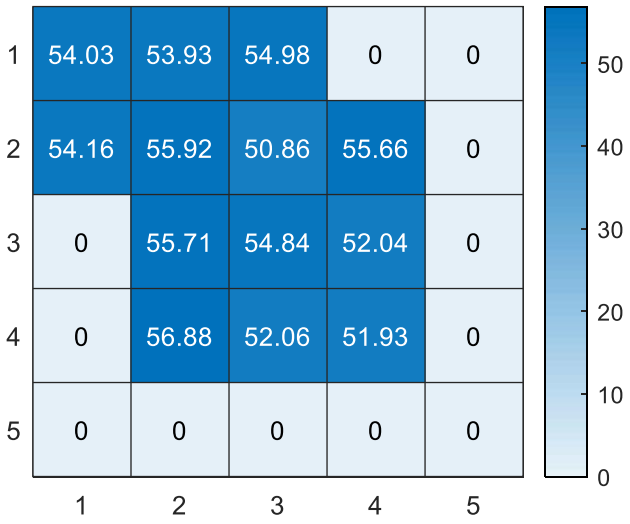




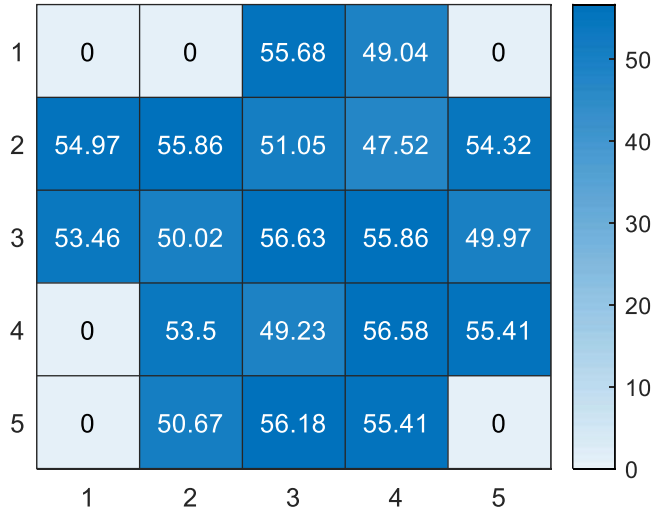


Beta source test using FPGA TDC

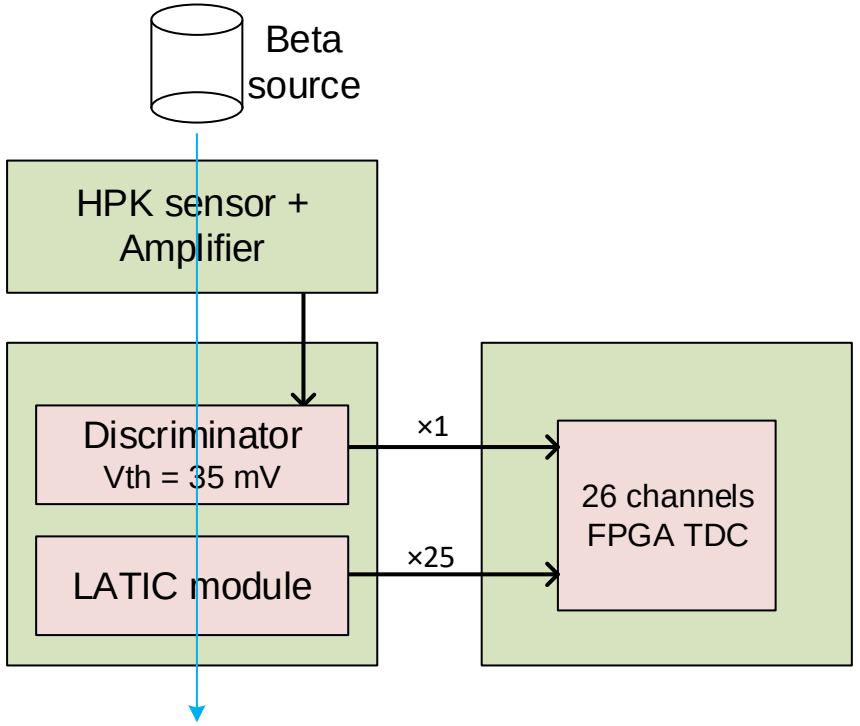
- Test setup:
  - HPK sensor + amplifier + discriminator
  - LATIC module
  - FPGA TDC
- Time resolution test results:
  - Data with TOT larger than 5ns were cut.



Hybrid1, HV=150V, T=20℃



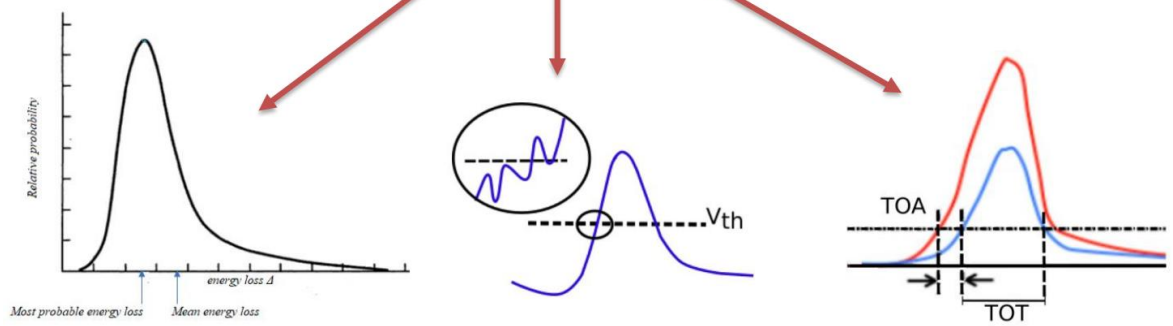
Hybrid2, HV=150V, T=20℃



Summary of time resolution test

- Factors affecting time resolution in LGAD readout：

$$\sigma^2_{T_{hit}} = \sigma^2_{Landau} + \sigma^2_{jitter} + \sigma^2_{TW} + \sigma^2_{clock} + \sigma^2_{TDC}$$



Test	Contribution items	σ	
Electronic test	Jitter	25 ps	Q=10fC
Laser test	Jitter, jitter of laser synchronization signal	22 ps	Q>10fC
Beta source test (Oscilloscope readout)	Jitter, landau, time-walk	~ 51 ps	Contribution of Landau and TW ~ 43 ps
Beta source test (FPGA TDC readout)	Jitter, landau, time-walk TDC	~ 53 ps	Contribution of TDC ~15 ps

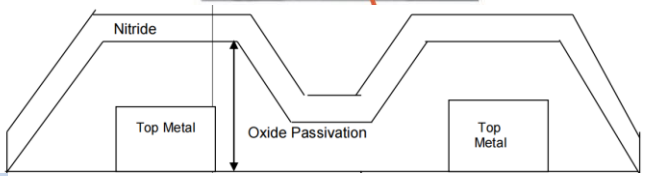
Summary

- The LGAD team at USTC has designed a prototype chip for LGAD readout.
- The flip-chip bonding of USTC IME sensor and LATICv2 has been completed.
- Testing for two hybrid have been conducted.
  - Hybrid testing provides reference for ASIC design.
  - Hybrids show good time performance in laser and beta source testing.
- Based on the test result, the revision of the ASIC and the exploration of flip-chip process are ongoing.

Backup

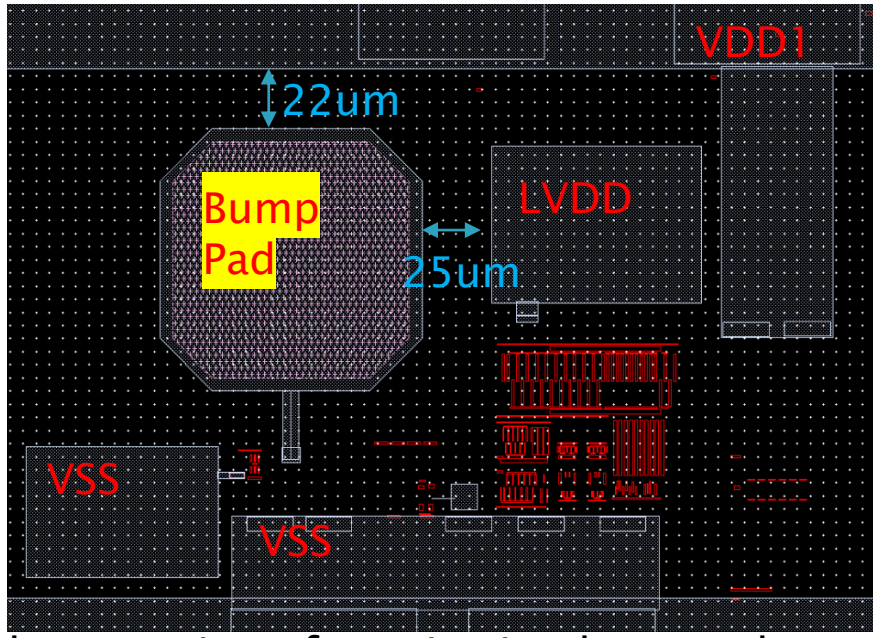
What happened with the abnormal channels?

- Abnormal phenomenon:
  - The output baseline of pre-amplifier is equal to analog power voltage.
  - This phenomenon did not occur during individual chip testing.
- Possible reason:
  - The input of pre-amplifier is connected to a high voltage.



Layer	Thickness (um) for Typical Capacitance	Thickness (um) for Best Capacitance	Thickness (um) for Worst Capacitance	Dielectric Constant
dpasv_nit	0.3	0.27	0.33	7
dpasv_oxd(9KA_TM))	1.99	1.79	2.18	3.9

Passivation layer parameters



Window opening of passivation layer and top metal.