The Upgrade of the ALICE Inner Tracking System: ITS3

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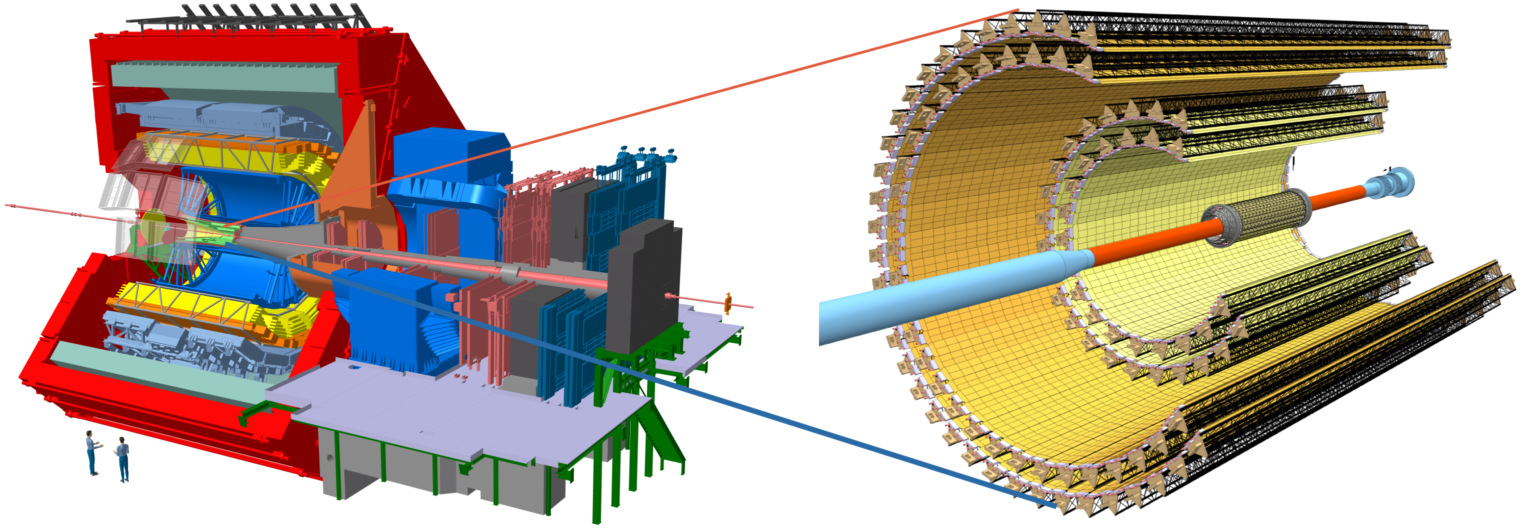
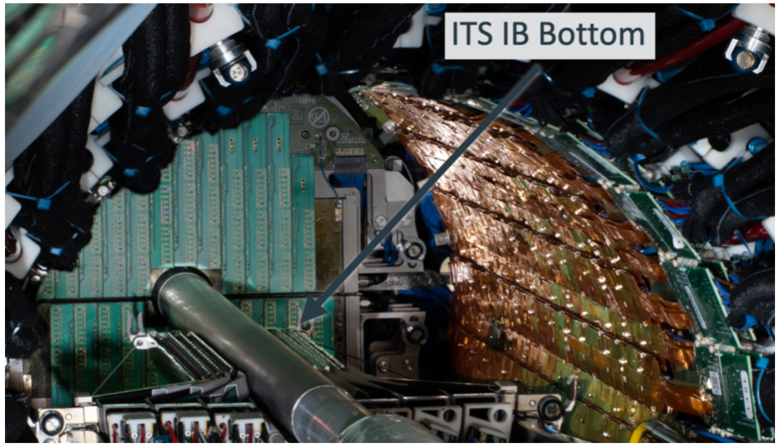
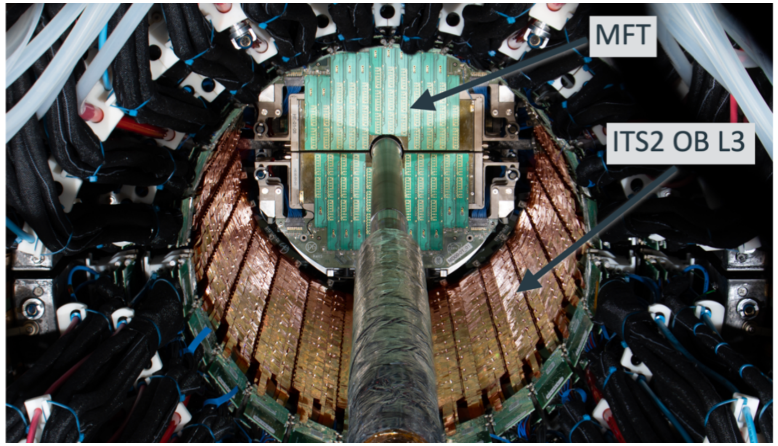
Xinxiang ,Henan

ALICE Inner Tracking System in run 3 (ITS2)







7 Layers:

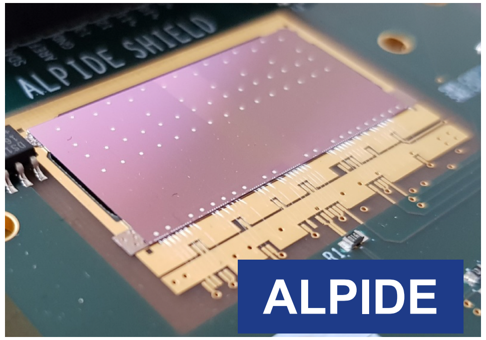
➡ 3 inner barrel (IB) and 4 outer barrel (OB)

Large active area and granularity

➡ $10 m^2$ active silicon area, 12.5×10^9 pixels

Built with ALPIDE chips

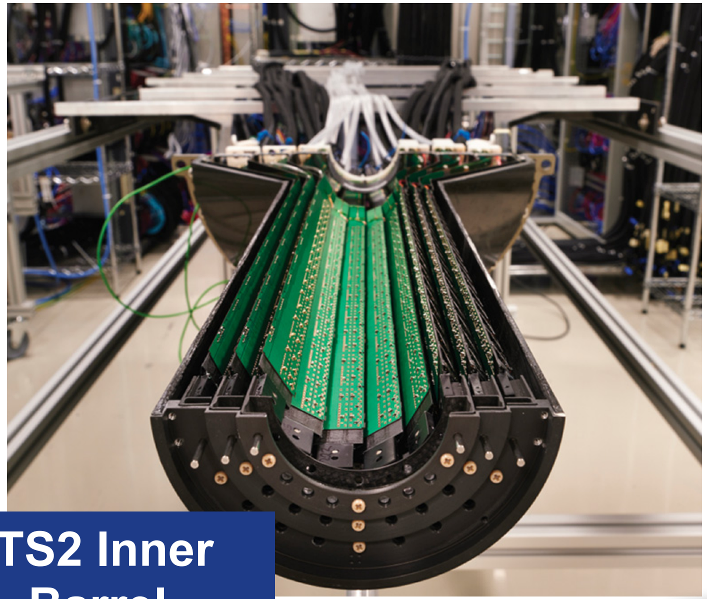
➡ 180nm CMOS MAPS, $15 \times 30 mm^2$, 512×1024 pixels



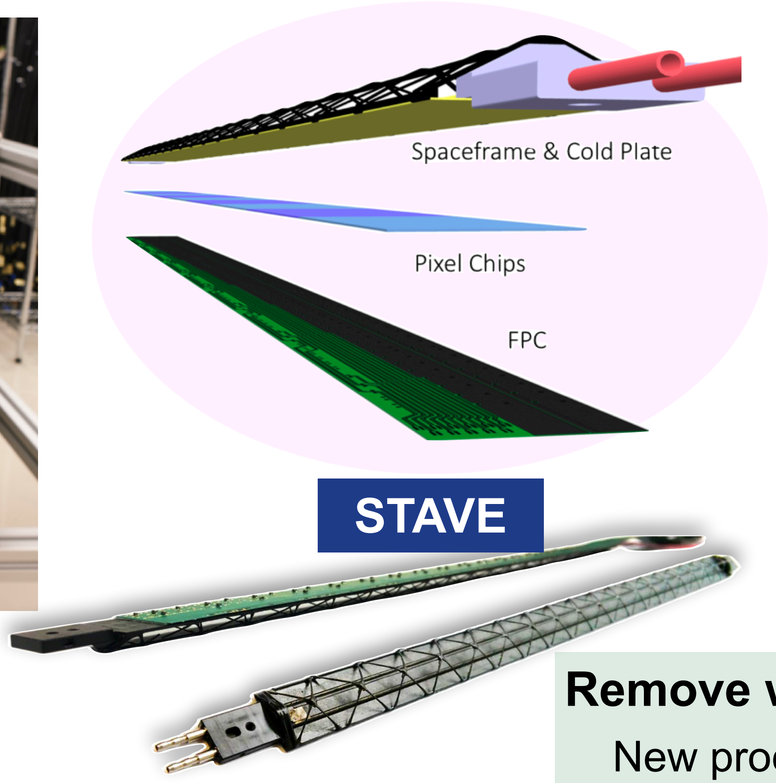
* M. Mager, for ALICE Collab, NIM-A 824, 434 (2016) * F. Reidt, for ALICE Collab, NIM-A 1005, 121793 (2021)

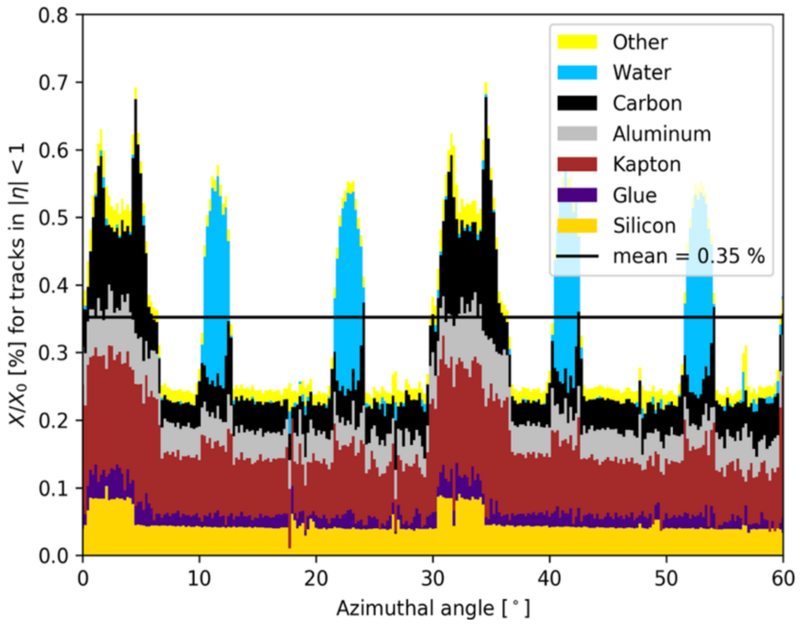
LHC LS2			LHC RUN3					LHC LS3				LHC RUN4		
2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	…

How to improve ITS2?



ITS2 Inner Barrel





Non-sensitive material

➡ Silicon has 1/7 of total material budget

Non-uniformly distributed material

➡ Stave overlapping, support and water cooling structure

Unable to be closer to the interaction point

➡ Mechanical constraints

Remove water cooling

New process chip (with lower power consumption) required to introduce air cooling

Remove the circuit board

New technology required to integrate data, control and power distribution on a single chip

Remove of mechanical support

New mechanical structure design required

ITS3: replacement of ITS2 inner barrel

Bent wafer-scale sensor ASIC

- ➡ 65 nm CMOS MAPS
- ➡ Power density < 40 mW/cm^2
- ➡ Fabricated with stitching

3 layers with 6 sensors(1 chip / half layer)

Air cooling between layers

Key benefit

Lower material budget

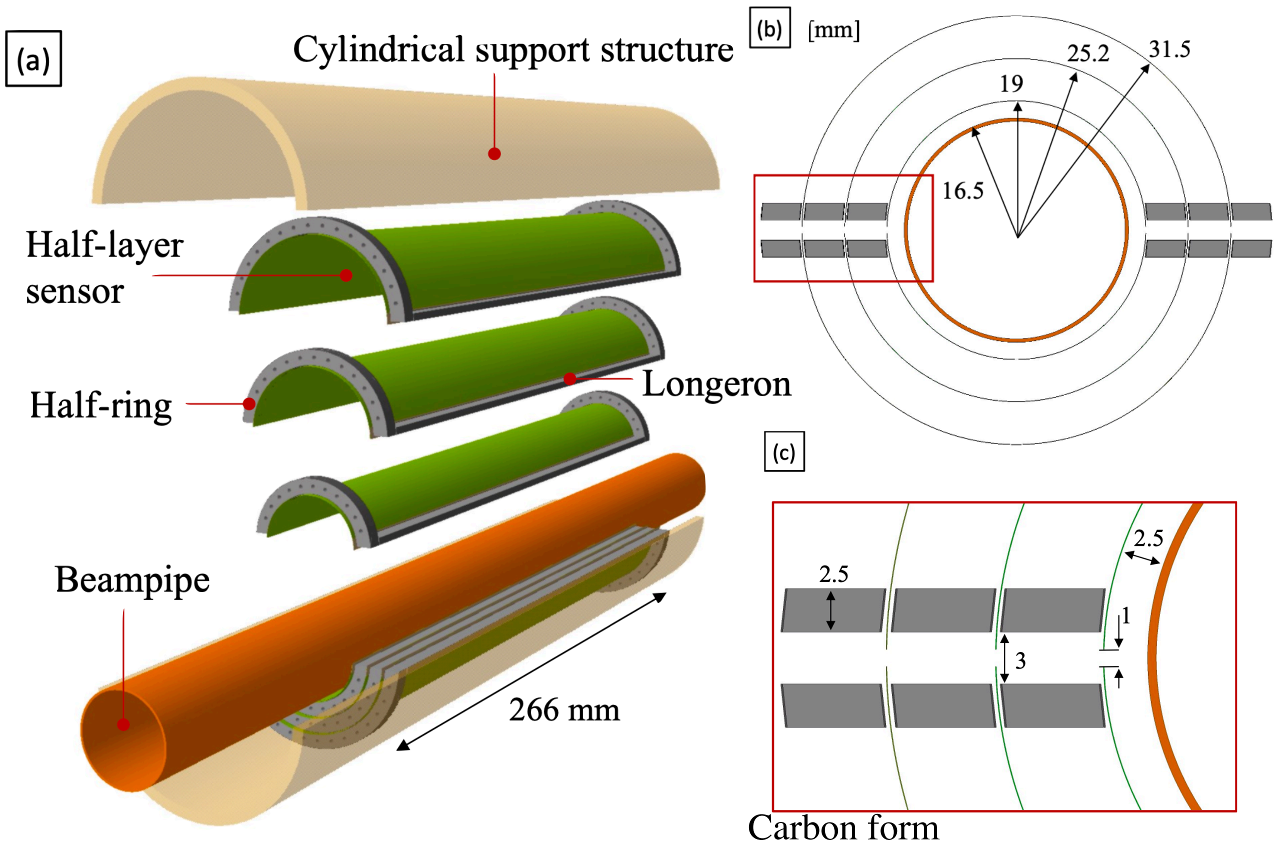
- ➡ 0.35% X_0 → 0.09% X_0 per layer

Uniformly distributed material

Closer to interaction point

- ➡ Beampipe: 18.2 mm → 16.0 mm
- ➡ Layer 0 position: ~24 mm → 19.0 mm

Schematic of ITS3:



ITS3 TDR: CERN-LHCC-2024-003

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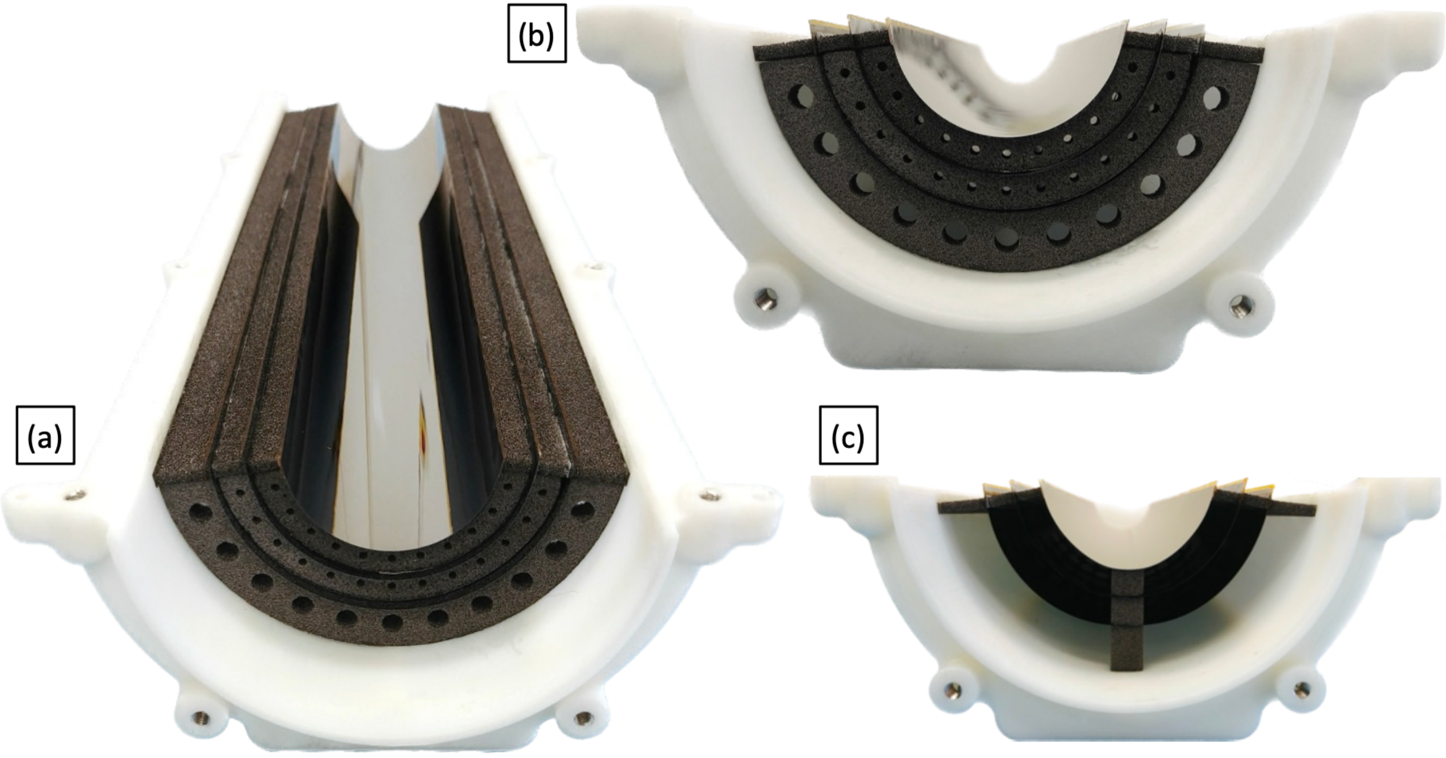
Actual image of engineering model:



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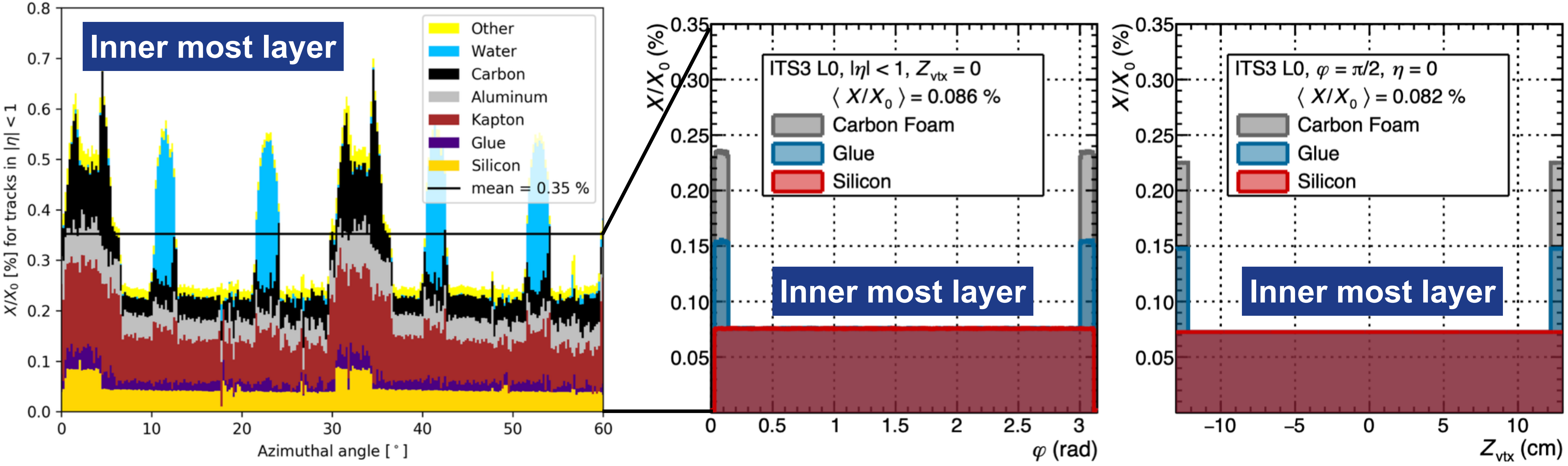
Material budget comparison between ITS2 IB and ITS3



ITS2 IB	ITS3

Various non-sensitive material

Silicon has 1/7 of total material budget.

Non-uniformly distributed material

Stave overlapping, support and water cooling structure.

Few of non-sensitive material

Sillicon dominates.

Uniformly distributed material

Only some lightweight carbon foam and glue distributed on the edge of the sensitive area.

Chip development roadmap

MLR1 (Multi-reticle Layer Run 1)

- **First 65nm process MAPS**
- APTS, DPTS, CE65
- Successfully confirmed the feasibility of the 65nm process for ITS3

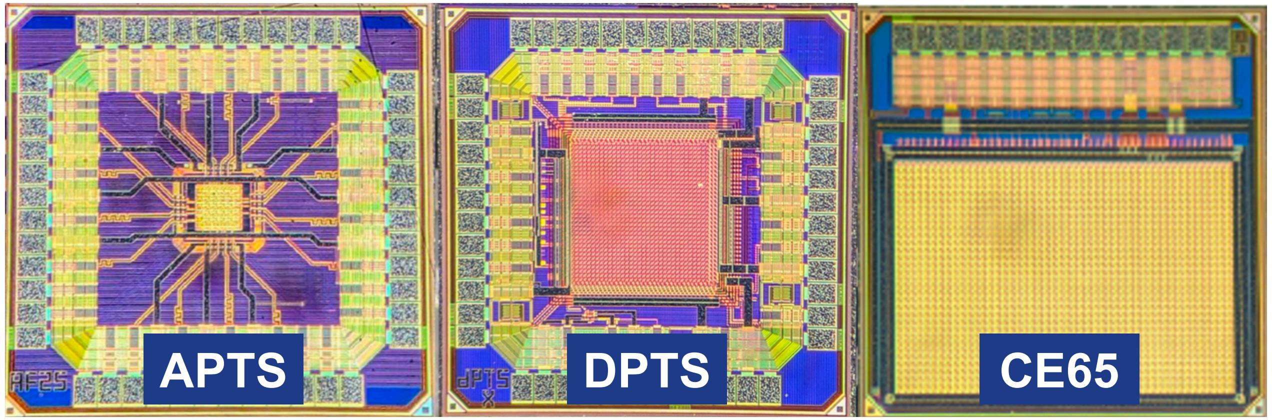
ER1 (Engineering Run 1)

- **First stitched MAPS**
- MOSS, MOST
- Successfully qualified the large scale sensor design

ER2 (Engineering Run 2)

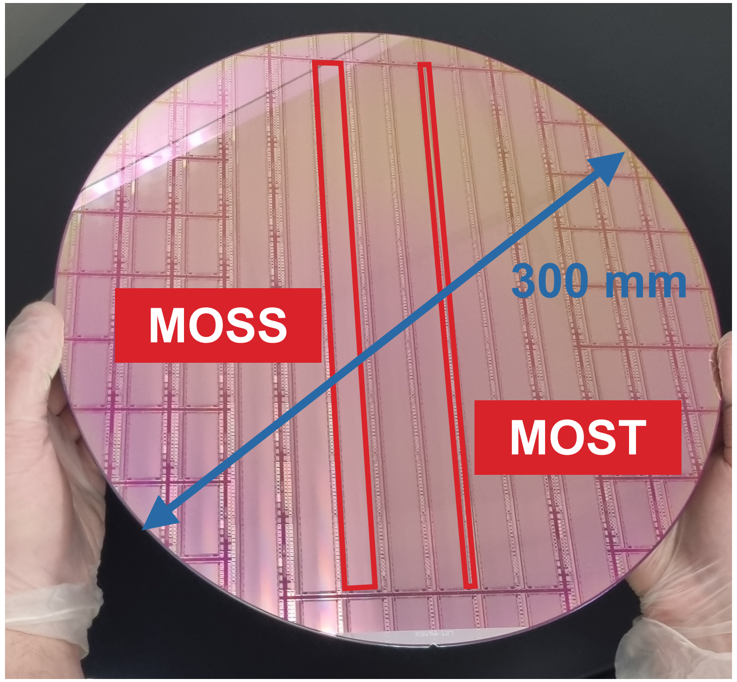
- **ITS3 sensor prototype**
- Specifications frozen
- Design ongoing

ER3 ITS3 sensor production



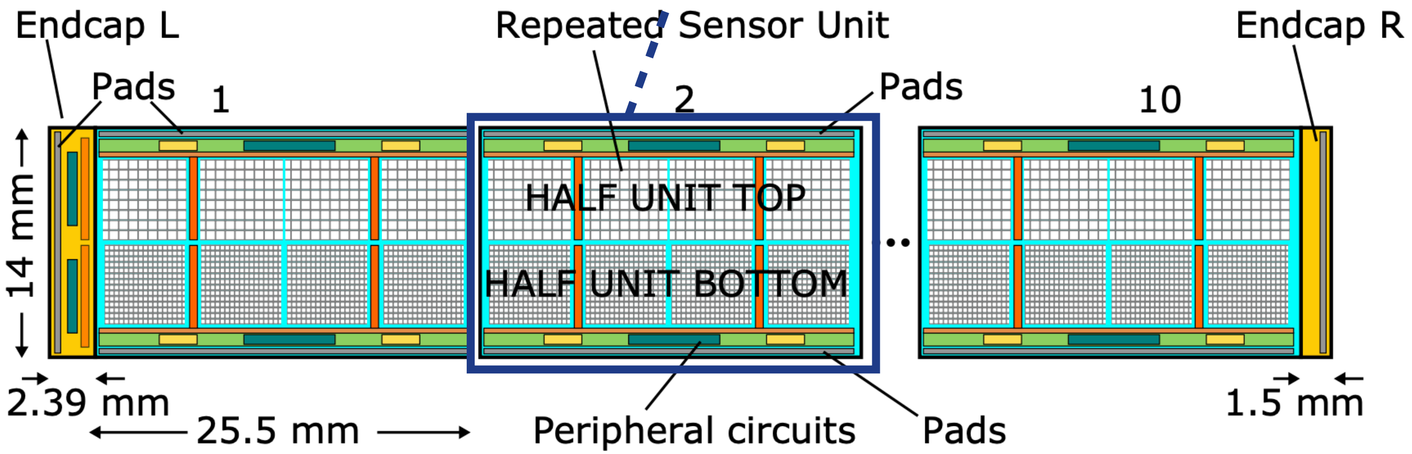
APTS
Analogue Pixel Test Structure
DPTS
Digital Pixel Test Structure
CE65
Circuit Exploratoire 65 nm

MOSS
Monolithic Stitched Sensor
MOST
Monolithic Stitched Sensor Timing



MOSS

- **First stitched chips for HEP!**
  - **Full module on a single chip**
  - **Wafer-scale** (14 x 259 mm)
  - **65 nm process**

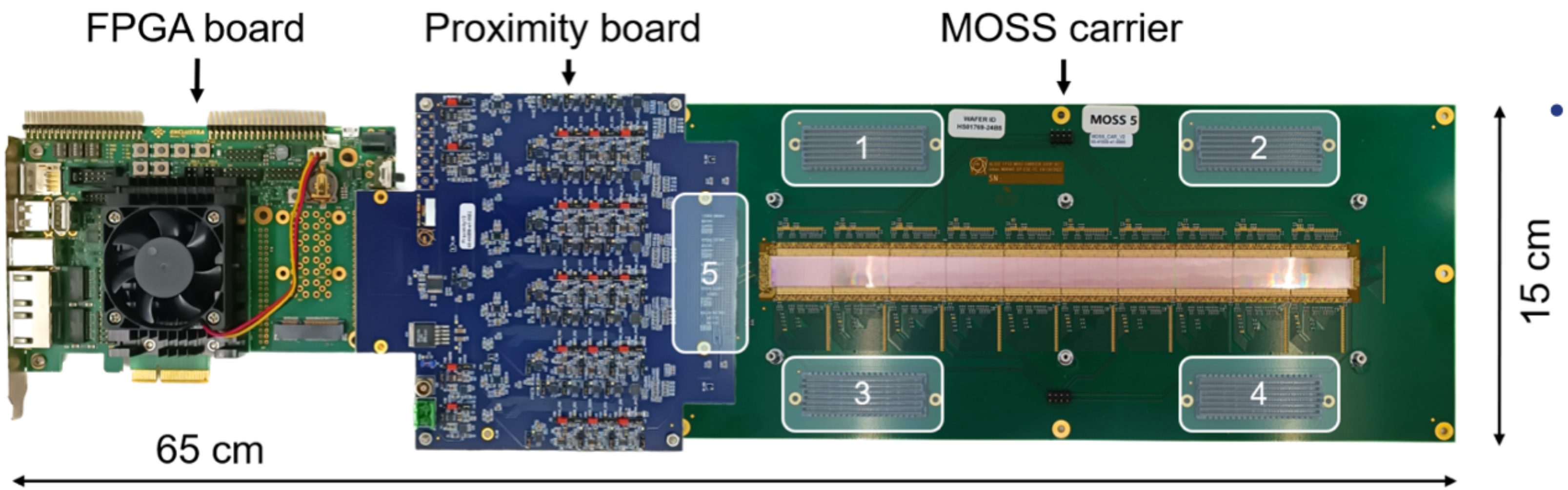


- MOSS is segmented into 10 RSU (repeated sensor units)
  - RSUs are divided into top and bottom half units with different pitches

	Pixel matrix	Pixel size
Matrices on the top	256 × 256	22.5 μm
Matrices on the bottom	320 × 320	18 μm

Functional Test System of MOSS Chip

A dedicated test system was developed to functionally characterize the MOSS chip.



- **The chip and carrier board are interfaced via five connectors:**
  - 1 Connector: Exclusively for the Laser Engine Controller (LEC)
  - 4 Connectors: Each handling five half-units

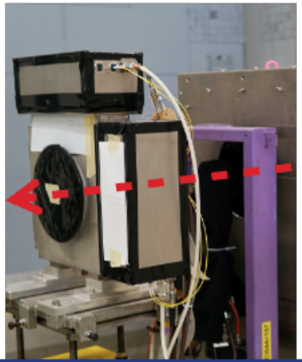
* O Abdelrahman et al., arXiv:2510.11463

- **FPGA and Proximity board:**
  - The FPGA and Proximity board are connected to the LEC board connector
  - The additional four numbered connectors connect to FPGA and Proximity boards for powering and characterization from the long edge of the chip.

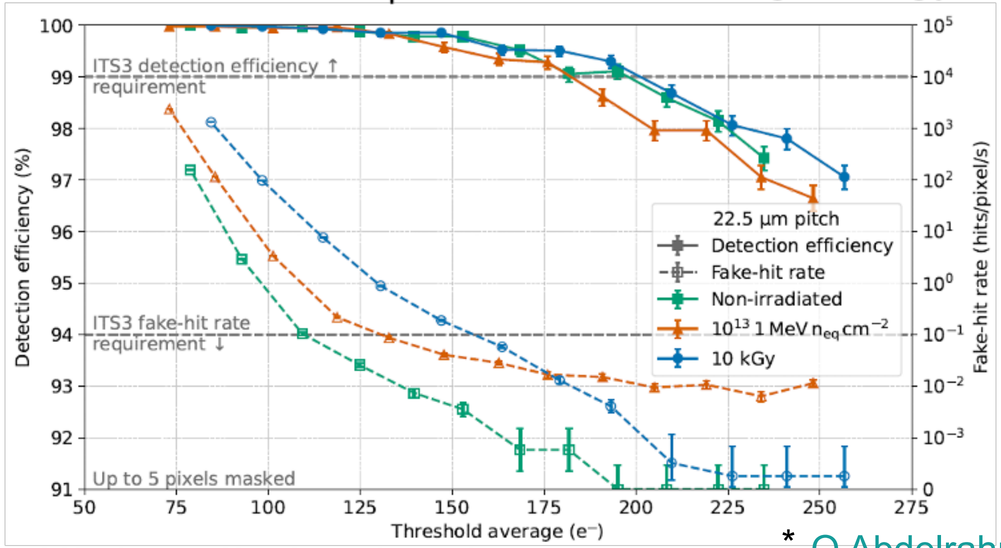
Testing results (selected)

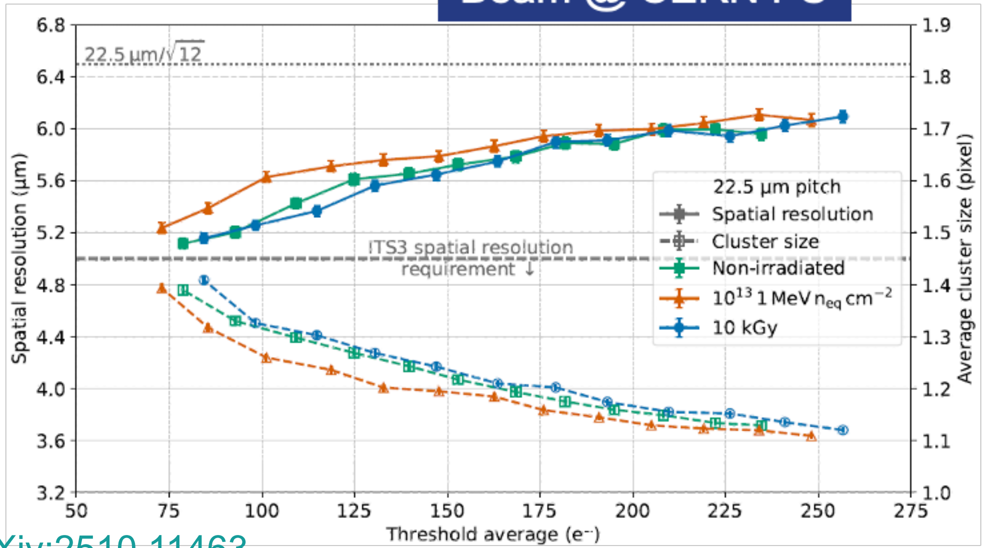
- **Target performance for ITS3 sensors**
  - Detection efficiency higher than 99%
  - Fake-hit rate lower than 10^{-1} $\text{pixel}^{-1}\text{s}^{-1}$
- **Expected radiation doses during ITS3 operation**
  - 10 kGy Total Ionising Dose (TID)
  - 10^{13} 1MeV n_{eq} cm^{-2} Non-Ionising Energy Loss (NIEL)

ITS3 Telescope @ CERN



Beam @ CERN PS





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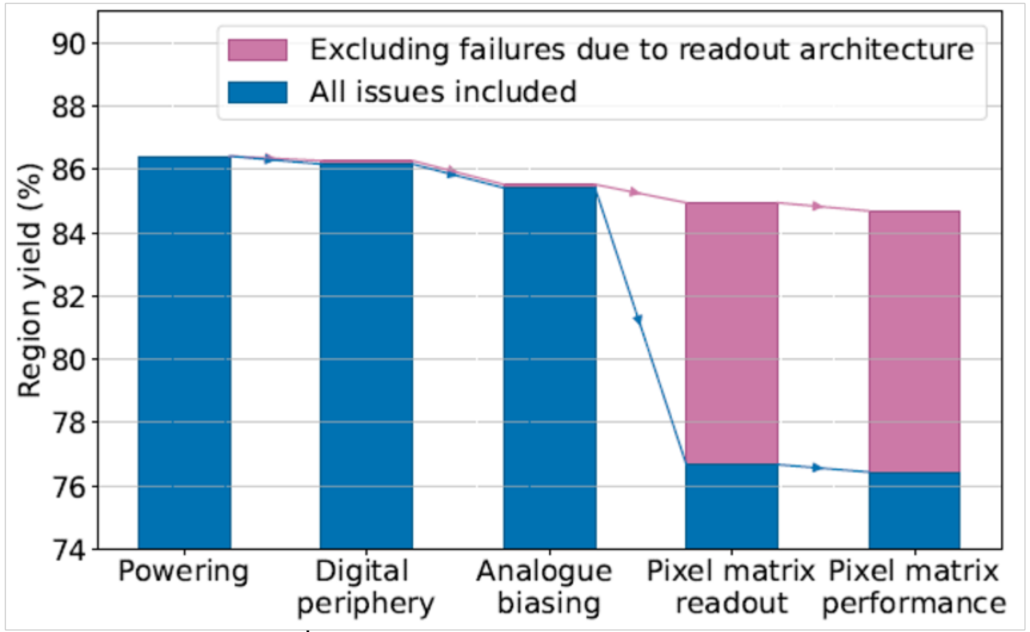
See details in Zijun's talk: Performance study of the MOSS chip for the ITS detector (11/1 3:00PM)

- **High radiation hardness**
  - Efficiency performance of irradiated chip under ITS3 requirement fully compatible with non-irradiated one
  - Same story for the resolution and cluster size as a function of charge collection threshold

Excellent performances of the 65 nm technology have been established experimentally!

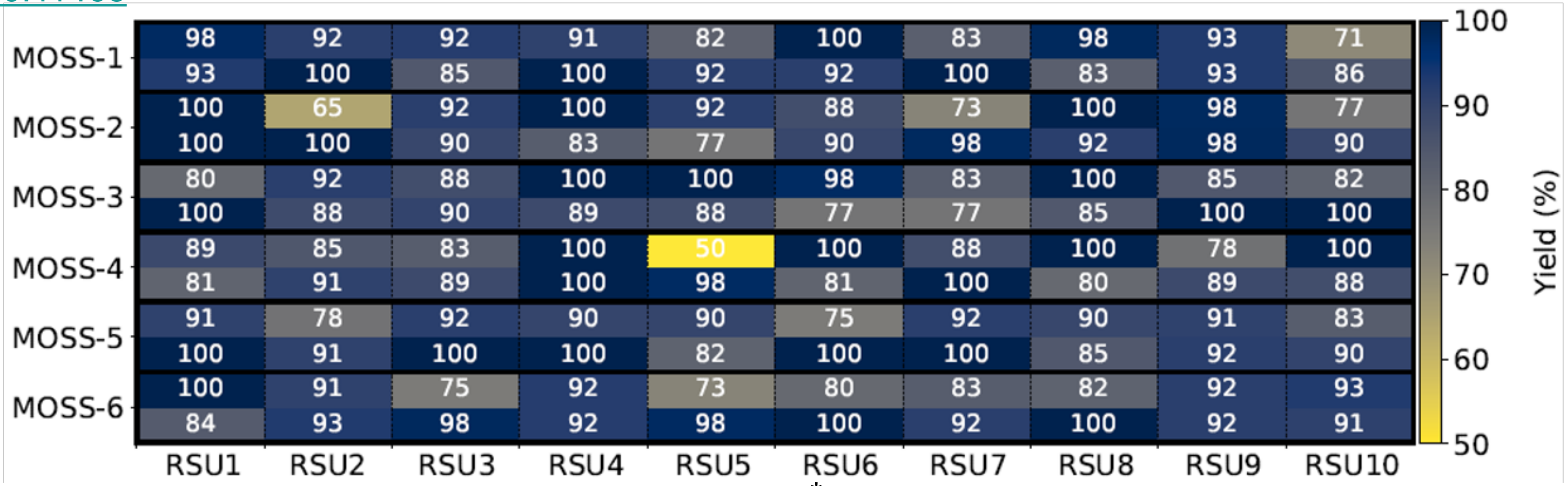
Yield



* O Abdelrahman et al., arXiv:2510.11463

- **The yield losses across the different chip block verifications**
  - The largest yield loss occurs during the powering test
  - Due to shorts in the power network from the new metal stack
  - Will be mitigated in the next chip submission

- **The functional yield of half-units**
  - No specific patterns are apparent
  - No top-bottom asymmetry within MOSS chips is observed



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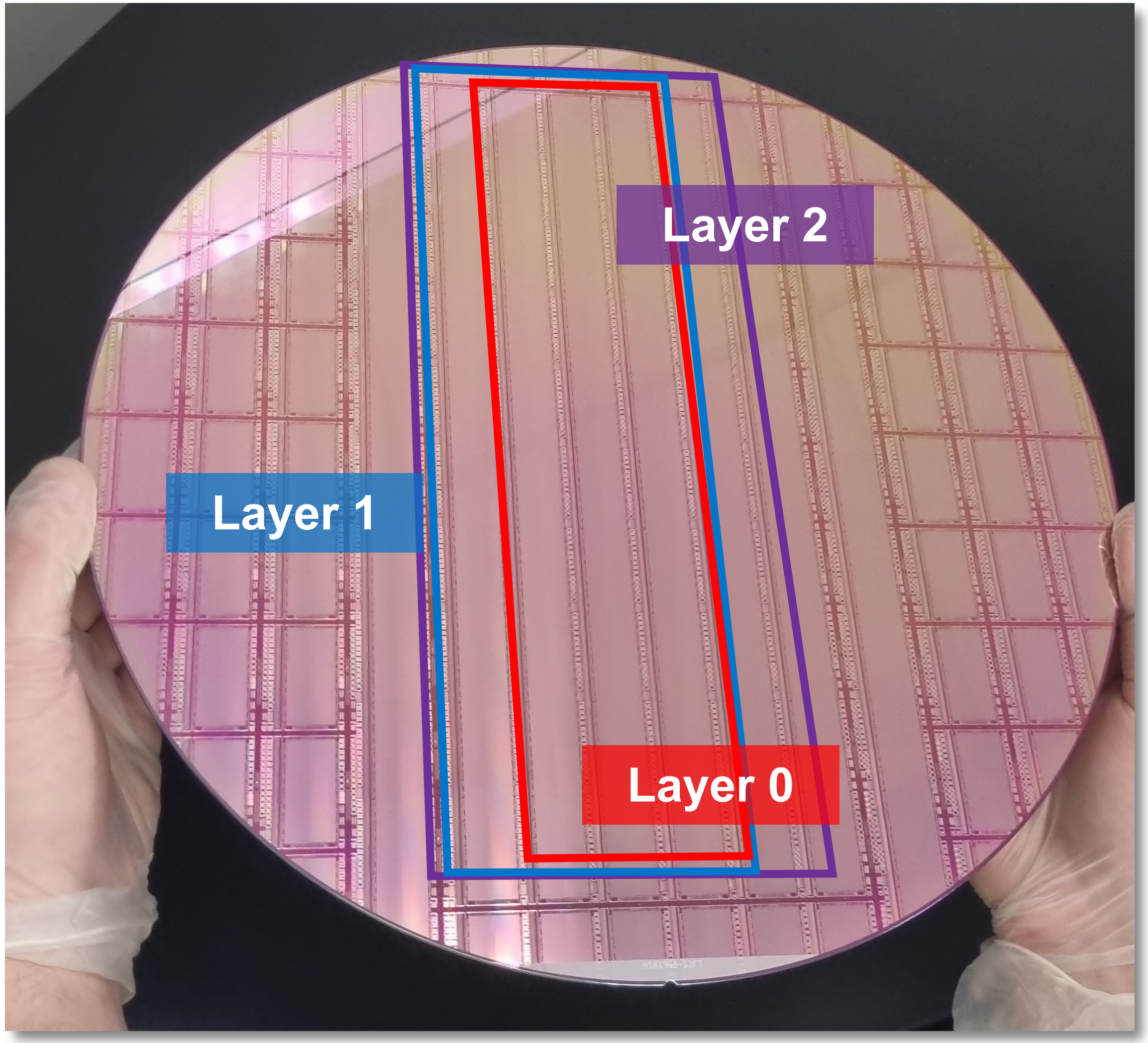
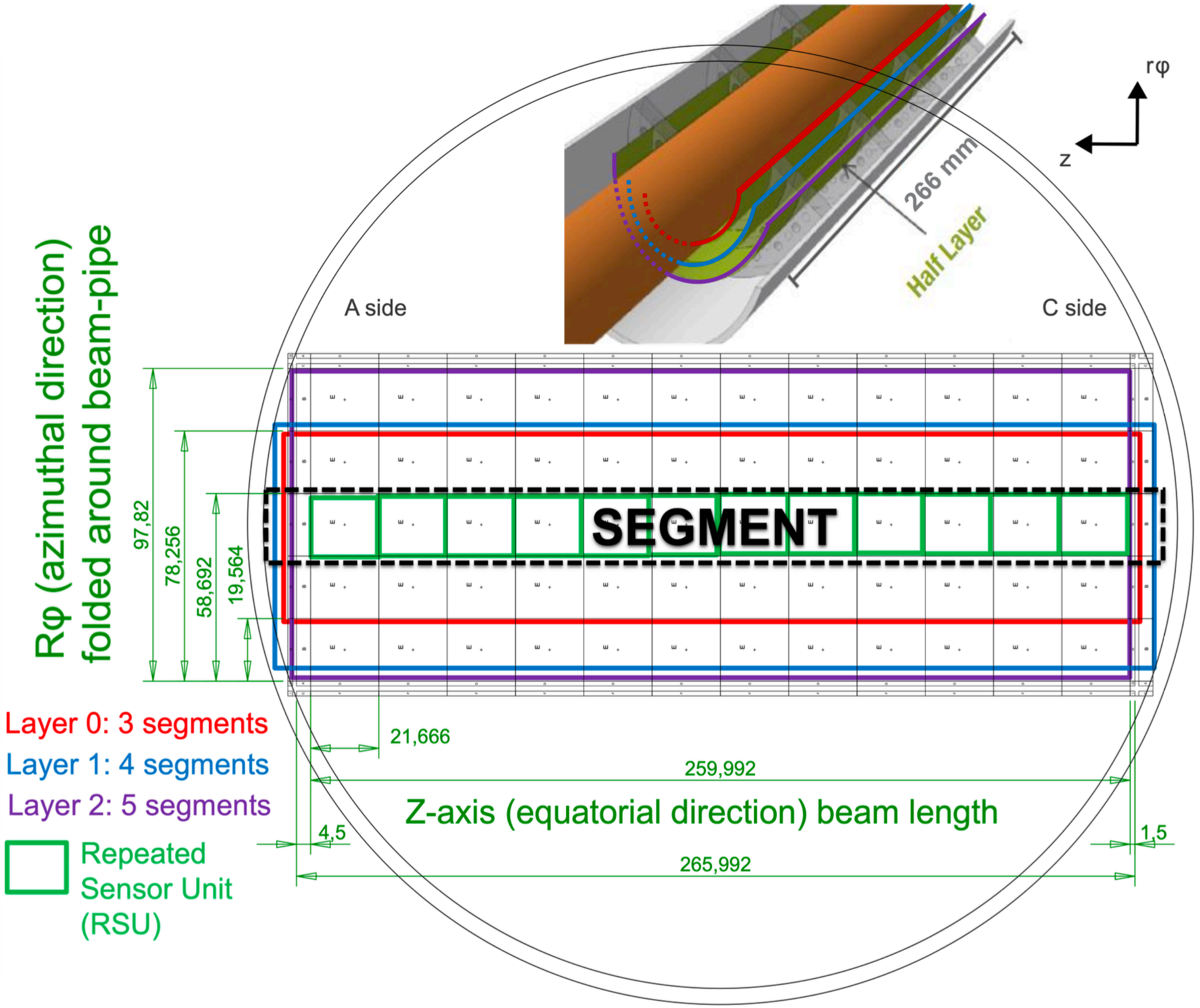
Final chip design — MOSAIX

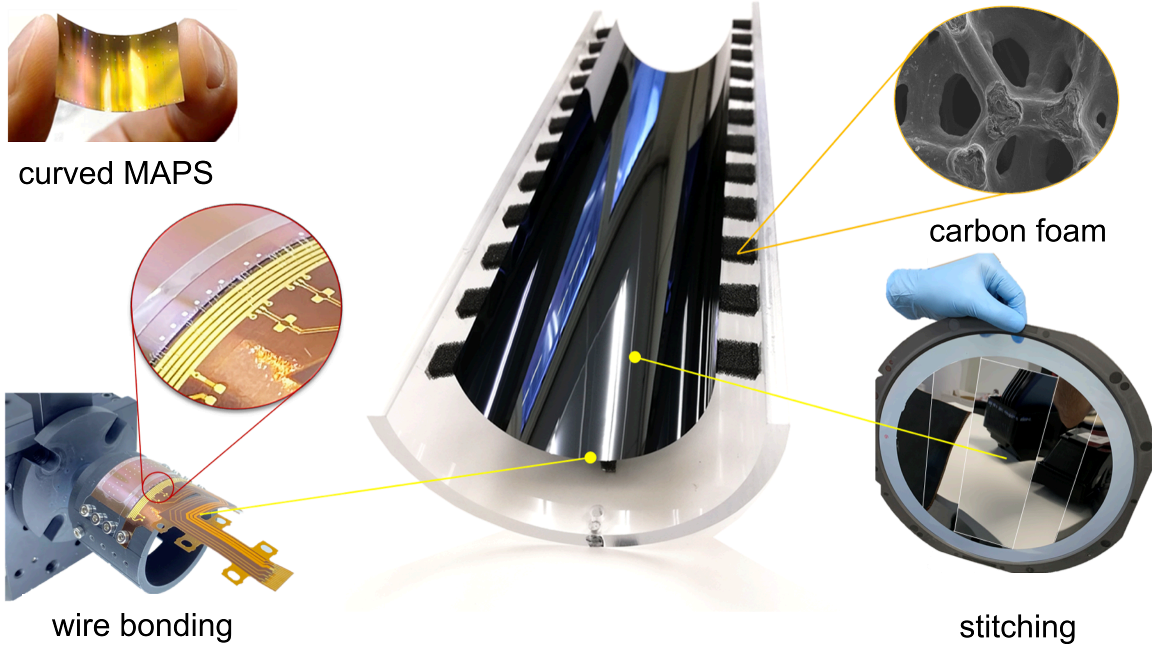




This is the real wafer-scale!

Summary and outlook

- **ITS3 — a bent wafer-scale monolithic pixel detector**
- **ITS3 project is on track for installation in LS3**
- **A twofold improvement in spatial resolution wrt. ITS2**
- **The following analysis significantly benefit from ITS3**
  - ➡ heavy flavor collectivity, thermal dielectron measurement
  - ➡ and many more analyses…



Thanks!