Sensor Development for LHCb Upstream Pixel Tracker

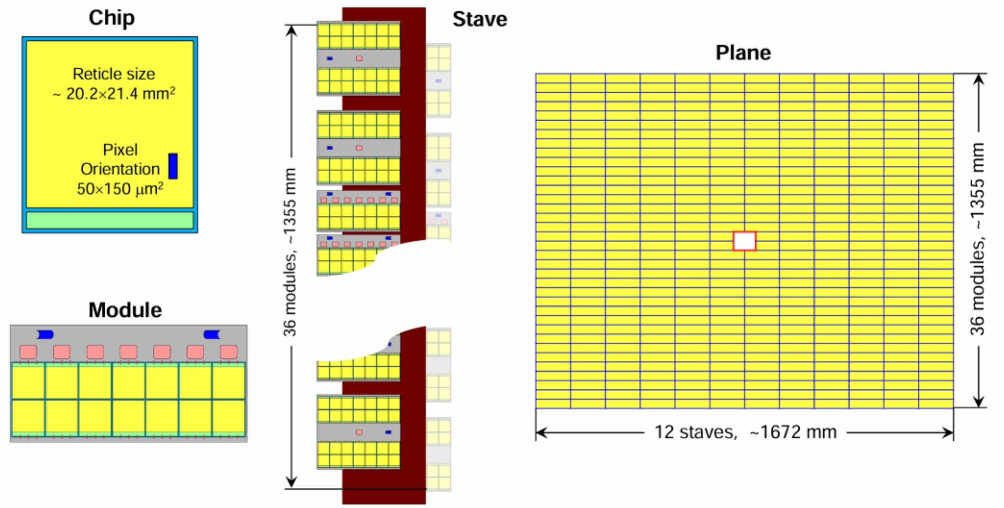
Cheng Zeng 曾程 (Institute of High Energy Physics, CAS)

On behalf of COFFEE team

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

HVCMOS for LHCb UP Tracker

- LHCb Upgrade II requires tracker with better radiation hardness and spatial resolution.



Upstream Pixel Tracker for LHCb Upgrade II

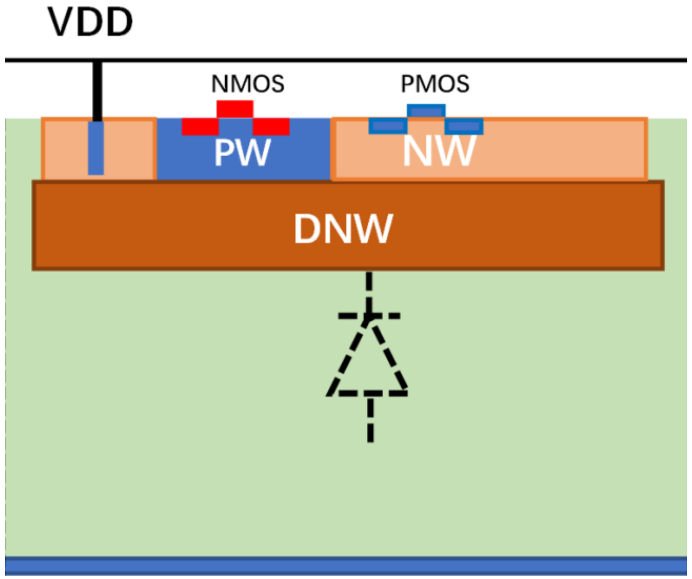
Area： $\sim 8\ \mathrm{m}^2$

Radiation hardness： $\sim 3 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$

Time resolution： $3-5$ ns, capability to tag 25 ns bunch crossing

Power consumption： $\sim 200\ \mathrm{mW/cm^2}$

- HVCMOS advantages:
  - MAPS, Excellent spatial resolution, no need to bump bond the sensor and ASIC
  - Large deep n-well as charge collection node, high voltage bias; Fast charge collection, less trap effect
  - Enclose readout circuit inside deep n-well. Intrinsically radiation hardness



Sensor cross section

zengcheng@ihep.ac.cn

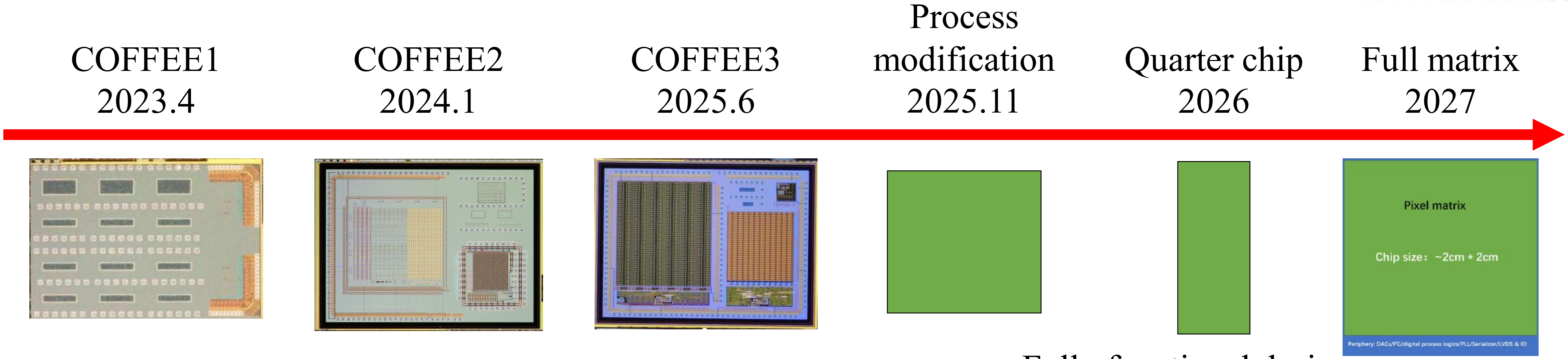
COFFEE Chips

CMOS sensOr in Fifty-FivE nanometer procEss chips

- Targeting to achieve full-size, full function chips meeting the LHCb UP Tracker requirements in a few year.
  - COFFEE1: Validate the 55 nm low leakage process
  - COFFEE2: Explore and validate the 55 nm HV-CMOS process
  - COFFEE3: Validate the readout circuit structures and core performances

COFFEE

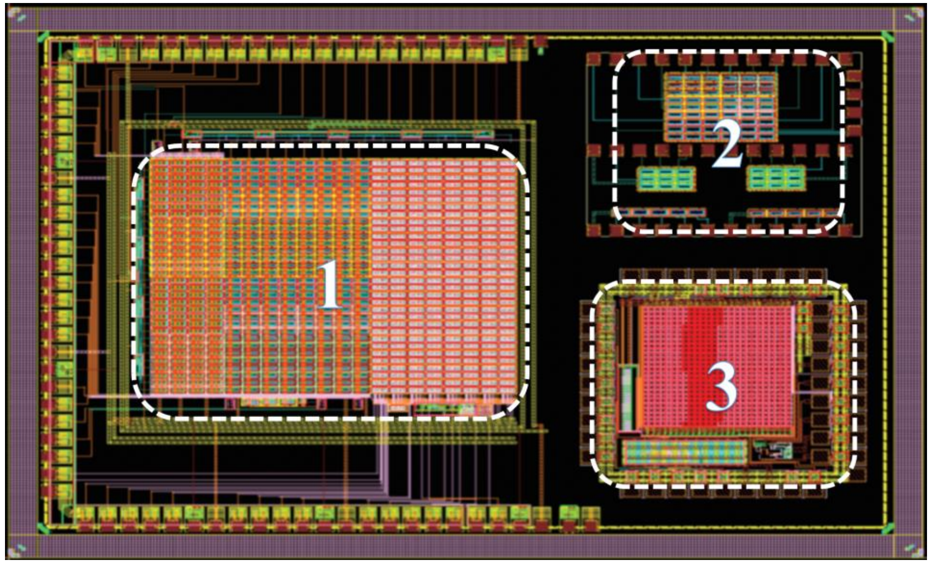
CMOS SENSOR IN
FIFTY-FIVE NM PROCESS



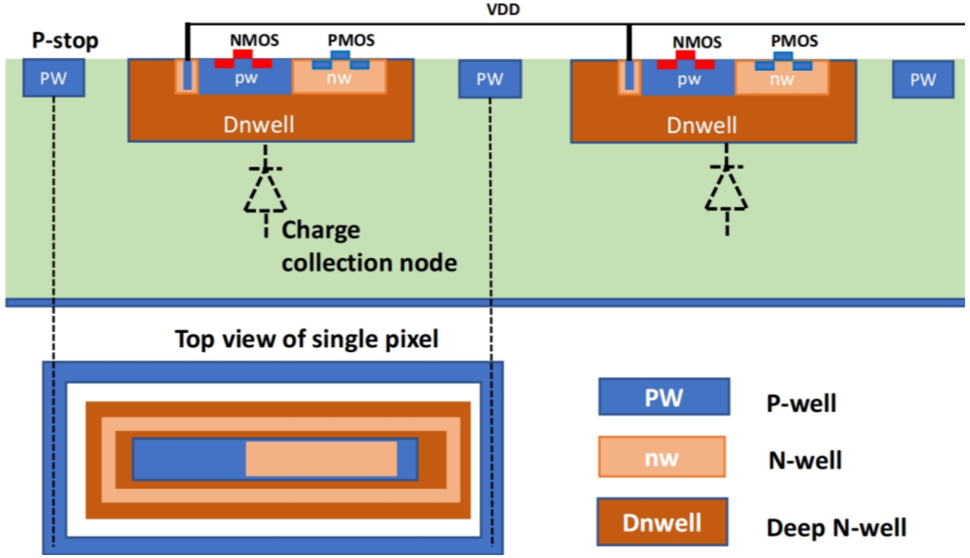
Fully functional design

COFFEE2 Introduction

COFFE2 chip, 3 × 4 mm^2, the first HVCMOS chip in 55 nm process, triple-well structure



COFFEE2 chip floorplan



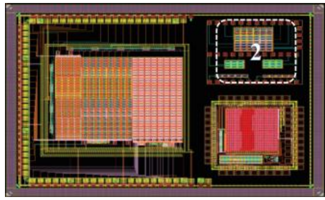
Sensor cross section

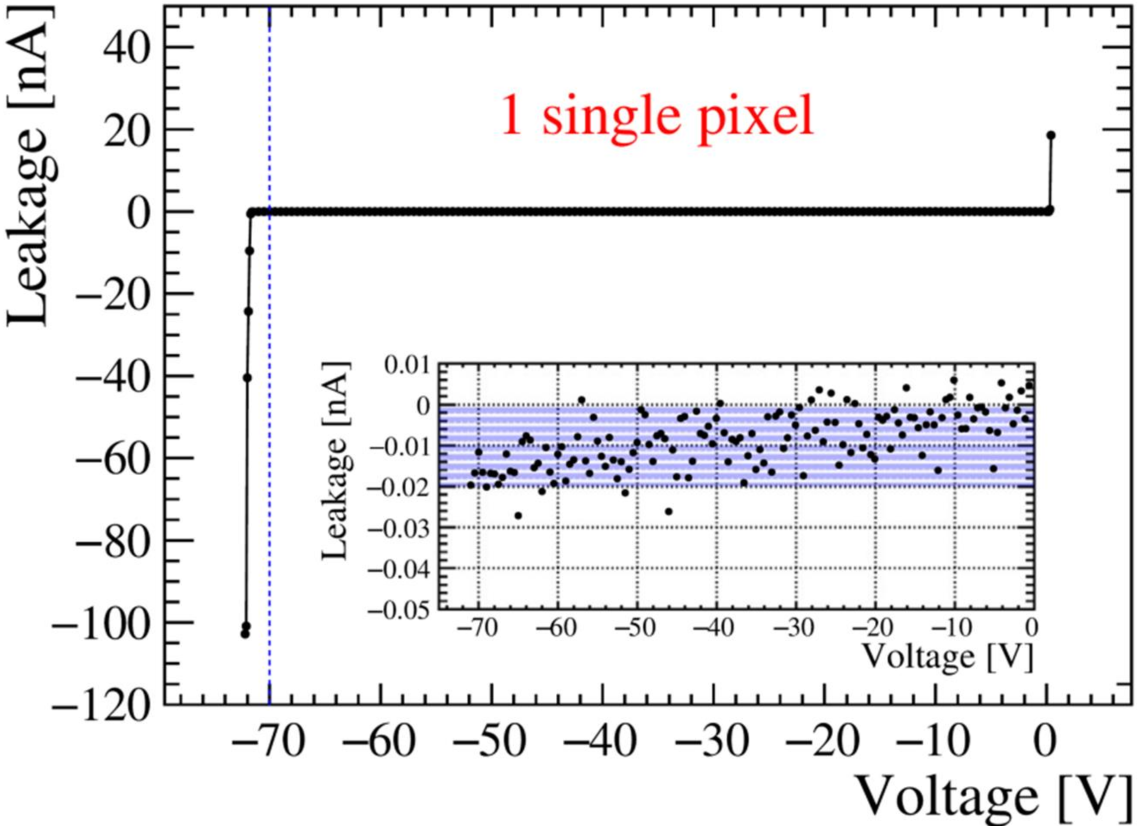
- Section 1: 32 rows × 20 columns pixels matrix, with sensor and in-pixel circuit. Studying for in-pixel charge sensitive amplifier (CSA), CMOS and NMOS comparator design for process validation. JINST 20 (2025) C10011
- Section 2: Passive diode, real validation of sensor.
- Section 3: 26 rows × 26 columns pixels matrix, with sensor, in-pixel circuit and digital readout periphery for novel electronics structure study. JINST 20 (2025) C03023

COFFEE2 Test

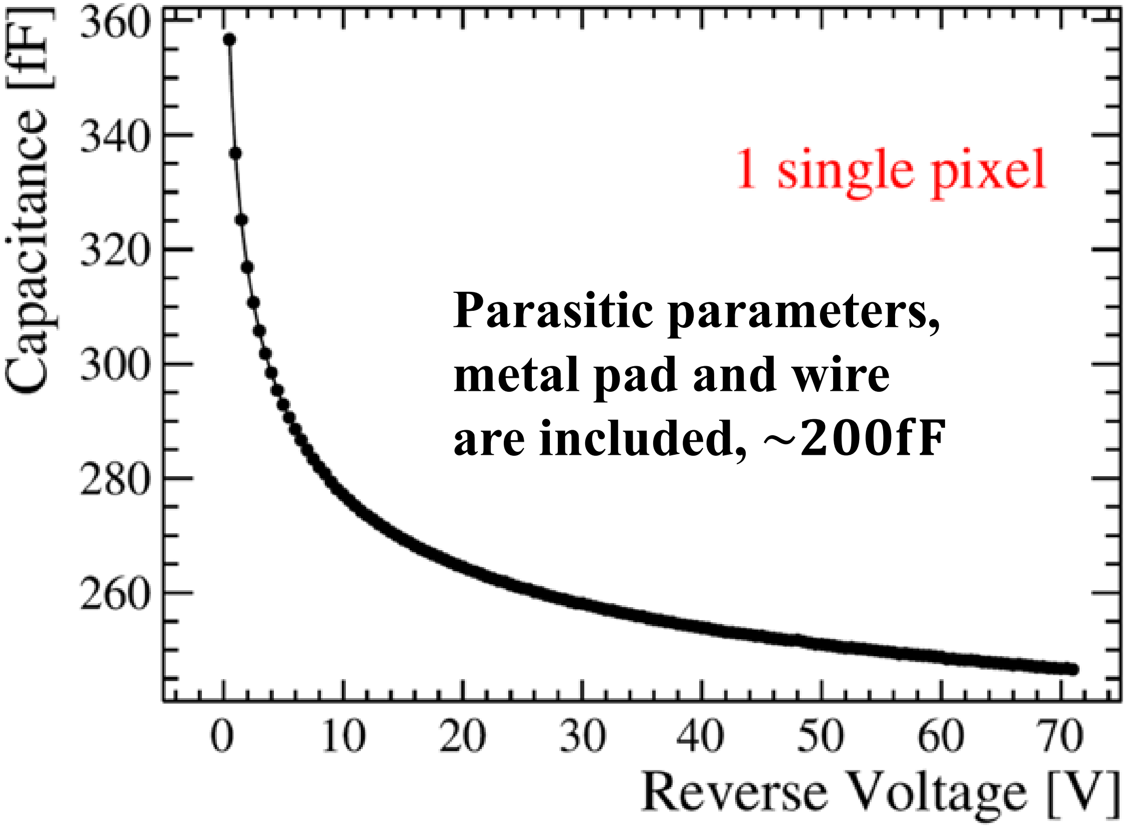
Section 2, Passive diode

- Breakdown Voltage: ~ − 70 V
- Leakage: ~10 pA
- Capacitance: 30~40 fF at −70 V





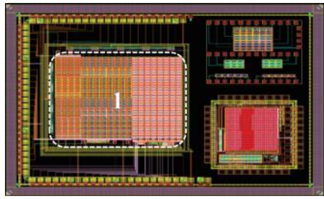
I-V curve



Parasitic parameters, metal pad and wire are included, ~200fF

C-V curve

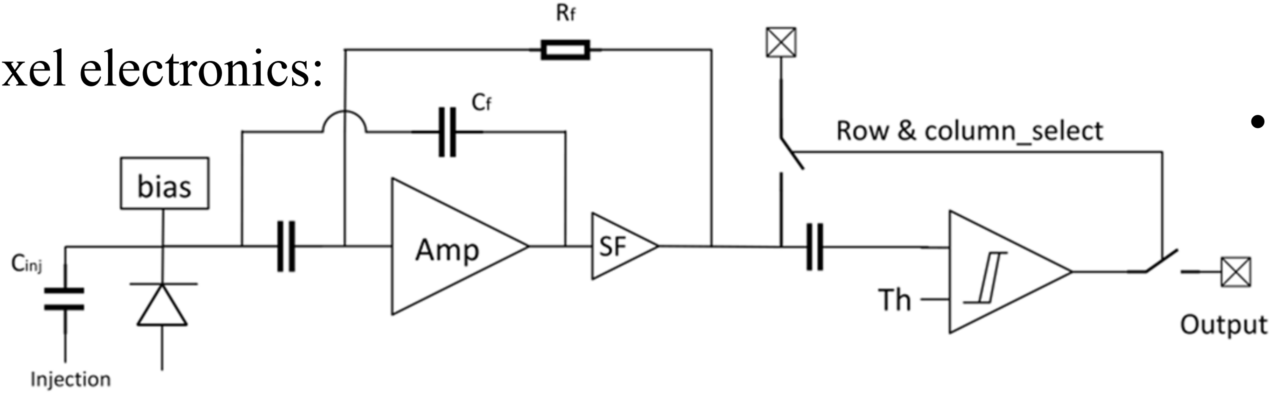
COFFEE2 Test



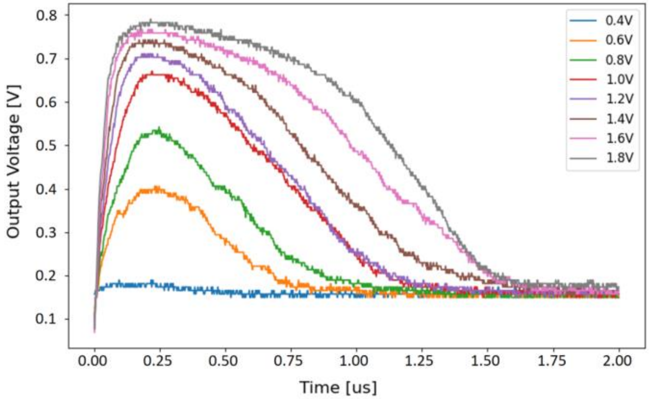
Section 1

- Charge injection test: JINST 20 (2025) C10011
  - CSA waveform in expected
  - CSA response curve consistent with simulation

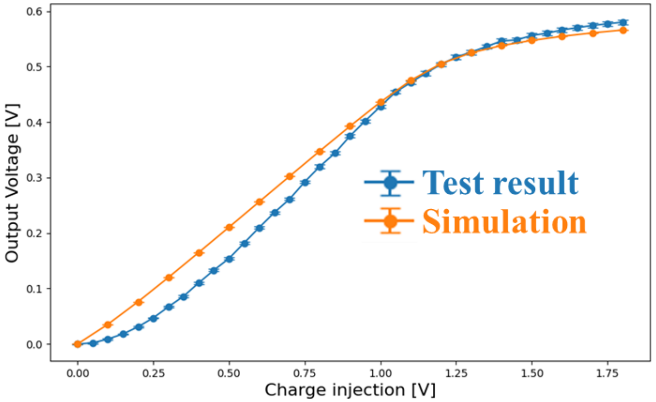
In-pixel electronics:



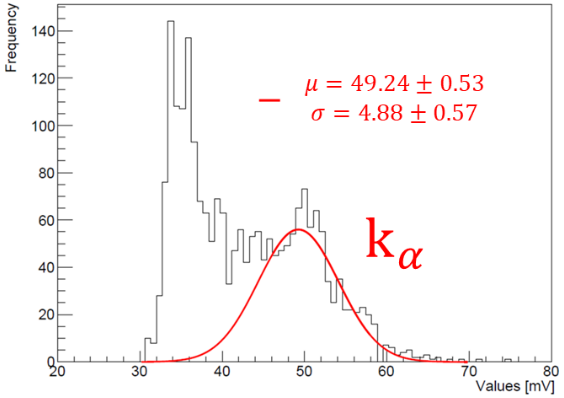
- Radioactive sources test:
  - ^{55}Fe (5.9 keV X-ray), Gaussian fit
    - μ~49 mV~1640 e^-
    - σ~4.9 mV~160 e^-
  - ^{90}Sr (β-source), Landau fit
    - MPV: ~34 mV~1120 e^-
    - Depletion depth: ~10 μm



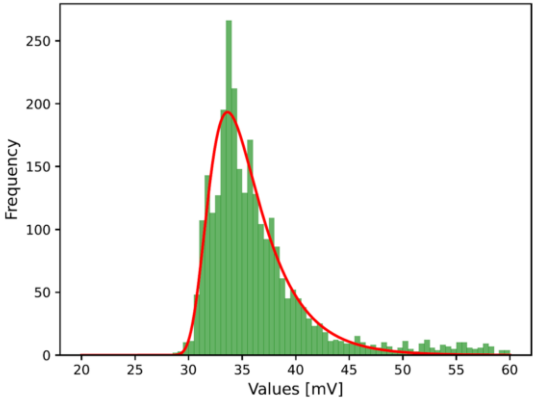
CSA output vs Vinj



CSA response curve



^{55}Fe test

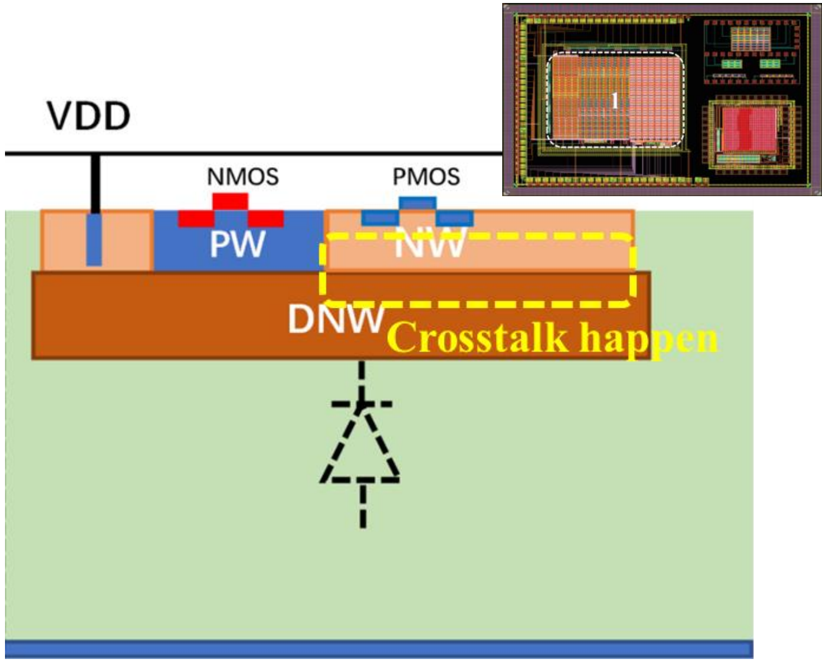


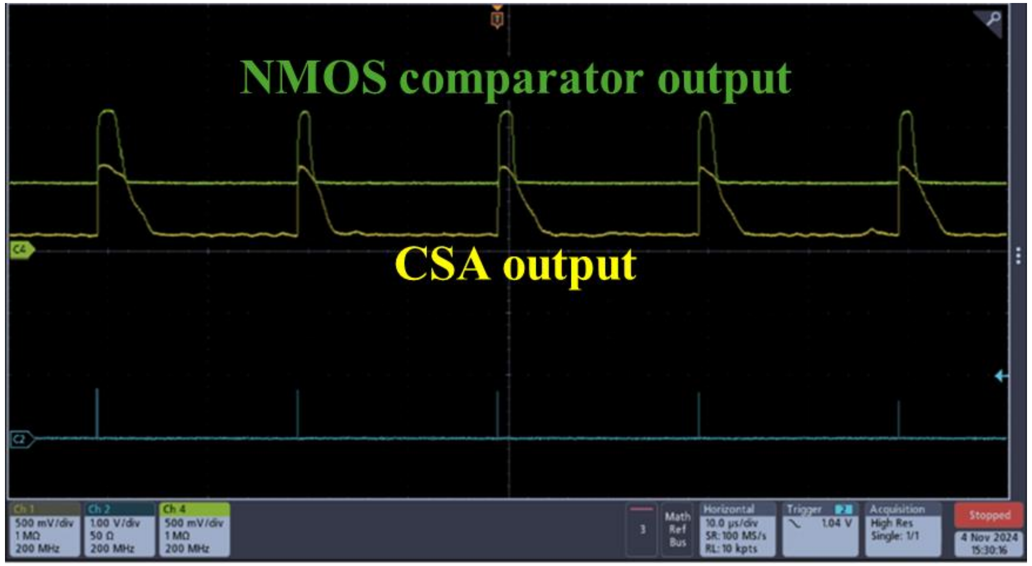
^{90}Sr test

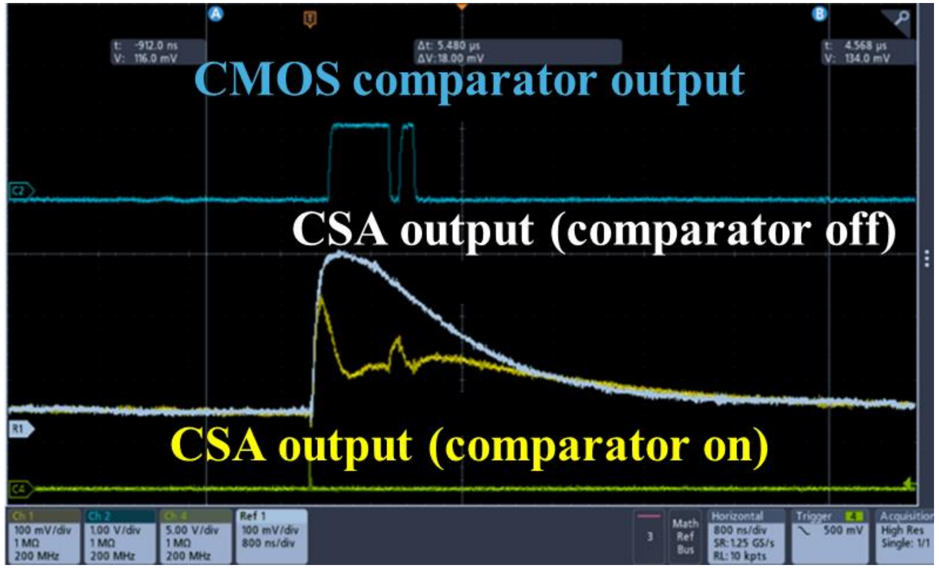
COFFEE2 Test

Section 1

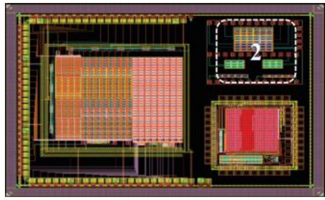
- Laser test : JINST 20 (2025) C10011
    - Two different in-pixel comparator design: CMOS and NMOS-only
    - Pixel with NMOS-only designed work well
    - Crosstalk issue seen in CSA output waveform when CMOS comparator is on
    - Potential flip in digital circuitry cause the disturbance between N-well of PMOS bulk terminal and deep N-well
    - The crosstalk can be mitigated by adding a p-layer for isolation, process modification is required.





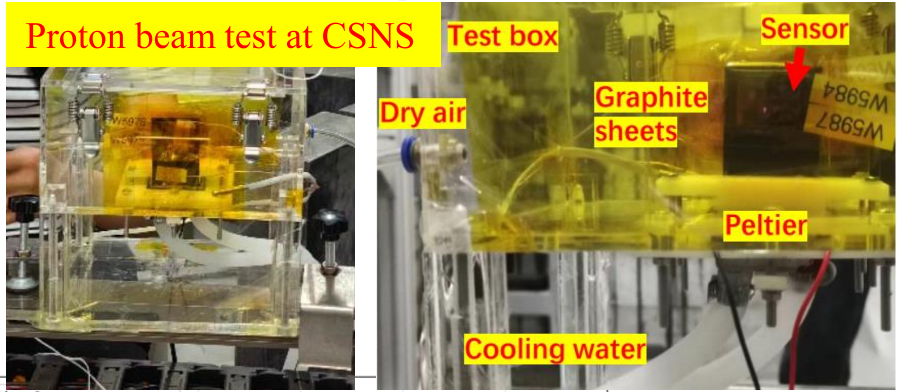


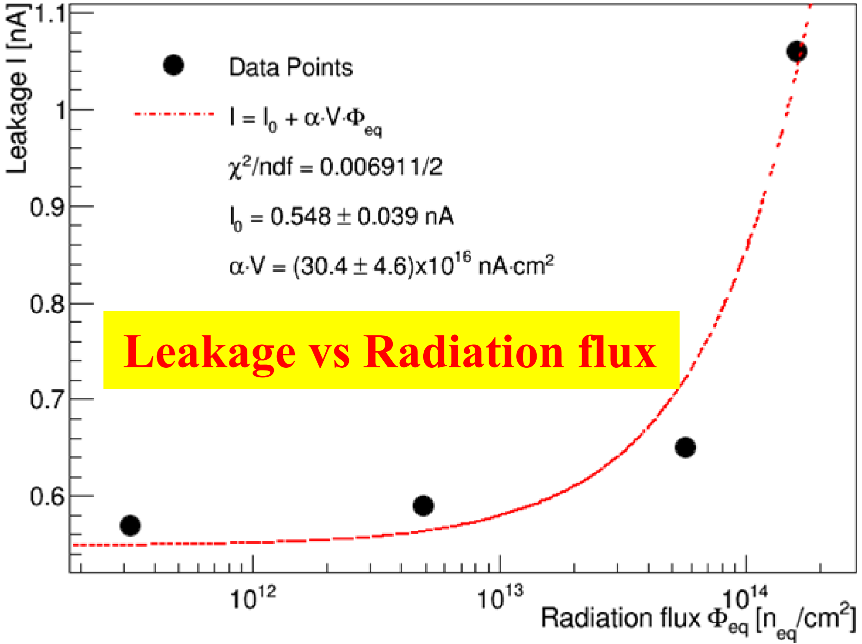
COFFEE2 Test

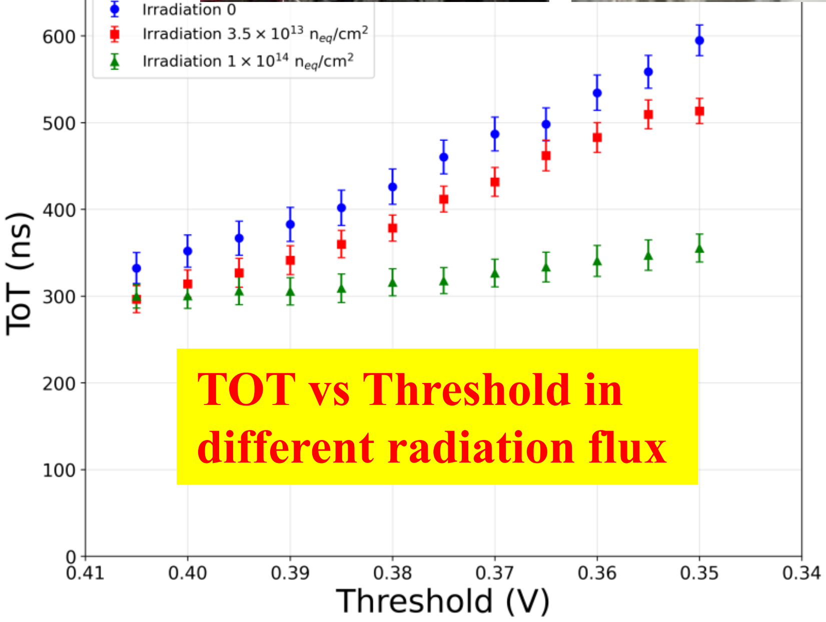


Radiation hardness test

- In LHCb UP Tracker, Radiation hardness target to $\sim 3 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$
- Proton irradiation at CSNS (China Spallation Neutron Source), up to $1.3 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$
- After $\sim 10^{14}\ \mathrm{n_{eq}/cm^2}$ radiation:
  - Leakage 10 pA → 1 nA
  - Capacitance and breakdown voltage remain unchanged
  - In-pixel circuit still work
- More studies are still ongoing


Proton beam test at CSNS

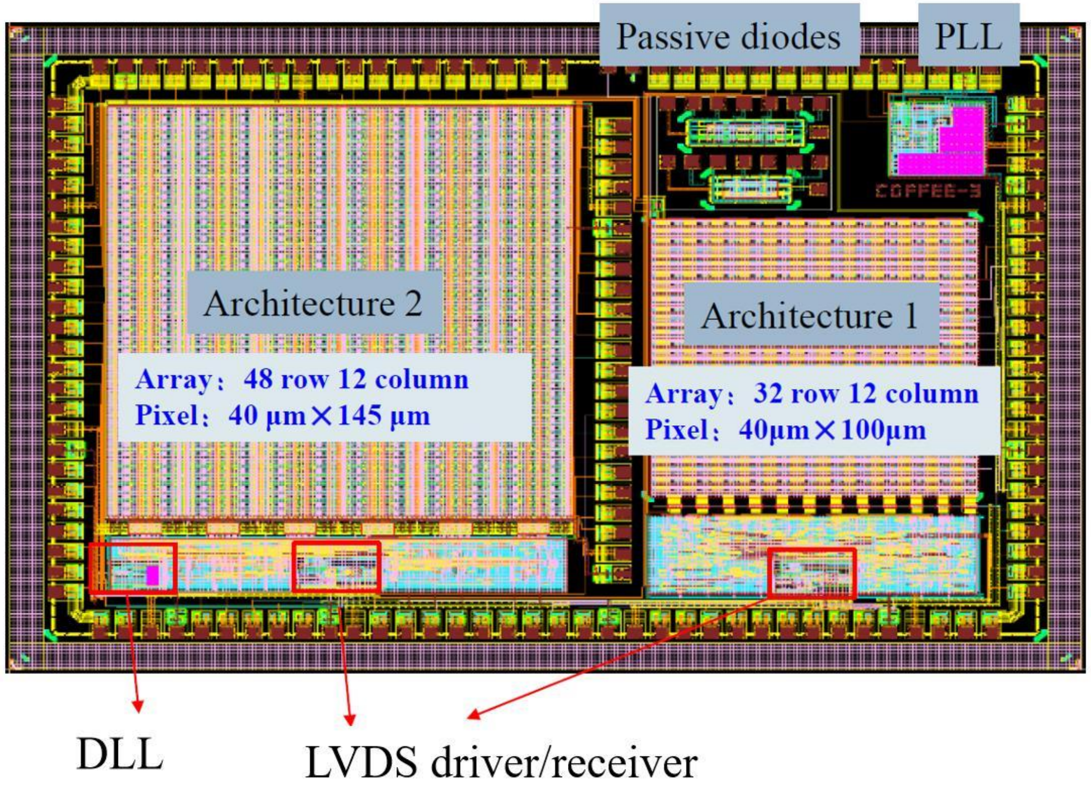

Leakage vs Radiation flux

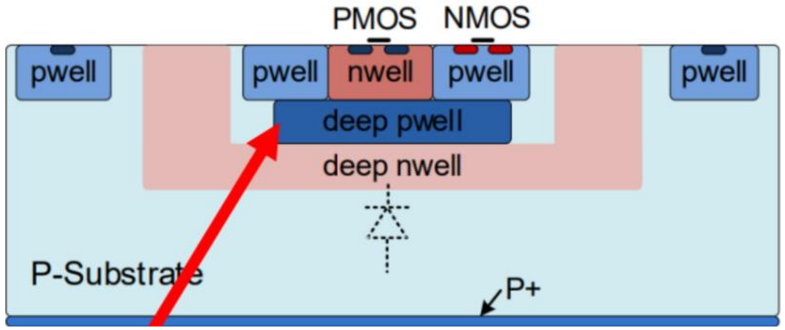

TOT vs Threshold in different radiation flux

COFFEE3 Introduction

COFFEE3 chip, $3 \times 4\ \mathrm{mm}^2$

- Passive diodes: same design as COFFEE2 chip, for further study of sensor and process
- Peripheral function modules: PLL, LVDS, DLL for IP accumulation and power consumption assessment
- Two pixel matrix readout architectures:
  - 1. CSA + NMOS design in-pixel, less crosstalk between analog and digital circuits
  - 2. CSA + CMOS design in-pixel, for future quadruple-well process. Advanced readout design, more suitable for high hit density situation
- Future quadruple-well process, add a deep p-well under n-well, reduce cross-talk between n-well and deep n-well



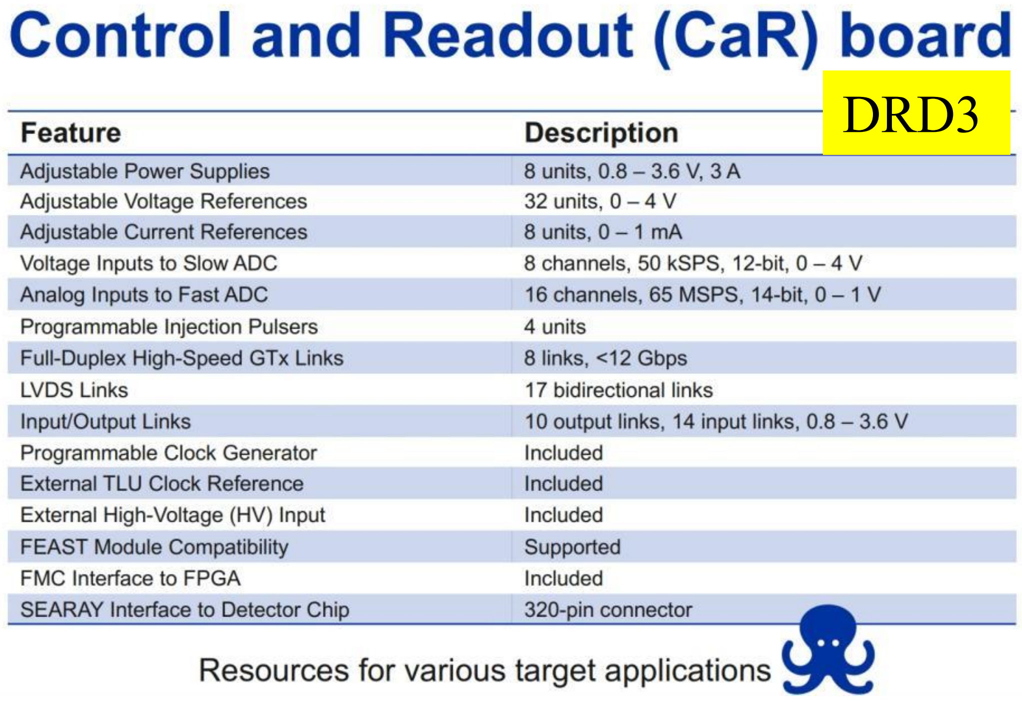


zengcheng@ihep.ac.cn

COFFEE3 Test

Pixels matrix array test system

- Test platform based on Caribou system: power, clock, DAQ, slow-ctrl, fast-readout, …
- PC + ZC706/ZCU102 + Caribou board + chip carrier board
- FE chip specific carrier board, firmware IP, software by ourself

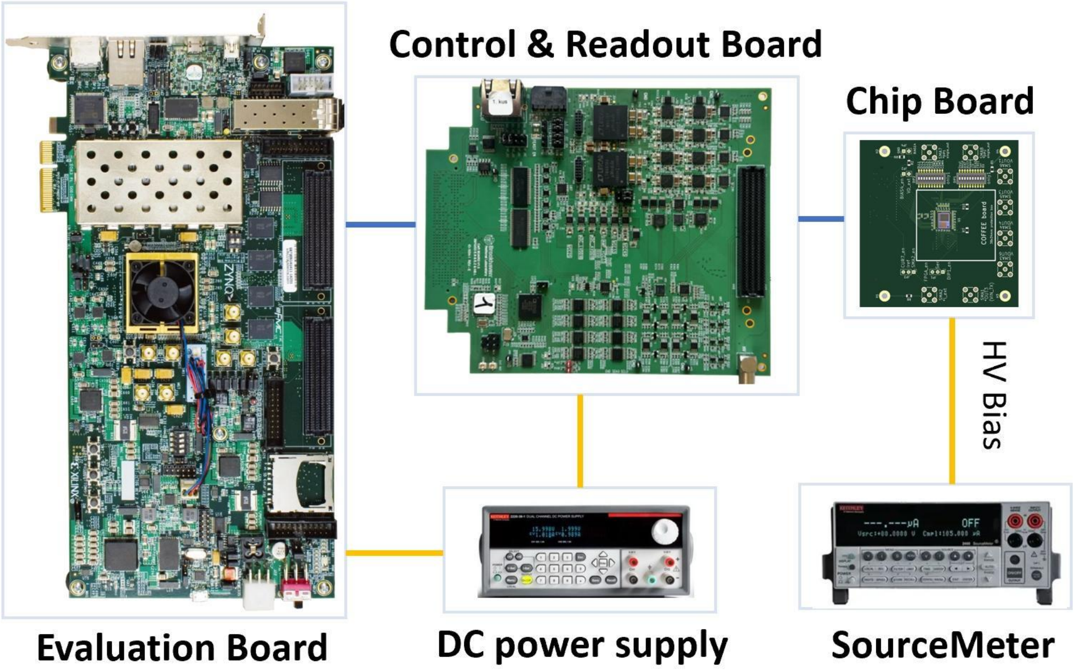


Control and Readout (CaR) board

DRD3

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

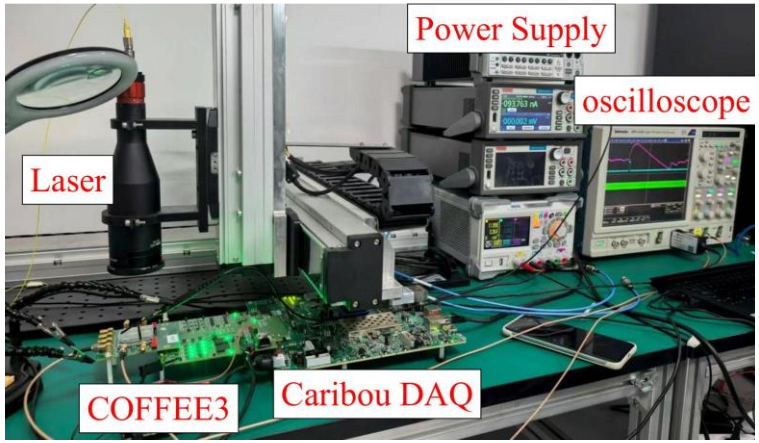
Resources for various target applications

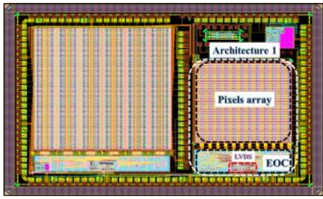


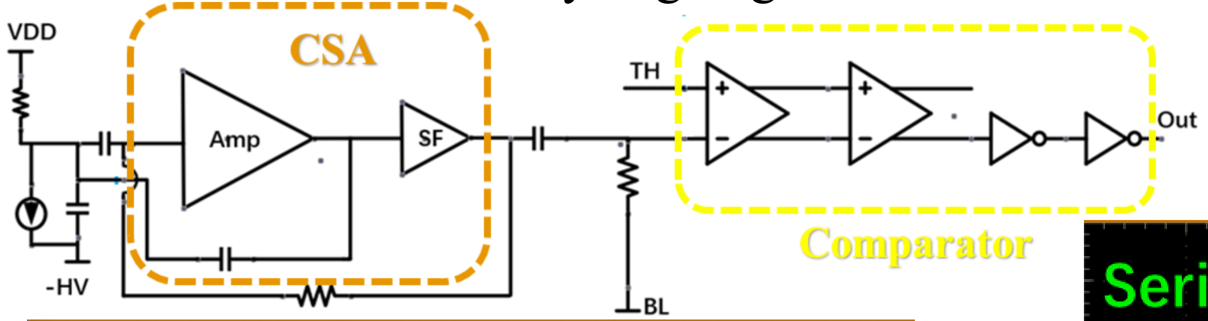
COFFEE3 Test

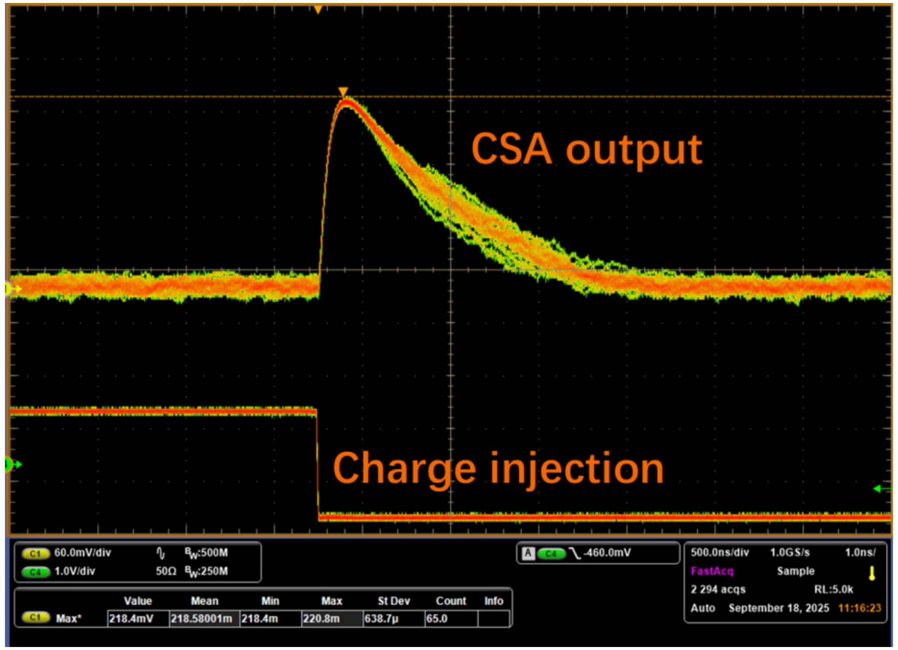
Architecture 1 test

- In-pixel circuit working well with charge injection and laser
- Digital readout function validated
- Radioactive source study ongoing

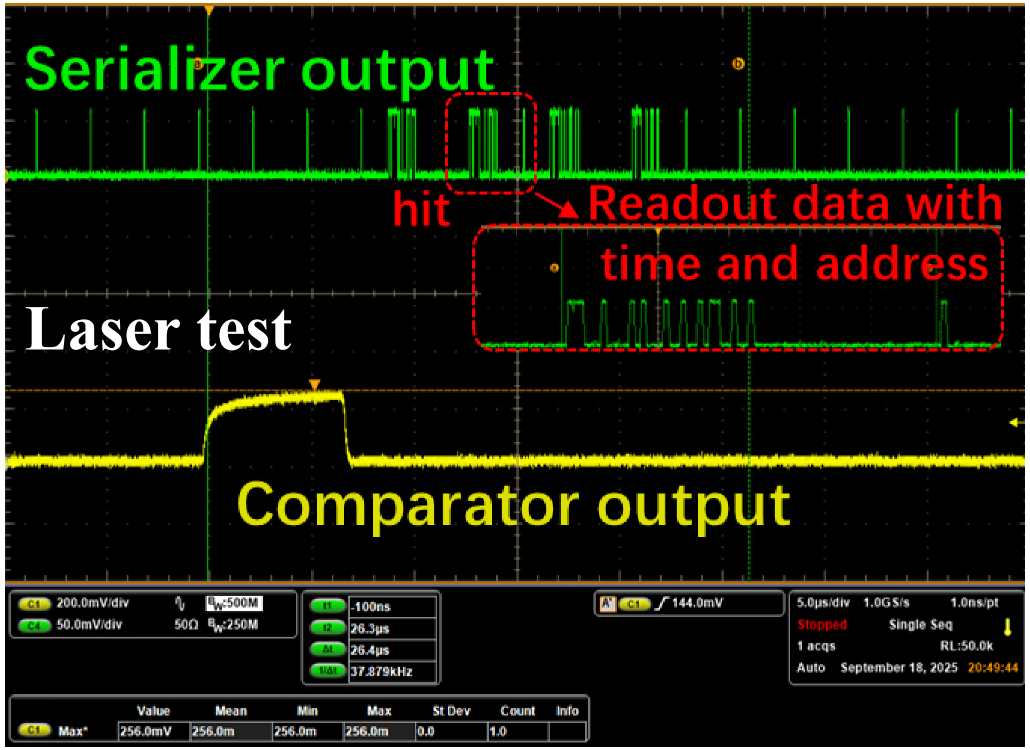




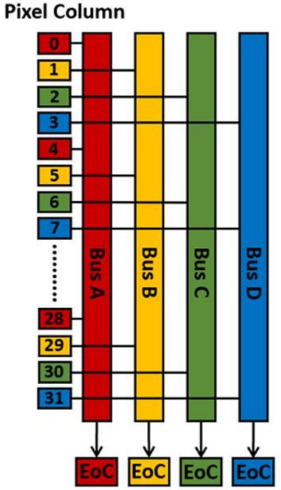




```
C1 60.0mV/div          BW:500M
C4 1.0V/div       50Ω  BW:250M
A C4 -460.0mV
500.0ns/div   1.0GS/s   1.0ns/
FastAcq       Sample
2 294 acqs    RL:5.0k
Auto   September 18, 2025  11:16:23
          Value     Mean         Min     Max     St Dev   Count  Info
C1 Max*   218.4mV   218.58001m   218.4m  220.8m  638.7μ   65.0
```



```
C1 200.0mV/div         BW:500M
C4 50.0mV/div     50Ω  BW:250M
t1   -100ns
t2   26.3μs
Δt   26.4μs
1/Δt 37.879kHz
A C1 144.0mV
5.0μs/div   1.0GS/s   1.0ns/pt
Stopped     Single Seq
1 acqs      RL:50.0k
Auto   September 18, 2025  20:49:44
          Value     Mean     Min      Max      St Dev  Count  Info
C1 Max*   256.0mV   256.0m   256.0m   256.0m   0.0     1.0
```

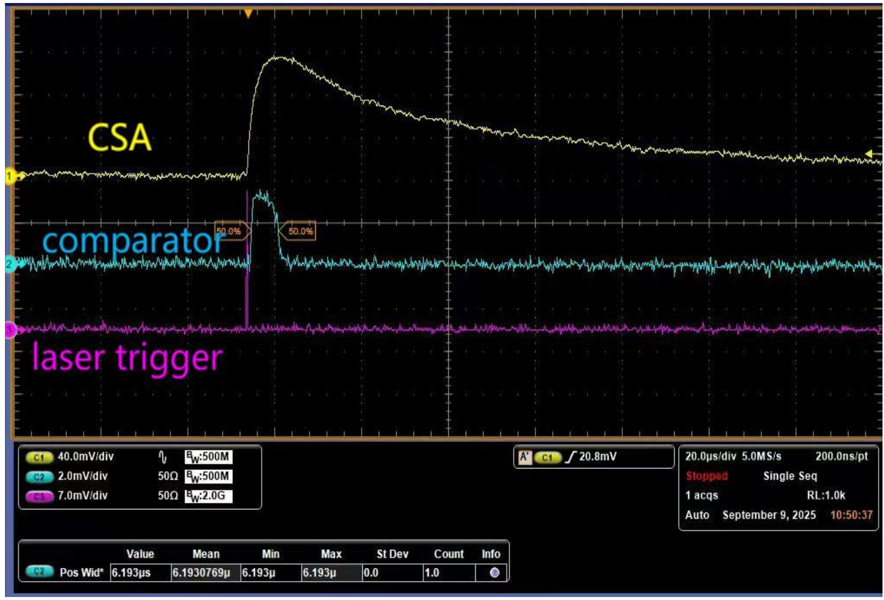


zengcheng@ihep.ac.cn

COFFEE3 Test

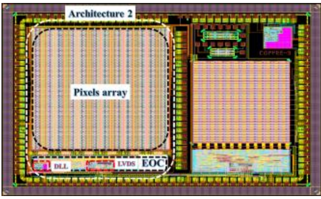
Architecture 2 test

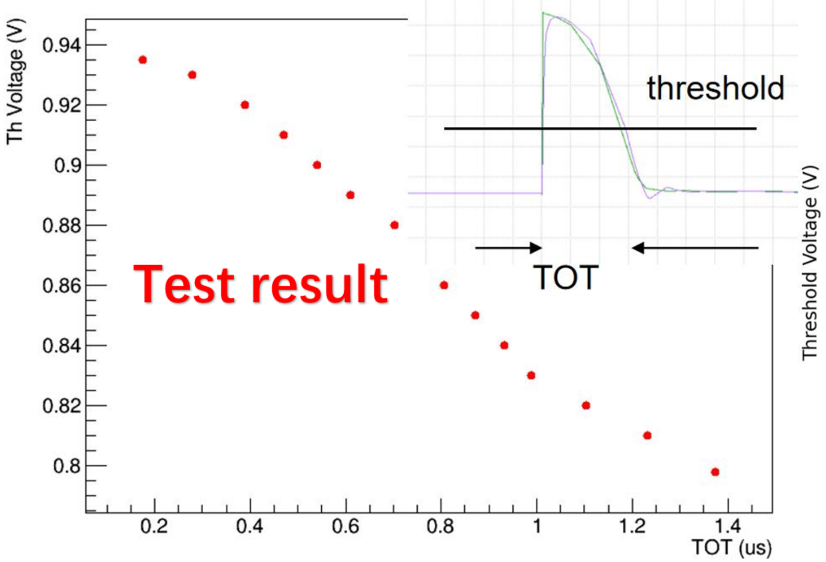
- In-pixel CSA and comparator output for laser signal
    - Typical time over threshold (TOT) of laser signal is consistent with simulation
- CSA response of ^{55}Fe signal can be seen, more study in near future

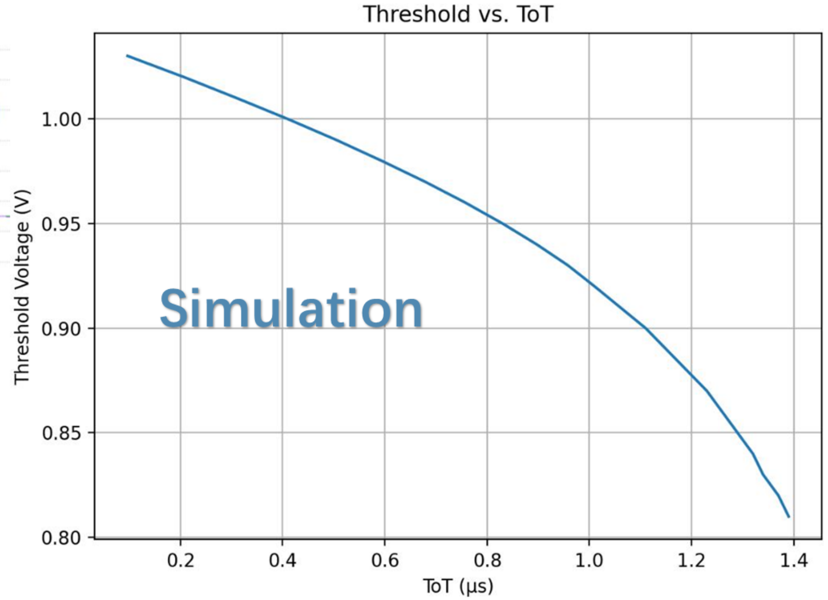


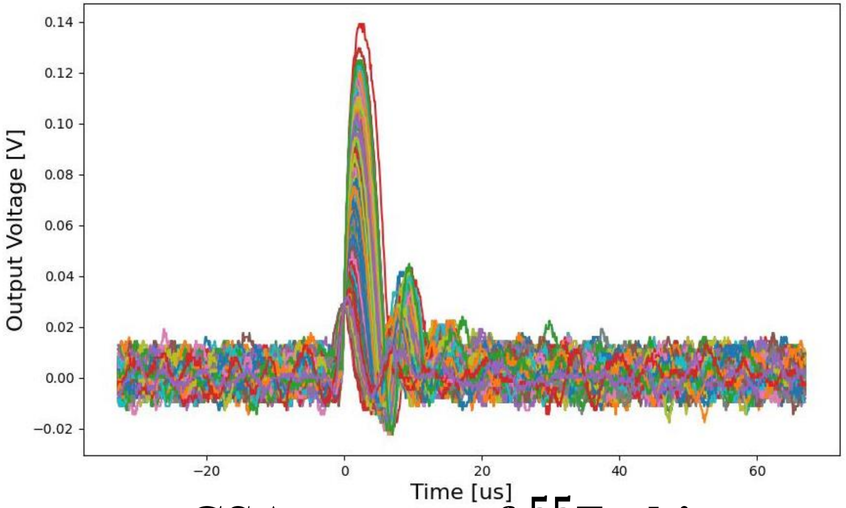
C1 40.0mV/div BW:500M
C2 2.0mV/div 50Ω BW:500M
C3 7.0mV/div 50Ω BW:2.0G
A' C1 20.8mV
20.0µs/div 5.0MS/s 200.0ns/pt
Stopped Single Seq
1 acqs RL:1.0k
Auto September 9, 2025 10:50:37

	Value	Mean	Min	Max	St Dev	Count	Info
C2 Pos Wid*	6.193µs	6.1930769µ	6.193µ	6.193µ	0.0	1.0	



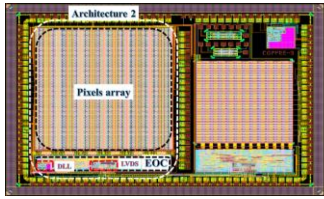






CSA output of ^{55}Fe hit

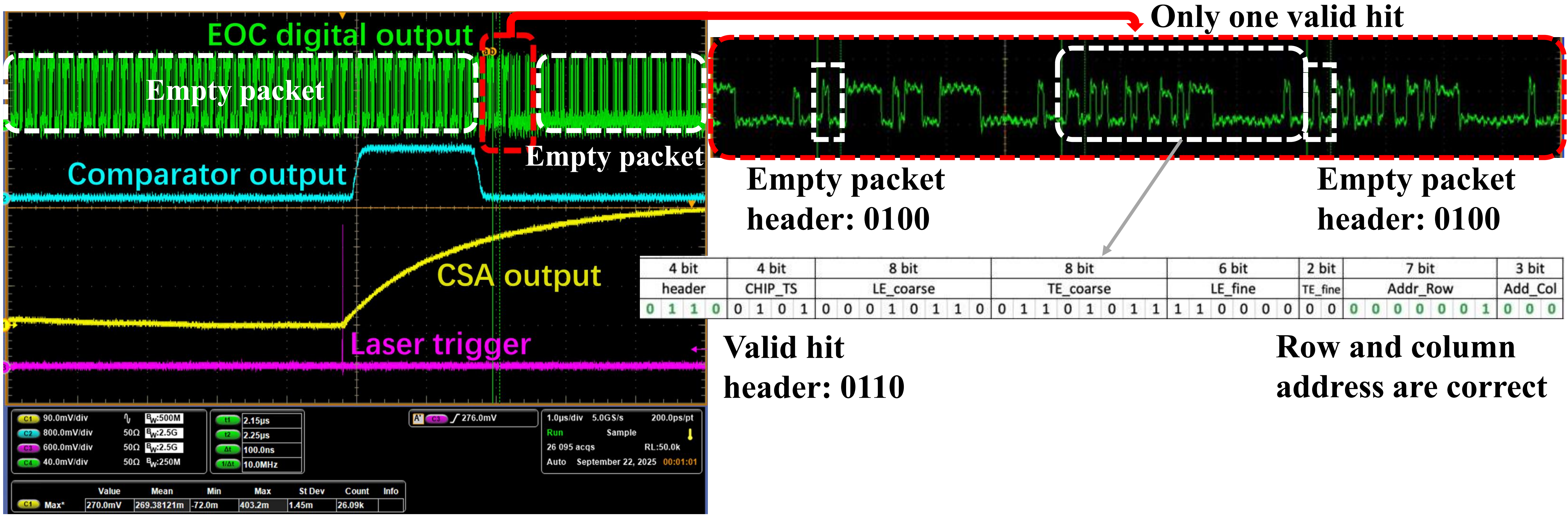
COFFEE3 Test



Architecture 2 test

- Full readout chain works well with laser test
  - Only unmask pixel column 0, row 1

Sensor diode → in-pixel (CSA, comparator, TDC) → End of column readout circuit → DAQ



C1 90.0mV/div BW:500M
C2 800.0mV/div 50Ω BW:2.5G
C3 600.0mV/div 50Ω BW:2.5G
C4 40.0mV/div 50Ω BW:250M

t1 2.15μs
t2 2.25μs
Δt 100.0ns
1/Δt 10.0MHz

A' C3 276.0mV

1.0μs/div 5.0GS/s 200.0ps/pt
Run Sample
26 095 acqs RL:50.0k
Auto September 22, 2025 00:01:01

	Value	Mean	Min	Max	St Dev	Count	Info
C1 Max*	270.0mV	269.38121m	-72.0m	403.2m	1.45m	26.09k	

Empty packet header: 0100

Empty packet header: 0100

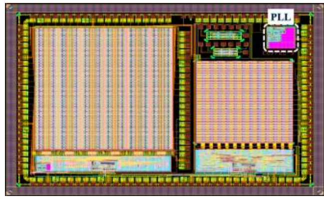
4 bit				4 bit				8 bit								8 bit								6 bit						2 bit		7 bit							3 bit		
header				CHIP_TS				LE_coarse								TE_coarse								LE_fine						TE_fine		Addr_Row							Add_Col		
0	1	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Valid hit header: 0110

Row and column address are correct

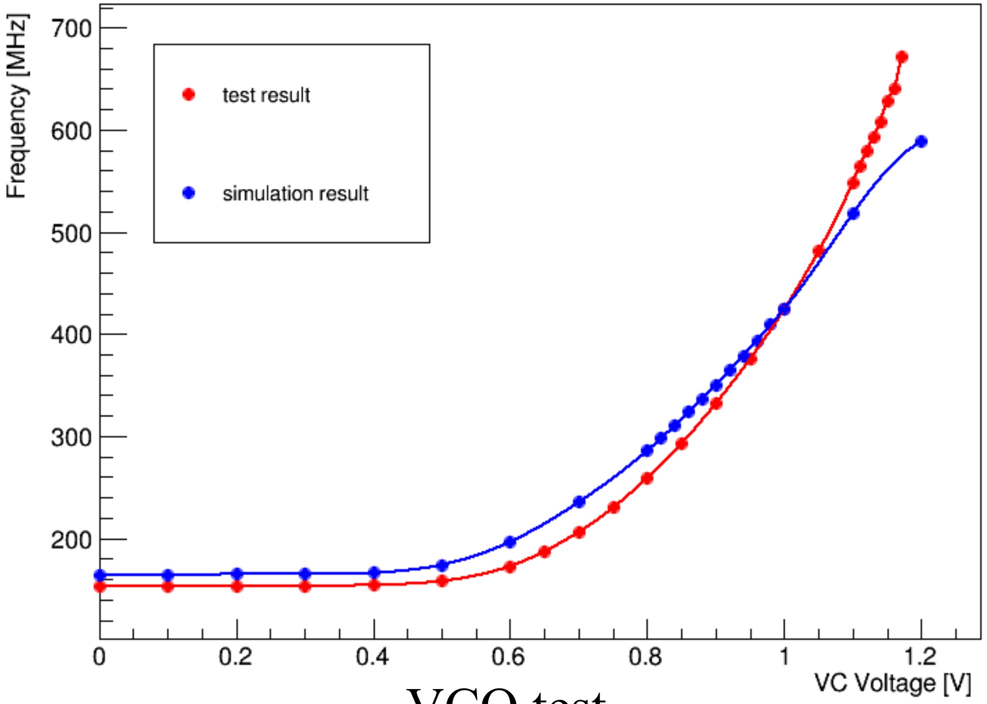
zengcheng@ihep.ac.cn

COFFEE3 Test

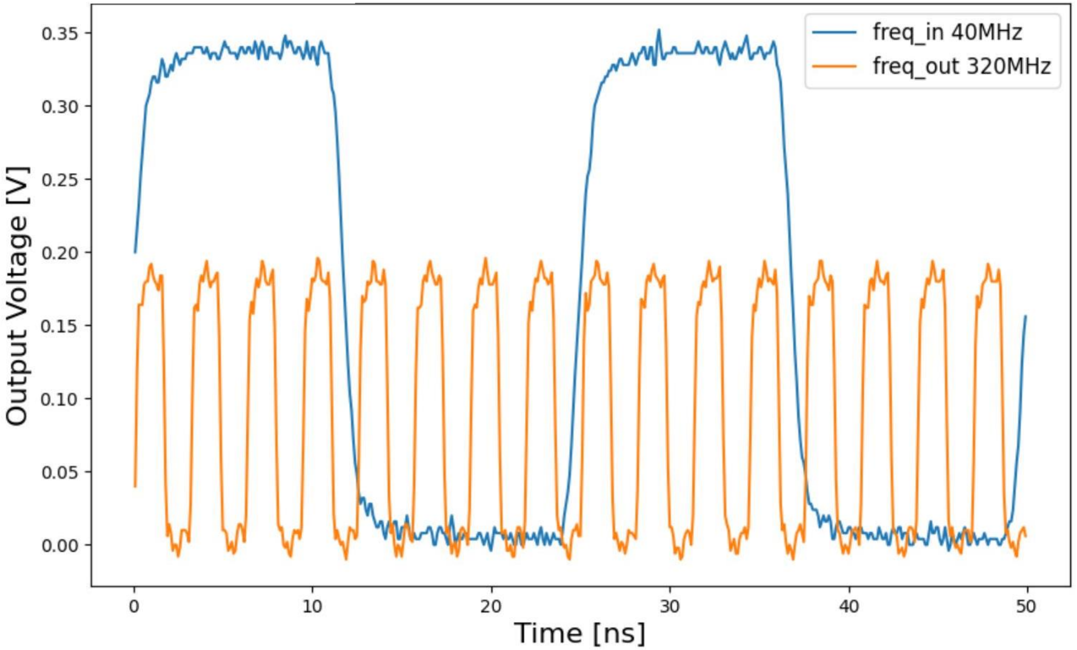


Phase locked loop (PLL) module

- Design for synchronizing the clock among chips and back-end DAQ
- Input CLK to generate internal clock to support TDC, high speed data transmission
- Voltage-Controlled Oscillator (VCO) and frequency multiply functions (x4, 8, 16) work well within the range up to 640 MHz
- Working fine from the room temperature to −50 ℃



VCO test

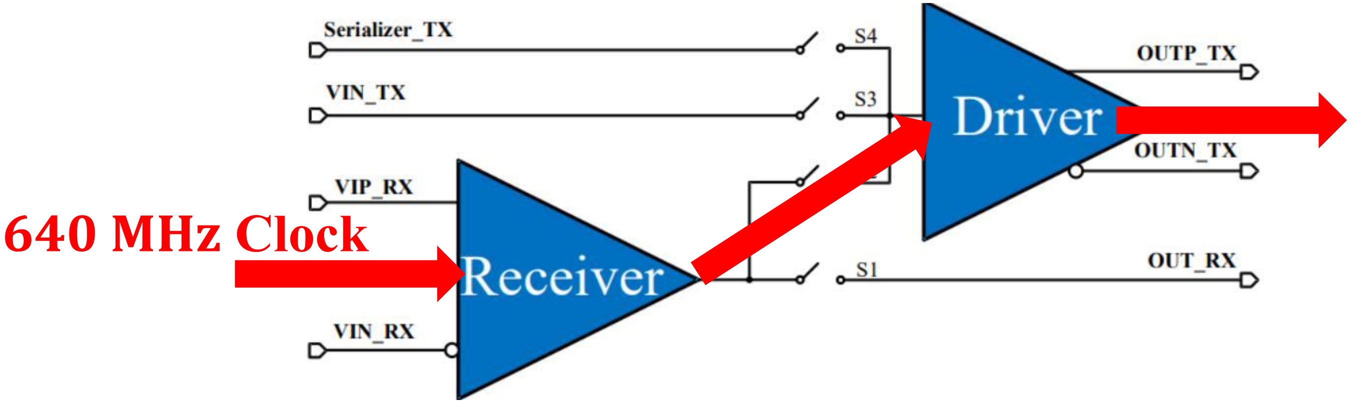


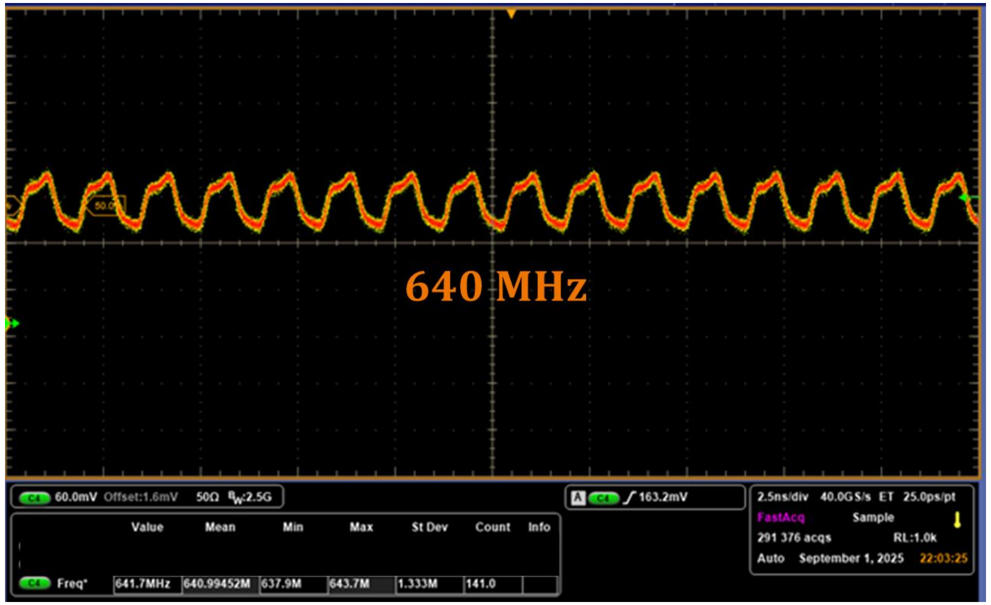
8x test, input 40 MHz, output 320 MHz

COFFEE3 Test

Peripheral circuit

- Data LVDS transceiver works up to 640 MHz supporting to 1.28 Gbps data transmission, to reduce common mode noise



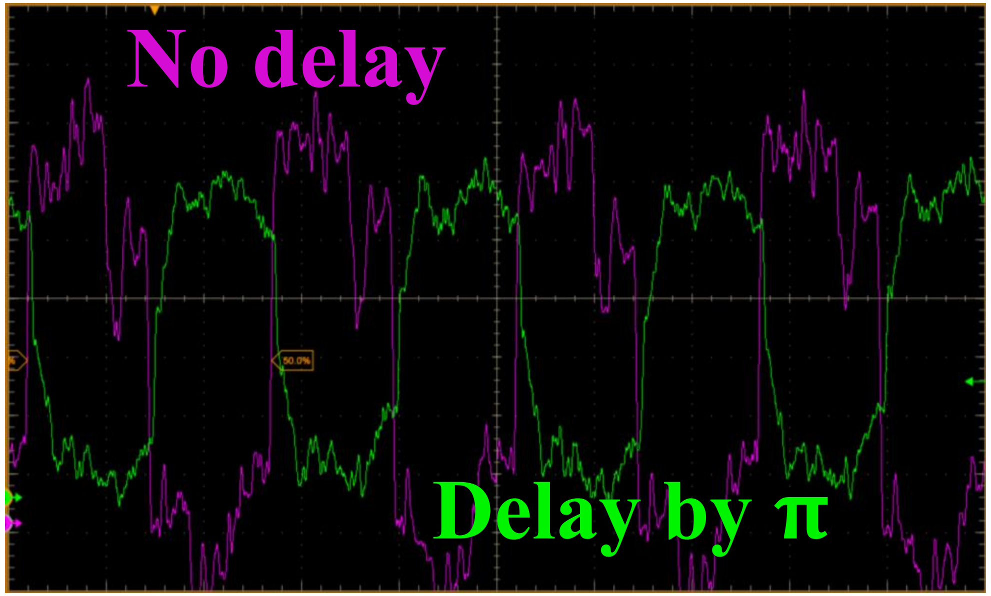


	Value	Mean	Min	Max	St Dev	Count	Info
C4 Freq*	641.7MHz	640.99452M	637.9M	643.7M	1.333M	141.0	

2.5ns/div 40.0GS/s ET 25.0ps/pt
FastAcq Sample
291 376 acqs RL:1.0k
Auto September 1, 2025 22:03:25

- Delay Locked Loop (DLL) delivers clock phase delay as expected, to eliminate timing errors generated during the transmission of clock signals within the chip

- Following successful validation, these modules (PLL, LVDS, DLL) can be used in future large chips



Summary

- HVCMOS prototyping chip in 55 nm process for UP at LHCb Upgrade II

- Many encouraging results from COFFEE chip:
  - Breakdown Voltage > 70 V, leakage ~10 pA
  - Two full readout pixel matrixes work well

- Future plan:
  - Full characterization of COFFEE3 chip:
    - Spatial and timing resolution, power consumption, radiation hardness
  - Seek process optimization for future chip design

Thanks for your attention!

Back up

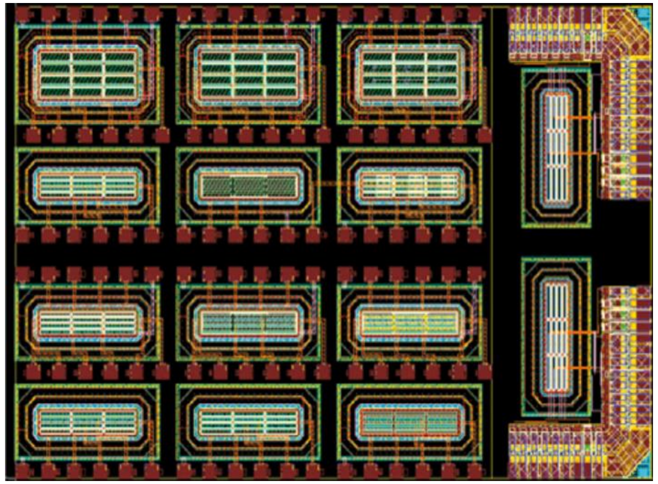
Back up

zengcheng@ihep.ac.cn

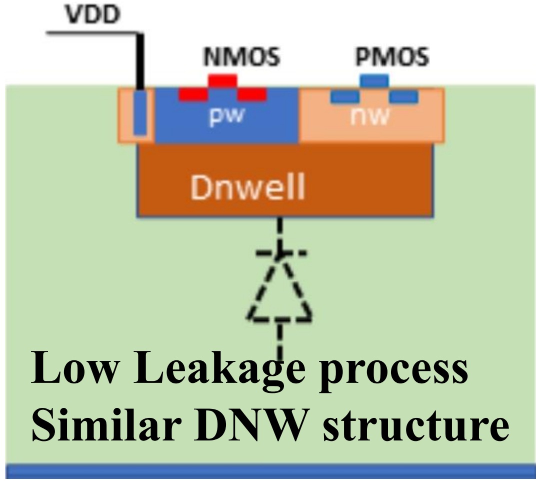
COFFEE1 Brief Result

COFFEE1 chip, 3 × 2 mm^2, verify the feasibility of 55 nm process. NIMA 1069 (2024) 169905

Pixel area
P-stop
DNW gap

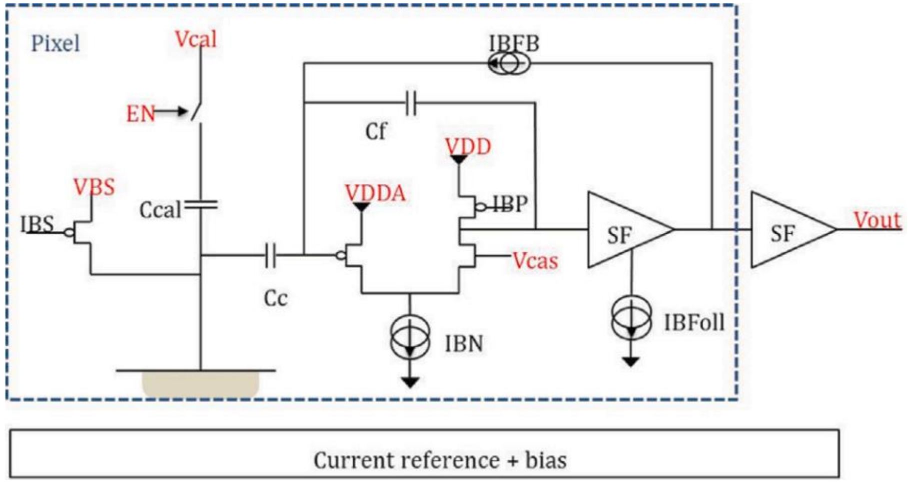


COFFEE1 chip floorplan



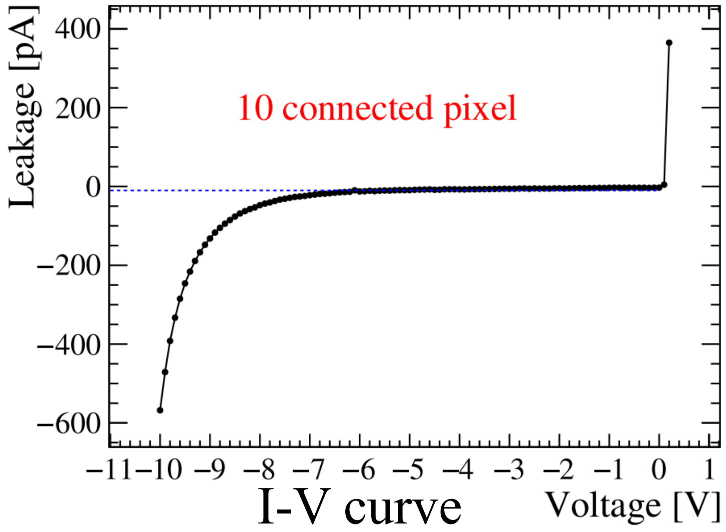
Low Leakage process
Similar DNW structure

Sensor cross section

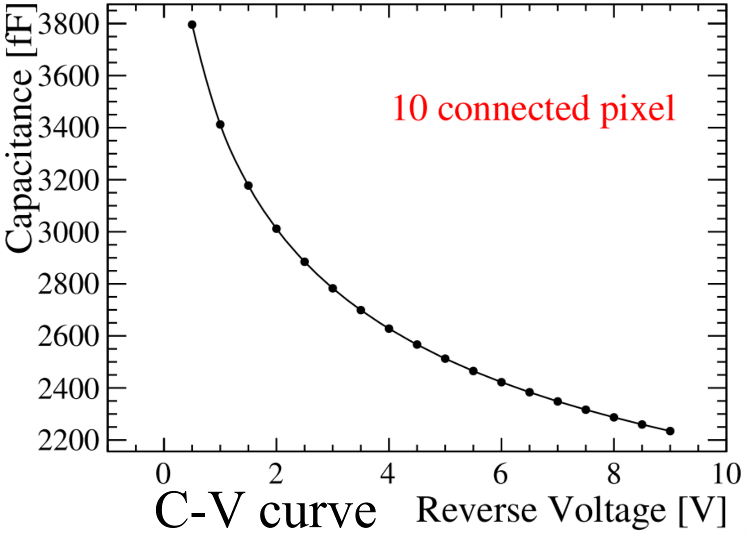


Schematic design of COFFEE1 in-pixel circuit

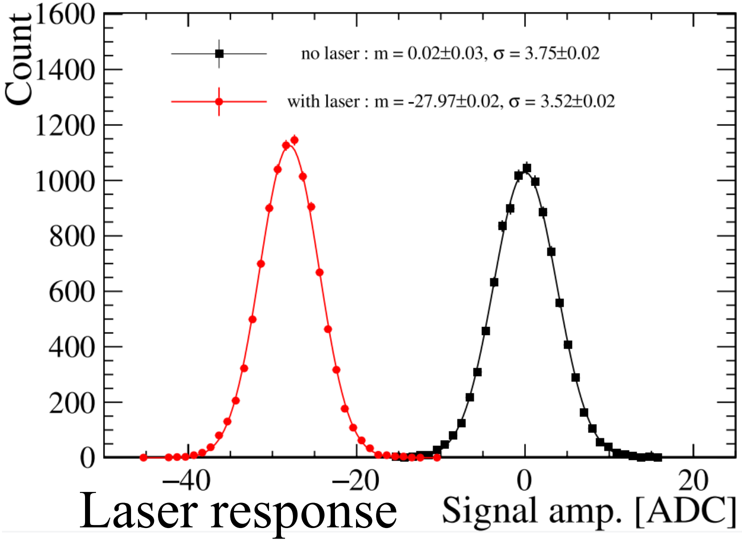
Breakdown Voltage: ~ − 9V, Leakage: ~pA, Capacitance: 150~200 fF, Laser response



I-V curve



C-V curve



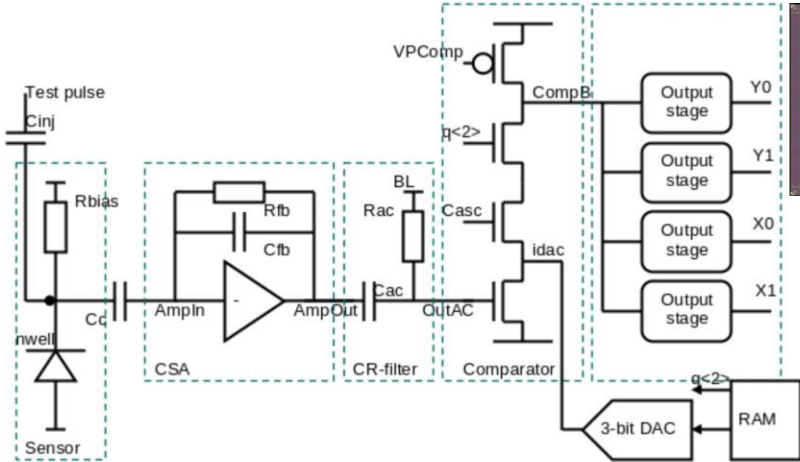
Laser response

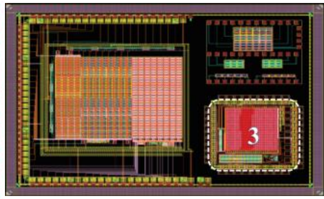
zengcheng@ihep.ac.cn

COFFEE2 Test

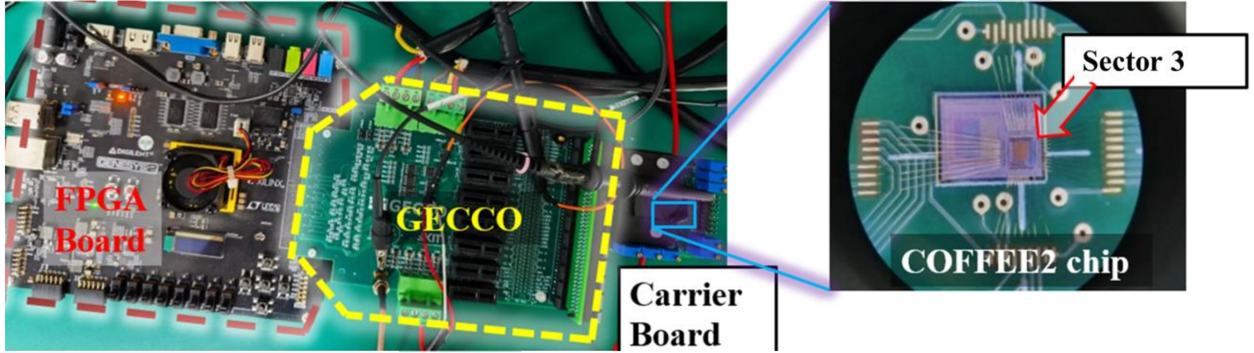
Section 3

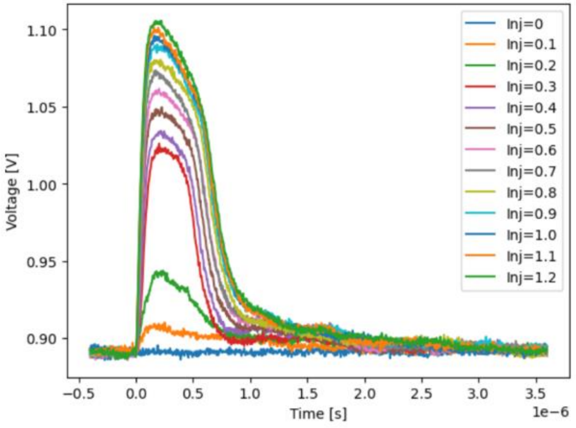
- Charge injection test: JINST 20 (2025) C03023
  - CSA waveform in expected
- Radioactive sources test:
  - ^{55}Fe (5.9 keV X-ray), Gaussian fit
    - $\mu\sim73$ mV$\sim1640\ e^-$
    - $\sigma\sim2.6$ mV$\sim58\ e^-$
  - ^{90}Sr (β-source), Landau fit
    - MPV: ~50 mV~1100 e^-
    - Depletion depth: ~10 μm

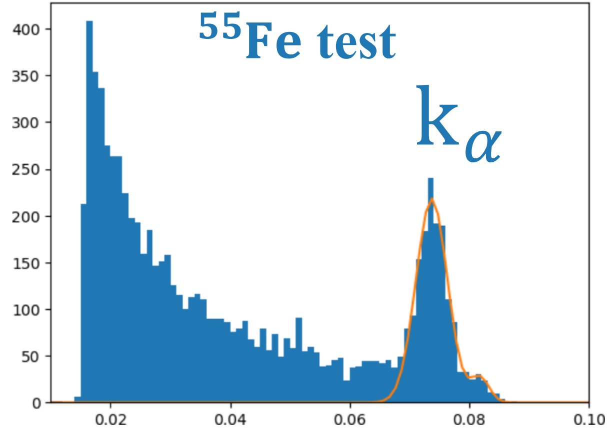


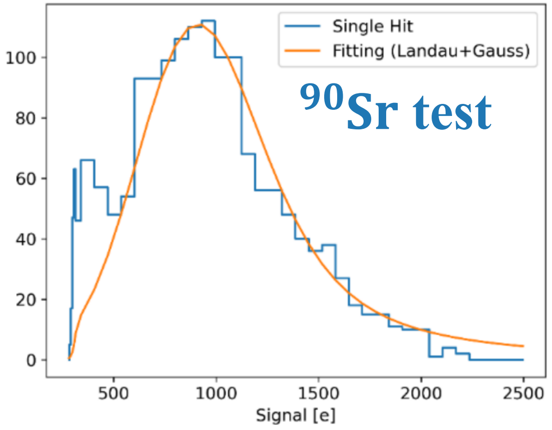


Test setup:









zengcheng@ihep.ac.cn