Timing measurements with the ATLAS HGTD at the HL-LHC

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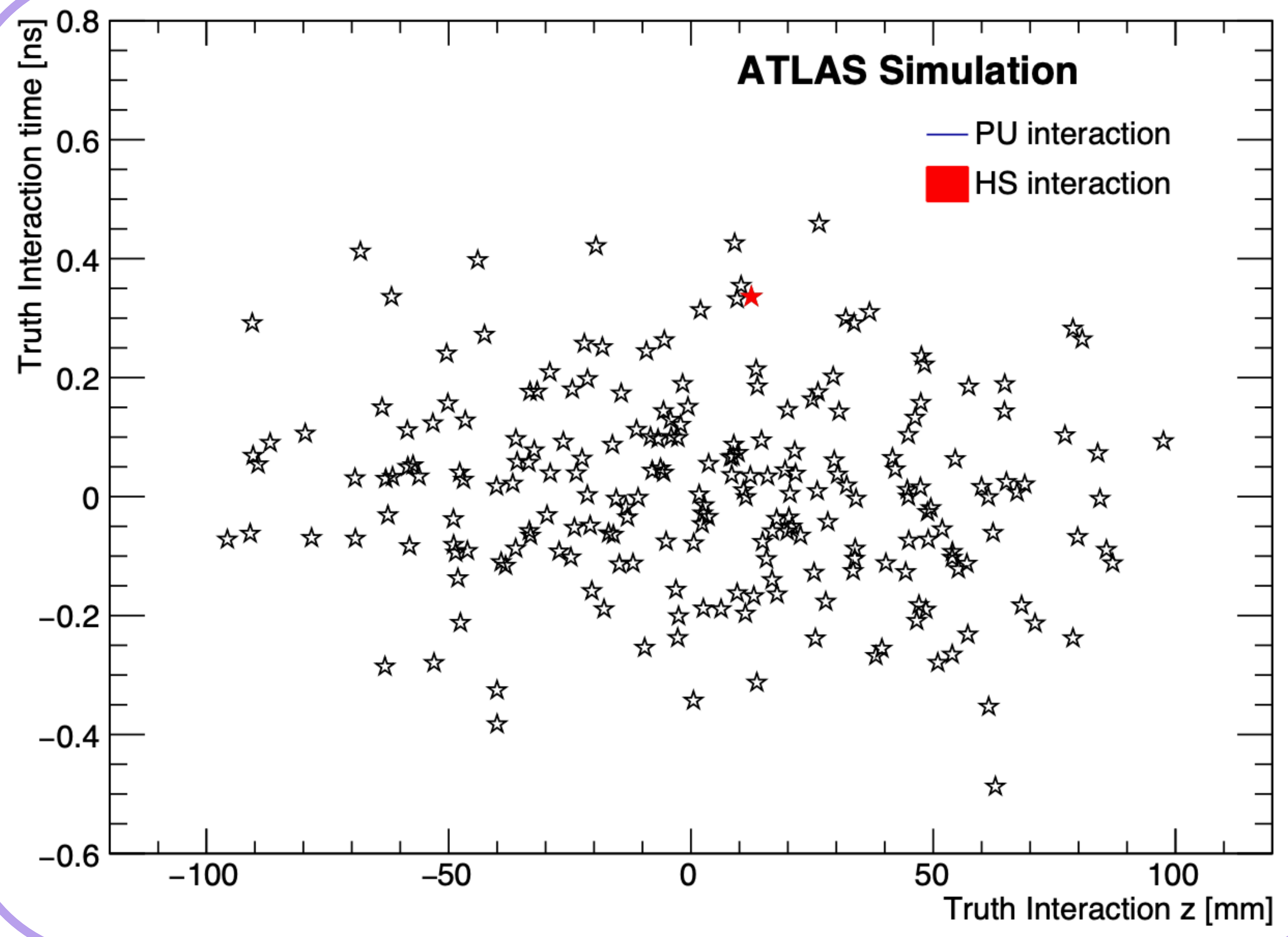
Introduction

- Timing precision of High Granularity Timing Detector (HGTD) takes into account effects from detector and the electronics (intrinsic resolution of the measurement) and the clock stability

$$\sigma_{tot}^2 = \sigma_L^2 + \sigma_{elec}^2 + \sigma_{clock}^2$$

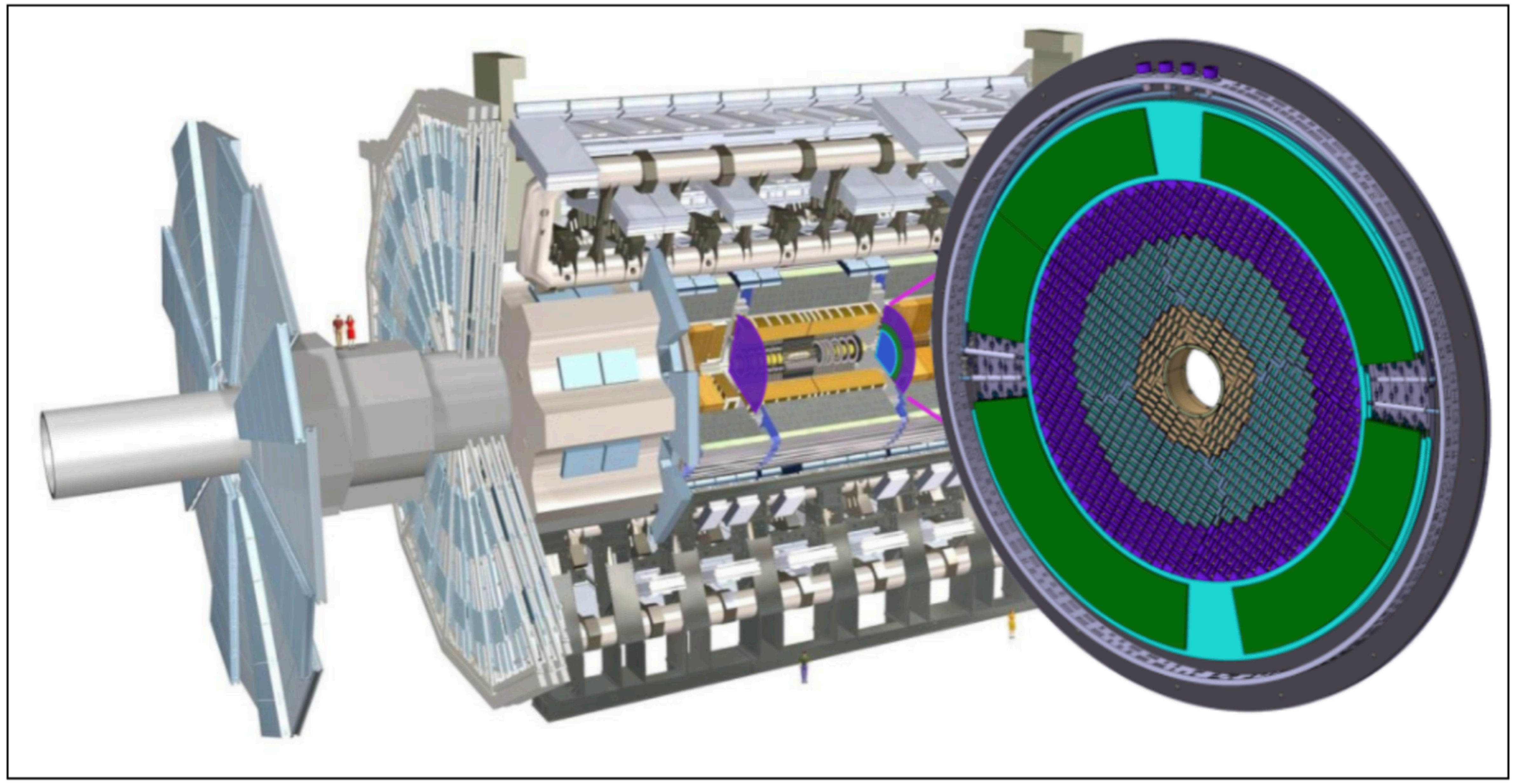
  - Clock contributions are separated in *fast* (jitters) and *slow* variations (biases)
- **Goal of timing calibration:**
  - Remove all the biases from all sources, via a data driven technique
  - All particles emitted from the same position z_0 at same time t_0, lead to the same measured time (t_{ref}) in all pixels.



- **In today's talk:**
  - Overview on the HGTD detector, timing simulation chain and effects impacting the timing resolution
  - Proposal of an algorithm to extract/assess the clock phase difference effect not previously considered
    - ***Studies shown are preliminary!***

HGTD in the ATLAS experiment

- The High Granularity Timing Detector (HGTD) will be crucial to pile-up mitigation at High Luminosity (HL) LHC
    - It will ebable the separation of vertices when z_0 (longitudinal track impact parameter) resolution becomes higher than the distance between two vertices (reduced number of vertices to be considered for a track)



Global view of the HGTD to be installed on each of two end-cap calorimeters (±3.5 m)

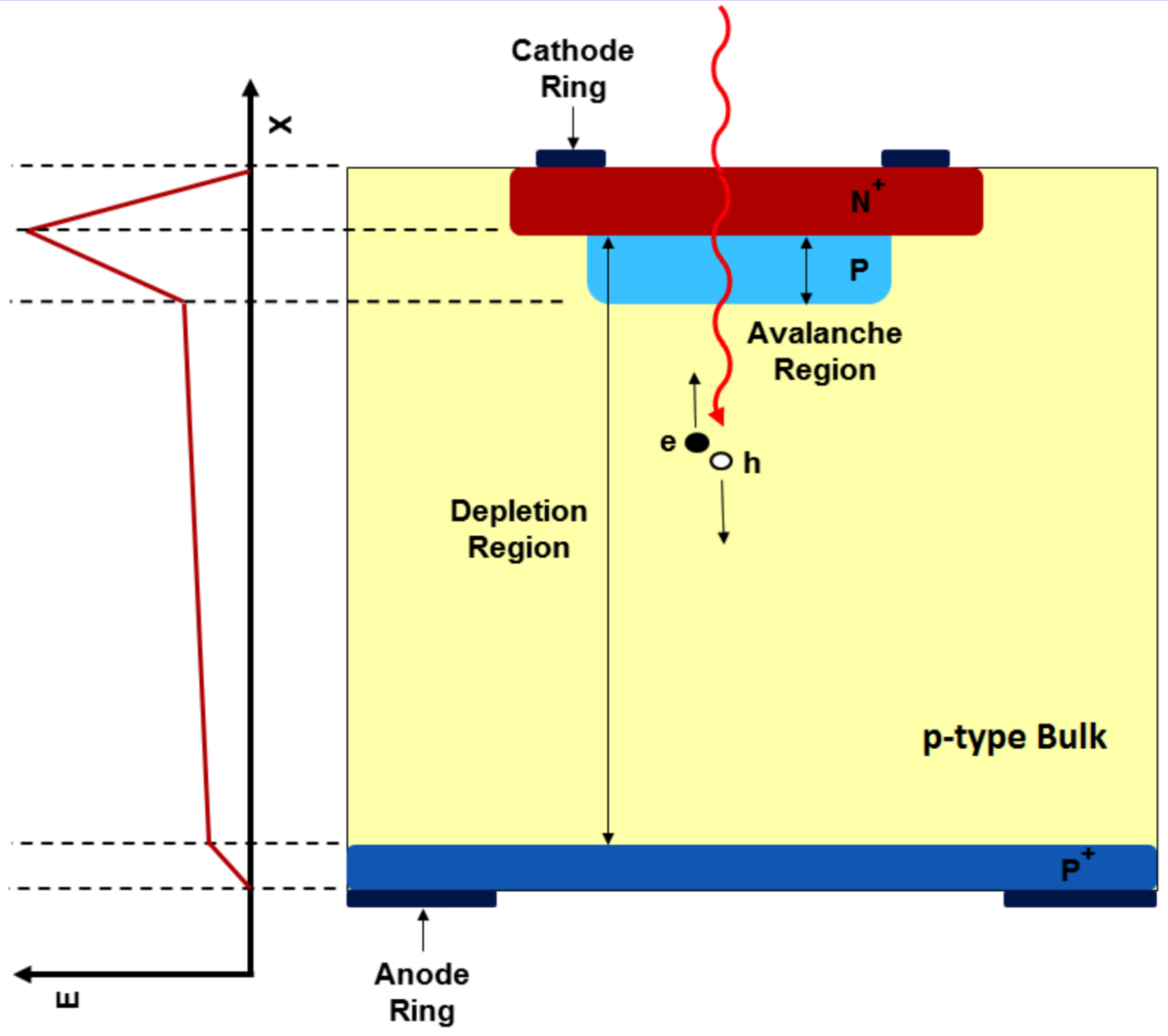
- Located at in the gap region between barrel and end-cap calorimeter (z = ±3.5 m (from IP))
- 2 instrumented double-sided layers (mounted in two cooling disks with sensors on the front and back of each cooling disk)
    - Active area of the detector is 120 to 640 mm
    - Rotated in opposite directions (15°-20°): maximize uniformity in N_hits per track
- Expected per-track timing resolution: better than 30 ps at the start of HL-LHC and about 50 ps by its end

A HGTD Module

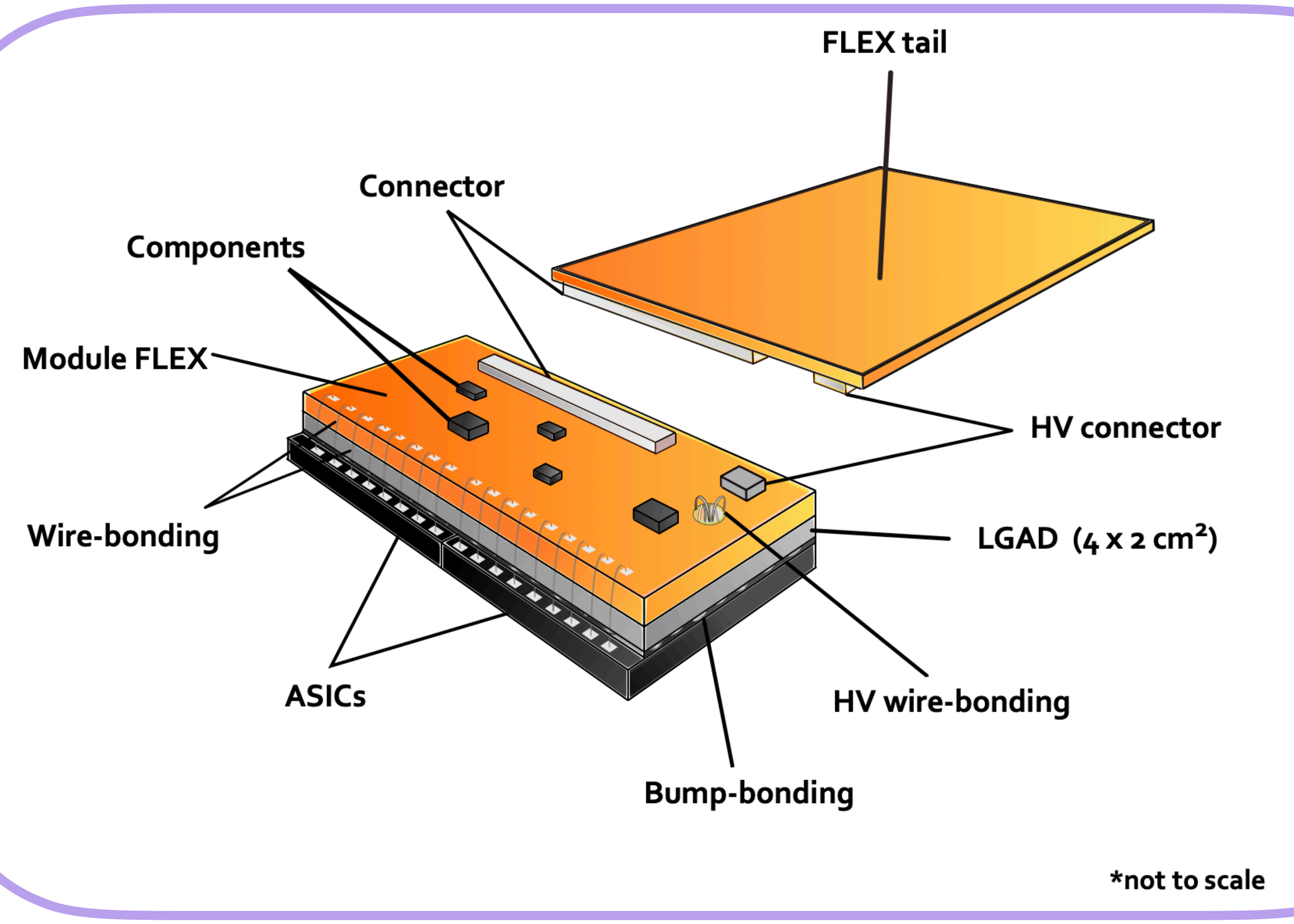
- A HGTD module is made up of 2 Low Gain Avalanche Detector (LGAD) sensors connected to 2 ALTIROC ASICs (for readout)

LGAD sensors

- n-on-p junction with an extra p^{+} gain layer
  - High electric field, charge amplication
    - Timing resolution improves significantly



- LGAD sensor is 15x15 pads
  - HGTD will have 8032 modules
- 2 ALTIROC ASICs, each reading a matrix of 225 (15 x 15) pads
- Each pad is 1.3 mm × 1.3 mm
- In total, HGTD has 3.6 M channels

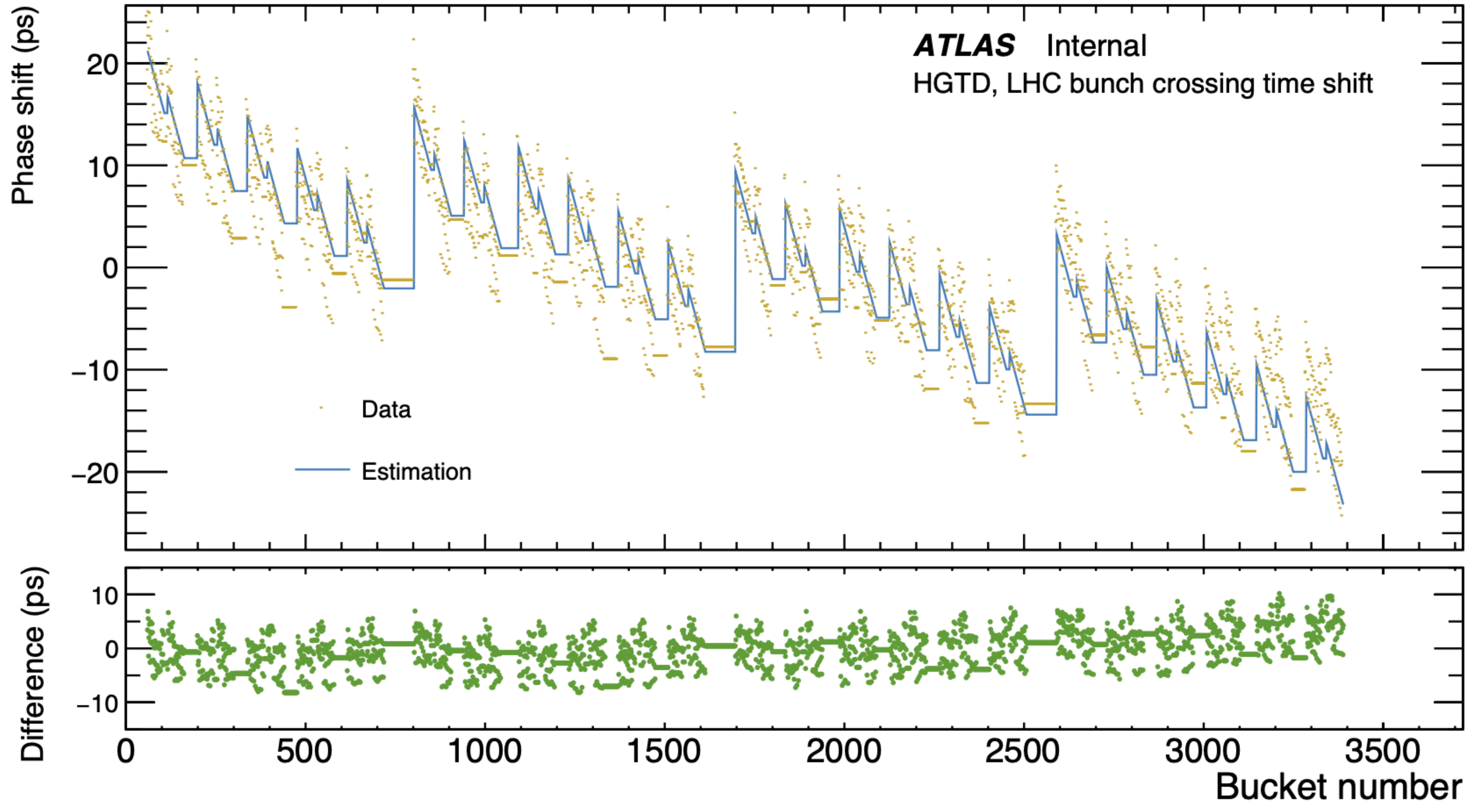


Effects on hit's time resolution

Examples of effects on hit's time resolution:

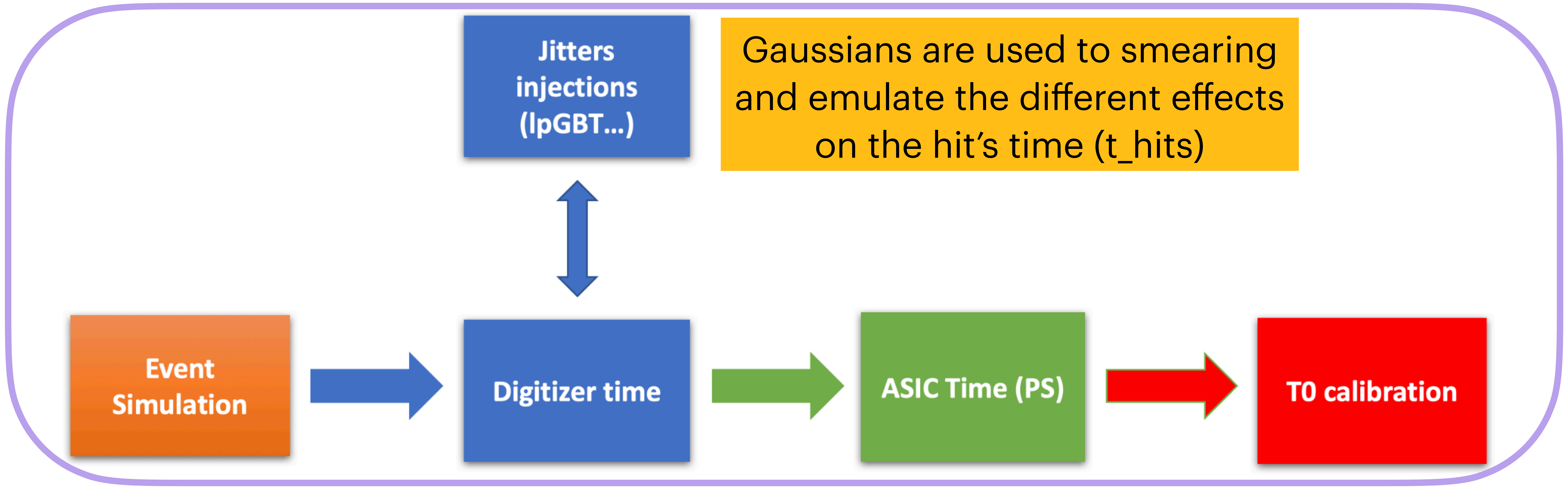
- *ALTIROC ASICS (front-end electronics)* ***(Jitter and static effect)***: clock distribution network within the front-end (ALTIROC) ASIC and resolution on the comparison between signal and clock distribution;
- *Flex cables* ***(Jitter)***: noise pickup and signal degradation as the clock travels over the long traces on the flexible printed circuit board;
- *lpGBT* ***(Jitter)***: radiation-tolerant ASIC that provides Timing and Trigger Control (TTC), Data Acquisition (DAQ) and Slow Control data (SC) in a single link. Variation from the clock as recovered and distributing it.
- Expected bunch crossing time offset is expected to be arounf 40ps; however, the deviation between the predicted and measure shift time is around 3ps.

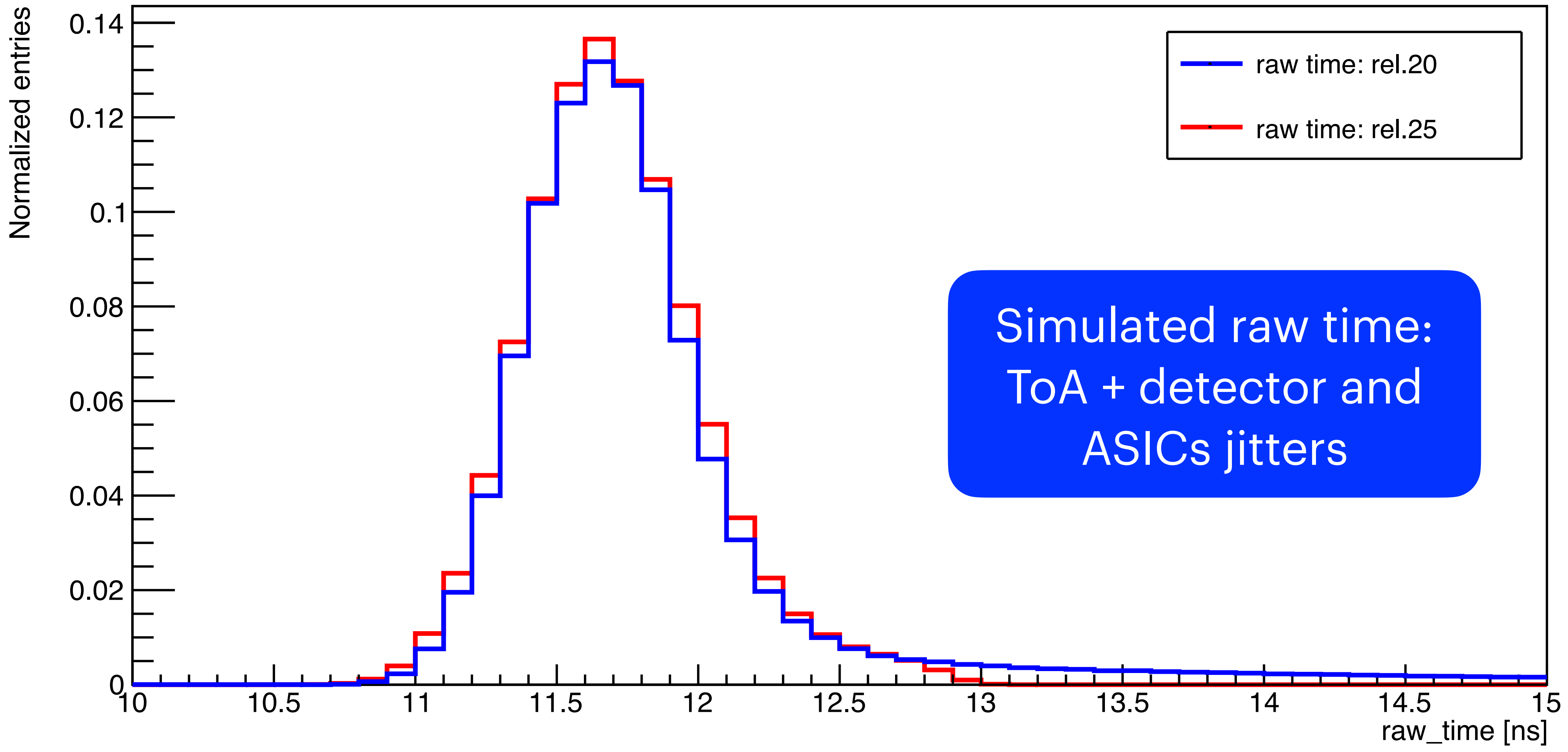
Template of the time shift introduced as a function of the bucket number in the smearing studies



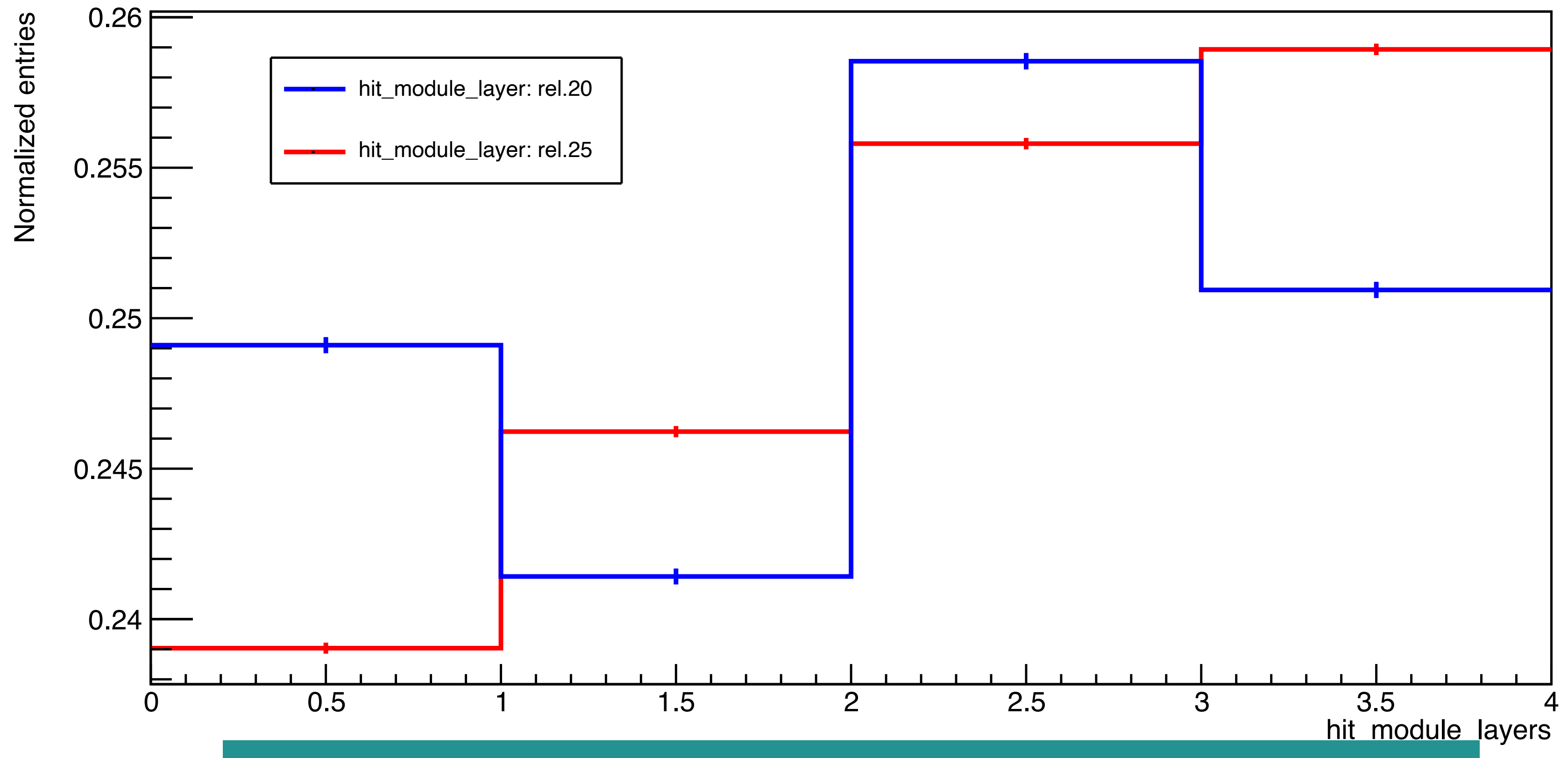
The residual effect has a RMS of 3.3 ps and is flat with respect to the bucket number.

Timing Simulation: Brief Overview



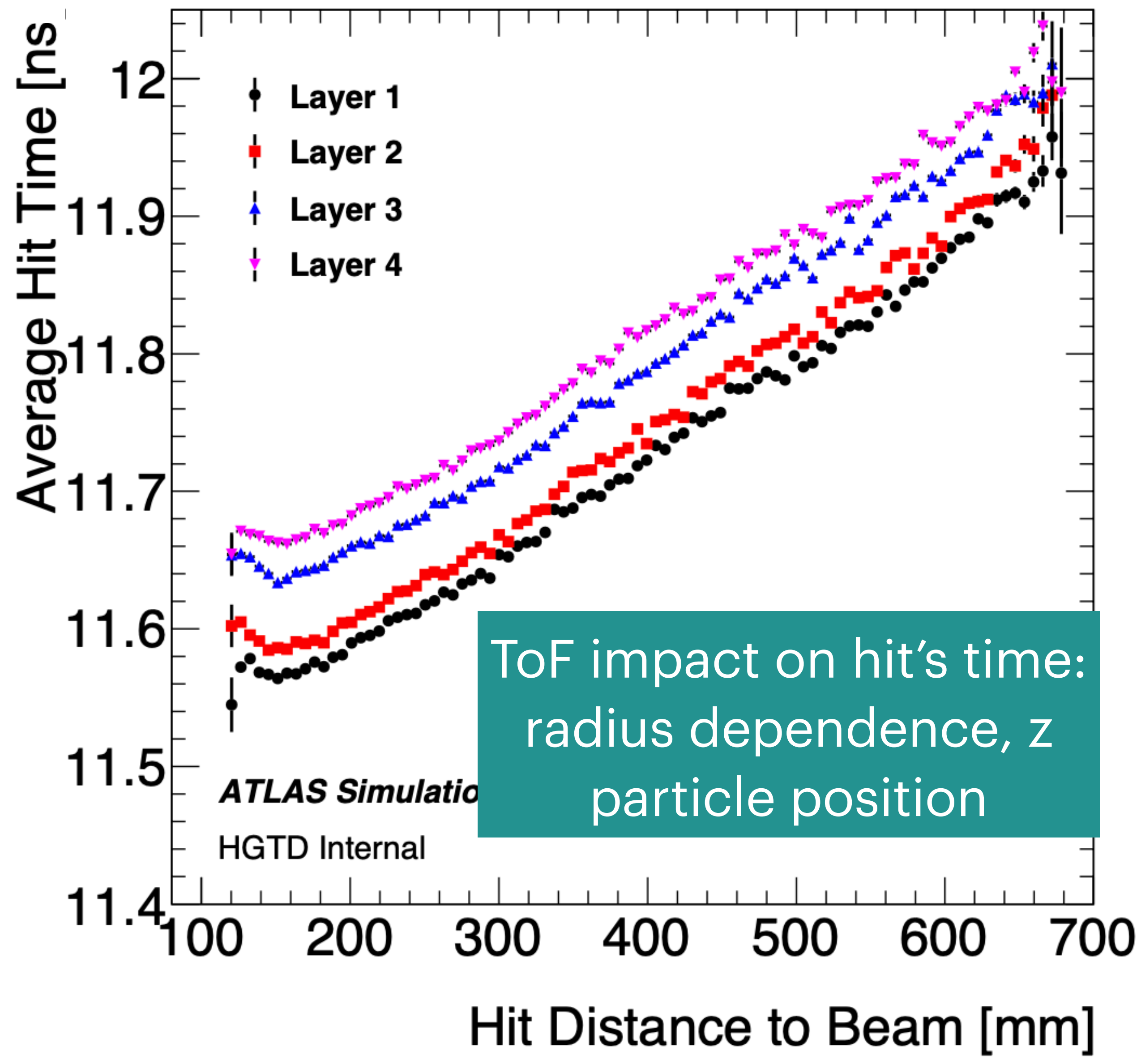


Absence of the tails wrt Rel. 20 n-tuple is expected due to the ASIC precision



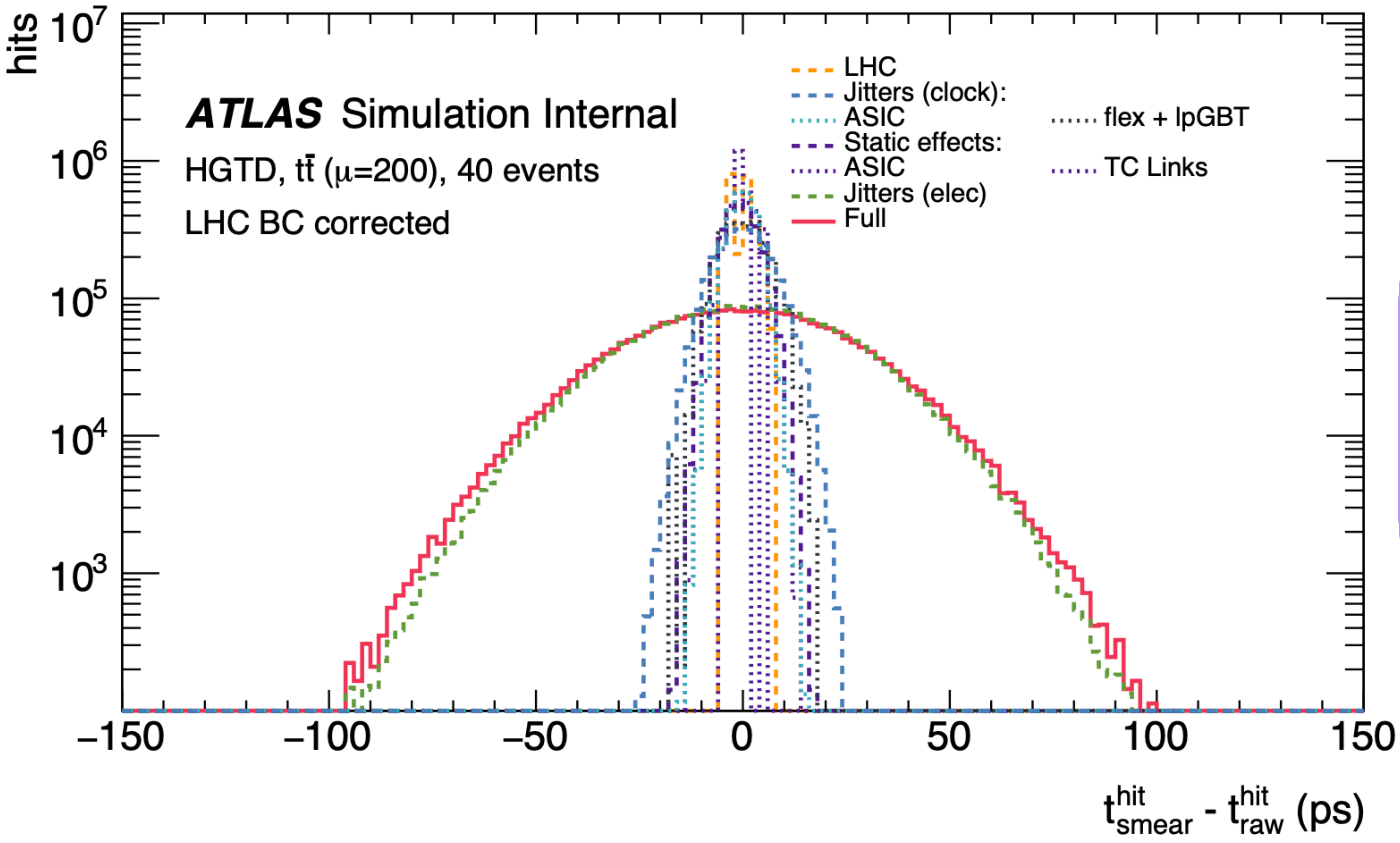
Reasonable behaviour: the further we go out, the more material is seen. So particles shower in HGTD as well.

RDO TTbar (**rel. 25**)



Effects impact on timing resolution

Preliminary result with release 25



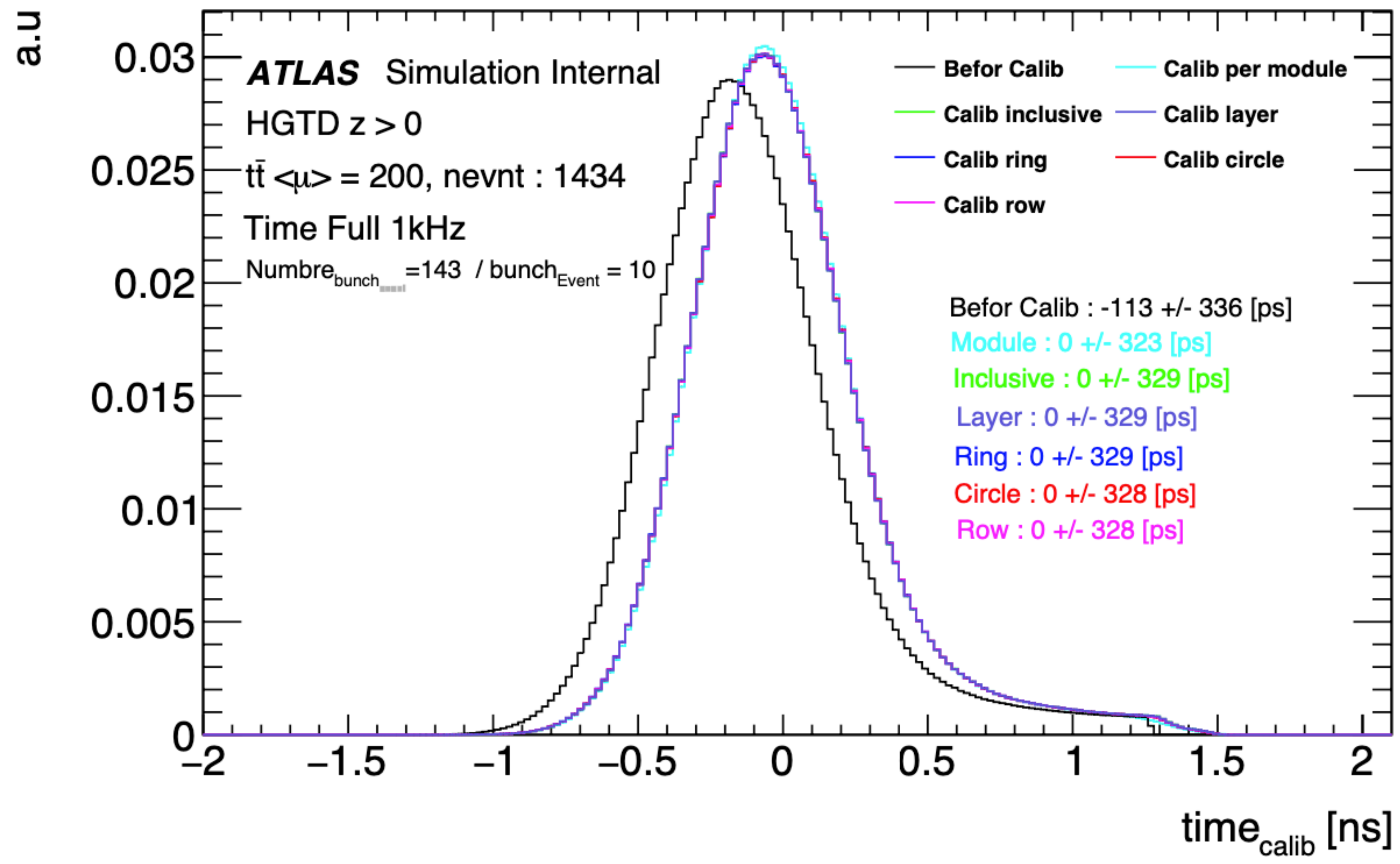
- **Difference between t^{hit}_{smear} and t^{hit}_{raw}**
  - t^{hit}_{raw} is the digitalized hit's time
  - t^{hit}_{smear} is t^{hit}_{raw} with some smearing emulating on an effect applied on top of it

- Additional studies and the development of tools to further understand the significant and missing effects are ongoing.

Clock phase difference effect: Motivation

- **Problem:** The time-of-arrival (TOA) of hits in the HGTD's LGAD sensors, measured by the ALTIROC ASIC, is referenced to a local LHC clock. However, the phase of this local clock relative to the original LHC clock is unknown and varies across different ALTIROCs due to the complex clock distribution network.
- **Challenge:** The ALTIROC ASIC has no built-in hardware to measure this clock phase information.
- **Proposed Solution:** A software algorithm is developed to calibrate and determine this systematic clock phase difference using data collected when the HGTD is fully installed and commissioned in ATLAS.
- **Goal:** To correct for systematic clock phase differences, which are a source of systematic error, and ensure accurate time measurements.
- **Limitation:** The proposed algorithm will not address random errors like clock jitter, which must be reduced to an acceptable level through hardware design.

ATL-COM-UPGRADE-2020-026 (REL. 21)



Algorithm flowchart for clock phase difference extraction

Hit RDO information

MC sample, with/without clock phase difference included (constant, randomize)

Compute expected TOF

c = 0.299792458m/ns (straight line assumption)
Hit path length = $\sqrt{(x-x_0)^2+(y-y_0)^2+(z-z_0)^2}$
TOF_hit = L_hit/c

Compute Pre-residual
u_i = hit_TOA - TOF_hit

Map residual withing 25ns BX window (+/-12.5ns)

$$r^{(0)}_{hit} = \mathrm{mod}\left(u_{hit} + 12.5\,\mathrm{ns}, 25\,\mathrm{ns}\right) - 12.5\,\mathrm{ns}\,.$$

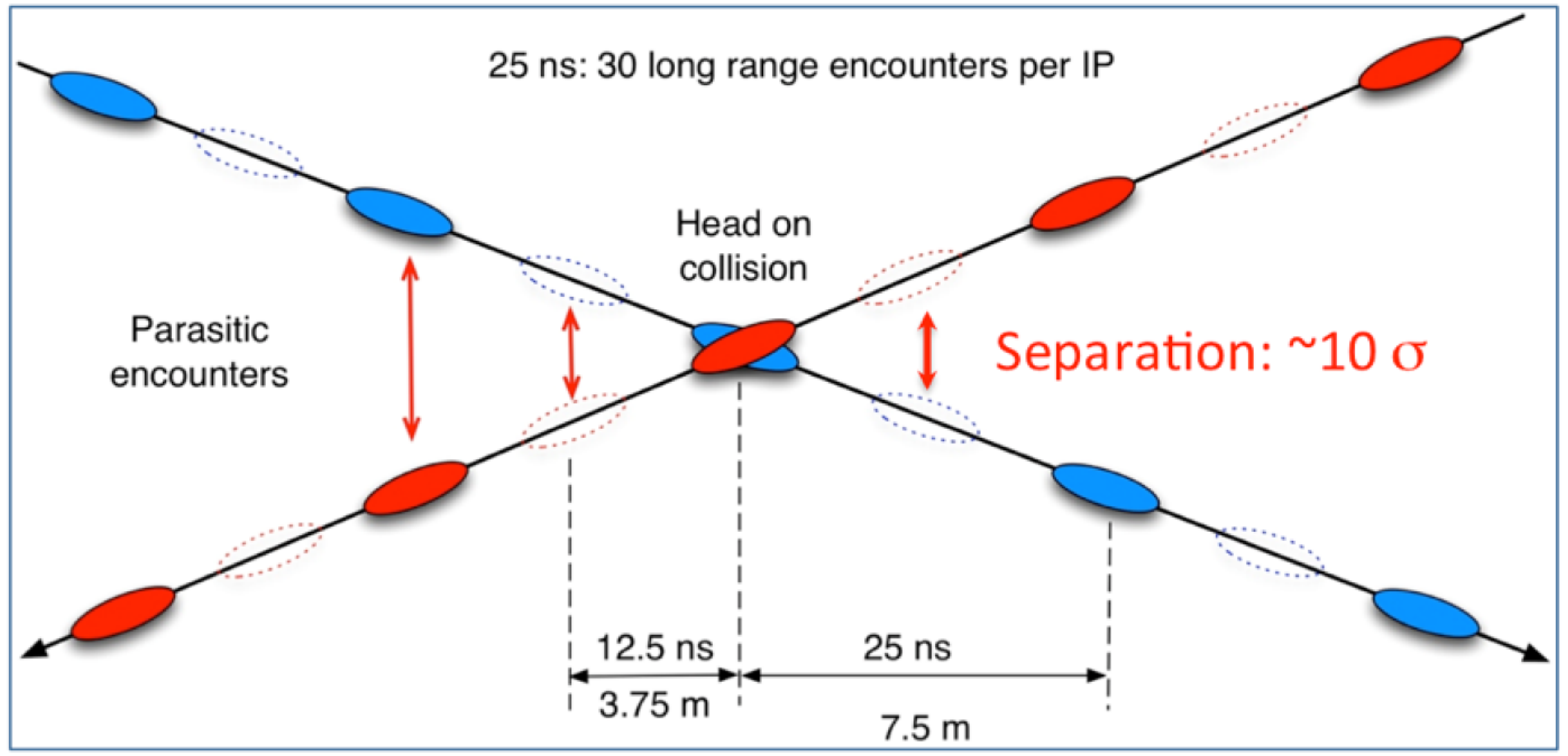
we can compute the **final residual** relative to the LHC clock's bunch crossing. It shows the precise time of the hit sensor TOA with respect to the current bunch crossing, indicating whether it was early or late

For each module: histogram the calculated final residuals (r(0)(hit)) from multiple events and get the average mean value

Histograms against module ID, or inner/outer radius, layers, etc...

Retrieving constant clock phase difference

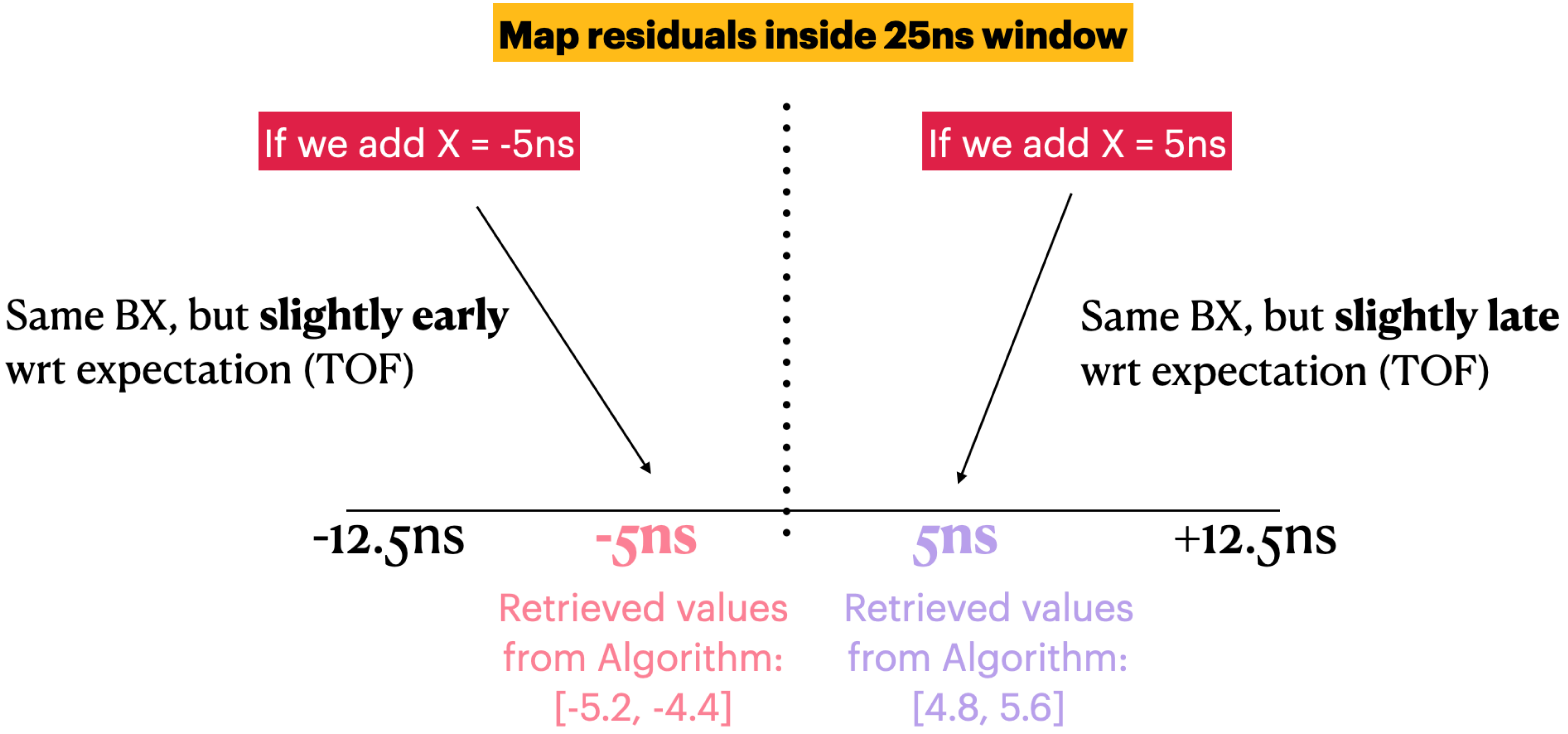
Input const. Clock phase difference X [ns]	Values retrieved [ns]
0	[-0.2, 0.6]
5	[4.8, 5.6]
-5	[-5.2, -4.4]
10	[9.8,10.6]
15	[-10.2,-9.4]
20	[-5.2,-4.4]
25	[-0.2,0.6]



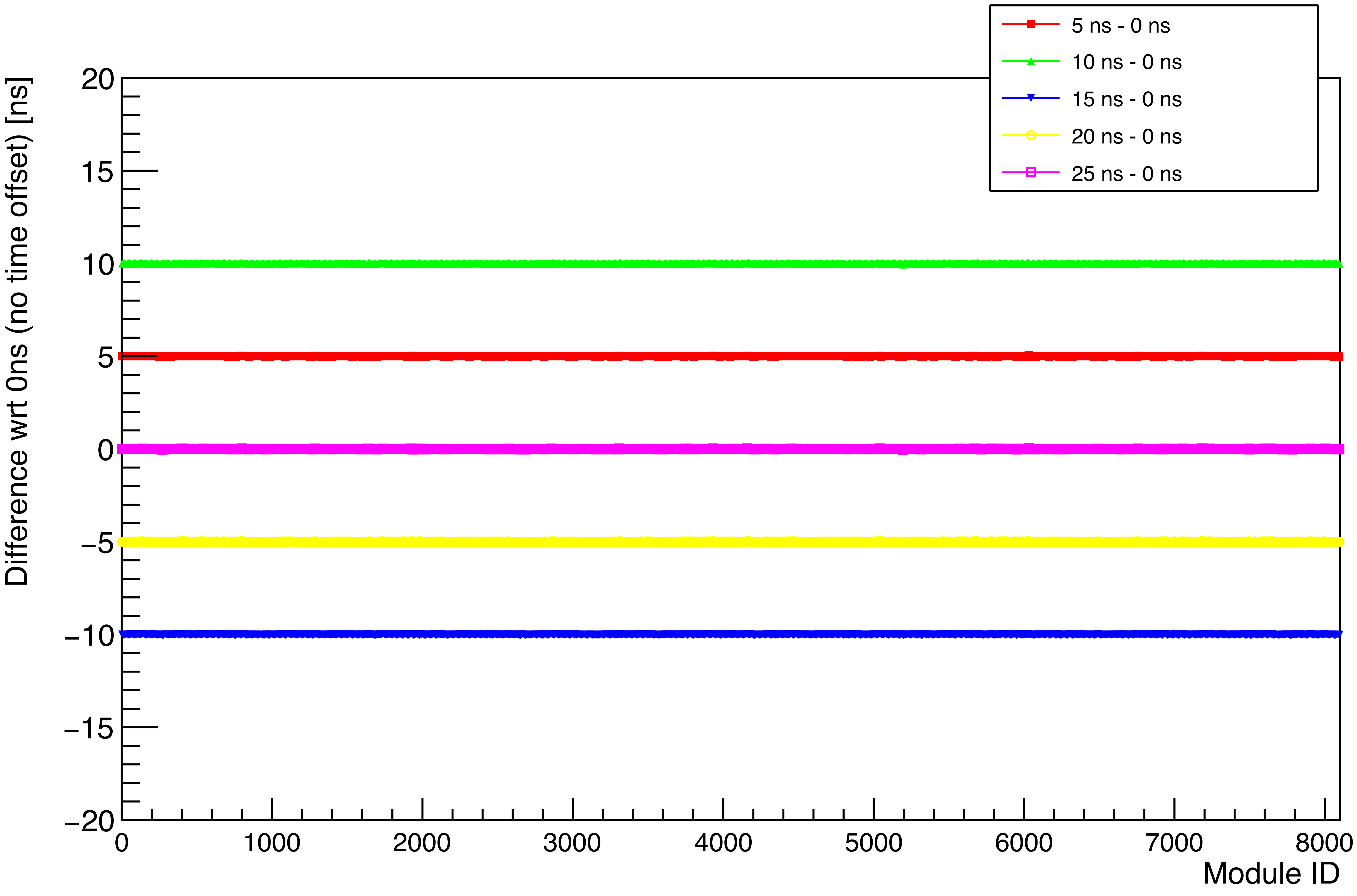
Reproduces reasonably the X [ns] (unknown) clock phase difference wrt 25 ns BX included in the sample to emulate the constant clock phase difference in real data

X>=15ns, we are reaching outside the 25ns BX window, at this point we could be reaching the previous or next BX

Representation for X = +\-5ns



Difference wrt 0ns (no clock phase difference)

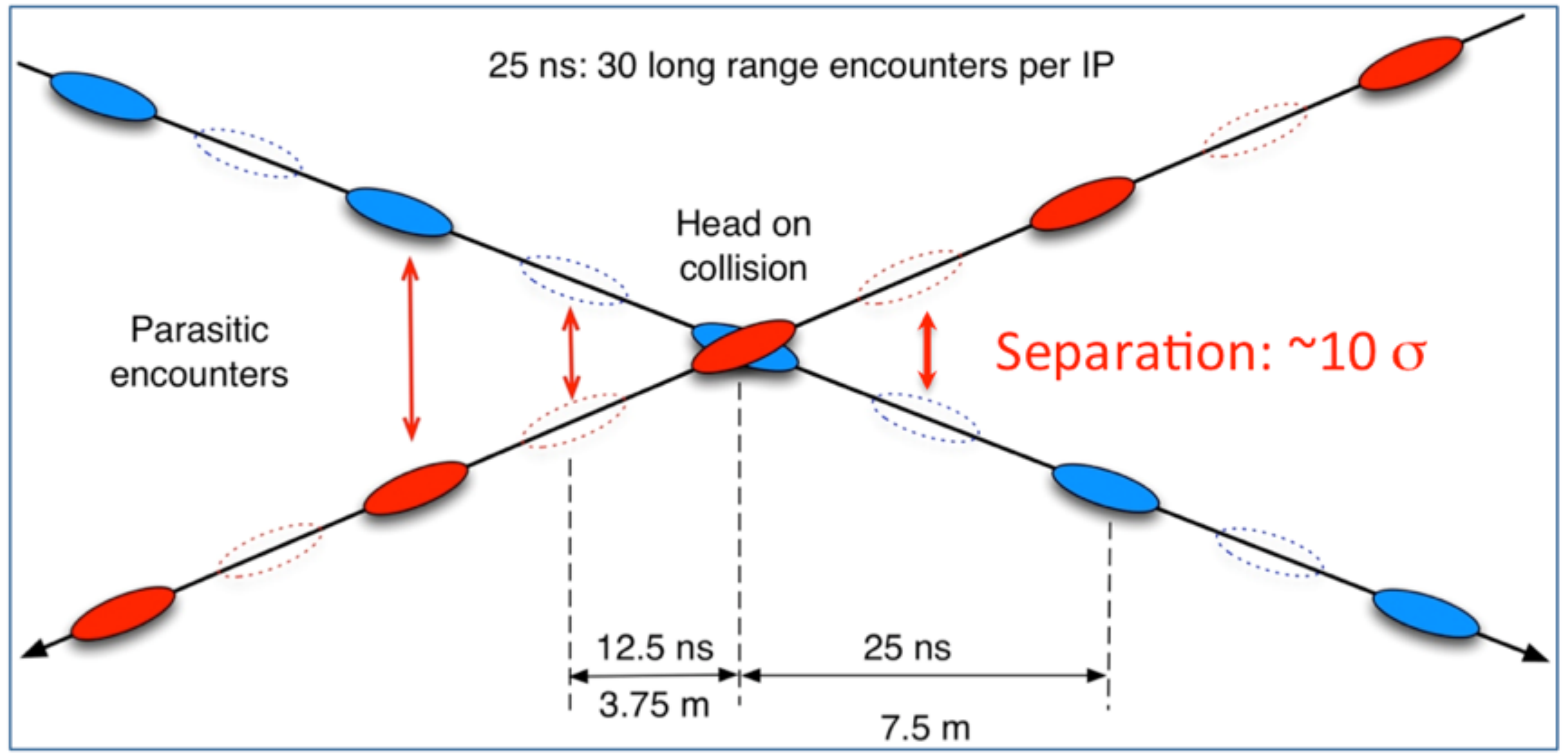


As can be seen, the algorithm is able to retrieve exact clock phase difference (constant) included in the TOA during digitalization (emulating what would be happening in real data)

Randomized clock phase difference wrt BX

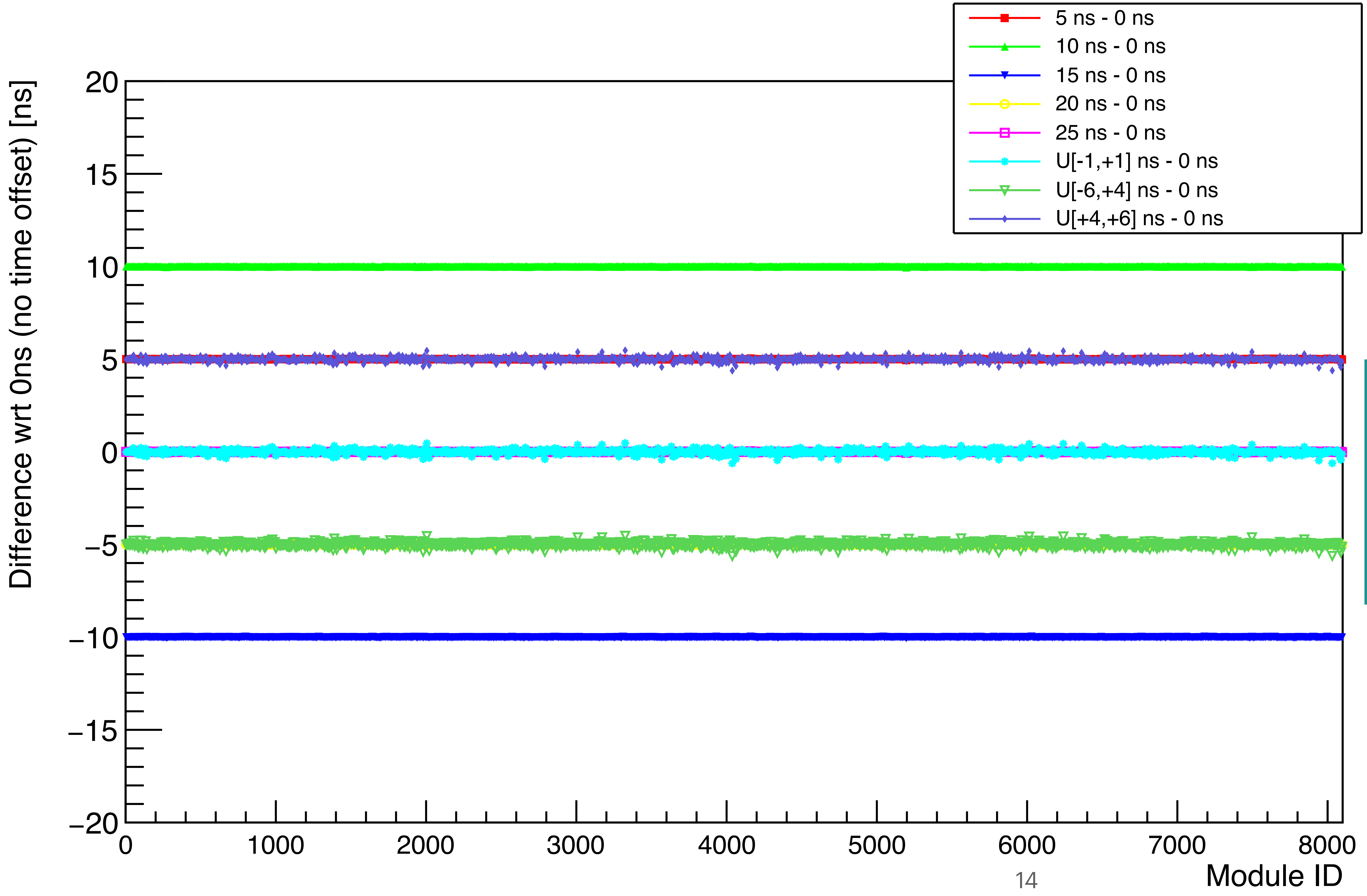
Summary

Input Randomize Shift [ns]	Values retrieved [ns]
[-1,1]	[-0.6, 0.9]
[4,6]	[4.4, 5.8]
[-6,4]	[-5.6, -4.2]



Reproduces reasonably the X [ns] (unknown) clock phase difference wrt 25 ns BX included in the sample to emulate the random clock phase difference in real data

Retrieved clock phase difference: constant and randomized



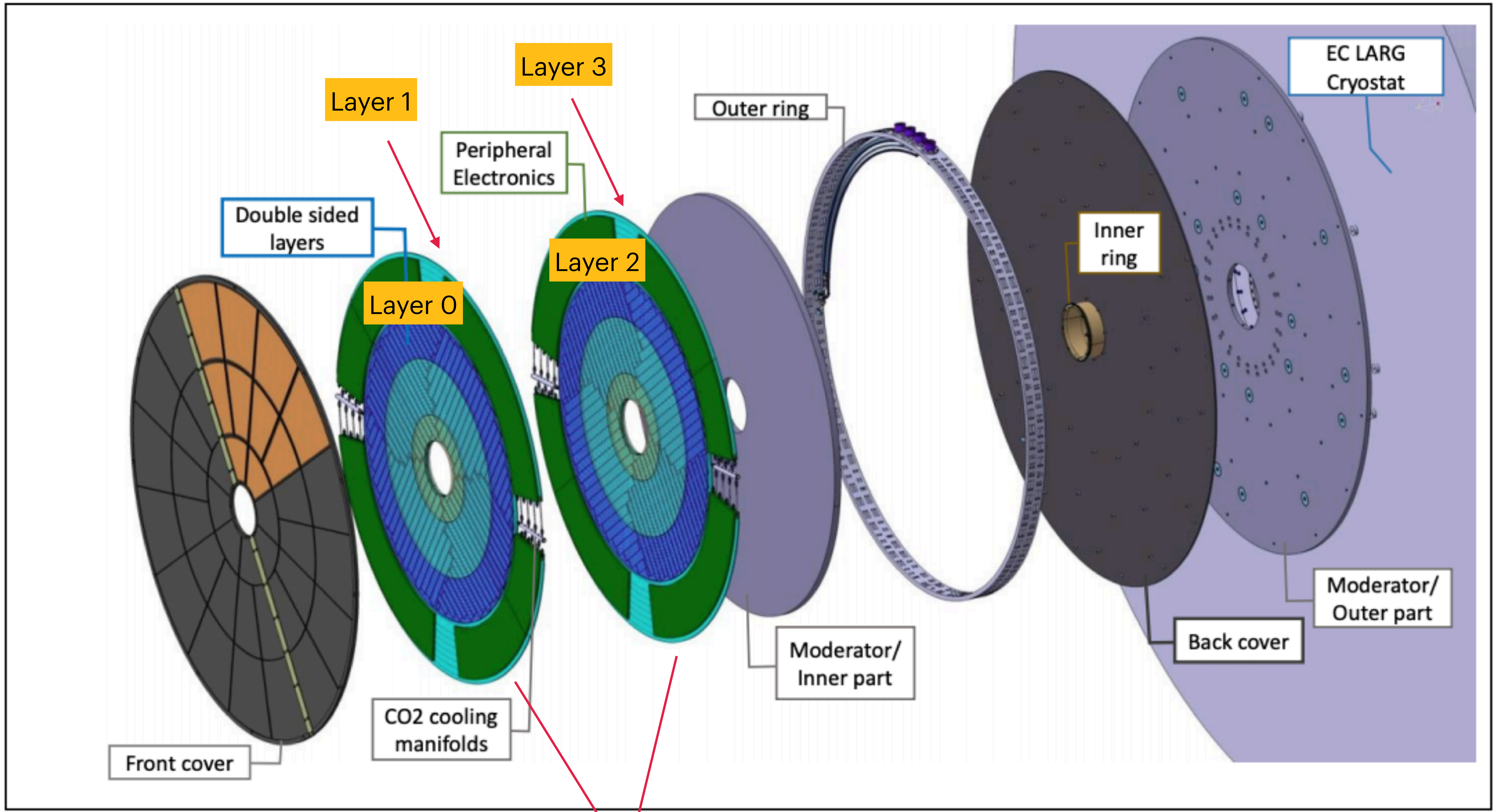
In the presence of a clock phase difference whose nature is random uniform distributed, the algorithm is also able to retrieve it (emulating what would be happening in real data)

Summary

- **At HL-LHC, increased pile-up will be a challenge for the physics program at LHC**
  - HGTD is proposed to complement ITK (spacial coordinates) and with the time-coordiante suppress the pile-up, this way improving particle-vertex assigment
  - Examples of effects which deteriorate the timing measurements and timing simulation approach were described
  - A brief overview of the timing simulation chain has been shown
  - **The proposal algorithm which enables to extract the clock phase difference using information which will be available in data collected with HGTD is presented**
    - Promising results is obtained while further tests are underway!
- **More studies are on-going to account for additional effects and improve calibration methodology, this way, further improving the previous measured timing resolution**

Back-up slides

HGTD overview I



Global view of the HGTD to be installed on each of two end-cap calorimeters (±3.5 m)

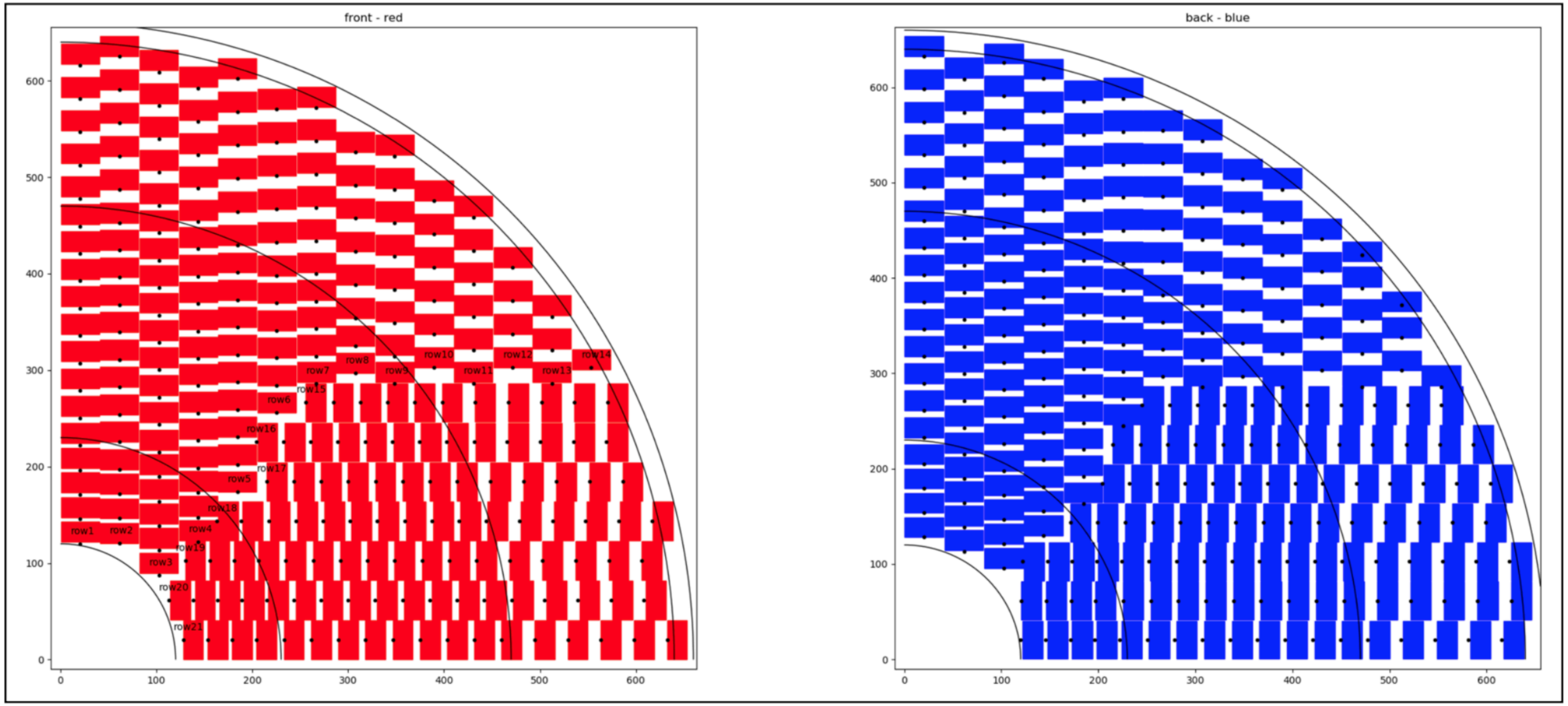
two instrumented double-sided layers (mounted in two cooling disks with sensors on the front and back of each cooling disk)

HGTD overview II

Pseudo-rapidity coverage	$2.4 < \|\eta\| < 4.0$
Thickness in z	75 mm (+50 mm moderator)
Position of active layers in z	± 3.5 m
Weight per end-cap	350 kg
Radial extension:	
Total	$110\,\text{mm} < r < 1000\,\text{mm}$
Active area	$120\,\text{mm} < r < 640\,\text{mm}$
Pad size	$1.3\,\text{mm} \times 1.3\,\text{mm}$
Active sensor thickness	50 µm
Number of channels	3.6 M
Active area	$6.4\,\text{m}^2$
Module size	30 x 15 pads ($4\,\text{cm} \times 2\,\text{cm}$)
Modules	8032
Collected charge per hit	> 4.0 fC
Average number of hits per track	
$2.4 < \|\eta\| < 2.7$ $(640\,\text{mm} > r > 470\,\text{mm})$	≈ 2.0
$2.7 < \|\eta\| < 3.5$ $(470\,\text{mm} > r > 230\,\text{mm})$	≈ 2.4
$3.5 < \|\eta\| < 4.0$ $(230\,\text{mm} > r > 120\,\text{mm})$	≈ 2.6
Average time resolution per hit (start and end of operational lifetime)	
$2.4 < \|\eta\| < 4.0$	$\approx$ 35 ps (start), $\approx$ 70 ps (end)
Average time resolution per track (start and end of operational lifetime)	$\approx$ 30 ps (start), $\approx$ 50 ps (end)

HGTD Modules positioning

- Module's position and readout rows numbers for the **front side of one disk (left)** and **back side of the same disk** (right)



Readout row: sets of modules whose flex cables (flexible PCB cables) are guided together towards larger radii to the peripheral on-detector electronics

Extend as a line of modules from lower to higher radii)

Effects on ToA: informations

Source	Modelisation	Effect (ps)	Frequency	Effect on	Reference	Included in simulation
LHC						
Bunch time shift	Dedicated root file	$\sim 5^*$	Repeating for every BC id	Event	[3, 4]	√
LHC clock transmission	Uniform	33	Constant	Event	[5]	
	Gausian	2	< 5 MHz			
Static						
TC Link	Uniform	10	Constant	Row	[6, 7]	√ (TBU)
ASIC	Gaussian	$5/\sqrt{2}$		Module		√
Jitters						
lpGBT	Gaussian	2.2	40 MHz	Row	[8]	√
Flex	Gaussian	5			[9]	√ (TBU)
ASIC	Gaussian	$5/\sqrt{2}$		Module	[10]	√
Sensor	Gaussian	25				√