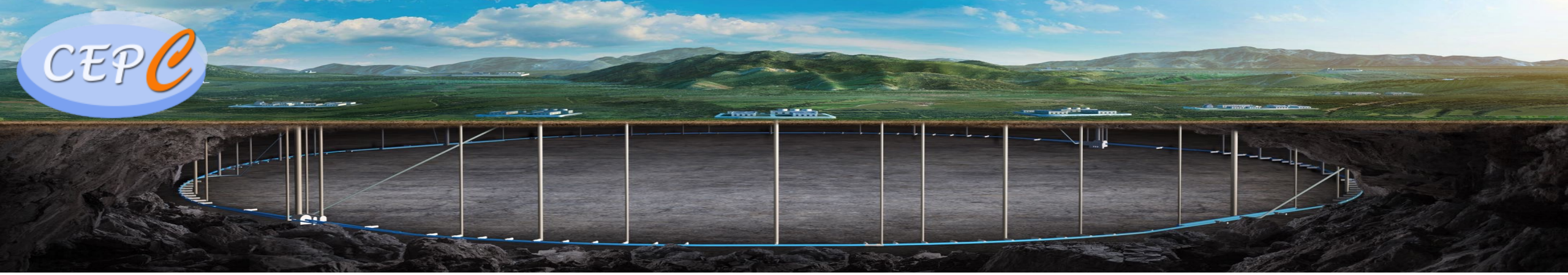

# CEPC vertex Detector

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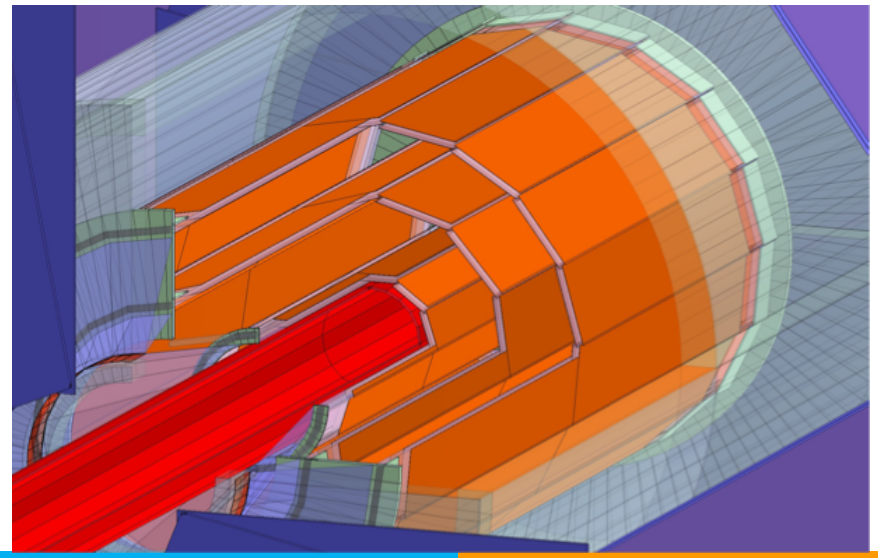
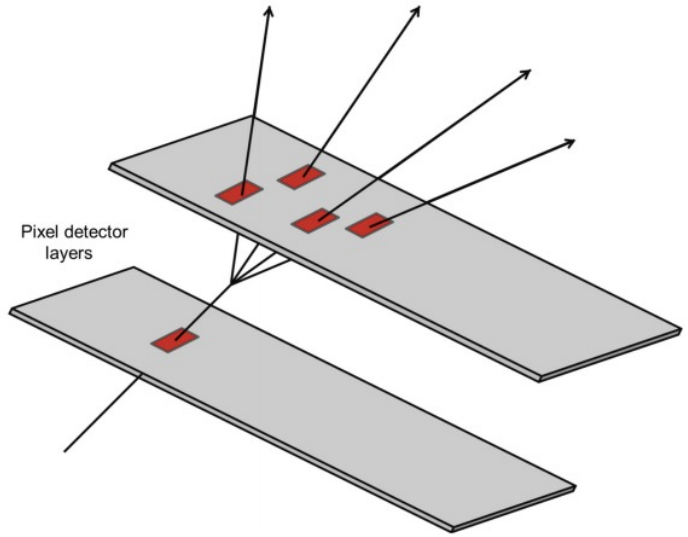
# Introduction: vertex detector

- Vertex detector optimized for first 10 year of CEPC operation (ZH, low lumi-Z runs)
  - Low lumi Z runs is ~20% instant luminosity of high lumi Z runs
- Motivation:
  - Aim for impact parameter resolution and vertexing capability
  - For H → bb/ H → cc/ H → light quark or gluons analysis
  - The observation H → cc or H → gg is important goal for CEPC





# Vertex Requirement

– Inner most layer (b-layer) need to be as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)

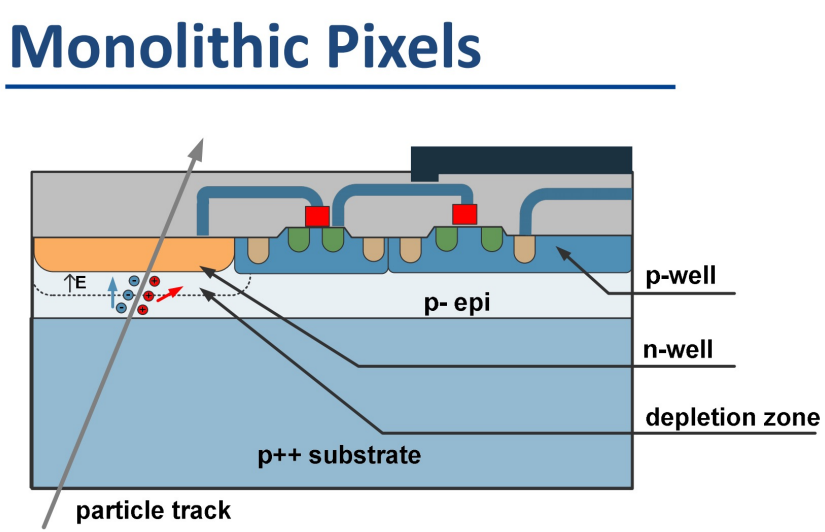
**Table 4.2:** Vertex Detector Design Parameters

| Parameter | Design |
|---|---|
| Spatial Resolution | $\sim 5$ μm |
| Detector material budget | $\sim 0.8\% X_0$ |
| First layer radius | 11.1 mm |
| Power Consumption | $< 40$ mW/cm$^2$ (air cooling requirement) |
| Time stamp precision | 100 ns |
| Fluence | $\sim 2 \times 10^{14}$ Neq/cm$^2$ (for first 10 years) |
| Operation Temperature | $\sim 5$ °C to 30 °C |
| Readout Electronics | Fast, low-noise, low-power |
| Mechanical Support | Ultralight structures |
| Angular Coverage | $\lvert\cos\theta\rvert < 0.99$ |

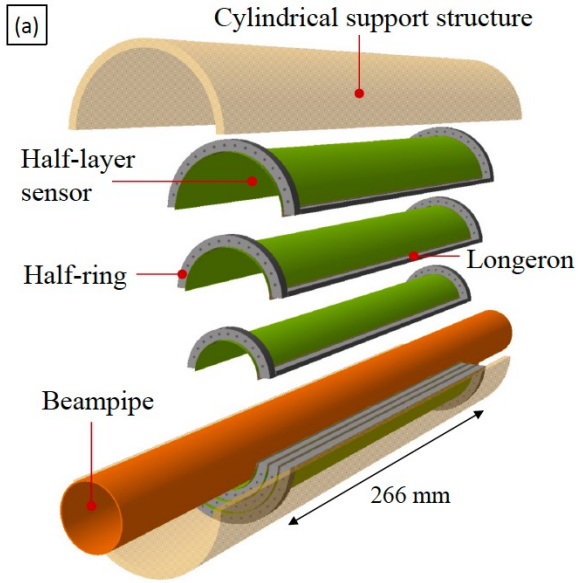
# Technology survey and our choices

- Curved MAPS chosen as baseline for Reference detector TDR. arXiv:2510.05260
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1] )
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder options)
  - Alternative: Ladder design based on CMOS MAPS

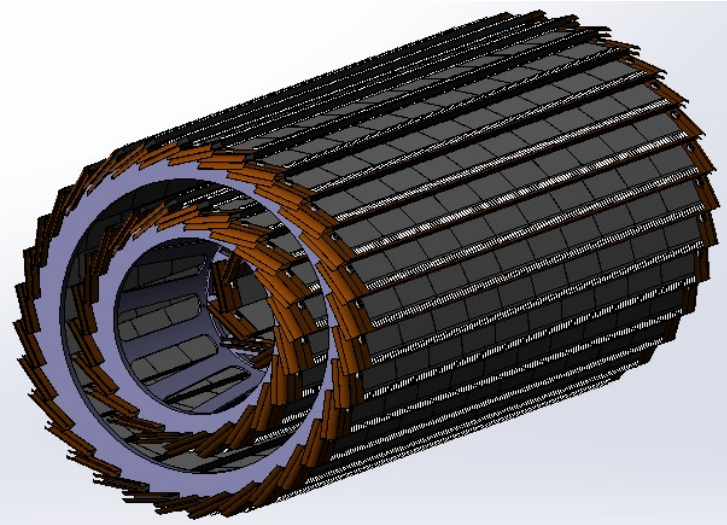
Monolithic active Pixel CMOS (MAPS)




Baseline: curved MAPS




Alternative: ladder based MAPS



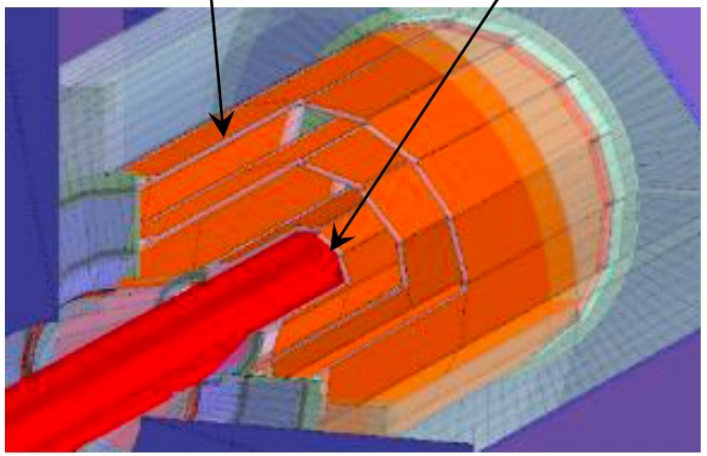
[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

# R&D status and final goal

| Key technology | Status | CEPC Final goal |
|---|---|---|
| CMOS chip technology | Full-size chip with TJ 180nm CIS | 65nm CIS |
| Detector integration | Detector prototype with ladder design | Detector with bent silicon design |
| Spatial resolution | 4.9 μm | 3-5 μm |
| Detector cooling | Air cooling with 1% channels (24 chips) on | Air cooling with full power |
| Bent CMOS silicon | Bent Dummy wafer radius ~12mm | Bent final wafer with radius ~11mm |
| Stitching | 11*11cm stitched chip with Xfab 350nm CIS | 65nm CIS stitched sensor |

# Silicon Pixel Chips for Vertex Detector

2 layers / ladder  $R_{in}$~16 mm



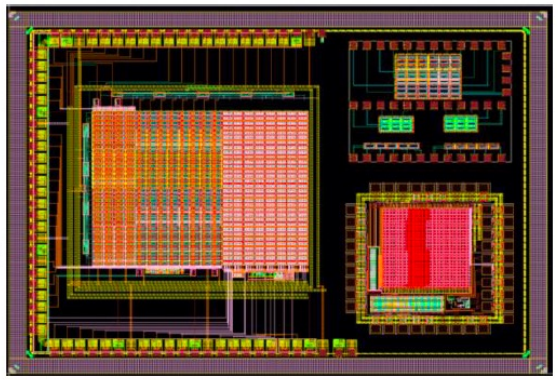
**Goal: σ(IP) ~ 5 μm for high P track**

**CDR design specifications**

- **Single point resolution ~ 3μm**
- **Low material (0.15% $X_0$ / layer)**
- **Low power (< 50 mW/cm²)**
- **Radiation hard (1 Mrad/year)**

**Silicon pixel sensor develops in 5 series: JadePix, TaichuPix, CPV, Arcadia, COFFEE**

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process

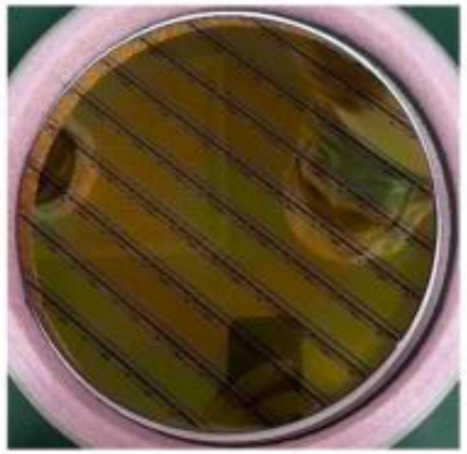


**JadePix**-3 Pixel size ~16×23 μm²

**Tower-Jazz 180nm CiS process**
**Resolution 5 microns, 53mW/cm²**

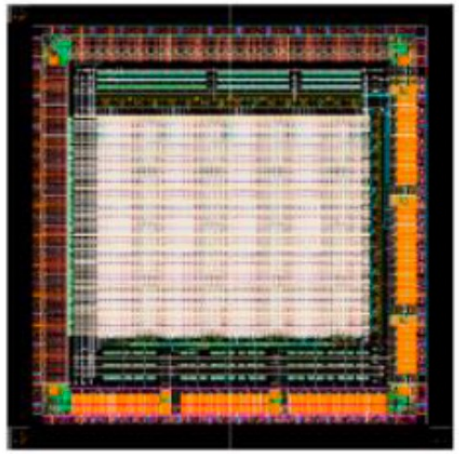
**MOST 1**

**TaichuPix**-3, FS 2.5x1.5 cm²
25×25 μm² pixel size

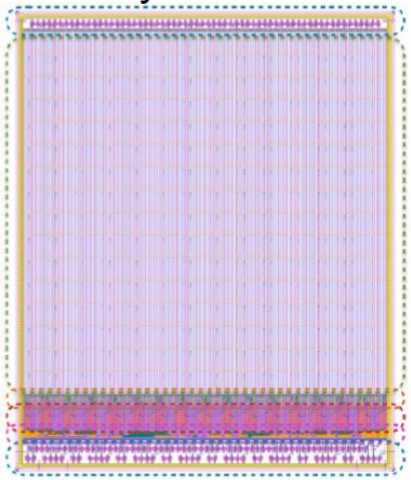


**MOST 2**

**CPV4** (SOI-3D), 64×64 array
~21×17 μm² pixel size

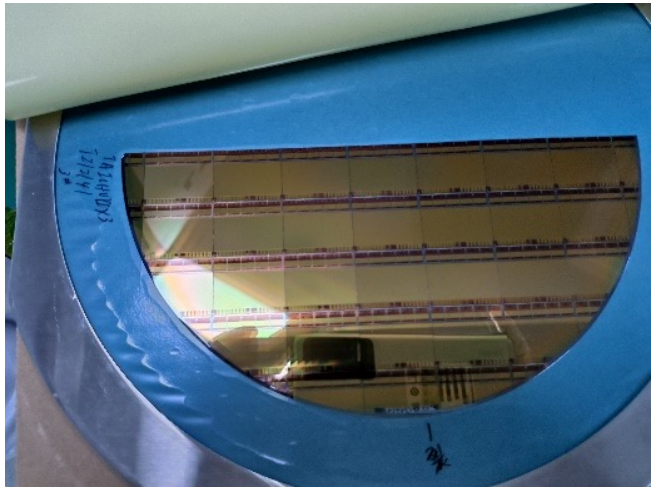


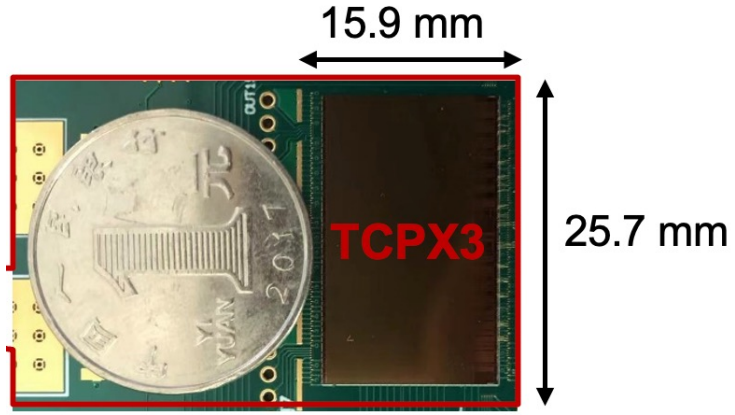
**Arcadia** by Italian groups for IDEA vertex detector
LFoundry 110 nm CMOS



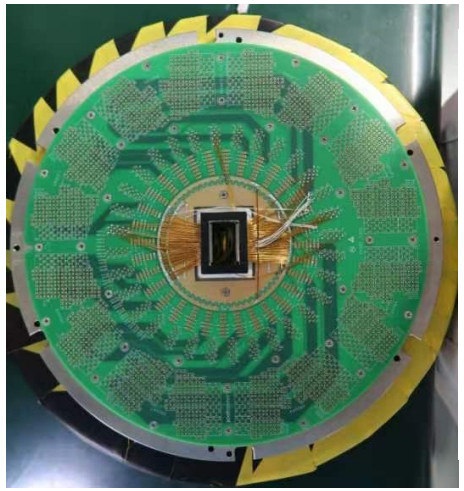
# R&D efforts: Full-size TaichuPix3

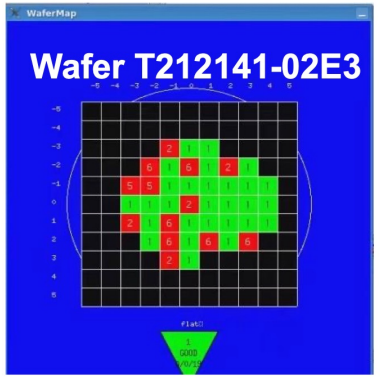
- Full size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array,  Chip Size：15.9×25.7mm
  - 25μm×25μm pixel size with  high spatial resolution
  - Process: Towerjazz 180nm CIS process
  - Fast digital readout to cope with ZH and Z runs (support 40MHz clock)





TaichuPix-3 chip vs. coin

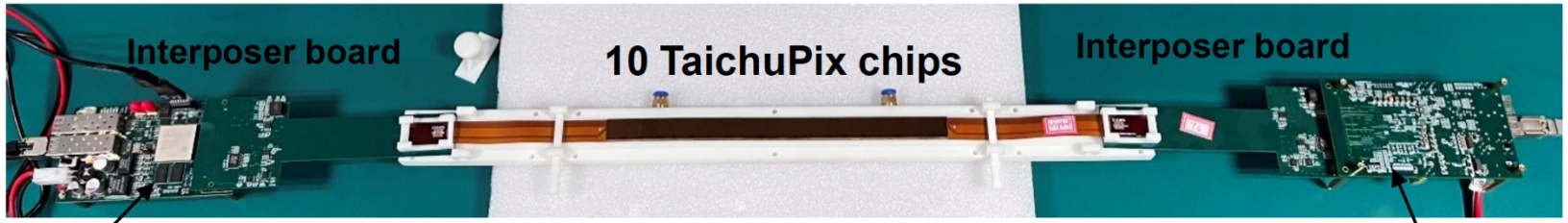




An example of wafer test result

| | Status | CEPC Final goal |
|---|---|---|
| CMOS chip technology | Full-size chip with TJ 180nm CIS | 65nm CIS |

# R&D effort: vertex detector prototype

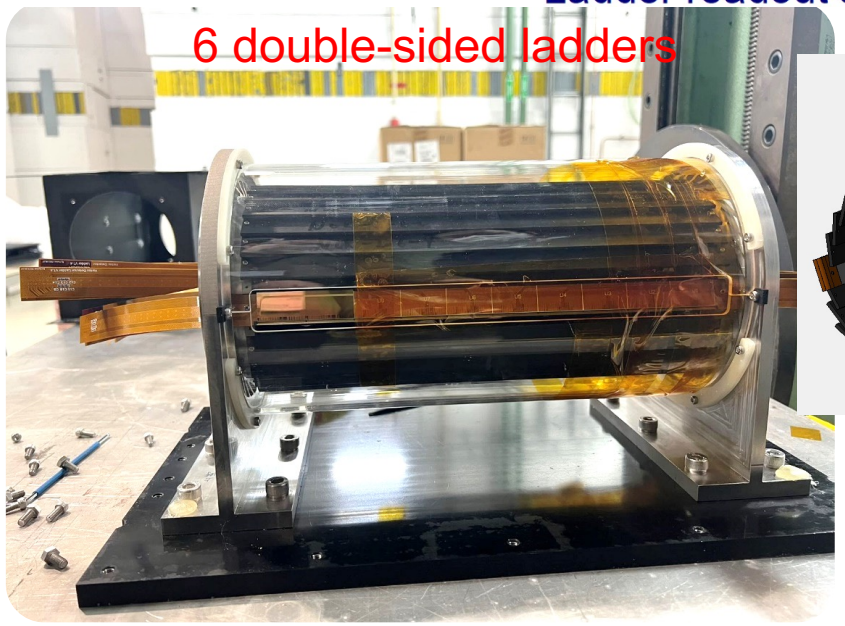


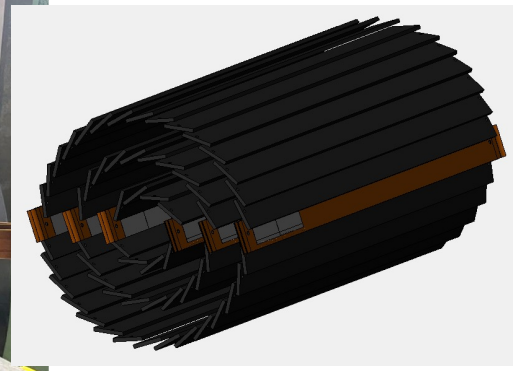

**TaichuPix**-based prototype detector tested at DESY in April 2023

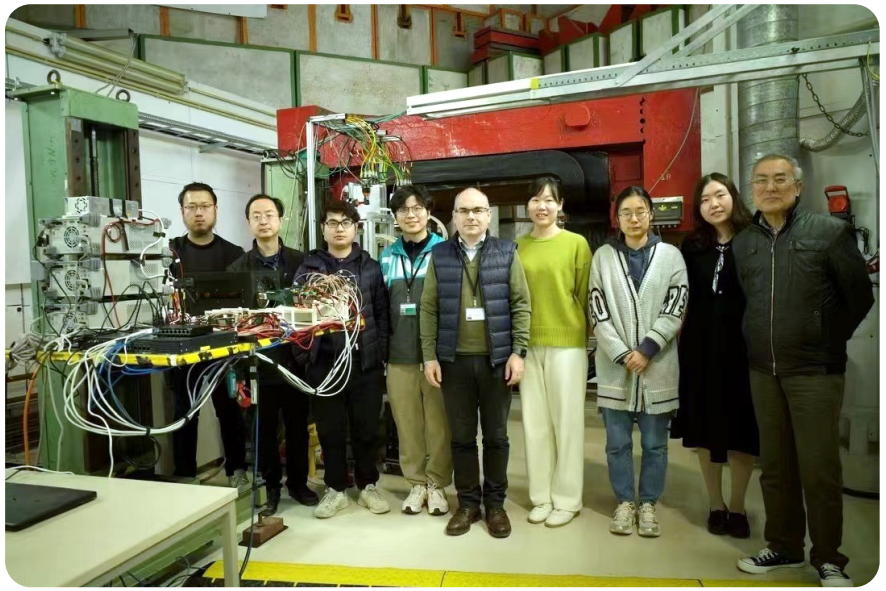
Spatial resolution ~ **4.9 μm**

Ladder readout system

6 double-sided ladders

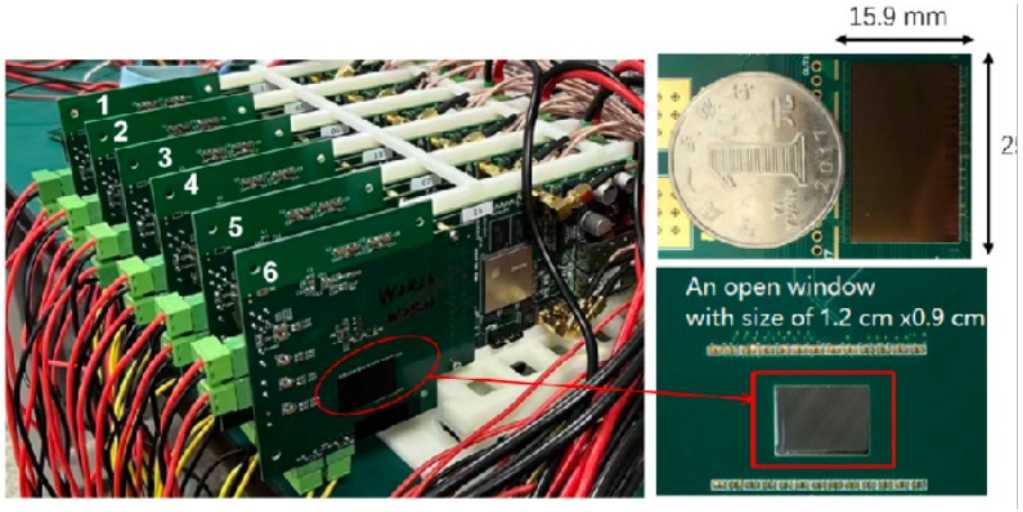


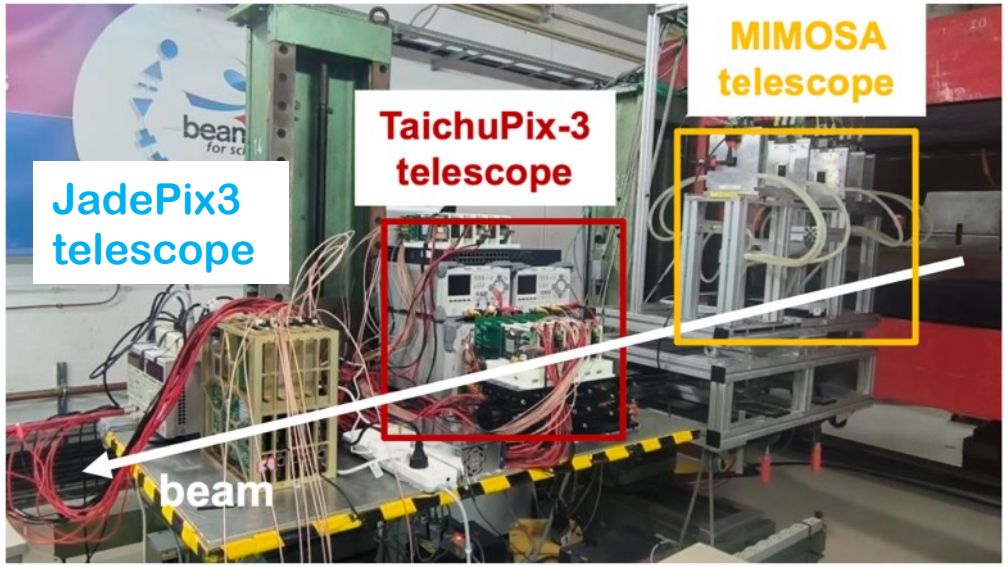




| | Status | CEPC Final goal |
|---|---|---|
| Detector integration | Detector prototype with ladder design | Detector with bent silicon design |

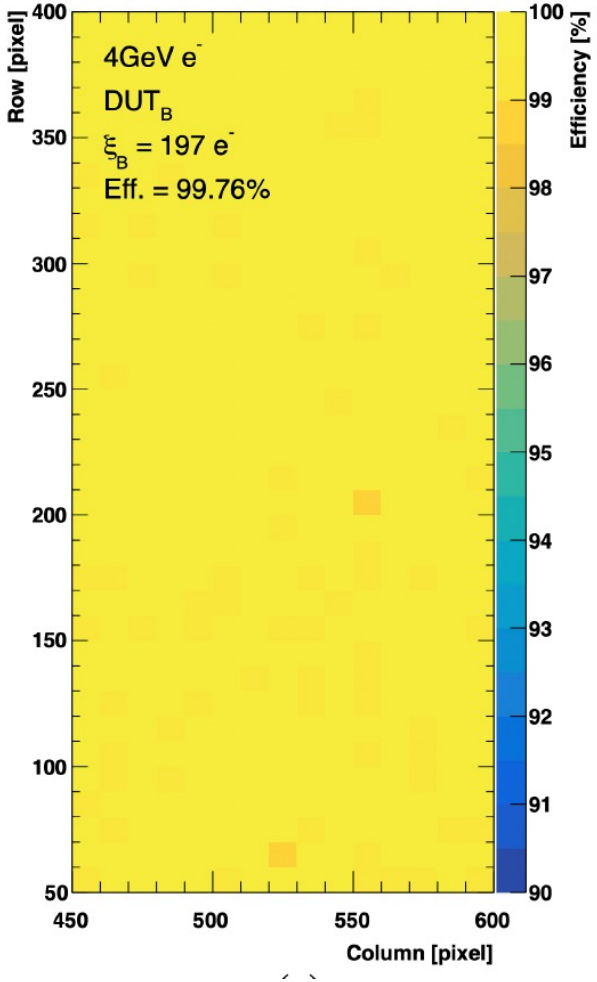
# R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY



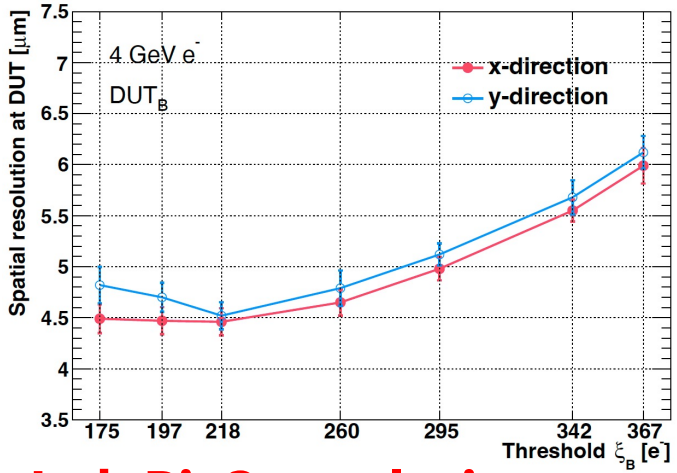




Spatial resolution 4~5um, Efficiency >99%

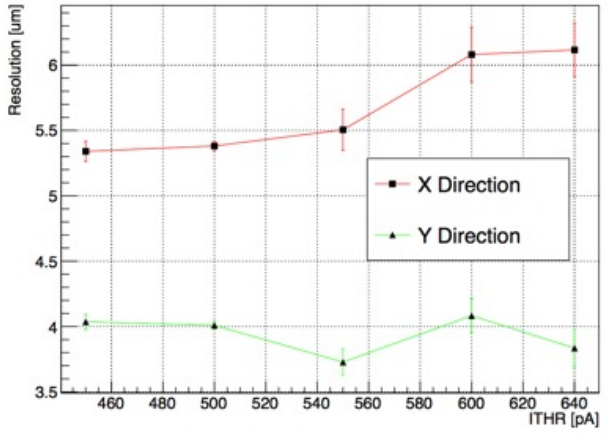
## TaichuPix3 efficiency




## TaichuPix3 resolution



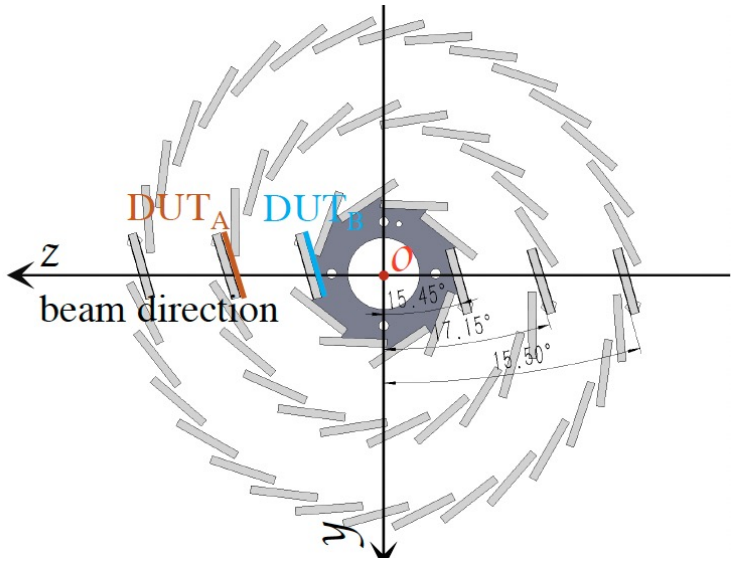

## JadePix3 resolution

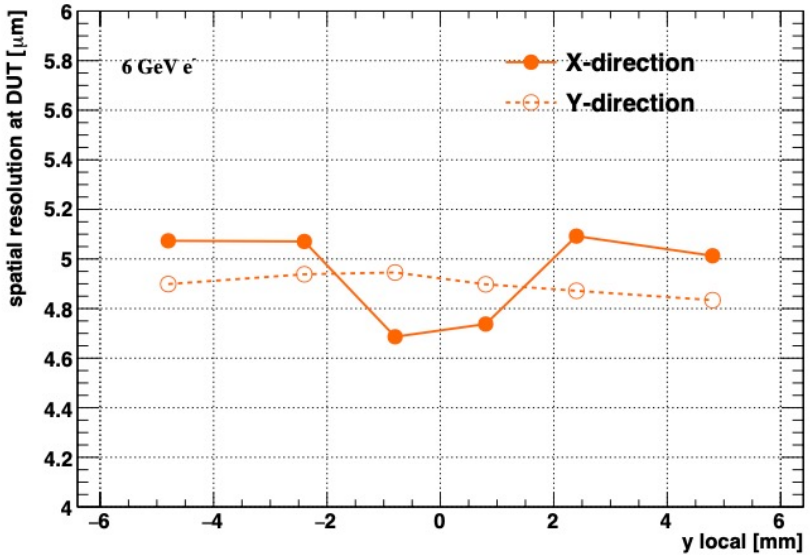



Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

# R&D efforts and results: vertex detector prototype beam test

Spatial resolution ~ **5 μm**

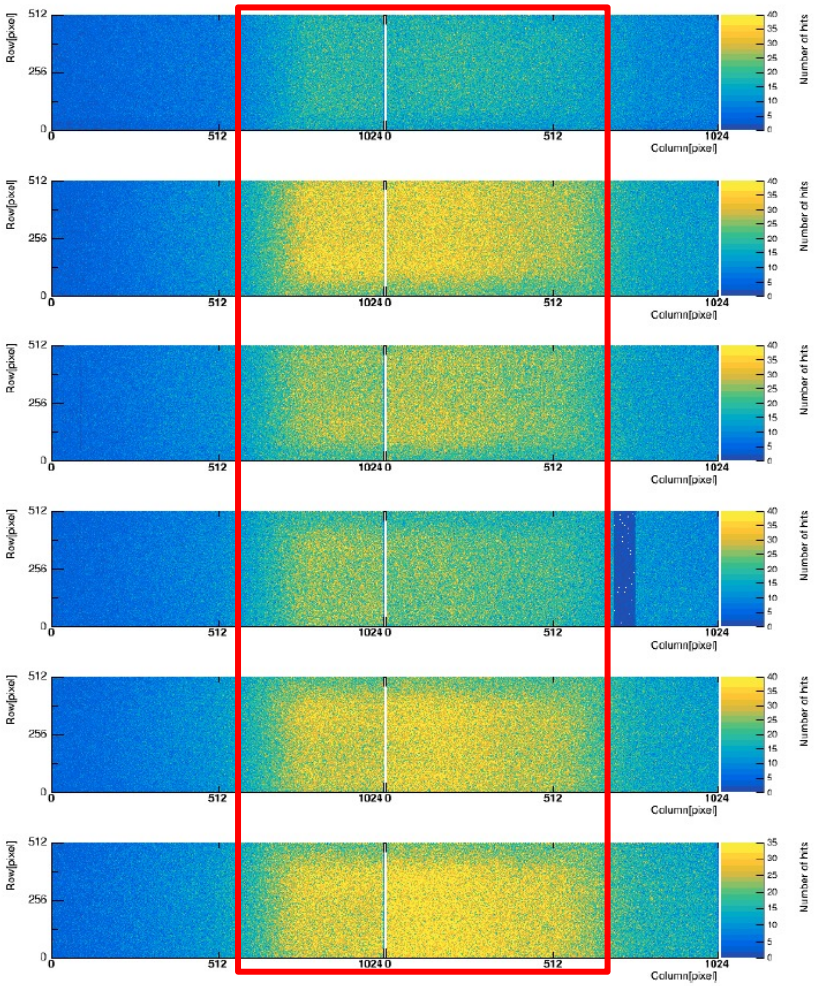



| | Status | CEPC Final goal |
|---|---|---|
| Spatial resolution | 4.9 μm | 3-5 μm |

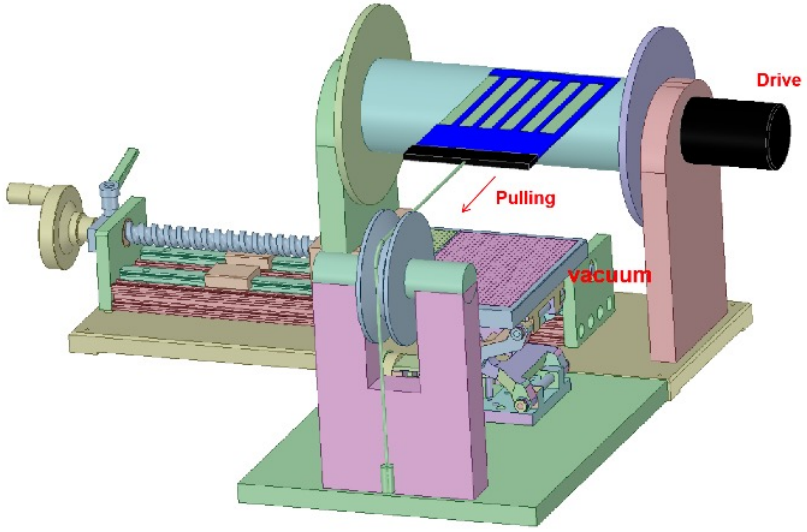
Hit maps of multiple layers of vertex detector

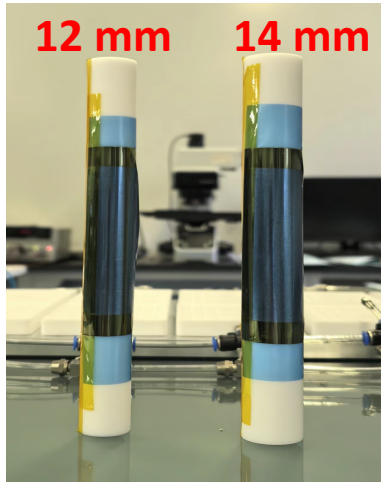
Beam spot



# R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm
  - The dummy wafer has been thinned to 40μm



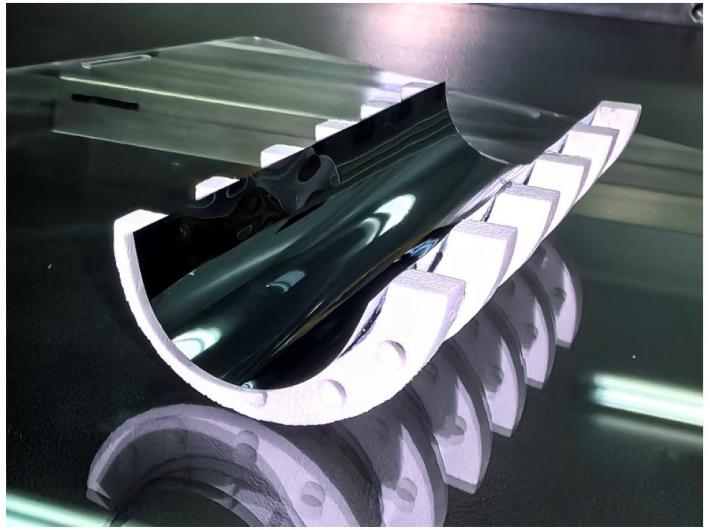
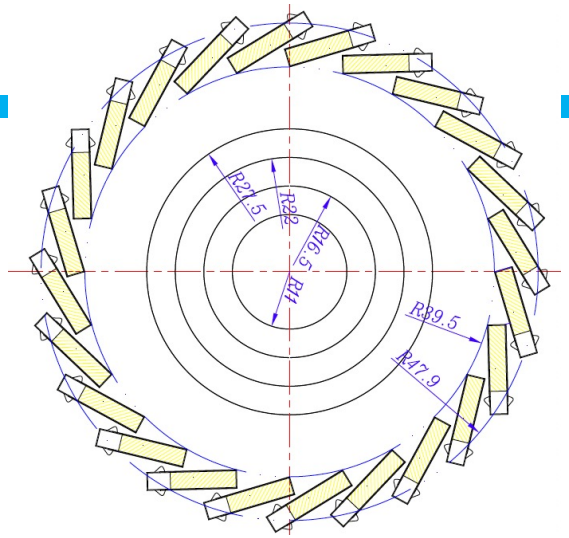



Figure 4.26: 12 mm bending radius.

| | Status | CEPC Final goal |
|---|---|---|
| Bent silicon with radius | Bent Dummy wafer radius ~12mm | Bent final wafer with radius ~11mm |

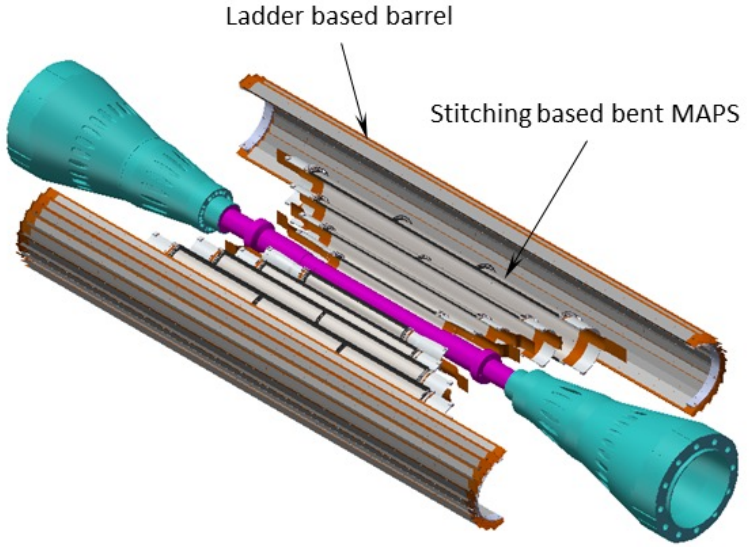
# Baseline in Ref-TDR: bent MAPS

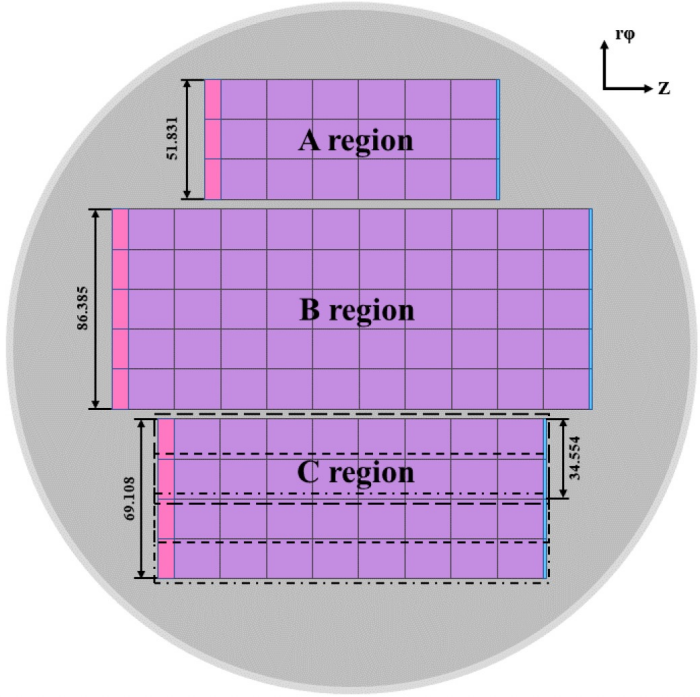
- 4 single layer of bent MAPS + 1 double layer ladder
  - Material budget is much lower than alternative option
- Use single bent MAPS for Inner layer (~0.15m$^2$)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area




Long barrel layout (no endcap disk)
to cover cos $\underline{\theta}$<=0.991

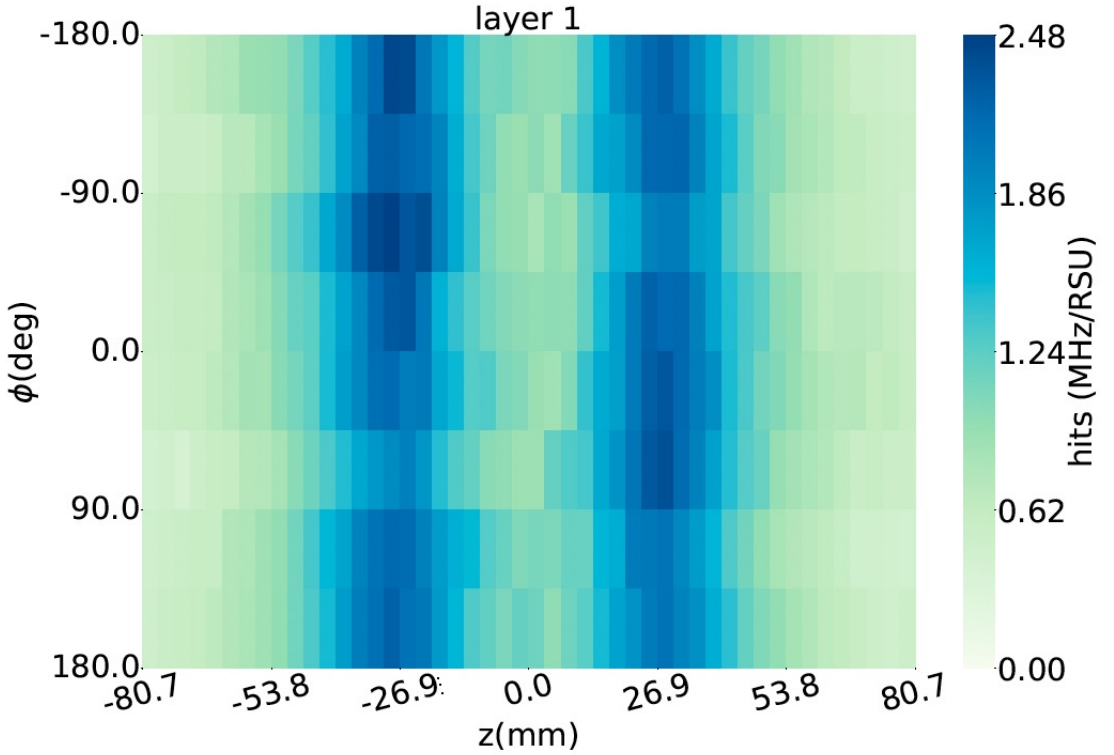
| layer/VXD X | radius .mm | length .mm |
|---|---|---|
| layer 1 | 11.06 | 161.4 |
| layer 2 | 16.56 | 242.2 |
| layer 3 | 22.06 | 323.0 |
| layer 4 | 27.56 | 403.8 |
| VXD 5 | 39.50 | 682.0 |



# Data rate estimation of vertex detector

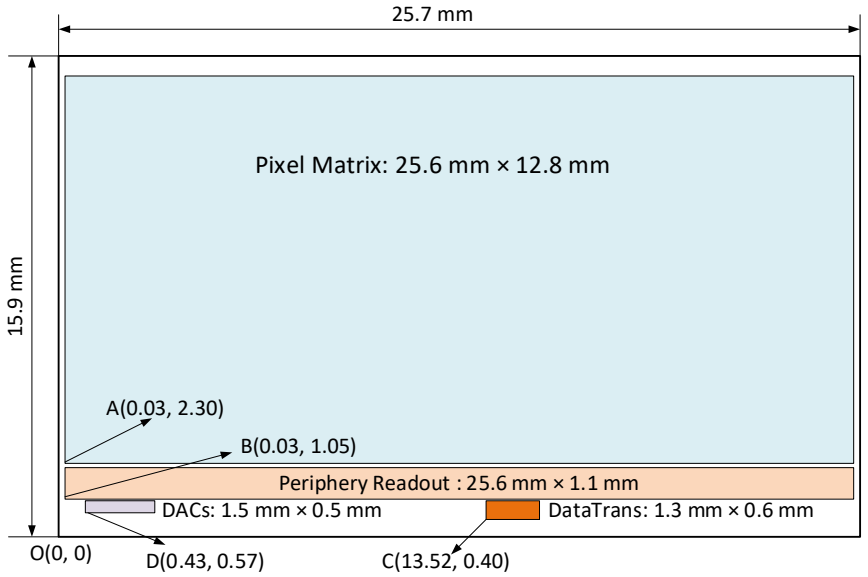
| Layer | Ave. Hit Rate ($MHz/cm^2$) | Max. Hit Rate ($MHz/cm^2$) | Ave. Data Rate ($Mbps/cm^2$) | Max. Data Rate ($Mbps/cm^2$) |
|---|---|---|---|---|
| Higgs mode: Bunch Spacing: 277 ns, 63% Gap | | | | |
| 1 | 1.2 | 1.4 | 130 | 170 |
| 2 | 0.34 | 0.54 | 35 | 56 |
| 3 | 0.086 | 0.17 | 9.8 | 19 |
| 4 | 0.039 | 0.087 | 5.1 | 16 |
| 5 | 0.013 | 0.077 | 1.7 | 12 |
| 6 | 0.009 | 0.043 | 1.2 | 6.6 |
| Low-luminosity $Z$ mode: Bunch Spacing: 69 ns, 17% Gap | | | | |
| 1 | 4.7 | 9.3 | 680 | 1400 |
| 2 | 0.45 | 0.75 | 60 | 120 |
| 3 | 0.16 | 0.38 | 23 | 96 |
| 4 | 0.096 | 0.23 | 15 | 78 |
| 5 | 0.022 | 0.048 | 3.2 | 7.2 |
| 6 | 0.017 | 0.036 | 2.4 | 6.1 |




- Data rate is dominated by background from pair productio...
  - Estimated based on old version of software
  - More details in Haoyu's MDI talk this afternoon
- WW runs and low Lumi Z runs (20% of high lumi Z)
- Data rate @1Gbps per chip for triggerless readout

# Chip design for ref- TDR and power consumption

- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm$^2$
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation




| | Matrix | Periphery | DataTrans. | DACs | Total Power | Power density |
|---|---|---|---|---|---|---|
| TaiChu3 180nm chip @ triggerless | 304 mW | 135 mW | 206 mW | 10 mW | 655 mW | 160 mW/cm$^2$ |
| 65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z ) | 60 mW | 80 mW | 36 mW | 10 mW | 186 mW | ~45 mW/cm$^2$ |

# Detailed design： Electronics

– Stitching layer : stitching and RDL metal layer on wafer to replace PCB

– Outer layer (L5/L6) : flexible PCB （ also used in alternative layout)

- Signal, clock, control, power, ground will be handled by control board through flexible PCB

Stitching layers : ALICE ITS3 like stitching

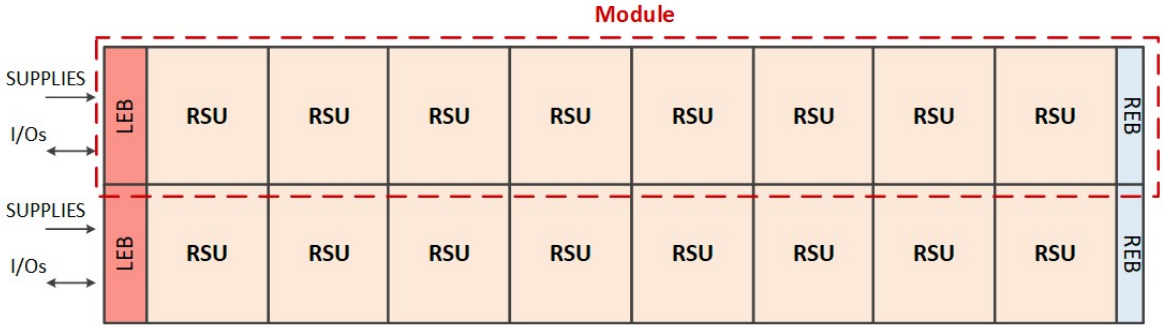



Figure 4.15

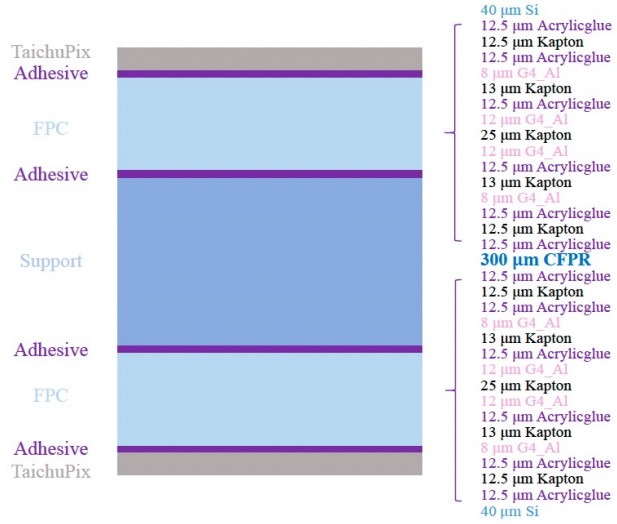
Table 4.12, Estimates of average power dissipation per unit area

| | Power density [mW/cm$^2$] |
|---|---|
| Repeated Sensor Unit | 38 |
| Left-End Block | 485 |

[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

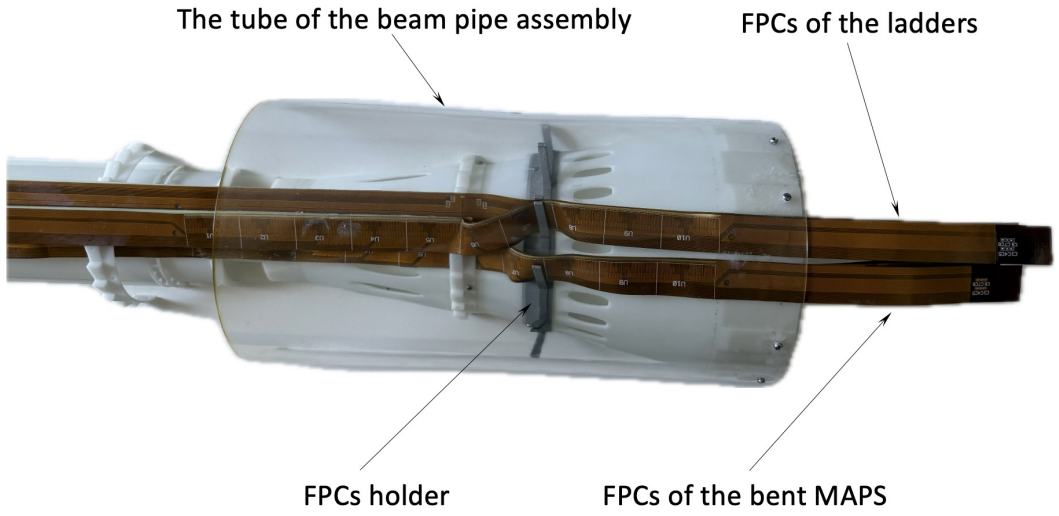
Outer layer (layer 5/6, )： flexible PCB


Ladder readout system



# Mockup to validate cable routing

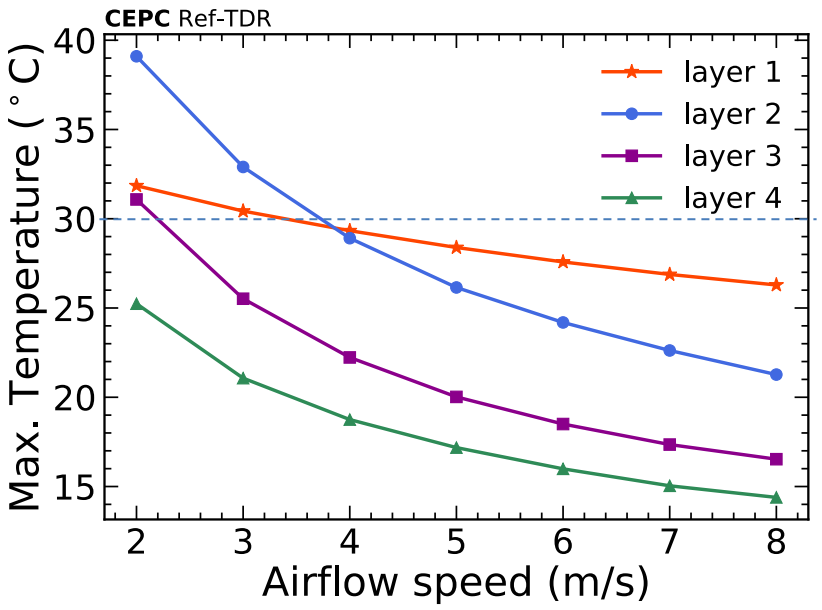
- Full-size 3D printed vertex detector and beam-pipe mockup
  - Validate there is enough space for cable routing and air cooling channel
  - The total cross-sectional area available for air cooling in the inner four layers is 12.6 $cm^2$



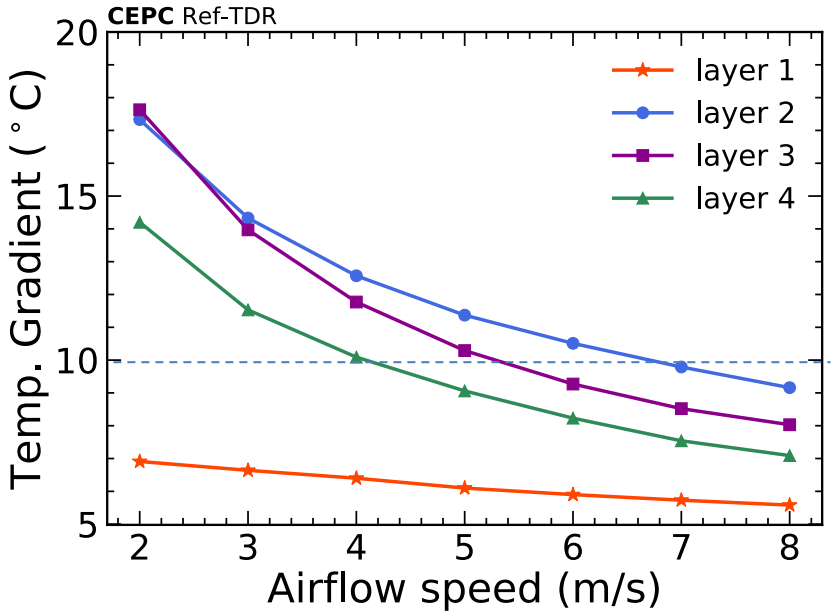

# Thermal simulation

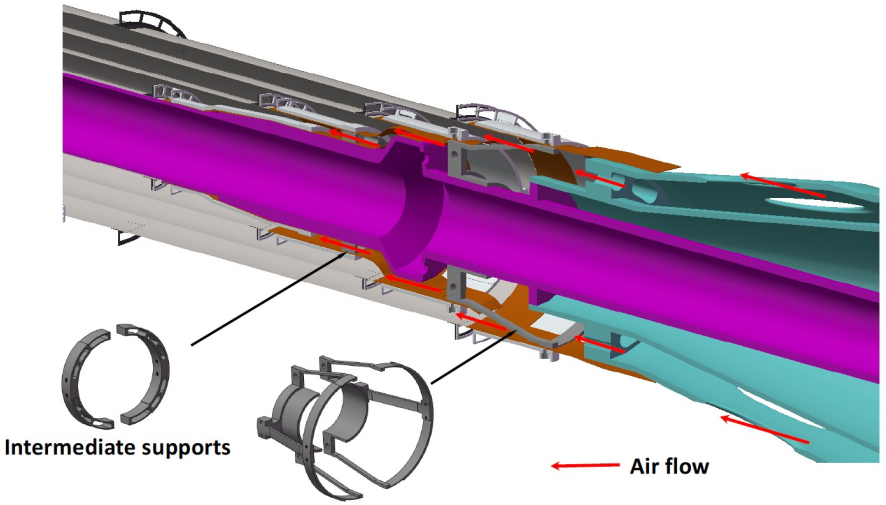
- New thermal simulation, baseline air speed increased from 3.5m/s to 7m/s
  - All Obstacles and Thermal gradients considered (just included support structure and flexible cable)
  - The simulation results indicate that the airflow is turbulent

Maximum temperature in stitching layers




Temp. Gradient in stitching layers



# Alignment in stitching layer

- Deformation mode simulated by FEA.

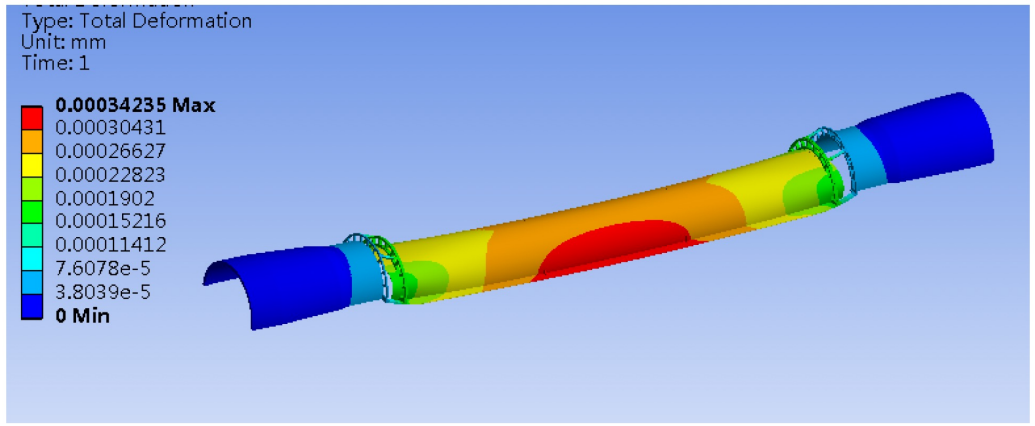
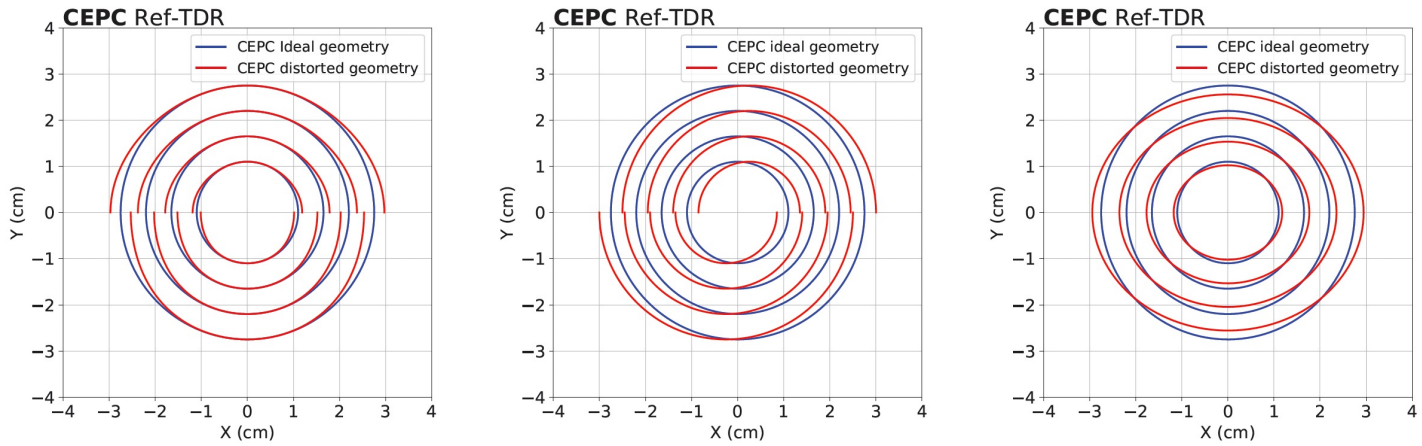
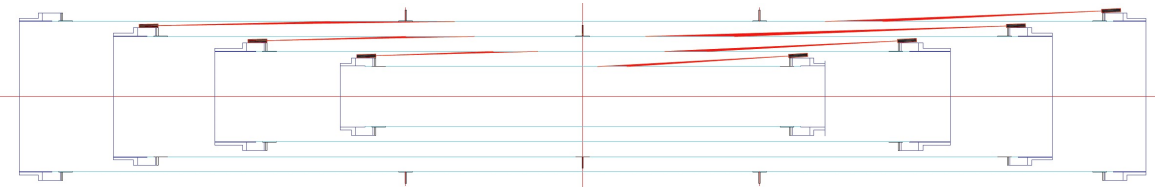


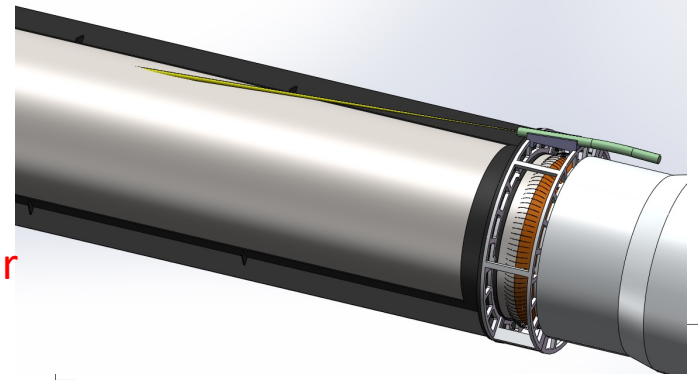

Figure 4.71: The simulated defromation of the inner layer bent MAPS half cylinder.



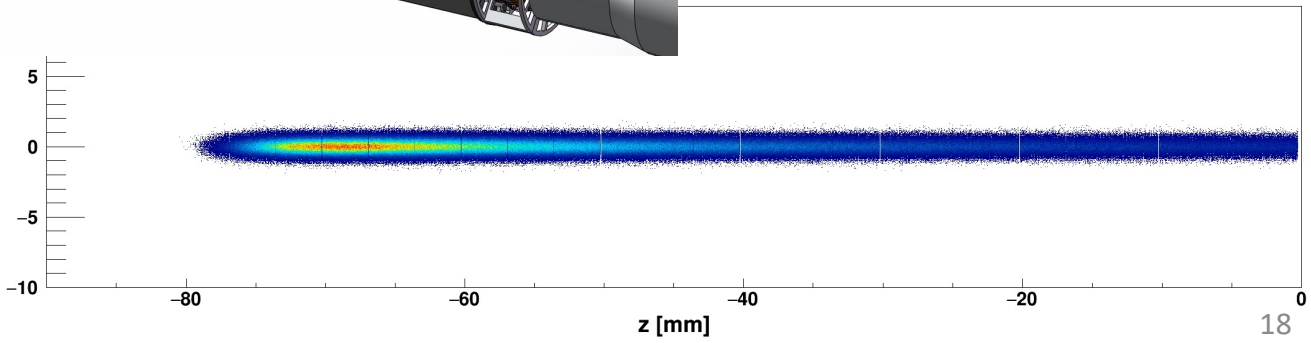

- Real time Deformation monitoring by infra-red laser alignment system

2D and 3D model on laser alignment system on vertex detector (inspired by CMS tracker laser alignment)





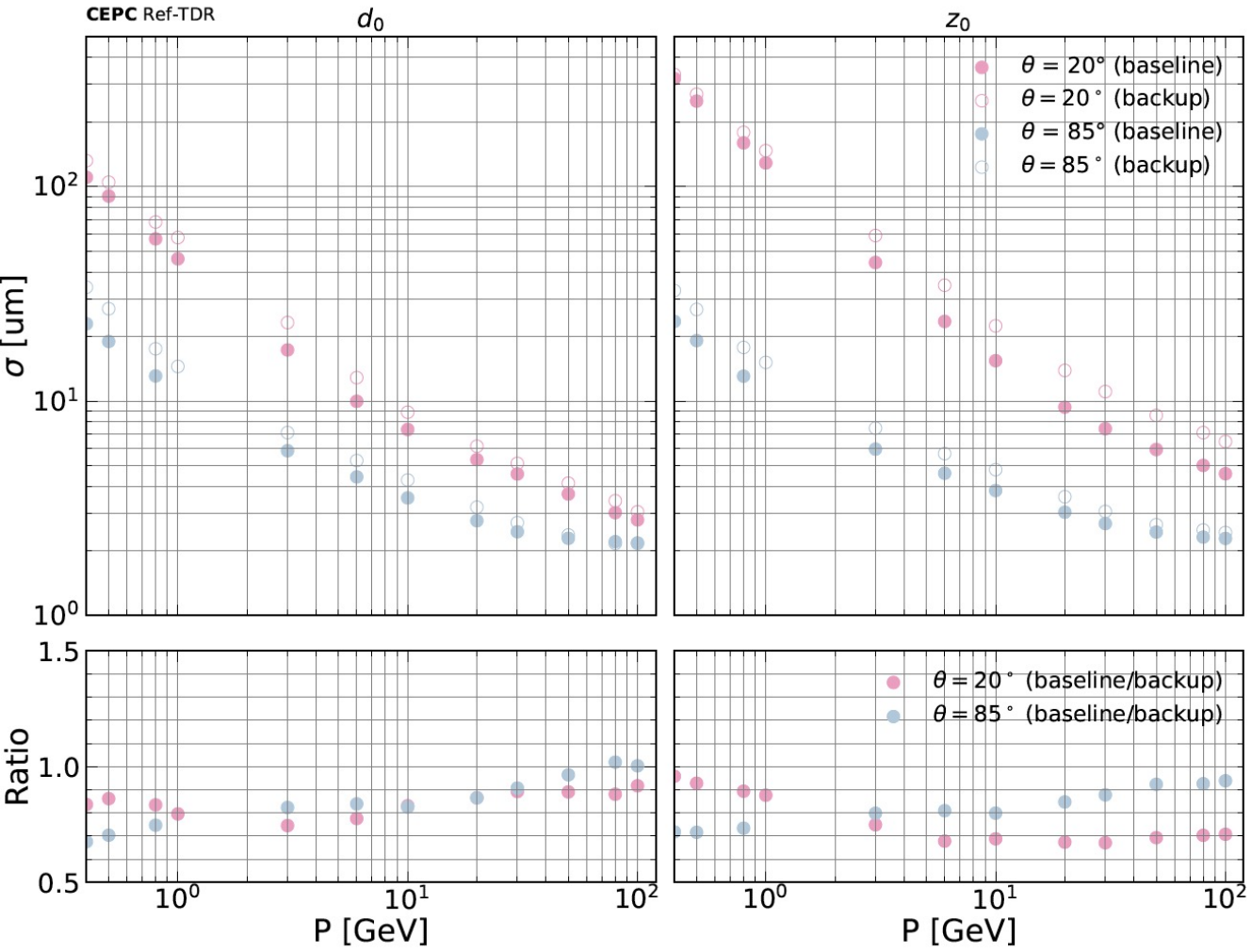
laser beamspot on bent-MAPS



# Performance: impact parameter resolution

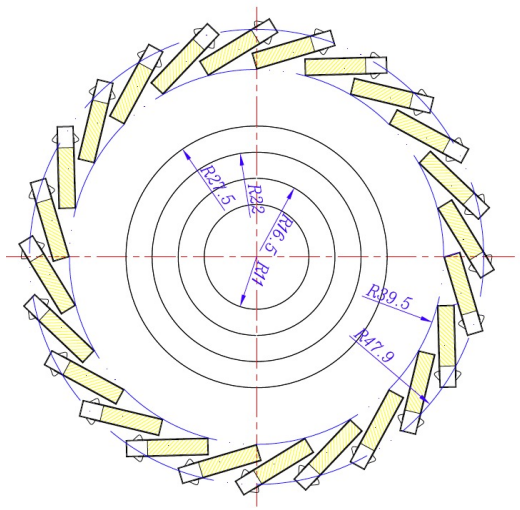
- Baseline has better resolution than alternative (ladder) (25-40%) in low momentum

d0 resolution: Baseline Vs backup layout

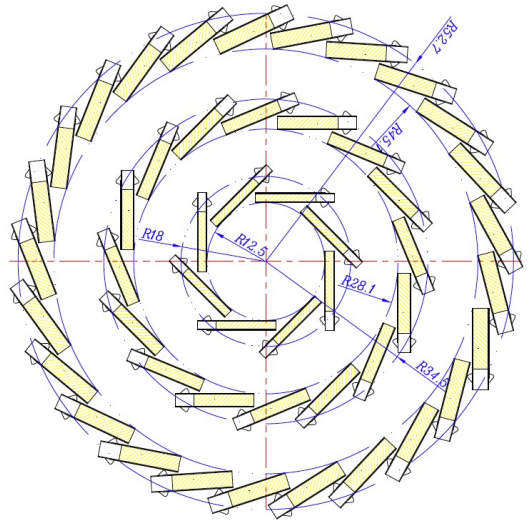



30%

Baseline layer
4 stitching +
1 double layer ladders



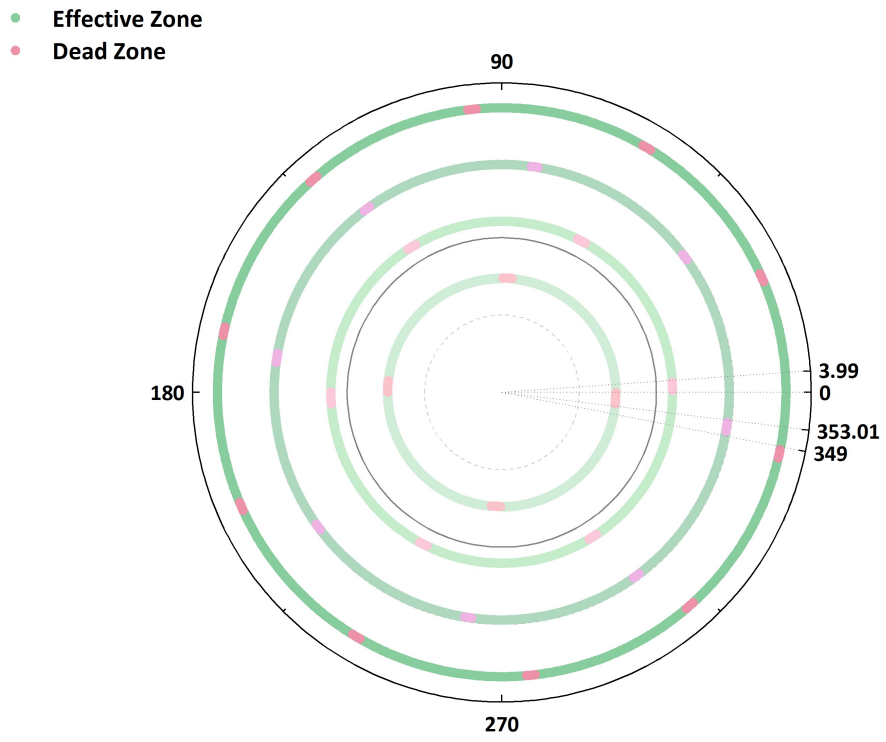

Backup layout
3 double layer ladders



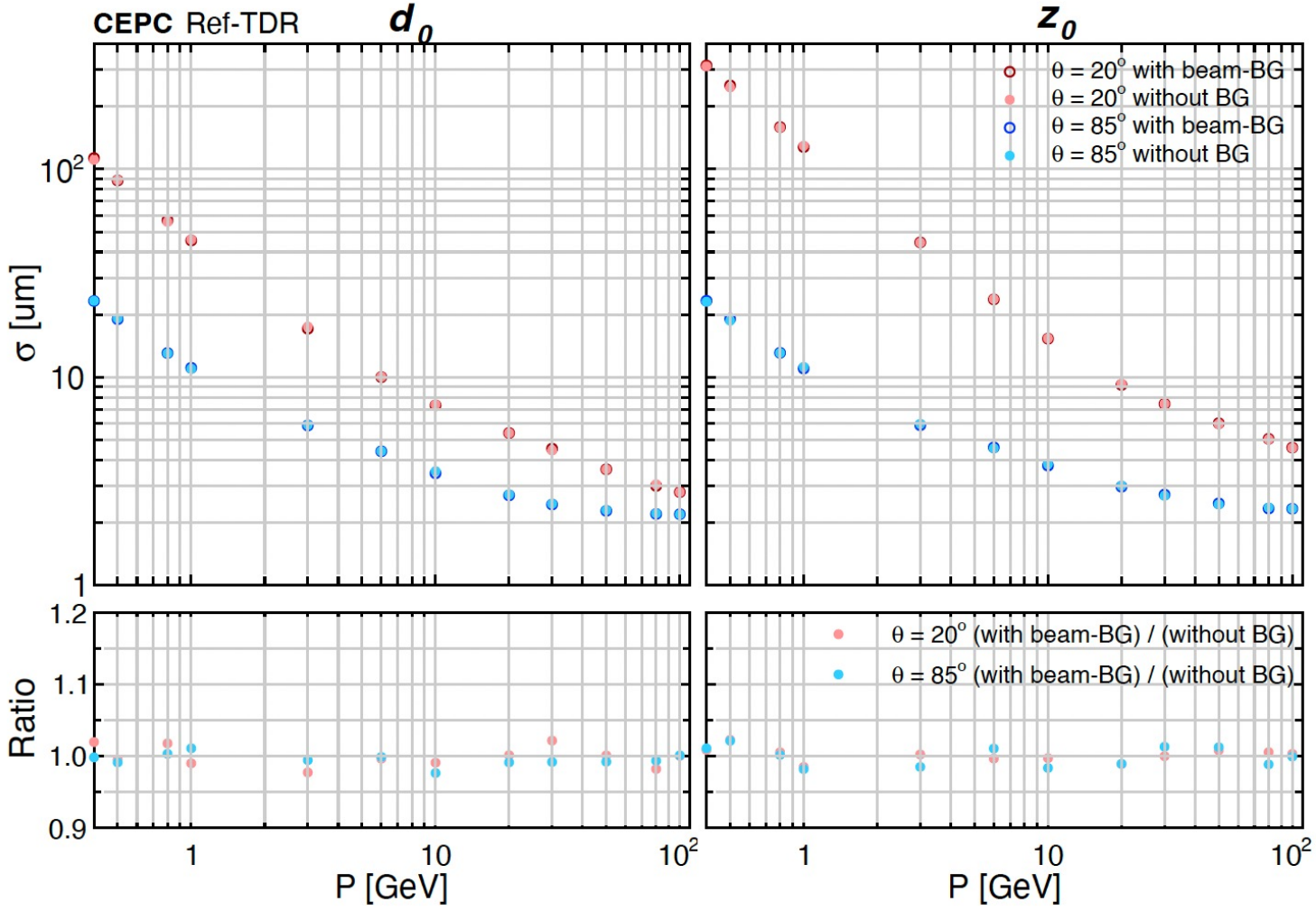
# Performance with beam background

The impact of beam background to performance has been updated.

– No visible effect in d0/Z0 resolution

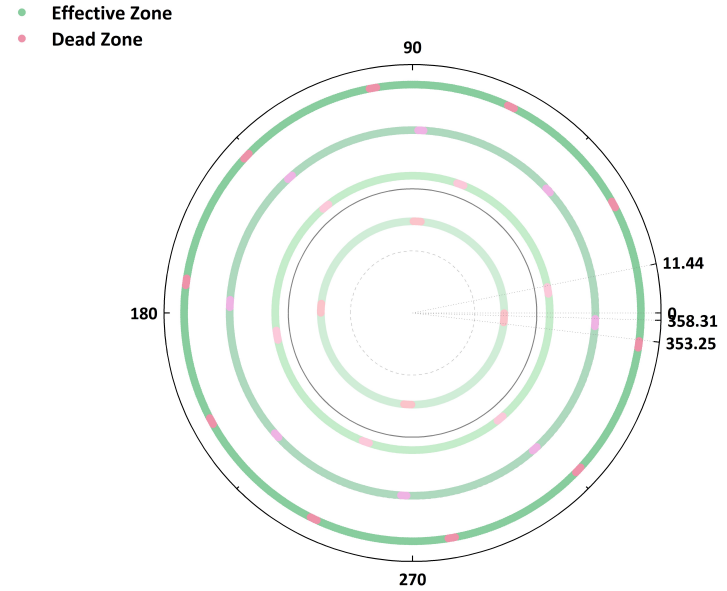



Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.



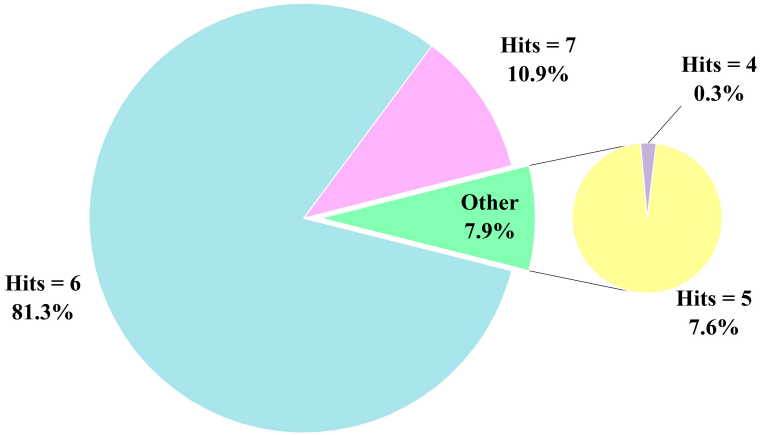
# Performance: Efficiency

- A few percent Inefficiency expected in stitching layer
- Sensor (RSU) has inefficiency region in power stitch
- 99.7% of the track with >=4 hits ( 6 hits expected)

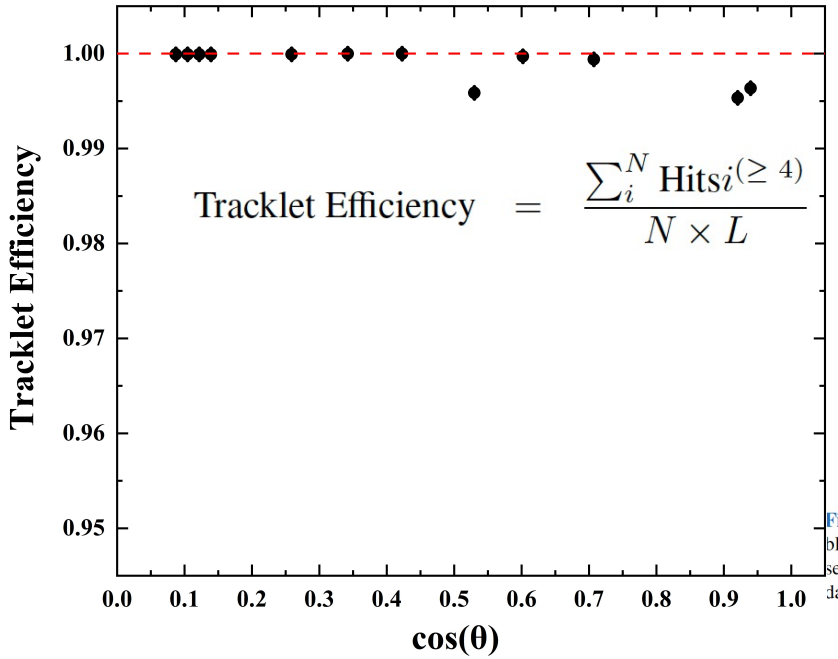



Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

Number of hits




Tracklet efficiency




RSU design

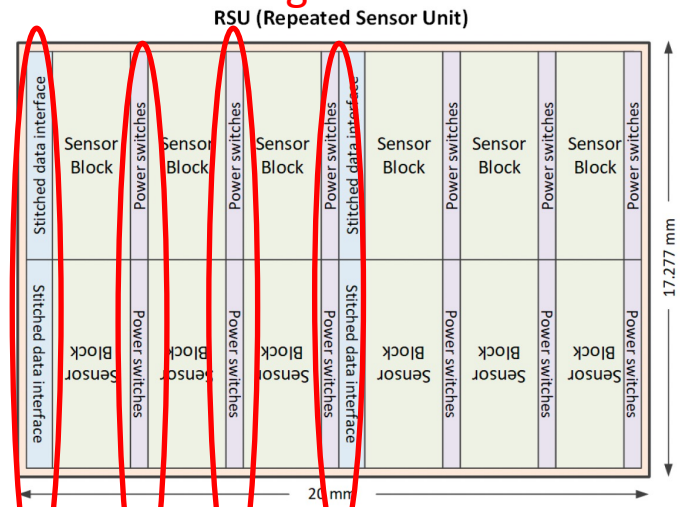



Figure 4.50: Proposed floor-plan for a repeated sensor unit (RSU) (not to scale). It contains several identical senso blocks. Each of them has a pixel matrix with its own biasing generator, slow control and periphery readout circuit. Each sensor block can be selectively switched on/off. The stitched data interface blocks are used to transmit control signals and data to the edge of the stitching sensor.

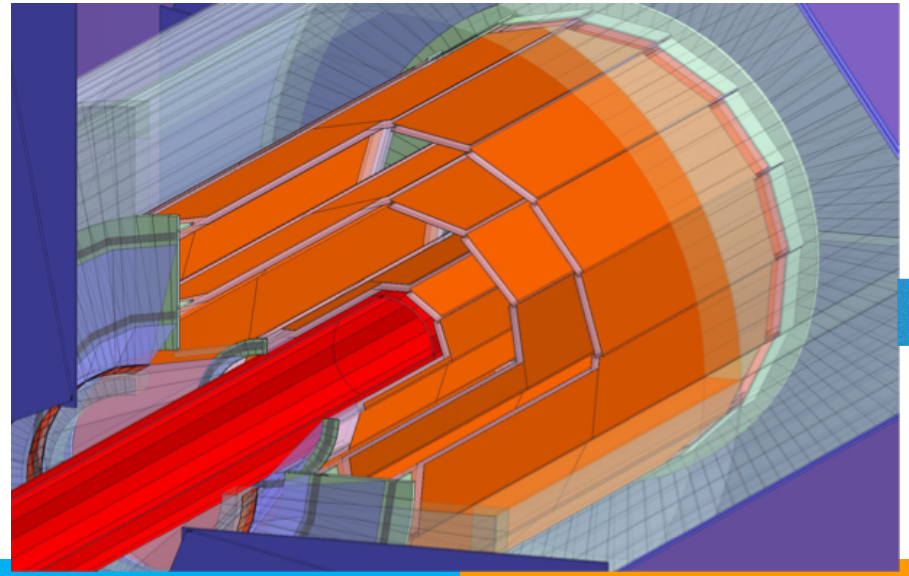
# Research team

- IHEP: 8 faculty,  2 postdoc, 5 students
- CERN: Recent joint R & D collaboration in HLMC 55nm aiming for ALICE3 upgrade
- IPHC/CNRS:  Christine Hu et al (3 faculty): Collaboration in FCPPL and DRD3
  - CEPC Jadepix design, ALICE ITS3 upgrade (especially on MAPS design, stitching)
- IFAE: Chip design , Sebastian Grinstein et al (2 faculty)
  - CEPC Taichupix chip design, ATLAS ITK pixel and HGTD upgrade
- ShanDong U.: Stitching chip design (3 faculty,  1 postdoc, 3 students )
- CCNU: chip design, ladder assembly (2 faculty , 3 students )
- Northwestern Polytechnical U. : Chip design (5 faculty, 2 students )
- Nanchang U. : chip design, (1 faculty,  1 students)
- Nanjing U.: irradiation study, chip design : (2 faculty,  4 students)
- NanKai U. : physics performance (1 faculty, 1 student)

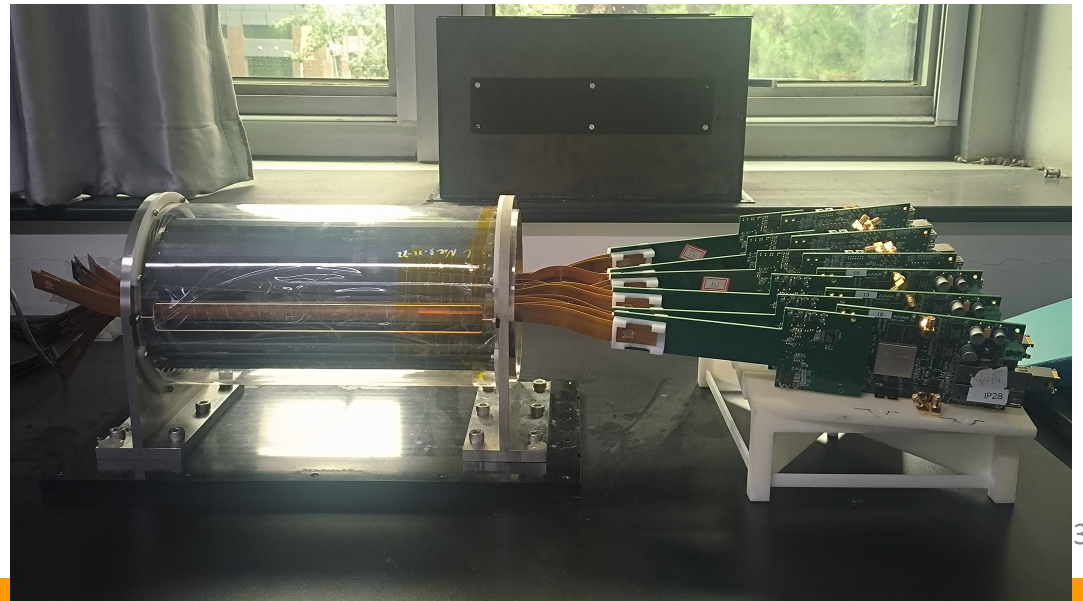
# Summary

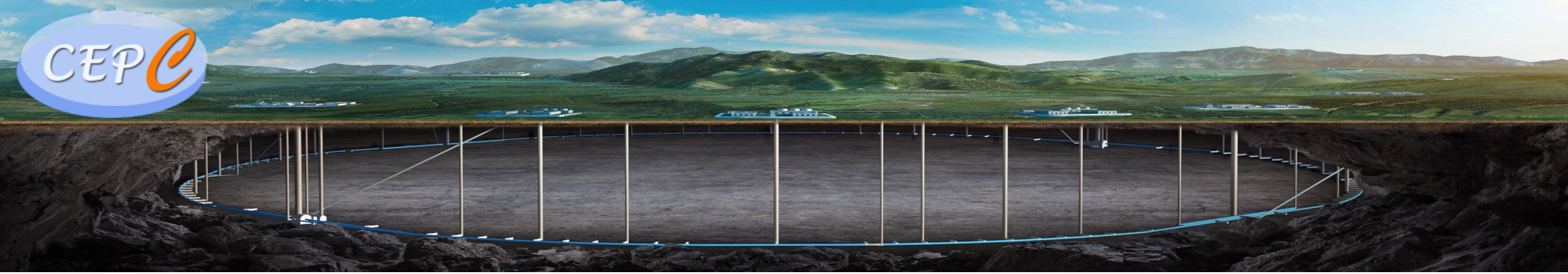
- 1st full-size Prototype based ladder design for CEPC vertex detector developed
- Curved MAPS option chosen as baseline for Reference detector TDR. （arXiv:2510.05260）
- We active expanding international collaboration and explore synergies with other projects
  - Recent collaboration with CERN on ALICE3 tracker upgrade
  - We are member of ECFA DRD3 collaboration

**CEPC vertex conceptional design (2016)**



**CEPC vertex prototype (2023)**





# Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

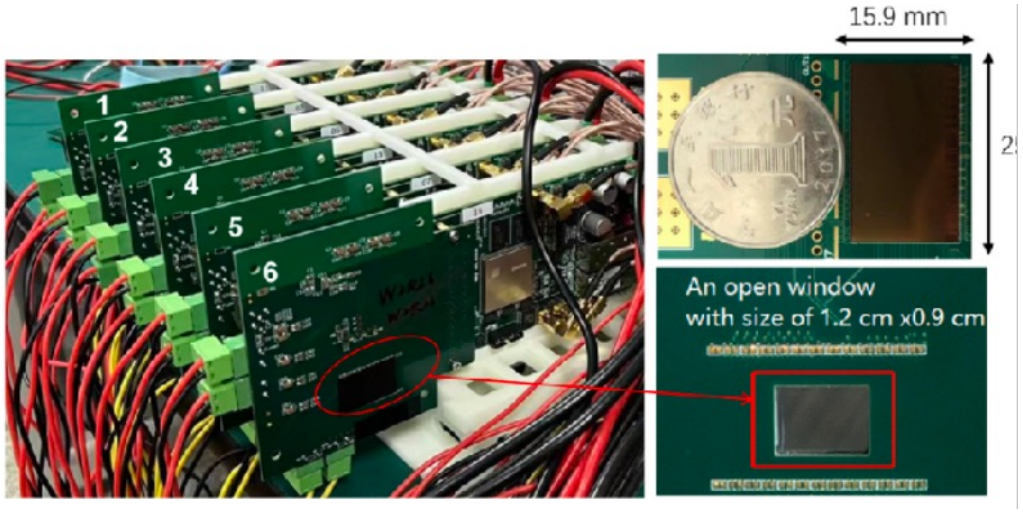
# Working plan

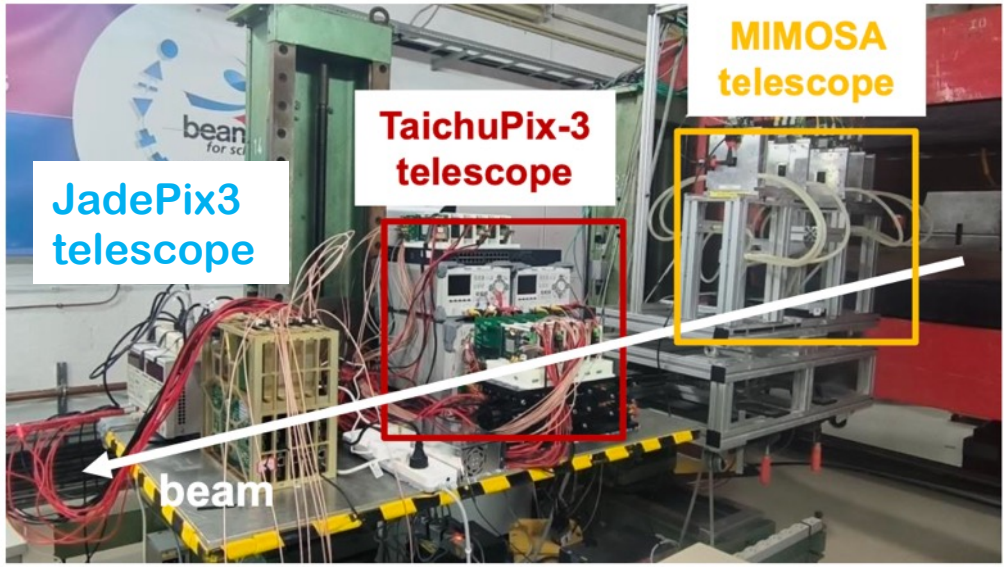
- Development of wafer-scale stitching MAPSs
  - Develop wafer-scale stitching with 180nm technology
  - The second-generation stitching chip will transition to 65 nm/55 nm
    - Baseline: TPSCo's 65 nm technology
    - Alternative: HLMC's 55 nm technology.
- Ultra-thin mechanical supports and low-mass integration techniques.
  - Start with prototype with dummy silicon wafer
- Construction of a full-scale VTX prototype to address challenges in mechanical precision, cooling performance, laser alignment, and system-level integration.

# Summary: working plan

| | Status | CEPC Final goal | CEPC Expected date |
|---|---|---|---|
| CMOS chip technology | Full-size chip with TJ 180nm CIS | 65nm CIS | 2027: Full-size 65nm chip |
| Spatial resolution | 4.9 μm | 3-5 μm with final chip | 2028 |
| Stitching | 11*11cm stitched chip with Xfab 350nm CIS | 65nm CIS stitched sensor | 2029 |
| Bent silicon with small radius | Bent Dummy wafer radius ~12mm | Bent final wafer with radius ~11mm | 2030 |
| Detector cooling | Air cooling with 1% channels (24 chips) on | Air cooling with full power | 2027： thermal mockup |
| Detector integration | Detector prototype with ladder design | Detector with bent silicon design | 2032 |

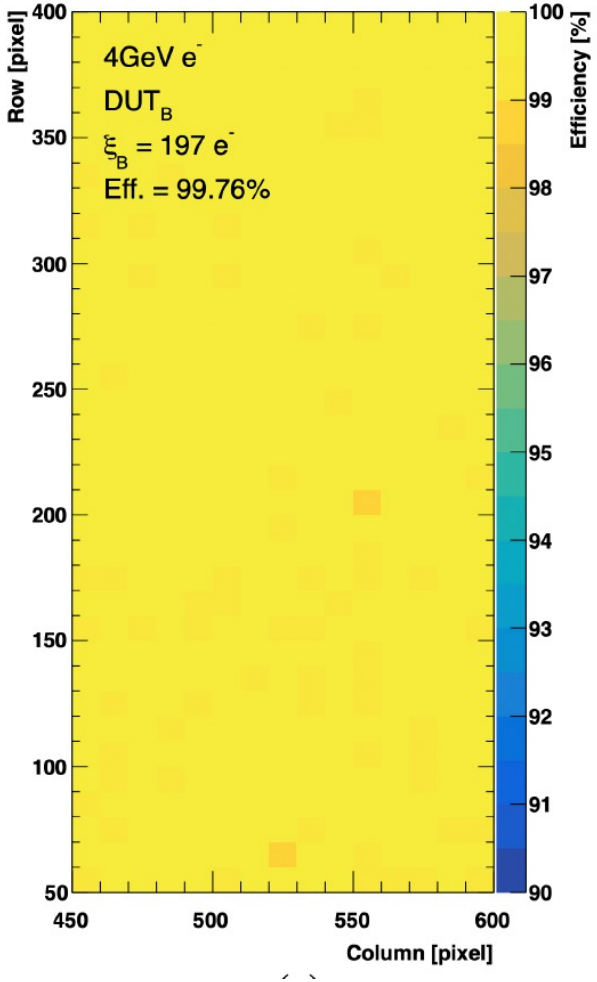
# R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY



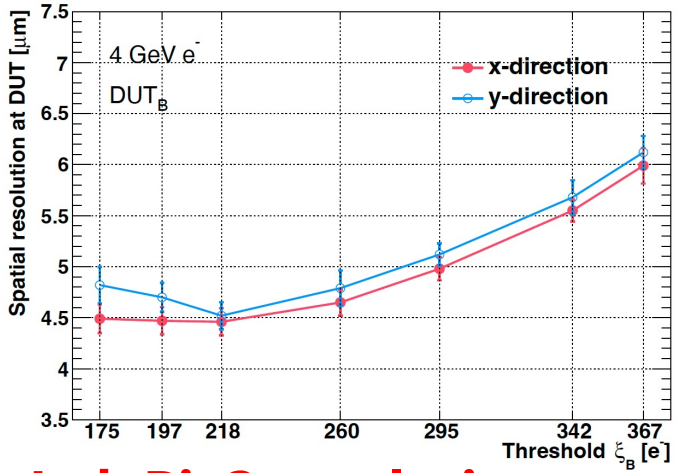




Spatial resolution 4~5um, Efficiency >99%

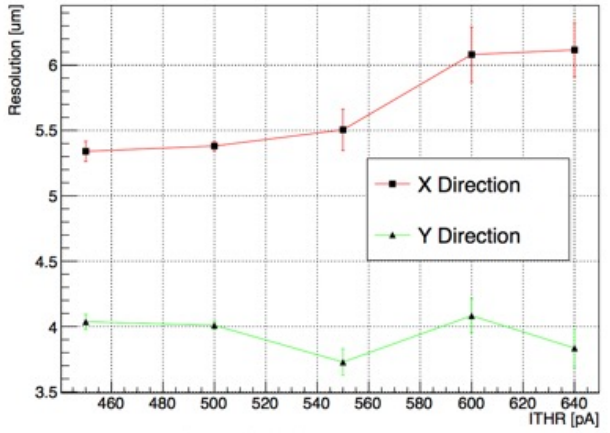
## TaichuPix3 efficiency




## TaichuPix3 resolution



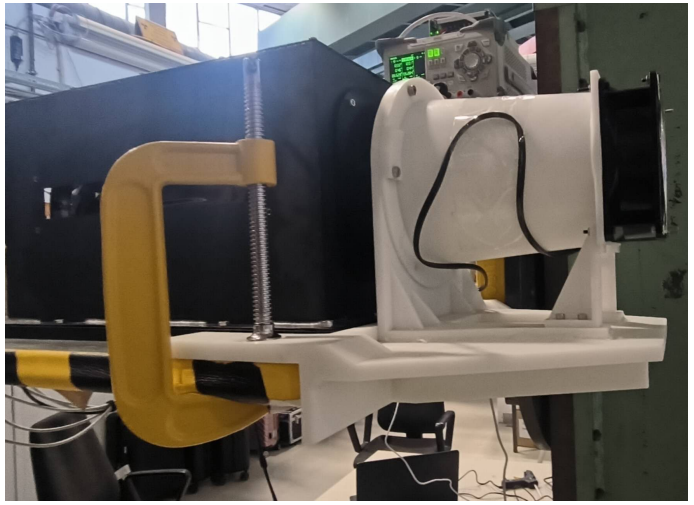

## JadePix3 resolution



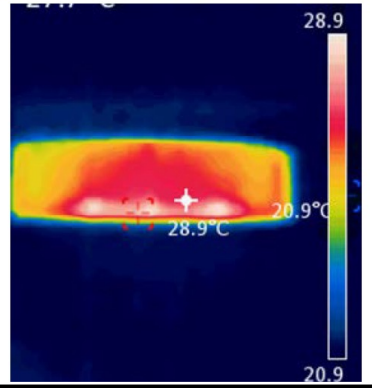

Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

# R&D efforts: Air cooling in vertex prototype

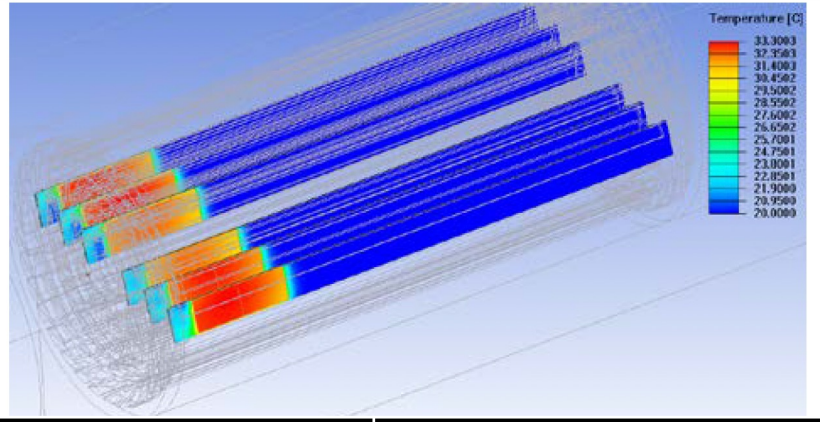
- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm$^2$ (17.5 MHz in testbeam)
  - Before (after ) turning on the cooling, chip temperature 41 °C (25 °C)
    - In good agreement to our cooling simulation
    - No visible vibration effect in spatial resolution when turning on the fan



Chip temperature under cooling during beam test: Max 28.9 ℃




Prototype cooling simulation： Max 33.3 ℃

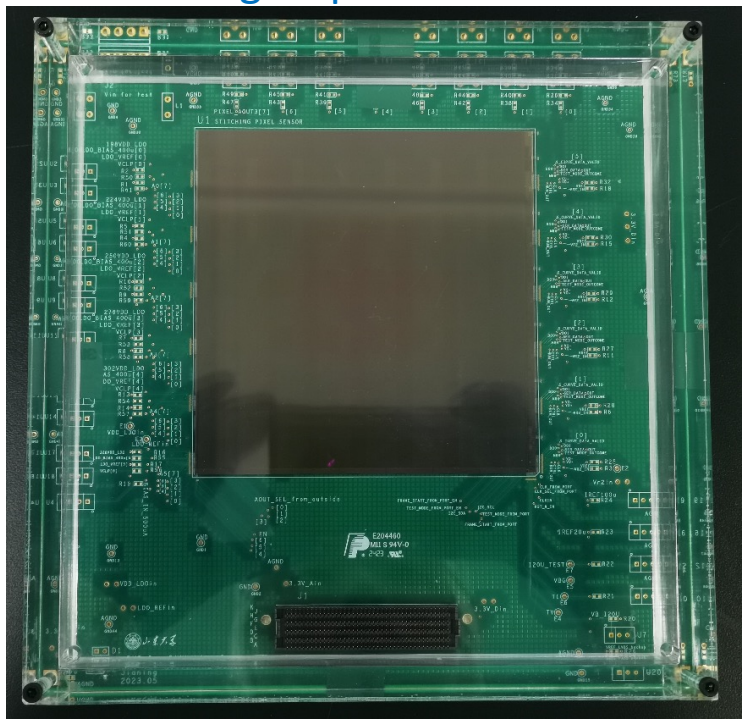


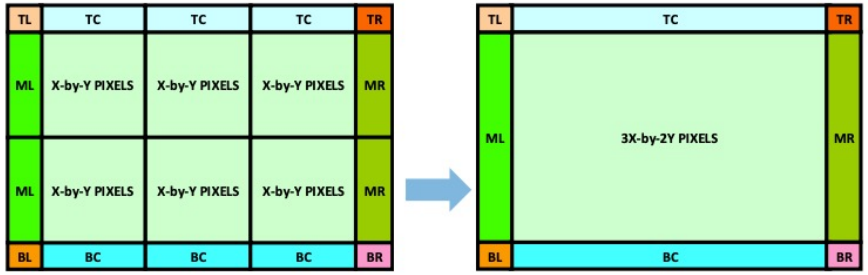

| Key technology | Status | CEPC Final goal |
|---|---|---|
| Detector cooling | Air cooling with 1% channels (24 chips) on | Air cooling with full power |

# R&D efforts and results: R & D for curved MAPS

- Stitching chip design (by ShanDong U.)
  - 350nm CIS technology Xfabs
  - Wafer level size after stitching ~11 ×11 cm$^2$
  - reticle size ~2 ×2 cm$^2$
  - 2D stitching
  - Engineering run, chip under testing

Stitching chip : 11 ×11 cm$^2$

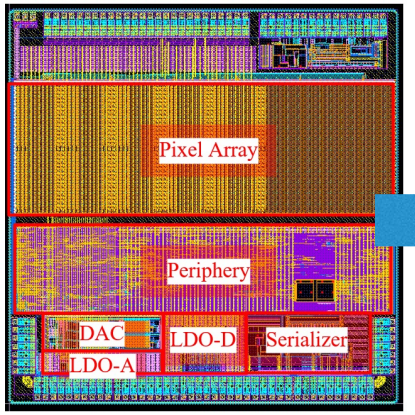


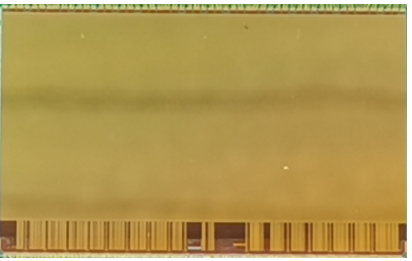



| Key technology | Status | CEPC Final goal |
|---|---|---|
| Stitching | 11*11cm stitched chip with Xfab 350nm CIS | 65nm CIS stitched sensor |

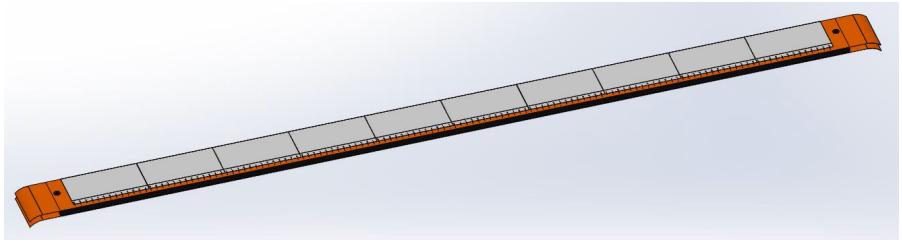
# Overview of CEPC vertex detector prototype R & D

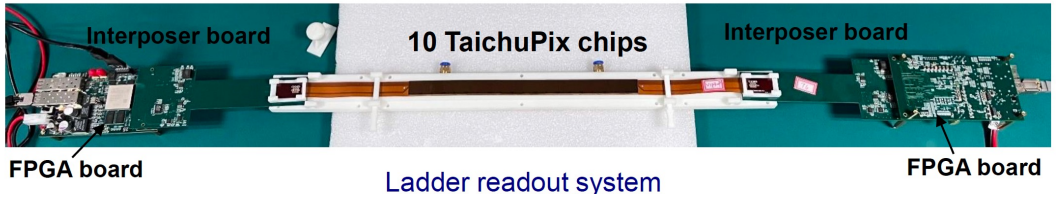
## CMOS Sensor chip development



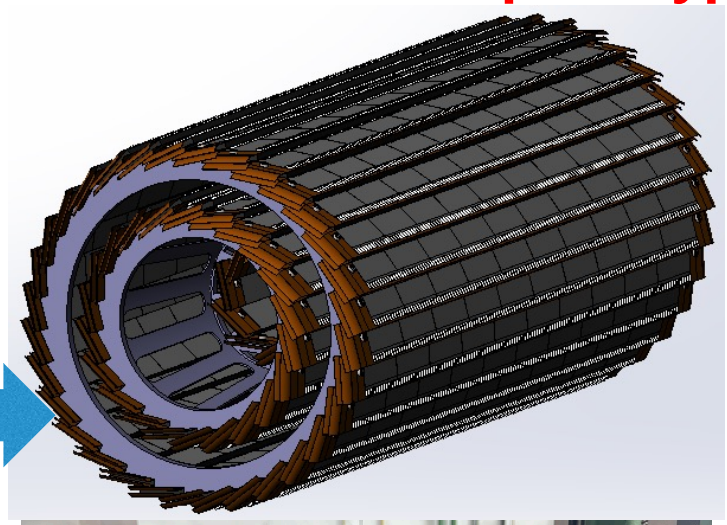
## Detector module (Ladder) Prototyping

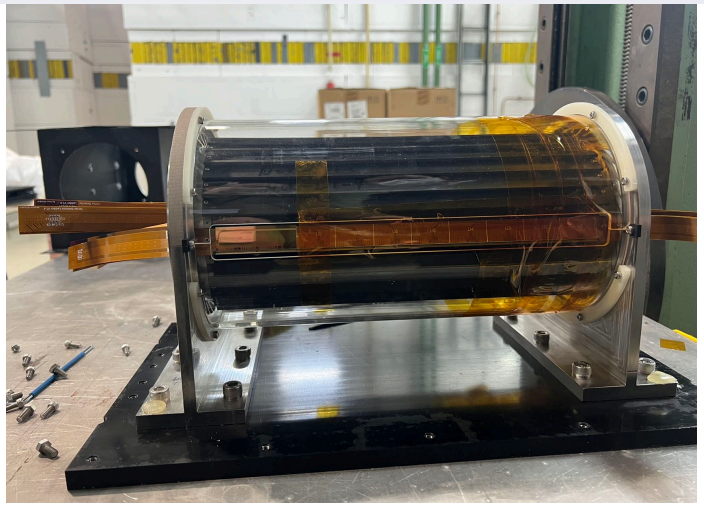





Ladder readout system

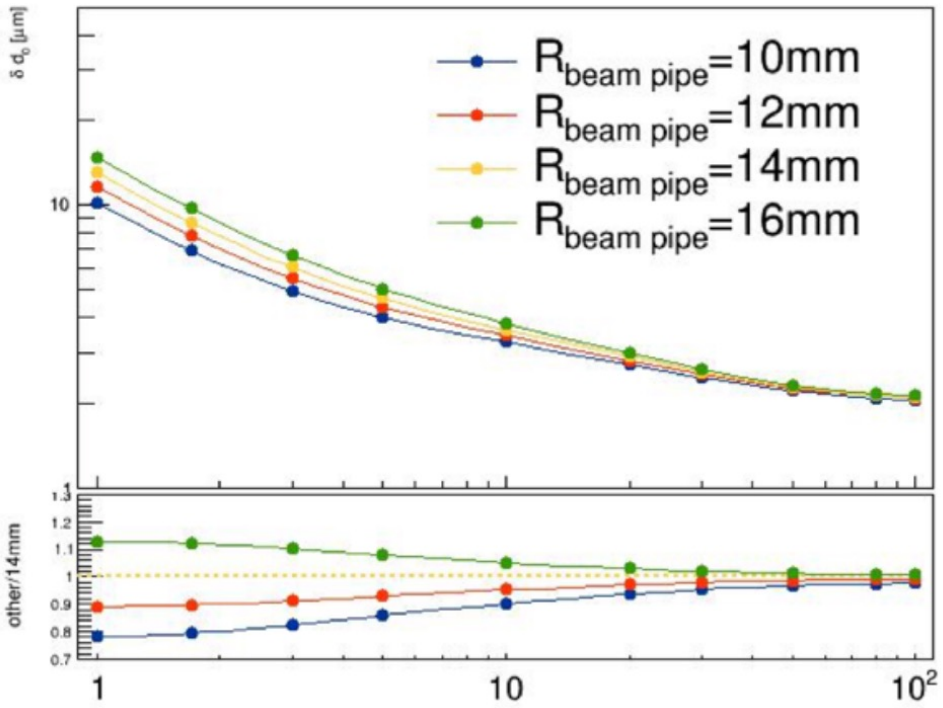
## Vertex detector prototype

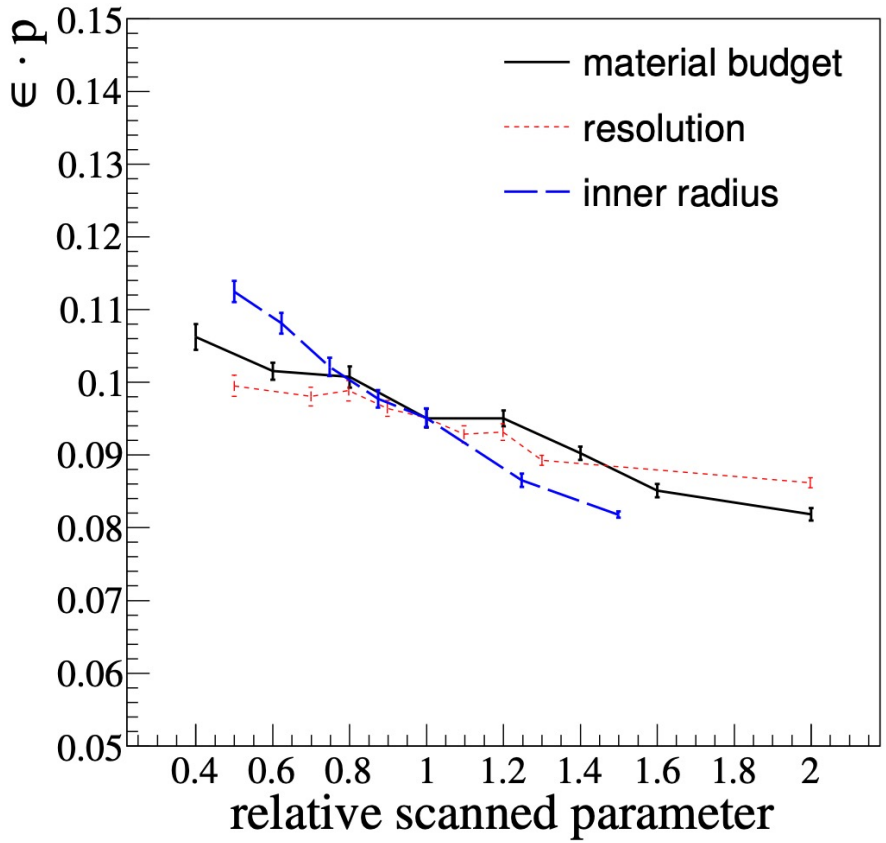




# Vertex Requirement

- 1st priority: Small inner radius, close to beam pipe (11mm )
- 2nd priority: Low material budget <0.15% X0 per layer
- 3rd priority: High resolution pixel sensor： 3~5 μm

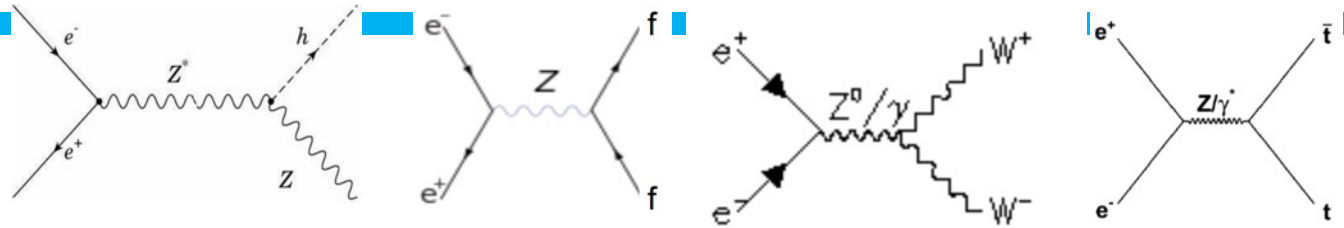


# CEPC physics program

**An extremely versatile machine with a broad spectrum of physics opportunities**

**→ Far beyond a Higgs factory**



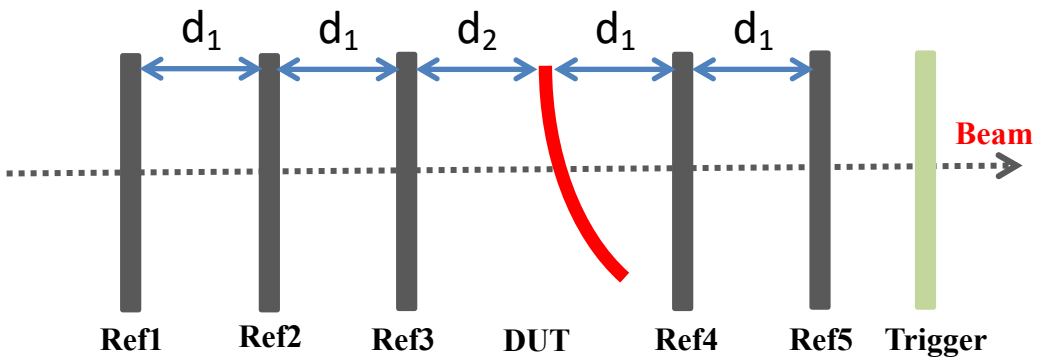

| Operation mode | | ZH | Z | $W^+W^-$ | $t\bar{t}$ |
|---|---|---|---|---|---|
| $\sqrt{s}$ [GeV] | | ~240 | ~91.2 | ~160 | ~360 |
| Run time [years] | | 10 | 2 | 1 | 5 |
| **CDR (30 MW)** | $L$ / IP [$\times 10^{34}$ cm$^{-2}$s$^{-1}$] | **3** | **32** | **10** | - |
| | $\int L\,dt$ [ab$^{-1}$, 2 IPs] | 5.6 | 16 | 2.6 | - |
| | Event yields [2 IPs] | $1\times10^6$ | $7\times10^{11}$ | $2\times10^7$ | - |
| Run Time [years] | | 10 | 2 | 1 | ~5 |
| **Latest** **30 MW** | $L$ / IP [$\times 10^{34}$ cm$^{-2}$s$^{-1}$] | **5.0** | **115** | **16** | **0.5** |
| **50 MW** | $L$ / IP [$\times 10^{34}$ cm$^{-2}$s$^{-1}$] | 8.3 | 191.7 | 26.6 | **0.8** |
| | $\int L\,dt$ [ab$^{-1}$, 2 IPs] | 20 | 96 | 7 | 1 |
| | Event yields [2 IPs] | $4\times10^6$ | $4\times10^{12}$ | $5\times10^7$ | $5\times10^5$ |

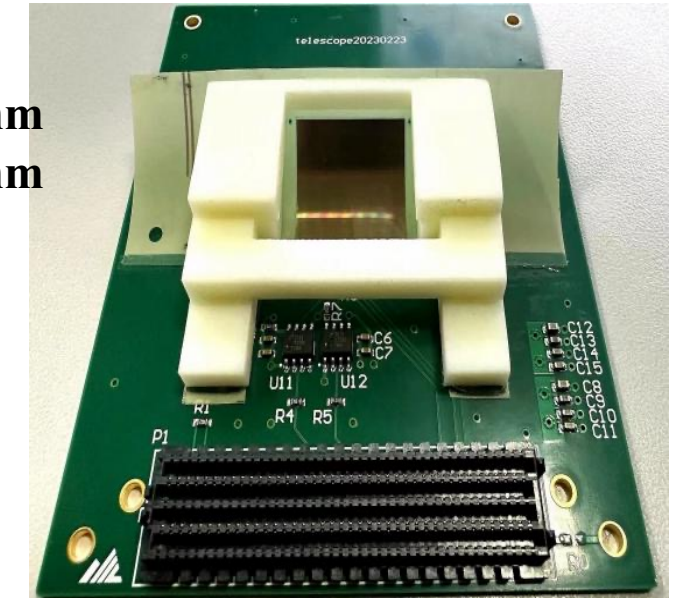
- Huge measurement potential for precision tests of SM: Higgs, electroweak physics, flavor physics, QCD/Top
- Searching for exotic or rare decays of H, Z, B and $\tau$, and new physics
- **CEPC community joined ECFA Phy focus**

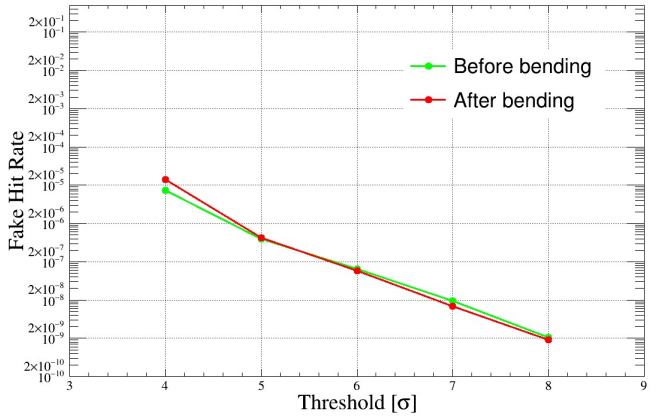
Both 50 MW and $t\bar{t}$ modes are currently considered as CEPC upgrades.

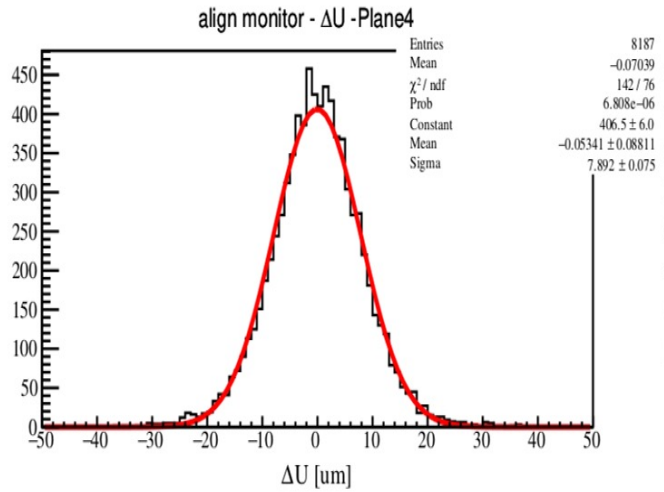
# R&D efforts : Curved MAPS testbeam

- R & D of curved maps with MIMOSA28 chip
  - No visible difference in noise level or spatial resolution before/after bending

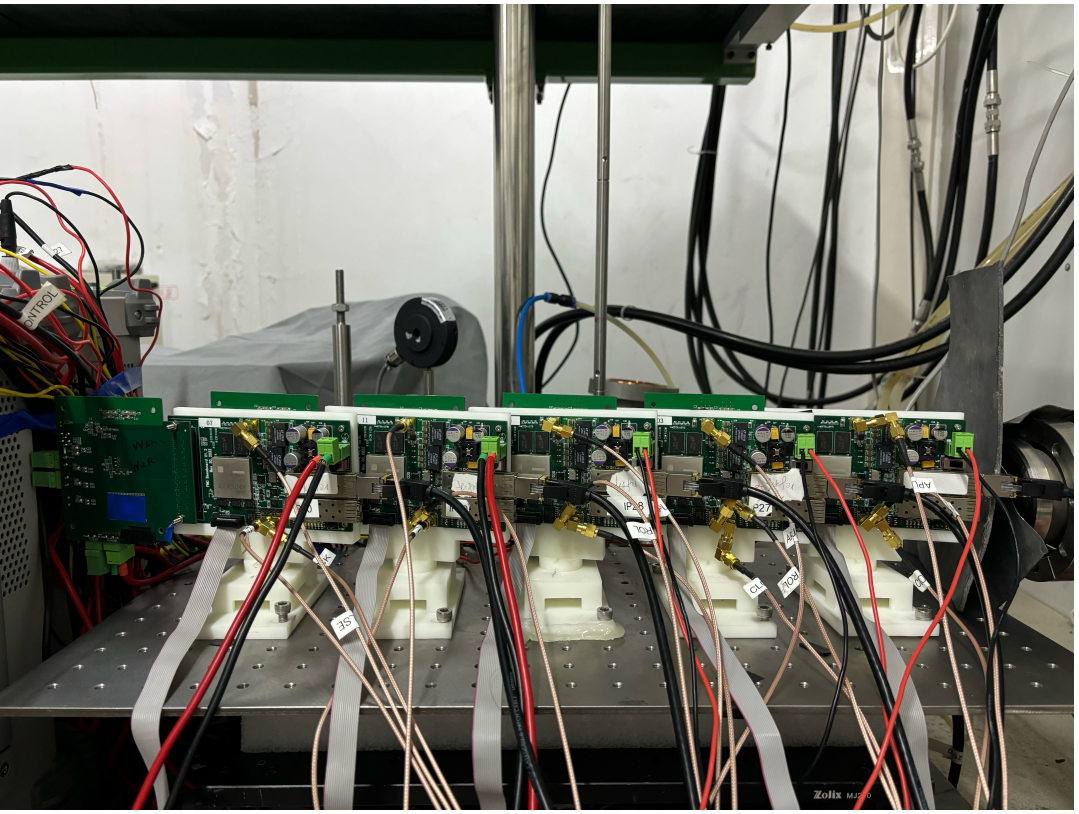


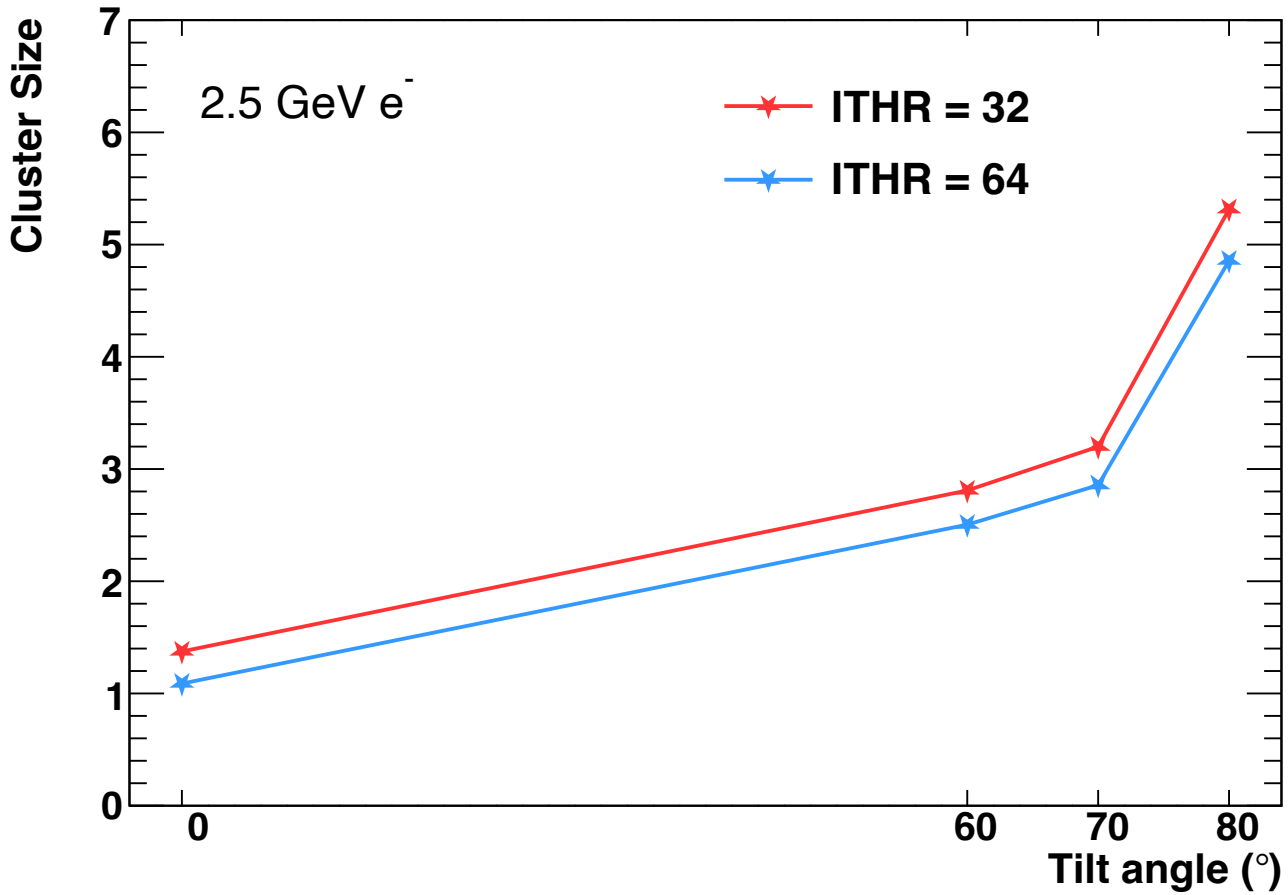



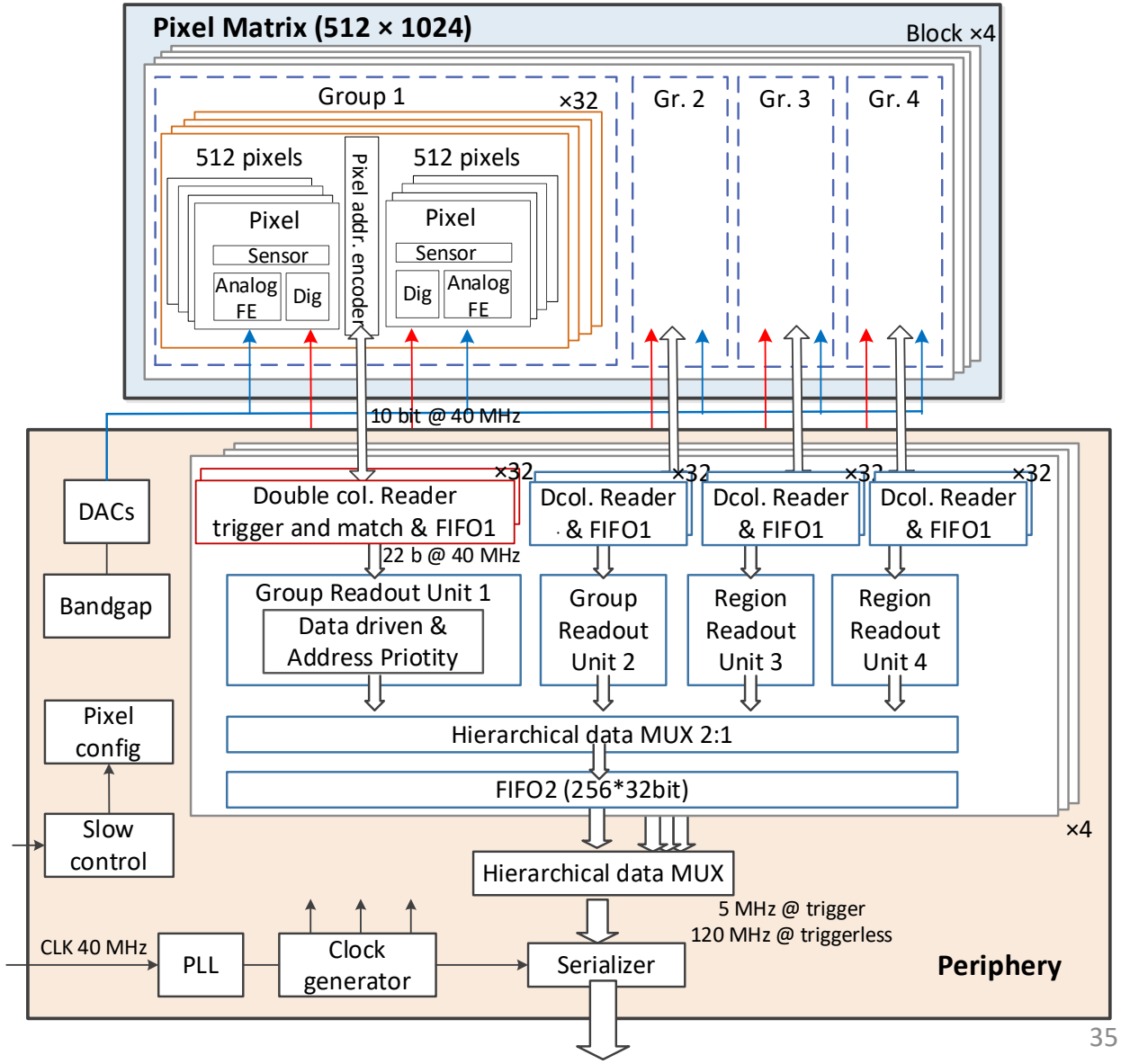
# Long barrel : cluster size vs incident angle





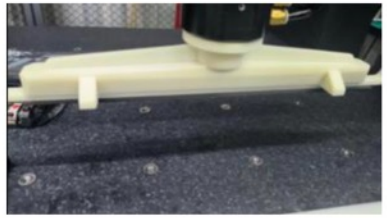
# TaichuPix design

- Pixel 25 μm × 25 μm
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
  - Priority based data-driven readout
  - Readout time: 50-100 ns for each pixel
- 2-level FIFO architecture
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- Trigger-less & Trigger mode compatible
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp
    only matched event will be readout
- Features standalone operation
  - On-chip bias generation, LDO, slow control, etc

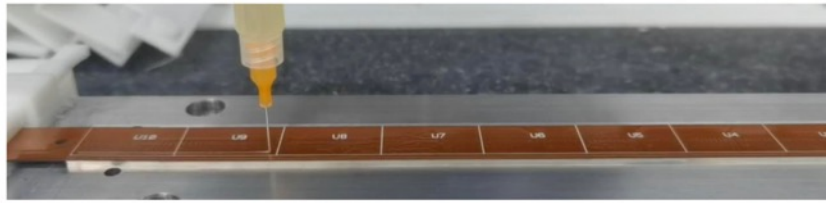


# TaichuPix3 vertex detector prototype

New pickup tools

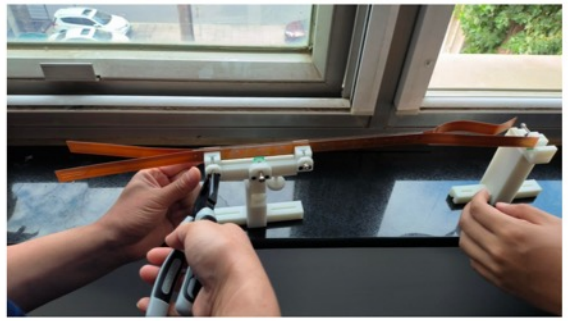


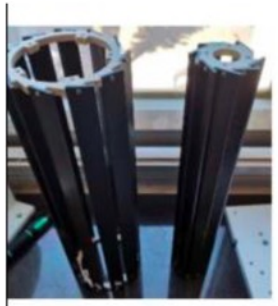
Dummy ladder glue automatic dispensing using gantry

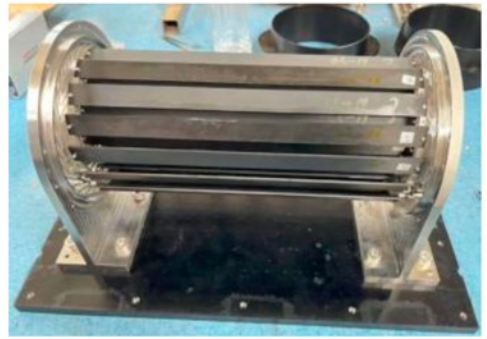


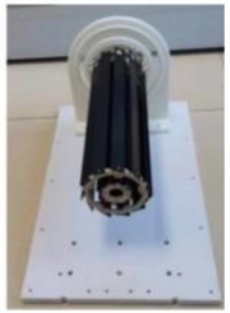
Ladder on wire bonding machine

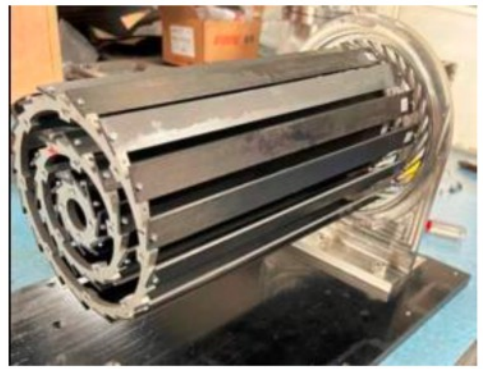
Dummy Ladder on holder











Ladder support tools

Ladder loaded on vertex detector

**The first vertex detector (prototype) ever built in China**

# Research team

- IHEP: overall intergration, chip design, detector assembly, electronics, offline
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  - DAQ: Hongyu Zhang
  - Detector assembly: Mingyi Dong
  - Physics:  Chengdong Fu, linghui Wu, Gang Li
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- ShanDong: chip design , Meng Wang, Liang Zhang, Jianing Dong
- CCNU: chip design, ladder assembly, Xiangming Sun, Ping Yang
- North West U. : Chip design Xiaoming Wei, Jia Wang, Yongcai Hu
- Nanchang U. : chip design,  Tianya Wu
- Nanjing: irradation study: Ming Qi , Lei Zhang