

3rd DRD3 Week Overview

<https://indico.cern.ch/event/1507215/>



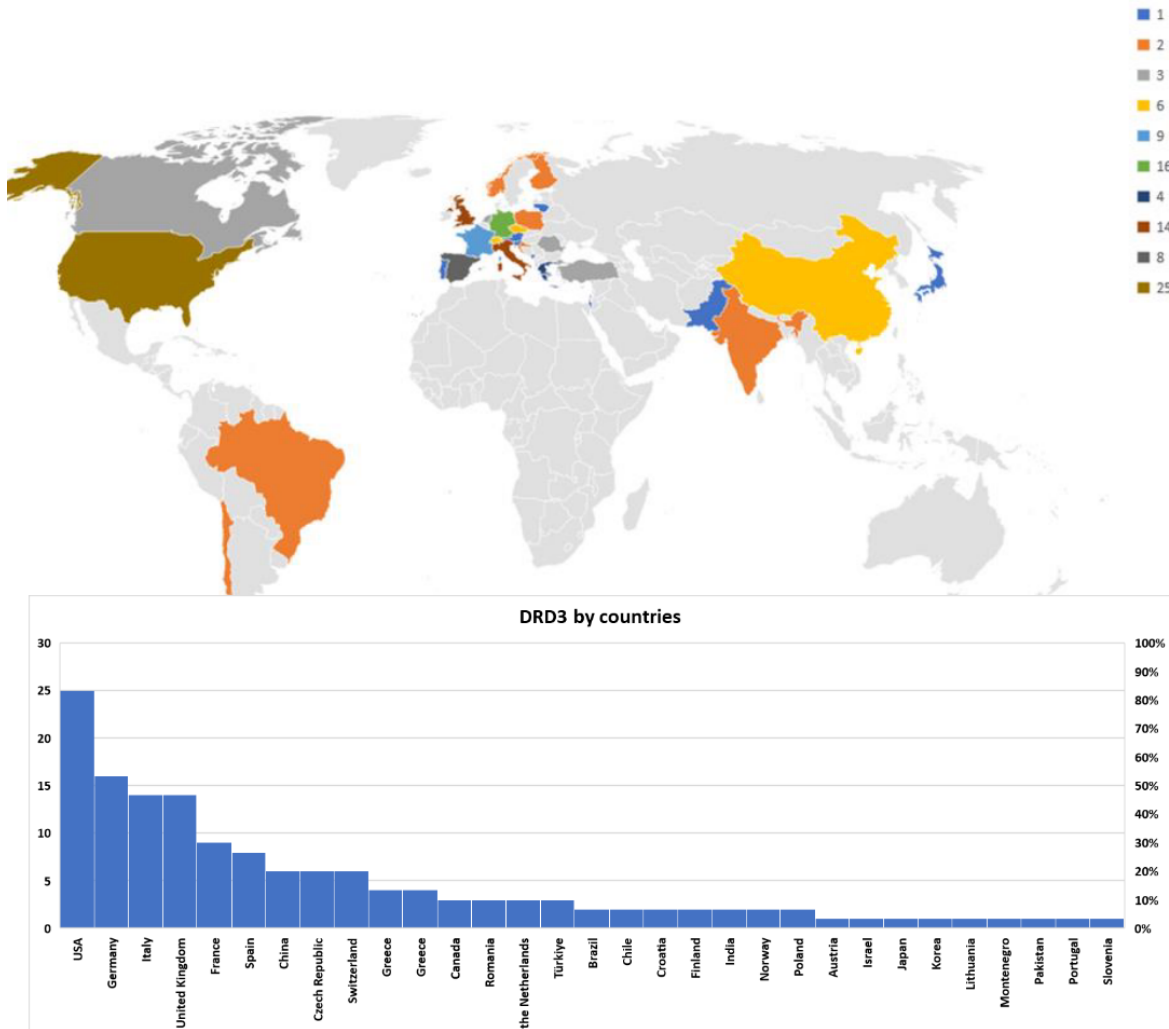
Xin Shi

13 June 2025

DRD3 Collaboration

146 institutions / 700++ people in the community e-group

Distribution of DRD3 members

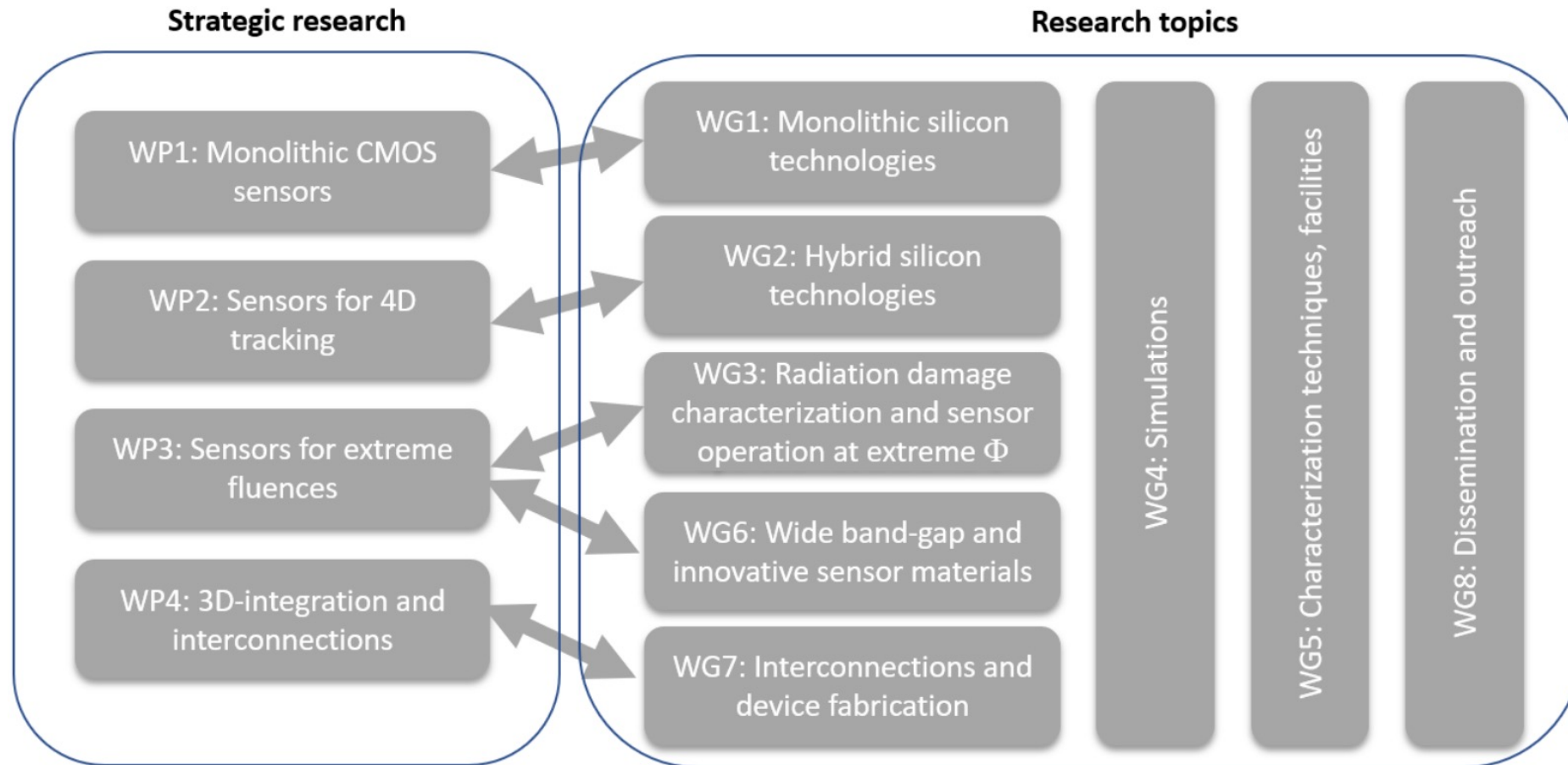


Main events since the last DRD3 week:

- Lots of scientific meeting across many WGs
- Preparation of WP projects – first “set” of projects is ready for approval at the CB
- MoU is in the final stages of preparation
 - gathered final information and confirmation on how the groups will participate
 - Already confirming first WP projects
- This year we had a first DRDC review
- We have New institutes wanting to join us.
- R&D work is ongoing in spite of large commitment of many groups to HL-LHC. The activities here are

Working Packages and Working Groups

- Relationship between Work Packages (WPs) and Work Groups (WGs)



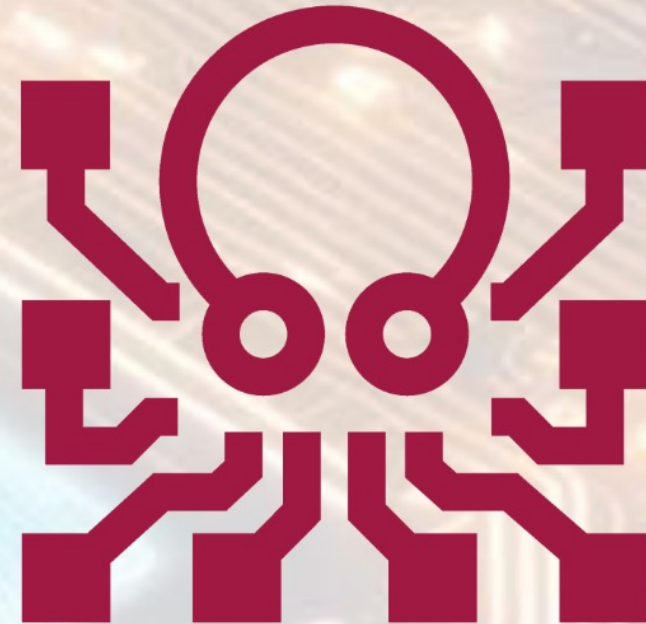
WG/WP1 - CMOS technologies

The First Monolithic Active Pixel Sensor Prototype for The OCTOPUS Project

DRD3 WG1/WP1 Project
OCTOPUS
Optimized CMOS
Technology for Precision
in Ultra-thin Silicon

Fadoua Guezzi Messaoud

On behalf of the OCTOPUS project
DRD3 Workshop June 2nd, 2025

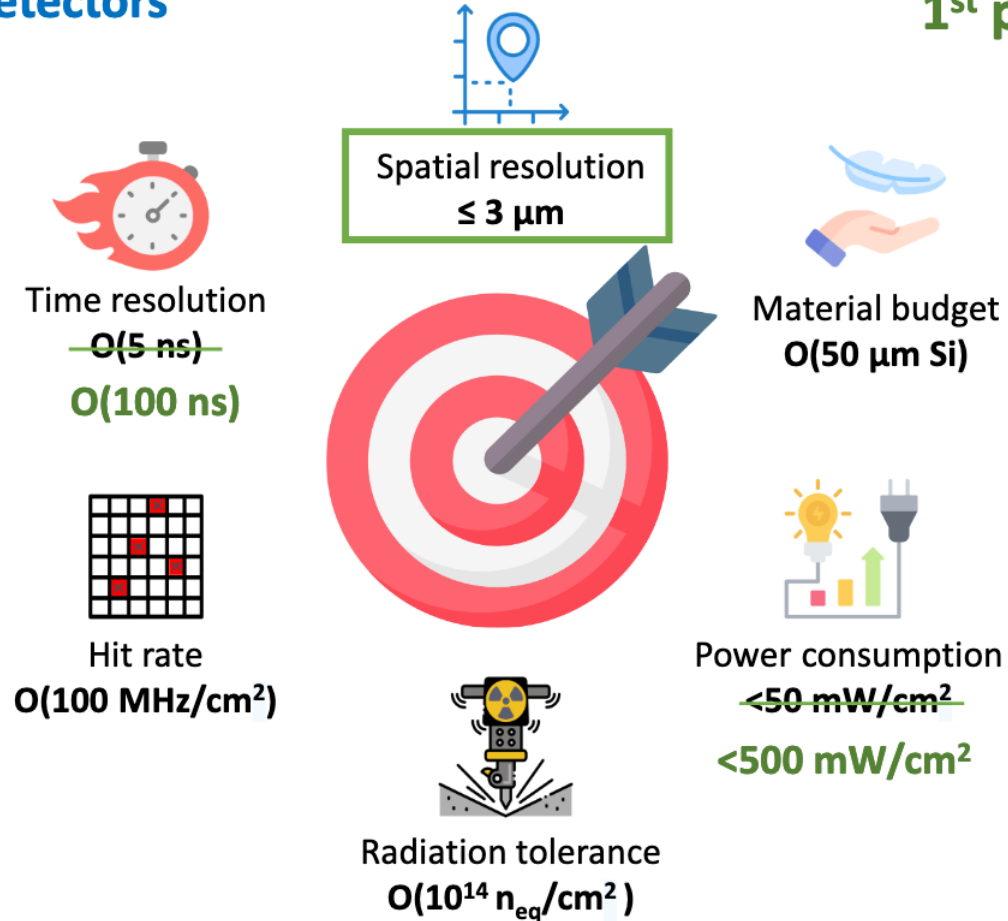


OCTOPUS Project: Final Target Specifications



Full size Demonstrator for future
Lepton collider vertex detectors

1st prototype

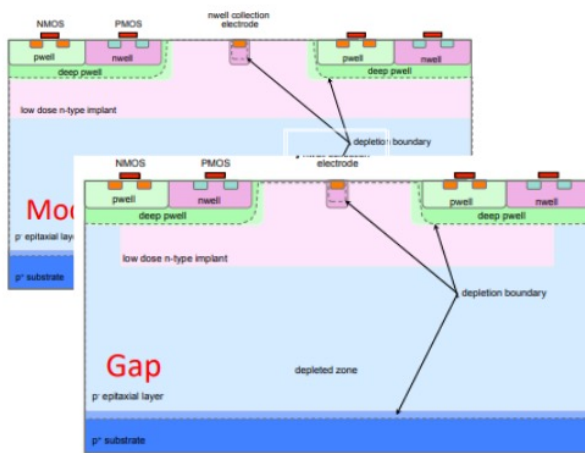


OCTOPUS Project: Technology Node

1st MAPS Prototype in TPSCO 65nm CIS

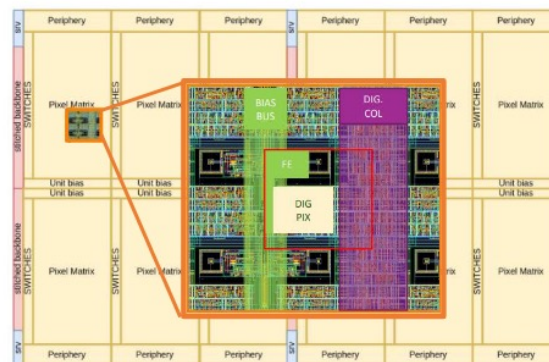
- ↪ Increase logic density
- ↪ Allow smaller pixels
- ↪ Decrease overall power consumption
- ↪ Several R&D ongoing for the next-gen MAPS
- ↪ Many Engineering run using 65 nm process:

Sensor Layout under study

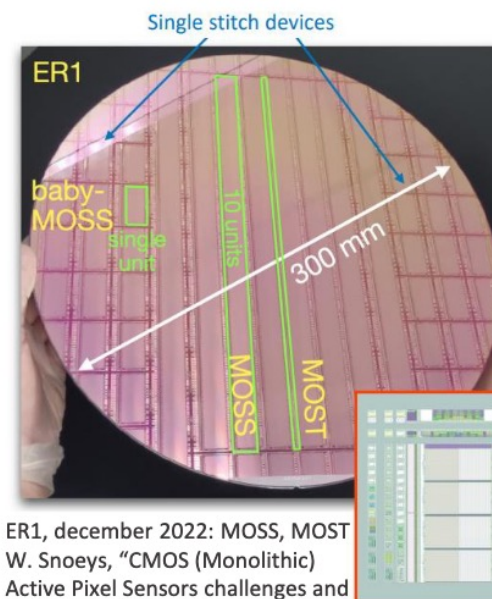


G. Vignola talk [Simulations of Monolithic Active Pixel Sensors for the OCTOPUS Project], DRD3 Workshop

- MLR1 (2021) and ER1 (2023)
- ER2 expected for June 2025



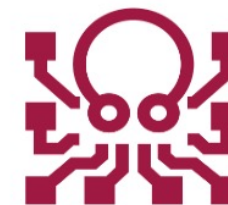
ER2 (Expected for June 2025): MOSAIX and chiplets
P. Vicente Leite, "Development of the MOSAIXchipfortheALICE ITS3 upgrade". TWEPP 2024



ER1, december 2022: MOSS, MOST
W. Snoeys, "CMOS (Monolithic) Active Pixel Sensors challenges and perspectives", Detector Seminar, CERN, December 6th, 2024



MLR1 (December 2020):
1.5 x 1.5 mm² test chips
Learn about the technology



Conclusion

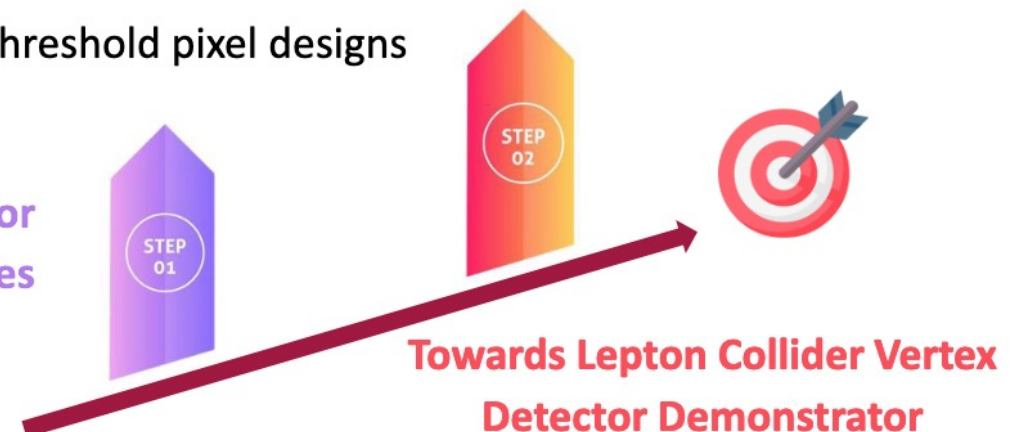
WP2 Summary: OCTOPUS Design



- ❑ OCTOPUS aims to develop a MAPS **vertex sensor demonstrator** for future lepton colliders
- ❑ Main target for the 1st prototype: a spatial resolution of 3 μm , will be used for the development of a sensor for the **next-generation of beam telescopes**
- ❑ ASIC design **in progress**:
 - Baseline architecture defined
 - ASIC design effort for first prototype started
 - Development of a high level model in progress
 - Alternative options to keep in mind: ultra-fine pitch pixels, two-threshold pixel designs



Towards a 1st Demonstrator
for Future Beam Telescopes



Design and characterization of CASSIA monolithic pixel sensors with gain

¹P. Bartulović, I. Berdalović, M. Jugović, B. Požar, T. Suligoj

²S. Haberl, A. Kotsokechagia, J. Lunde, H. Pernegger, C. Solans Sanchez



¹Micro and Nano Electronics Laboratory

Faculty of Electrical Engineering and Computing
UNIVERSITY OF ZAGREB, CROATIA

²CERN EP-ADE-TK

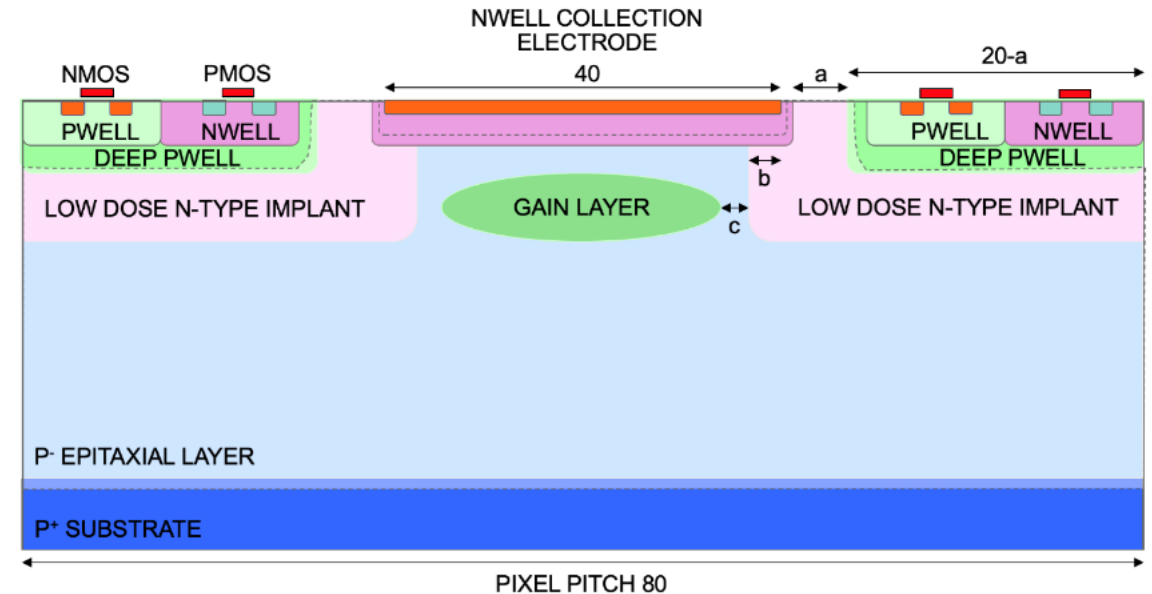


CASSIA (CMOS Active SenSor with Internal Amplification)



- goal – implement active sensors with internal gain in foundry CMOS process in order to:

- ① simplify in-pixel electronics due to higher input signals (e.g. reduce power consumption)
- ② improve timing resolution and response time (e.g. for future 4D tracking)
- ③ improve signal-to-noise ratio (e.g. for improved radiation hardness)



- implementation – add gain layer underneath collection electrode in modified Tower 180 nm process – allows for in-pixel integration of sensor with gain and analog/digital readout electronics
- choice of gain layer allows for breakdown voltage engineering
- choice of reverse bias allows for operation in either low-gain (LGAD) or high-gain (SPAD) mode

- CASSIA1 prototype implements 4 versions (M1-M4) of 3x3 mini-matrices containing sensors with gain
- I-V curves of M2 and M3 show good response to illumination and a wide voltage range for gain tuning
- in-pixel gain scans show uniform gain over the gain layer area, with gradual drop of gain outside GL area
- pulsed laser measurements show comparable response in LGAD mode for all mini-matrices
- CASSIA2 builds on the sensor structures with gain demonstrated in CASSIA1 by:
 - integrating them with an analog front-end + discriminator (LGAD mode)
 - integrating them with various quenching circuits (SPAD mode)
 - implementing a simple readout architecture for reading out small pixel matrices
- tape-out imminent, diced chips expected to be back for testing in Q4 2025

Design of COFFEE3, a small prototype for 55nm HVCMOS validation

Yang ZHOU (IHEP)

On behalf of the HVCMOS sensors in 55nm process collaboration

- Previous results from COFFEE2
- Project description
- Design of COFFEE3:
 - Process condition, architectures, simulation performances
 - Leverage the potential of the advanced process node;
- Summary and Outlooks



CMOS STRIPS

A POSSIBILITY FOR LARGE SCALE

Ingrid M. Gregor
on behalf of the CMOS Strips Collaboration

Jan-Hendrik Arling, Marta Baselga, Naomi Davis, Leena Diehl, Jochen Dingfelder,
Ingrid-Maria Gregor, Marc Hauser, Lennart Huth, Fabian Hügging, Karl Jakobs, Michael
Karagounis, Roland Koppenhöfer, Kevin Alexander Kröninger, Fabian Simon Lex,
Ulrich Parzefall, Niels Sorgenfrei, Simon Spannagel, Dennis Sperlich, Jens Weingarten



technische universität
dortmund



NEXT STEPS - FULL MONOLITHIC!

MASS = Monolithic Active Strip Sensors

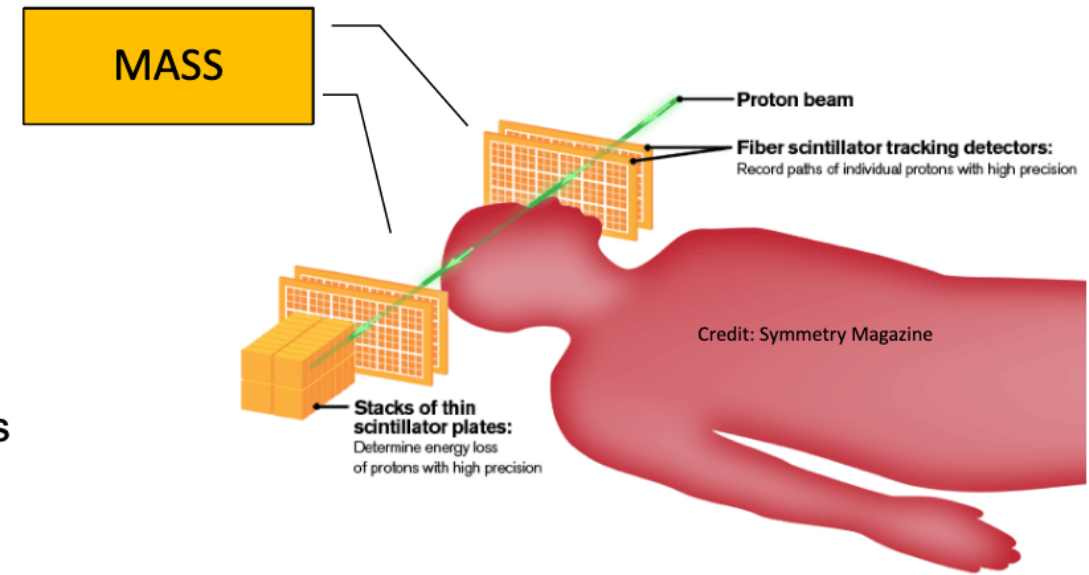
- To fully profit from the use of a CMOS process the front-end should be implemented
 - Ease of module building
 - Reduction of material
 - Possibly also reduction of costs
- Gives also the opportunity to advance field of applications: e.g. medicine
- Currently discussing a possible submission to LFoundry later this year together with other collaborators
 - Submission based on existing building blocks for front-end
 - No stitching as this aspect fully understood
 - Some testing features

Parameter	HEP application	Other application
Charge injection	10bit, 0-50ke (a la FE-I4)	10bit, 20ke-200ke (300ke)
Range threshold	1ke	~ 30ke
Noise	try for 100 - 300e	
ToT resolution	(need to be able to do c.o.g. clustering)	few ke at 40ke-300ke
Best operating point	low charge (high efficiency after irradiation)	close to Bragg peak -> threshold ~50-100ke, ToT max for 350ke
Tests	• different strip lengths (via wirebonding more strips) -> performance of the amplifier (noise, timing)	
Charge deposition (maximum)	12ke before irradiation	300ke (150µm*6keV/µm/3.6eV per e/h pair)
Charge deposition (minimum)	~7ke after irradiation	41ke (150µm*1keV/µm/3.6eV per e/h pair) for 150 MeV protons

POSSIBLE APPLICATION OUTSIDE HEP

MASS in Medical Physics

- Tracking Detectors for Proton CT Systems
 - Often using hybrid strip detectors for tracking
 - Tracking resolution profits from thinner sensors
 - Large area detectors for large field-of-view
 - Faster detectors could make pCT feasible (currently data-taking at very low beam current, i.e. protons per frame, non-standard accelerator operation hinders clinical application)
- Beam Monitoring in Proton and Ion Therapy
 - Radiation hard, low mass, large area, high count-rate detectors for high-intensity treatment modalities: FLASH therapy
 - Potential to replace ionisation chambers, which will suffer from saturation (high occupancy)
- Proton Radiography for Head and Neck treatments
 - Large dynamic range for charge measurement to allow measurement of stopping power in patient



Towards an OpenSource DMAPS project proposal

Manuel Handta, Marco Huebner, Dennis Hunter, Daniel Muenstermann,
Steffen Reith, Marc Stoettinger (HSRM)
Ivan Peric (KIT)

Why OpenSource again?

Issue:

- ▶ We use “large” and somewhat exotic process nodes that are in danger of becoming unavailable (change of ownership, foundry oversubscribed or going bankrupt)
- ▶ Due to proprietary processes and PDKs, we cannot just transfer our designs to alternative processes/foundries and partially not even discuss about details with collaborators thanks to NDAs
- ▶ Access to MPWs sometimes limited

Solution/Proposal:

- ▶ Use OpenSource!
 - ▶ If the PDK (and ideally the process) is OpenSource, other foundries could step in and offer to process our ASICs
 - ▶ The usage of OpenSource chip design tools would save cost and allow for commercial spin-offs without Cadence license fees
 - ▶ Ties in with European strategies for digital sovereignty/resilience



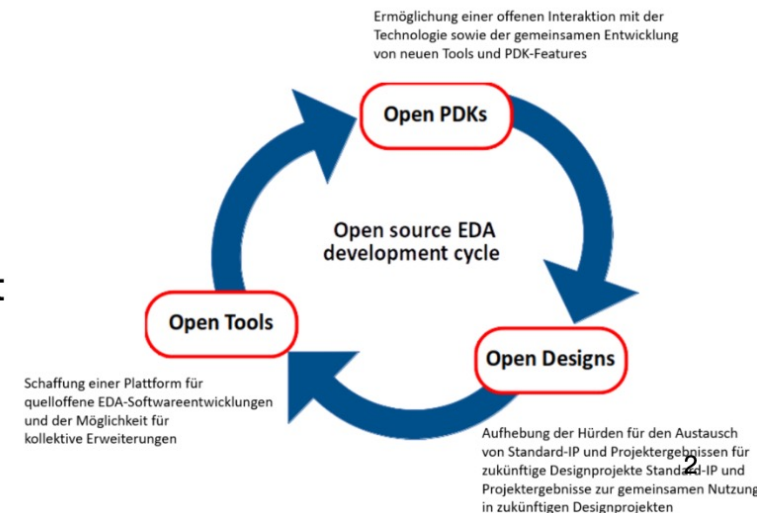
FOSS 130nm Production PDK
github.com/google/skywater-pdk

IHP-GmbH/IHP-Open-PDK



130nm BiCMOS Open Source PDK, dedicated for Analog, Mixed Signal and RF Design

12 Contributors 23 Issues 4 Discussions 317 Stars 43 Forks



How to proceed?



- ▶ So: should this become a WP1 proposal?
 - ▶ Does it match the strategic research goals set out in the research proposal? Should digital sovereignty/resilience be(come) a virtue on its own for DRD3?
 - ▶ However, addresses one of the processes mentioned and might also relate to RG1.5?
 - ▶ As far as I can tell today, work on the EDA-tool development process might be on equal footing with any “proper” sensor development - ok for DRD3?
 - ▶ Difficult to estimate a “proper” schedule
- ▶ Or rather a WG1/common project proposal?
 - ▶ DRD3 approval and common fund contribution would help with PCBs and applying for national funding for a PhD student and (re-)submission of a larger chip
- ▶ Please reach out to me if you are interested in the effort!

DRD3 - Solid State Detectors - Research Proposal (Version 3.1) -

DRD3 Proposal Team

May 27, 2024

WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: $\leq 3 \mu\text{m}$ position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm ² , 1 GHz/cm ² with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} neq/cm^2 NIEL and 500 MRad
RG 1.5	Low-cost large-area CMOS sensors

D1.1	Several MPW1.1 submissions in the identified technology processes (TJ/TSI 180 nm, LF 110/150 nm and IHP 130 nm in 2024, and TJ 65 nm in 2025)
D1.2	Several MPW1.2 submissions in the identified technology processes (TJ/TSI 180 nm, LF 110/150 nm and IHP 130 nm in 2026, and TJ 65 nm in 2027)

HV-CMOS Pixel Detector Demonstrator with Serial Powering and Innovative Interconnections

3rd DRD3 Week on Solid State Detectors R&D
Amsterdam, 2-6 June 2025

Attilio Andreazza

Yanyan Gao

Università di Milano and INFN

University of Edinburgh

CCF Project Proposal by

Birmingham, Bristol, Edinburgh, FBK, Heidelberg, Hochschule RheinMain, IHEP,
KIT, Lancaster, Milano, Pisa, Torino, Trento

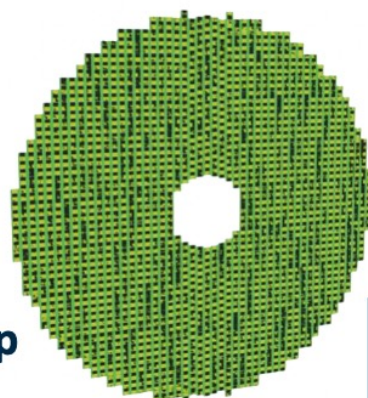
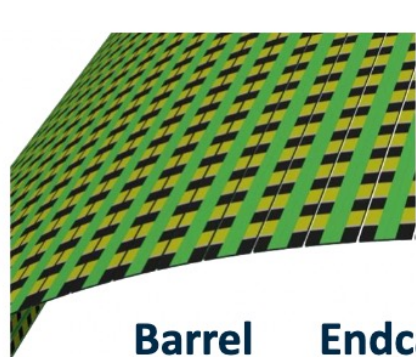
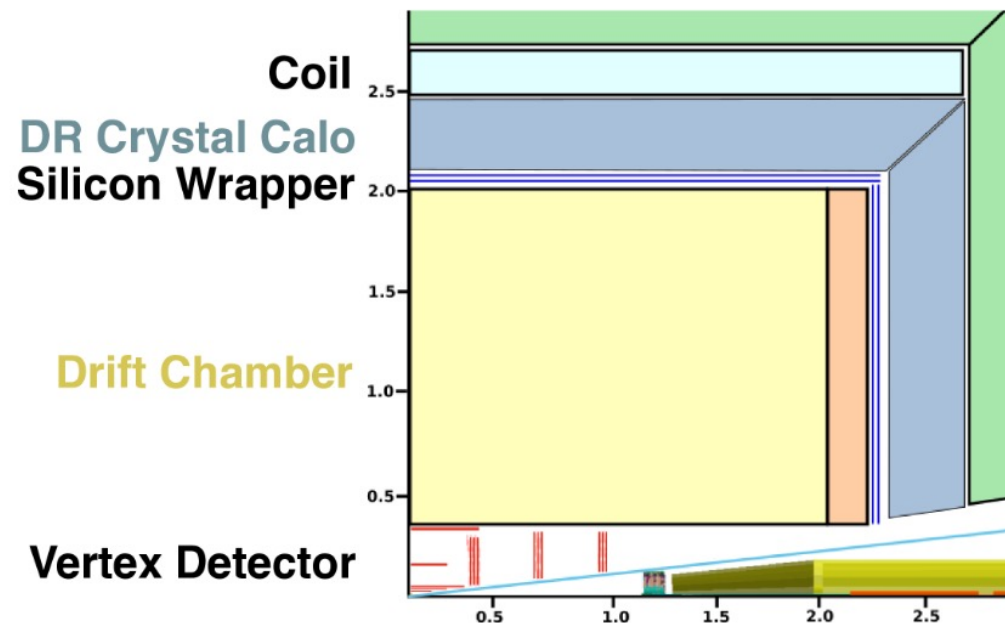


UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

Project proposal

- This proposal aims to develop a **large area HV-CMOS pixel detector demonstrator** for large-scale production in **future Higgs factory** experiments, based on **multi-chip modules** with **data aggregation** and **serial powering**.
- These multi-chip modules, including **low-mass multilayer flexible PCBs**, will then be integrated in staves, where modules will be powered in serial mode utilising the on-chip Shunt Low Drop Out (SDLO) regulators. Together with data aggregation, this will substantially **reduce the number of stave data and power connections**.
- **Low-mass aluminium flex productions**, innovative connection methods (e.g. single-point Tape Automated Bonding), **low-mass mechanical support**, and **efficient cooling technologies** will be explored for overall system optimization in power and material budget.
- *The expertise gained by the participating institutes will be beneficial for the integration of future full-size devices that will be developed by the strategic DRD3 projects in the next few years*

Project motivation: Higgs Factories

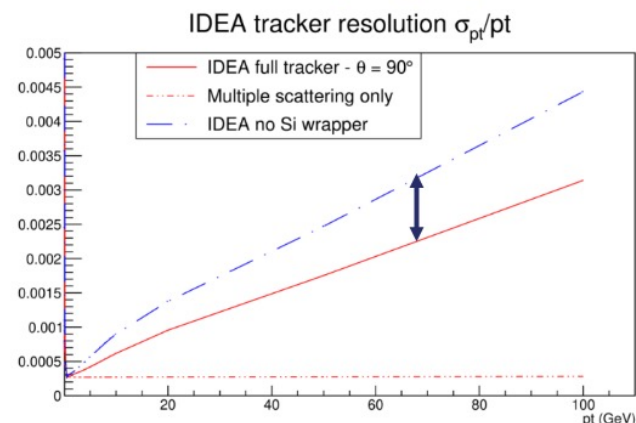


The IDEA detector
concept for FCC-ee
[arXiv:2502.21223](https://arxiv.org/abs/2502.21223)

Silicon tracking in different regions

(IDEA concept shown here, but general considerations are valid for all layouts)

- **inner vertex detector ($R=1.4-3.3$ cm)**
 - 3-5 μm resolution, $O(200 \text{ MHz}/\text{cm}^2)$, very low material
- **outer vertex detector ($R=13-31$ cm)**
 - $\sim 7 \mu\text{m}$ resolution, 27 ns timestamp, $O(40 \text{ kHz}/\text{cm}^2)$
 - material is a concern
- **silicon wrapper/TOF ($R/z = 200$ cm)**
 - $\sim 7 \mu\text{m}$ resolution, 27 ns timestamp
 - **100 m² (2 layers): $\sim 2.5 \cdot 10^5$ chips, ~ 100 kW power**



Conclusions

- Future experiments will need to develop large tracking systems with **low-mass services** (both electrical and thermal) and **efficient power distribution and data handling**
- In particular there is an increase in interest in the deployment of **Aluminum conductor flexible PCB**
- This *Common Project* aims to gather groups already addressing this topic in different experiments
 - timescale for some experiments is not far away
 - prototyping solutions for system issues in parallel to sensor development
 - share information about AI flexible PCB vendors
 - stimulate the development of IP implementing features for system level integration also in the developing projects within DRD3-WP1
 - cost benefit from synergies with already running projects

Novel energy-sensitive x-ray cameras, record fusion-plasmas, real-time monitoring and the need of radiation-hardened detectors

L. F. Delgado-Aparicio¹, T. Barbui¹, R. Barnsley², D. Vezinet³, R. Dumont⁴, N. Fedorczak⁴, J. Morales⁴, T. Fongueti⁴, P. Manas⁴, S. Mazzi⁴, X. Litaduon⁴, F. Imbeaux⁴, K. Hill¹, M. Bitter¹, N. Pablant¹, J. Wisniewski¹, B. Luethi⁵, M. Rissi⁵, T. Donath⁵, L. Glatt⁵, P. Hofer⁵, and N. Pilet⁵

¹ Princeton Plasma Physics Laboratory, Princeton, NJ, USA

² ITER Organization, Saint-Paul-les-Durance Cedex, France

³ Commonwealth Fusion Systems, Devens, MA, USA

⁴ CEA, IRFM, Saint-Paul-les-Durance Cedex, France

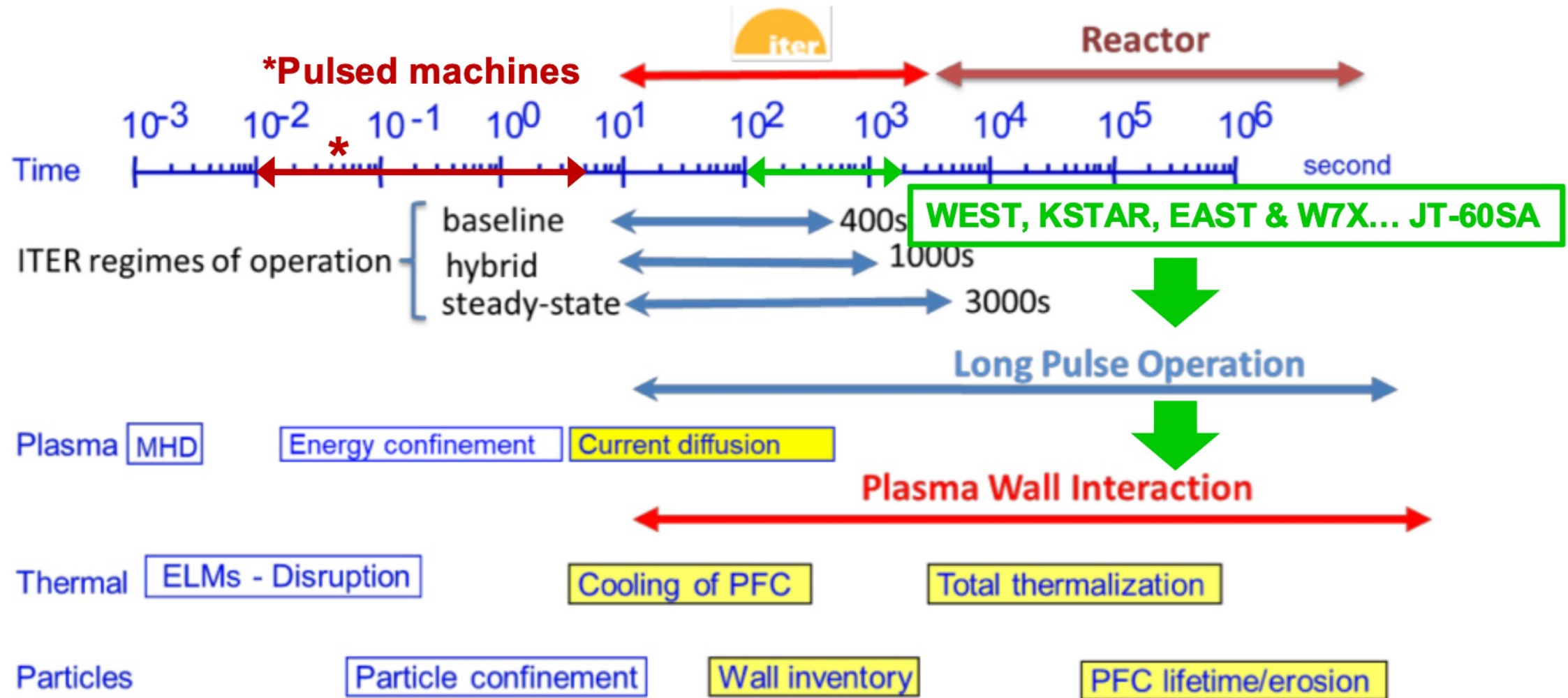
⁵ DECTRIS Ltd., 5405 Baden-Dattwil, Switzerland

DRD3

Amsterdam, Netherlands

Tuesday, June 3rd, 2025

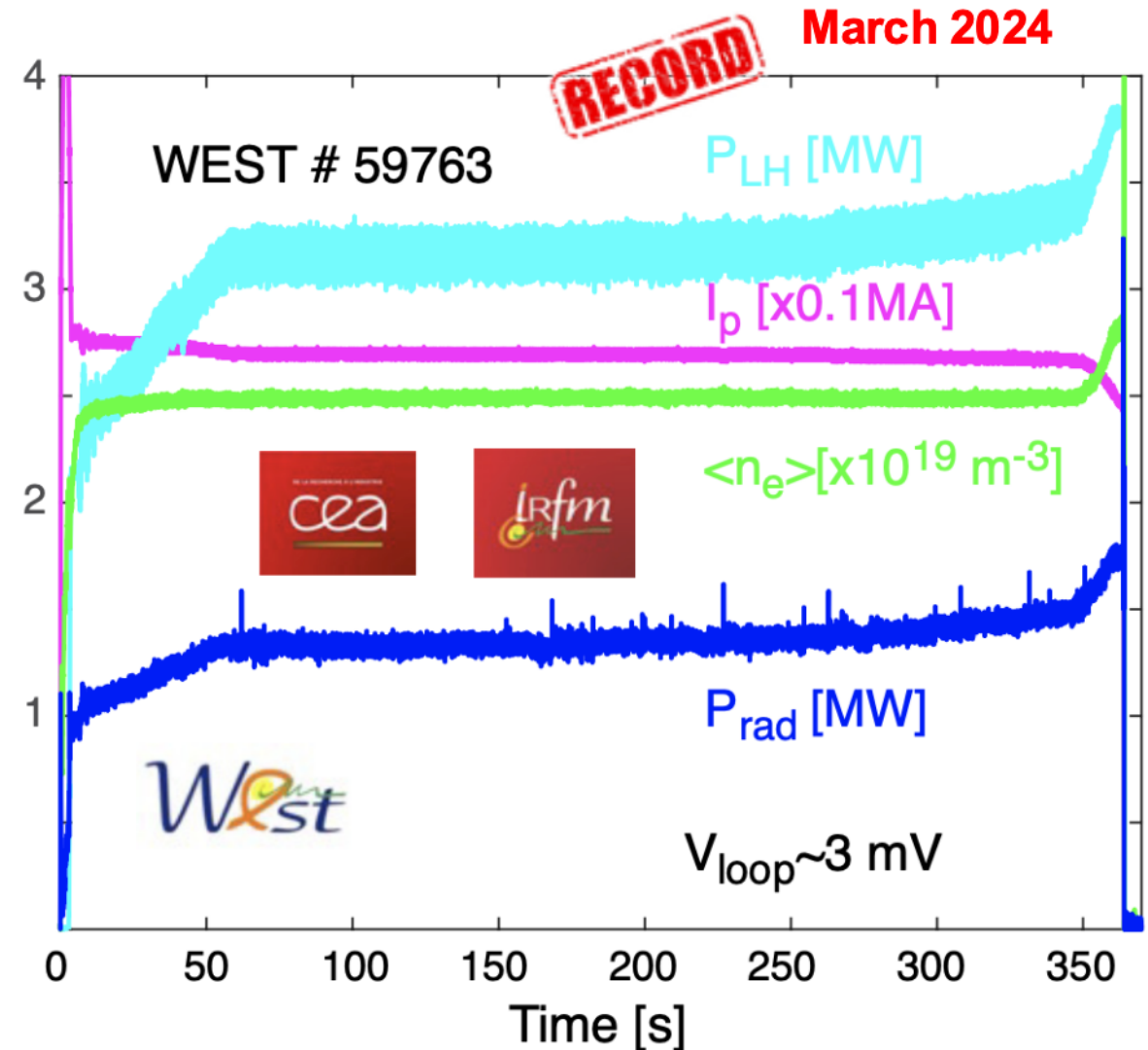
Long pulse operations (LPO) open a new era of expertise, training (e.g. physics and engineer) & collaborations



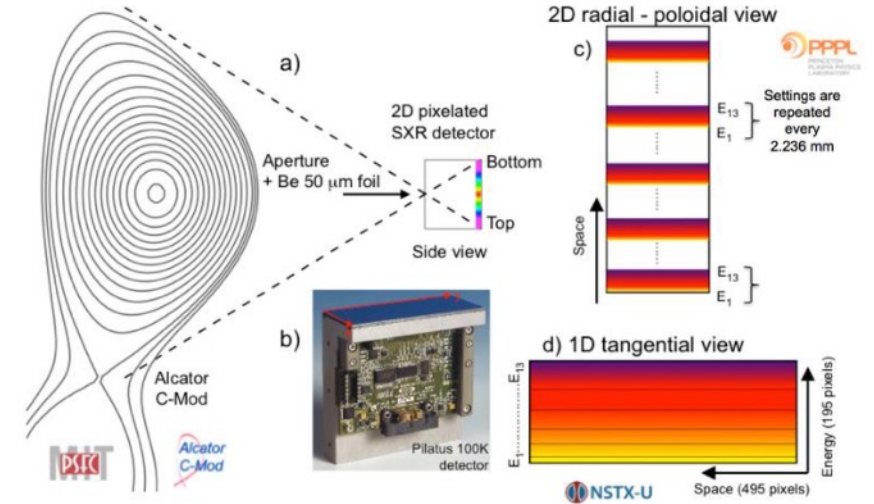
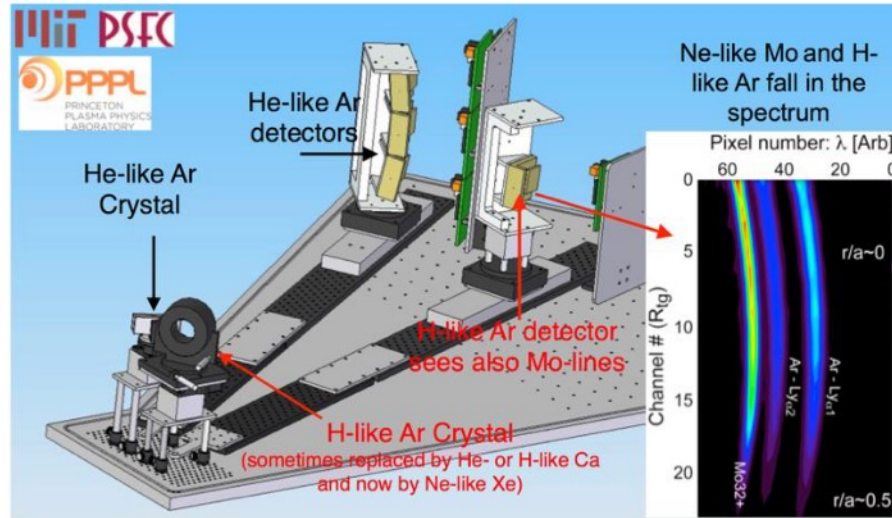
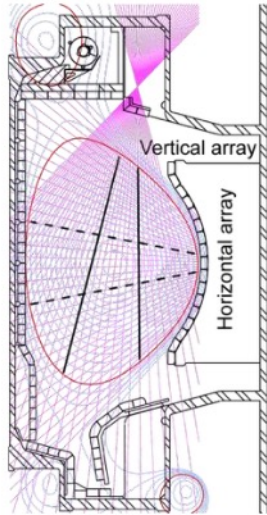
Long pulse operations (LPO) open a new era of expertise, training (e.g. physics and engineer) & collaborations

Long pulse operation (LPO) redefines all our diagnostic timescales over eight-nine orders of magnitude

- $\times(10^8-10^9)$
- $\tau_{\text{MHD}} \sim 1 - 100 \mu\text{s}$
 - $\tau_{\text{ELM}} \lesssim 1 \text{ ms}$
 - $\tau_{\text{UFO}} \sim 20\text{-}50 \text{ ms}$
 - $\tau_{\text{Transport}} \sim 1\text{-}20 \text{ ms}$
 - $\tau_{\text{E}} \sim 50\text{-}70 \text{ ms}$
 - $\tau_{\text{Ex:e,i}} \sim 250 \text{ ms}$
 - $\tau_{\text{Ip}} \sim 100 \text{ s}$
 - $\tau_{\text{PMI}} \sim 100\text{'s s}$



Summary



- ① With the selection of W for modern machines, understanding the sources, transport and confinement of high-Z impurities is crucial to SPARC and ITER success.
- ② $P_{\text{rad}} \gtrsim \frac{1}{2} P_{\text{input}}$ and $P_{\text{rad,X}} \lesssim 90\% P_{\text{rad}}$
- ③ Modern x-ray diagnostics help us probe: n_Z , $T_{e,i}$, $V_{\phi,\theta}$, Z_{eff} & $n_{e,\text{fast}}$ and their profiles!
- ④ Urgent need of rad-hardened sensors (e.g. UV as well as soft & hard x-rays) !!!
- ⑤ Need better neutron monitors for DD and DT (2.5 vs 14.1 MeV): flux and spectra!!!
- ⑥ Now we have a private sector !!!

WG2/WP2 - Hybrid Silicon Technologies

WG6/WP3 - Non-silicon-based detectors

