R&D for KLM upgrade

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51st B2GM KLM Parrel Session

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Outline

- Last B2GM:
  - Development of MPT2321 back-end system:
    - 1. Development of test system

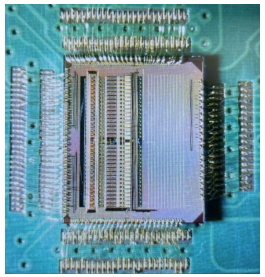
- This B2GM:
  - Test of MPT2321 back-end system:
    - 1. Single photon spectrum
    - 2. Signal to noise ratio
    - 3. TDC performance
    - 4. Power consumption

Motivation

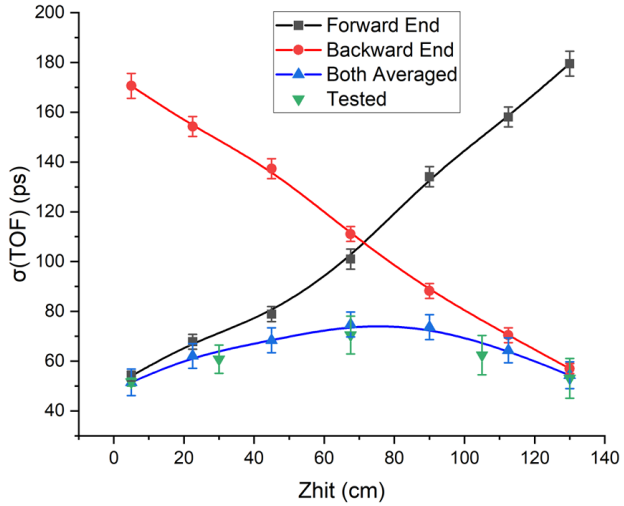
- Front end test results
  - 1. Time resolution of 1.35m-long GNKD scintillators is less than 70 ps.
  - 2. Time resolution of new 50cm-long GNKD scintillators is about 45 ps.
- The development of front end is almost done.

Back end electronics is needed !!!

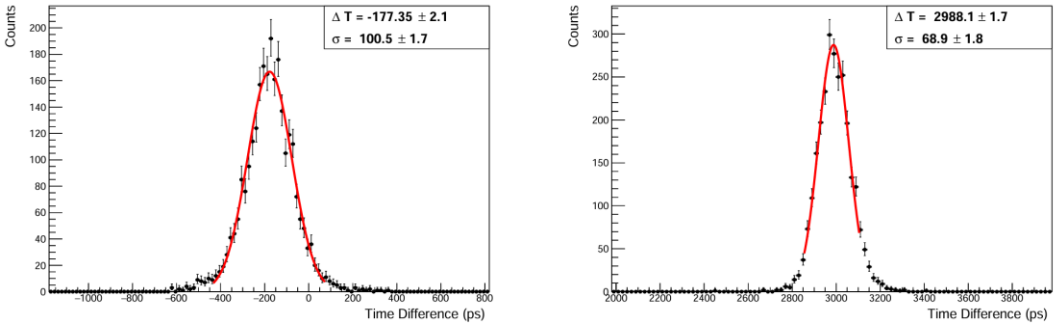
- The development of Back-end electronics system based on MPT2321 chip is progressing.



MPT2321 chip



Time resolution as a function of scintillator position



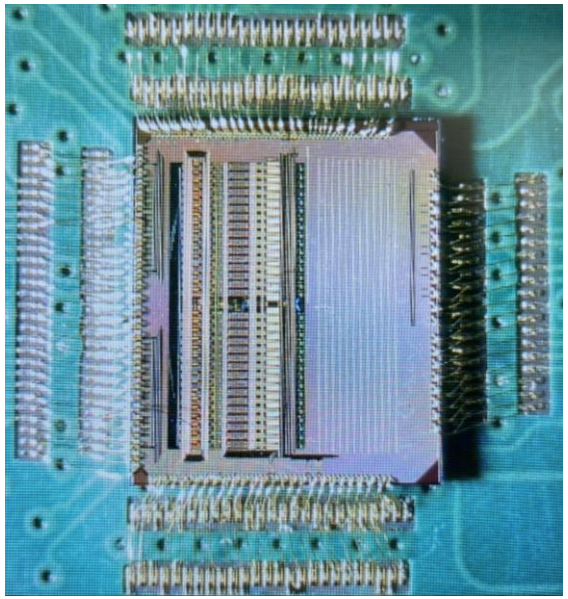
GNKD_4 scintillator's central position time resolution test using dual-end read out scheme

Introduction of MPT2321 chip

The MPT2321 chip is a SiPM signal processing SoC chip designed for high-precision time-of-flight signal processing.

Features

- 32 input channels
- Automatically select the range of measurement signals
- 50ps precision 20-bit TDC
- 12bit ADC
- Complete on-chip signal processing
- Standard IIC Bus Control
- 8b10b encoding transmission
- Multichannel LVDS data transmission
- 12 Mcps transmission event rate
- High integration, low power consumption
- 200M data transmission rate
- The maximum charge measurement dynamic range is 2.4 nC
- Minimum detectable signal range 4fC

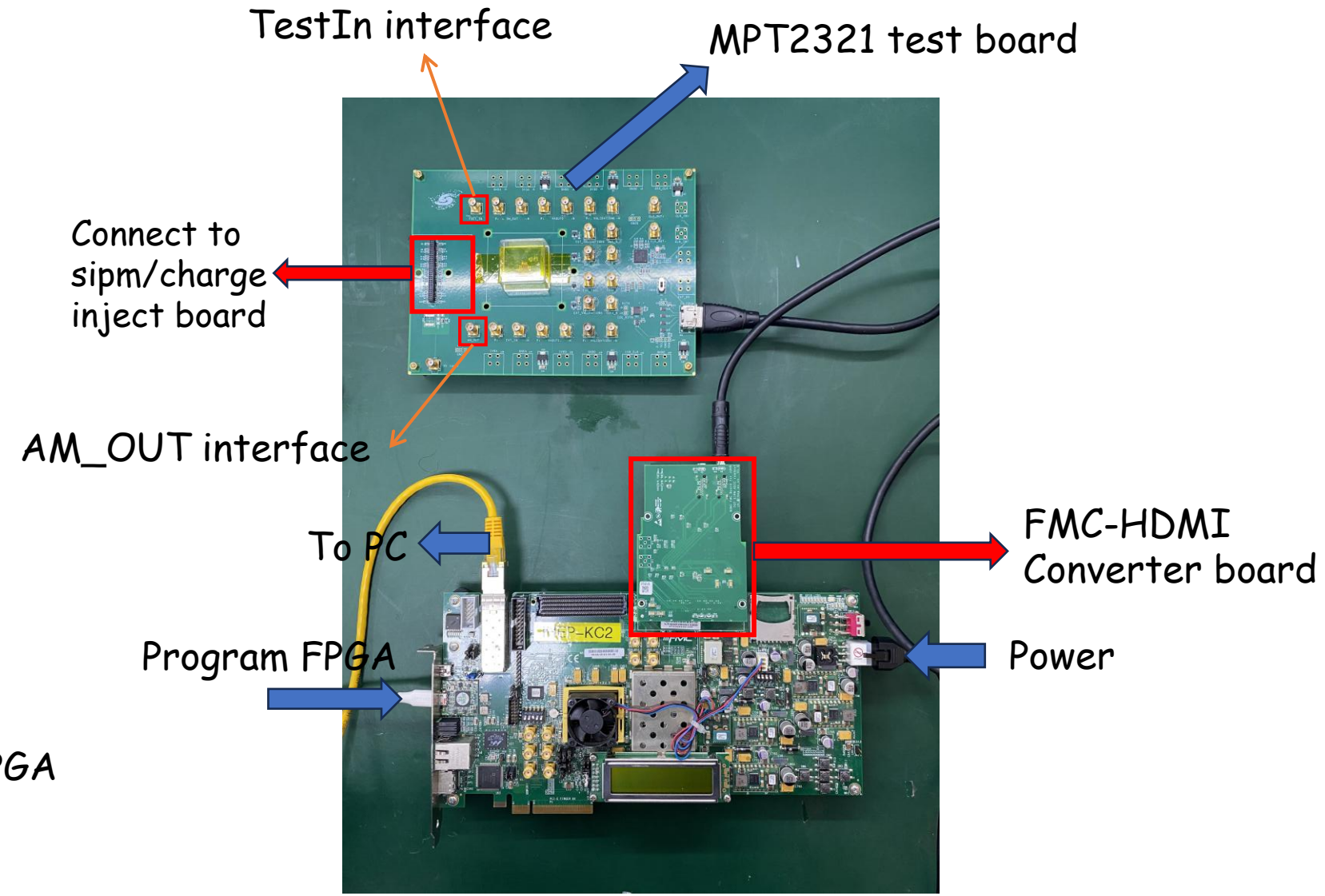


MPT2321 chip

宇称电子 MICROPARITY Sensor and Science

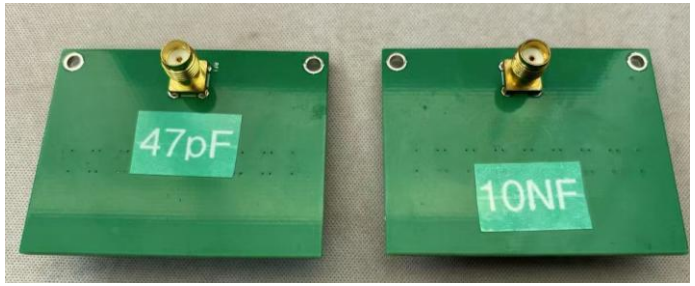
Setup of test system

- FPGA Board: KC705 of Xilinx
- Signal input to MPT2321
  - Female Header
  - TestIn interface
- MPT2321 to FPGA
  - HDMI
  - FMC-HDMI Converter
- FPGA to PC
  - RJ45-SFP converter
  - USB-JTAG to program FPGA

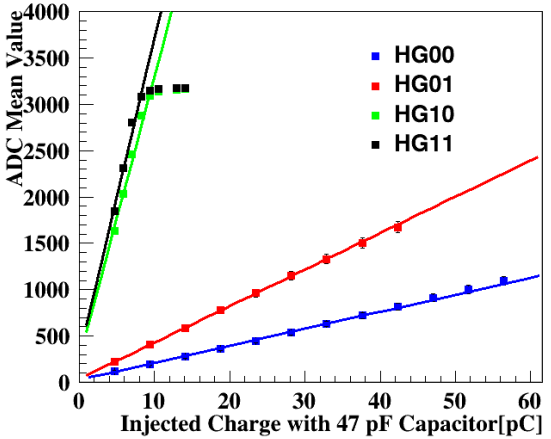


Test Results - Charge inject linearity

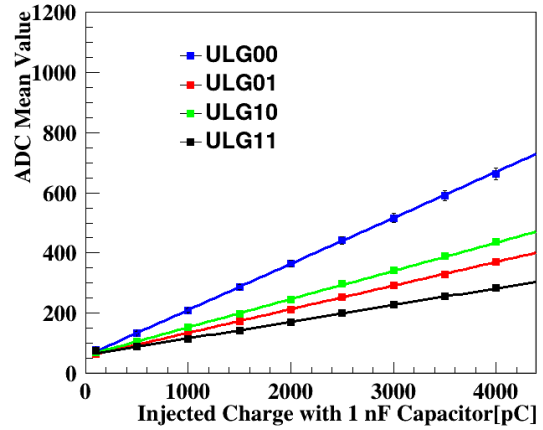
- Measurement Method
  - Inject Pulse through Charge inject board
- Injected Charge: $Q = \Delta V \times C$
- Capacitor of Charge inject board
  - High-Gain mode: 47pF
  - Low-Gain mode: 1nF



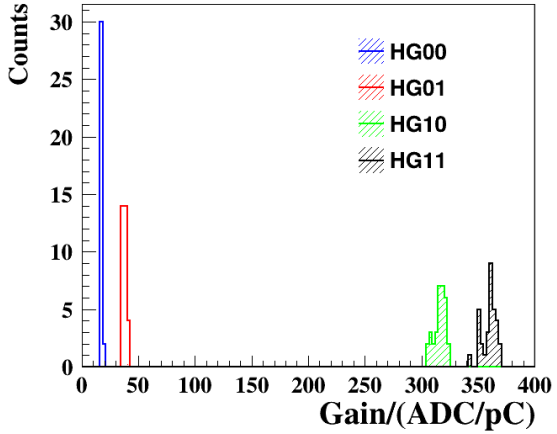
Charge Injection board



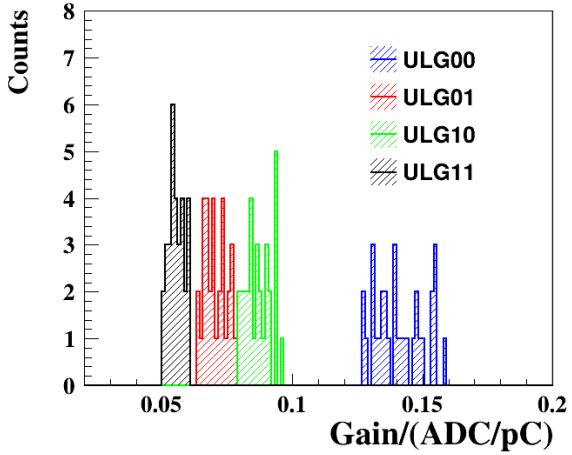
High-Gain mode



Low-Gain mode



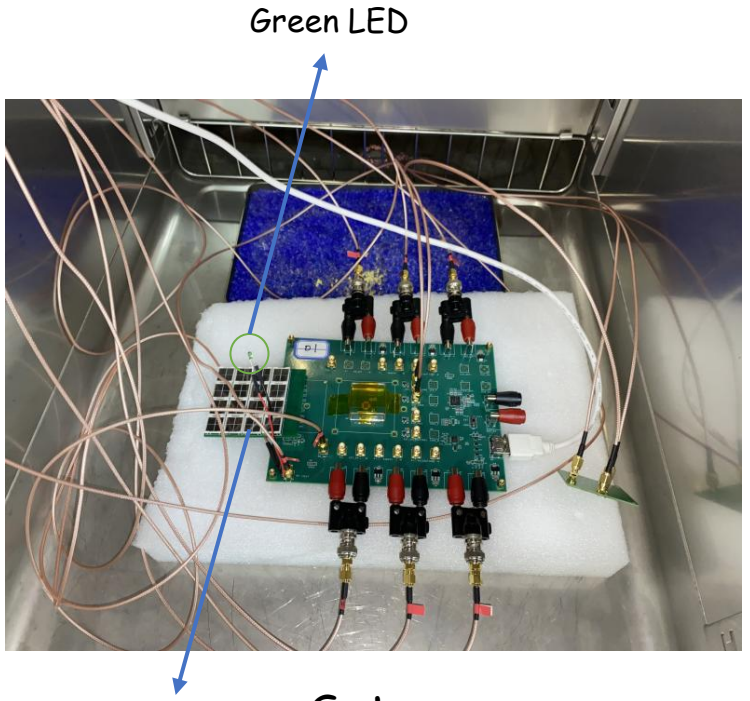
High-Gain mode



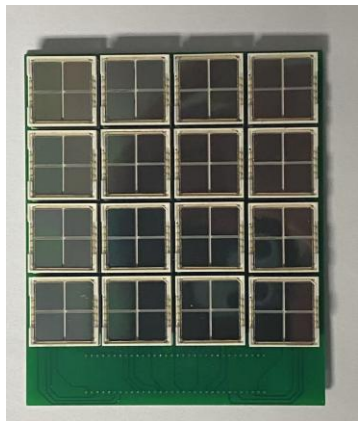
Low-Gain mode

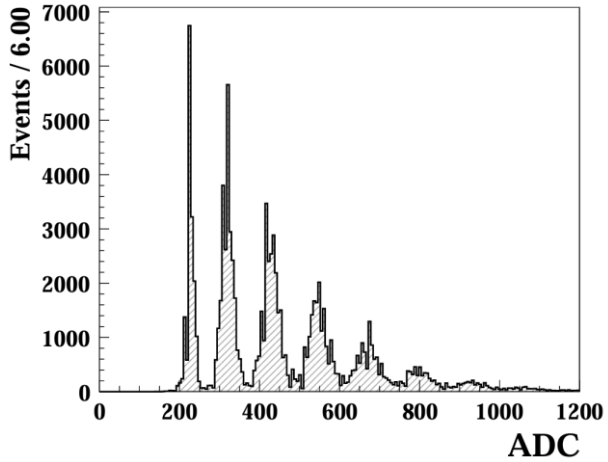
Test Results - Charge spectrum

- SiPM type: S13371-6050CQ-02
- Measurement Method
  - Green LED drove by pulse signal
  - Pulse signal
    - Width: 10 ns
    - Amplitude: 1.070 V
  - Using external trigger mode
    - Same frequency with LED driver pulse

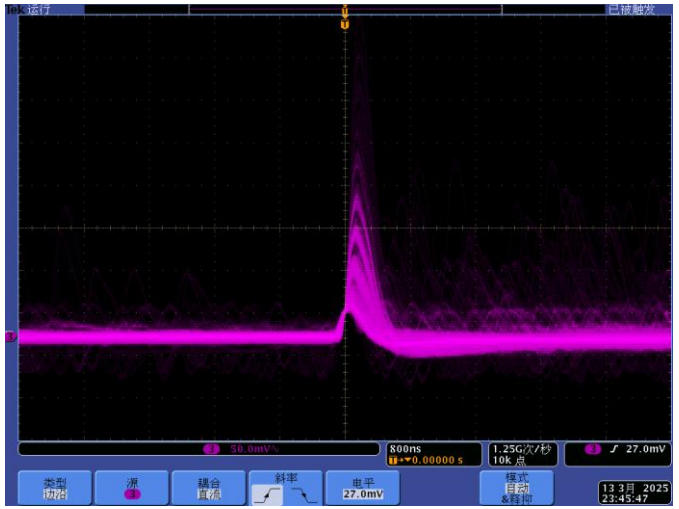


Setup





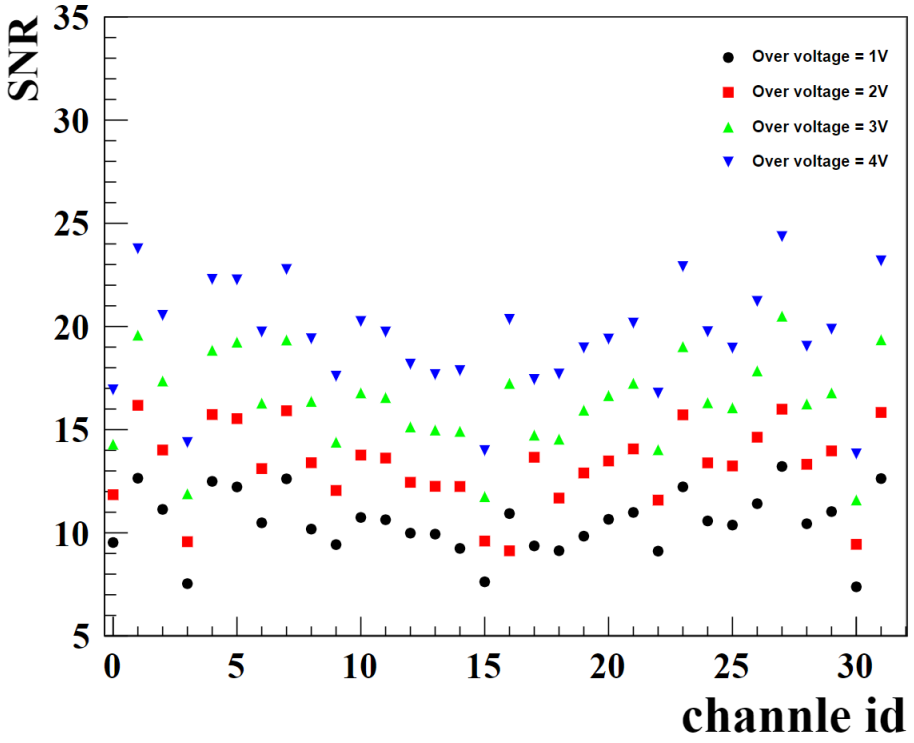
Charge spectrum of one channel



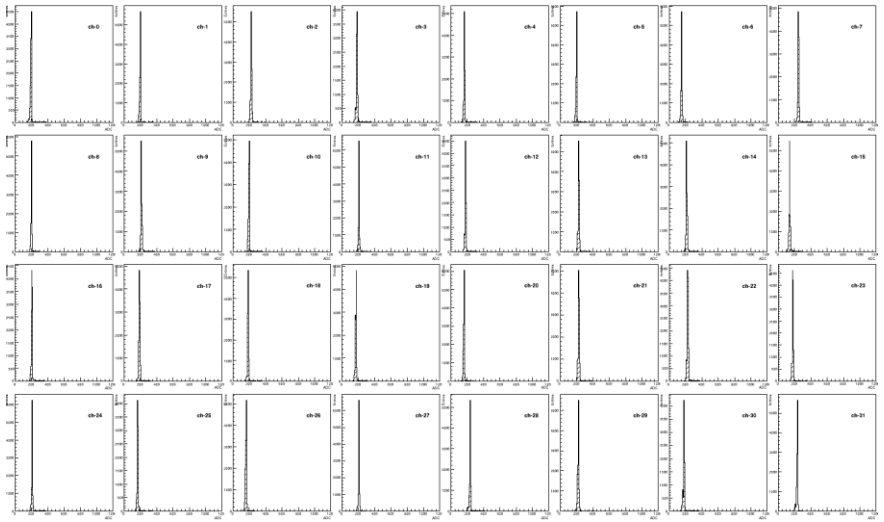
Waveform from AM_OUT

Test Results - Signal-to-noise ratio (SNR)

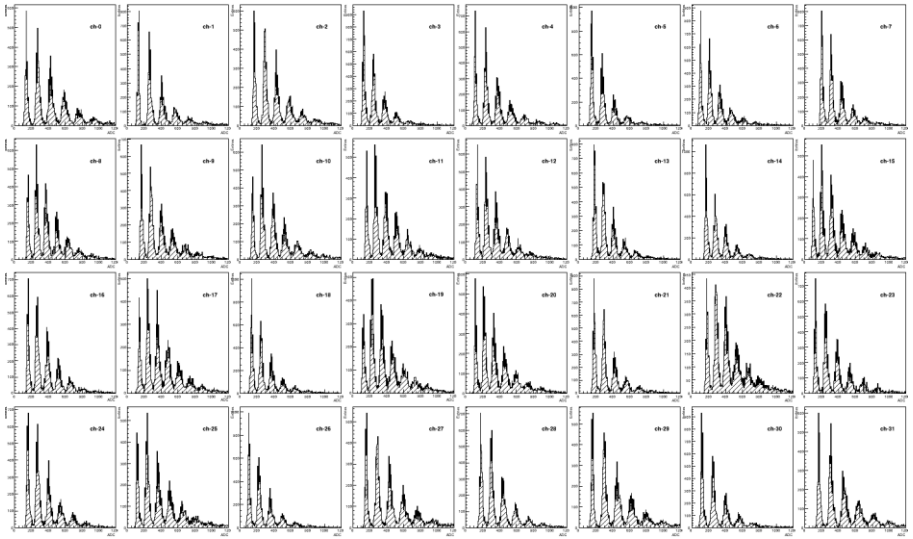
- Signal-to-noise ratio
  - Ratio of the gain and the standard deviation of the pedestal



SNR of each channel



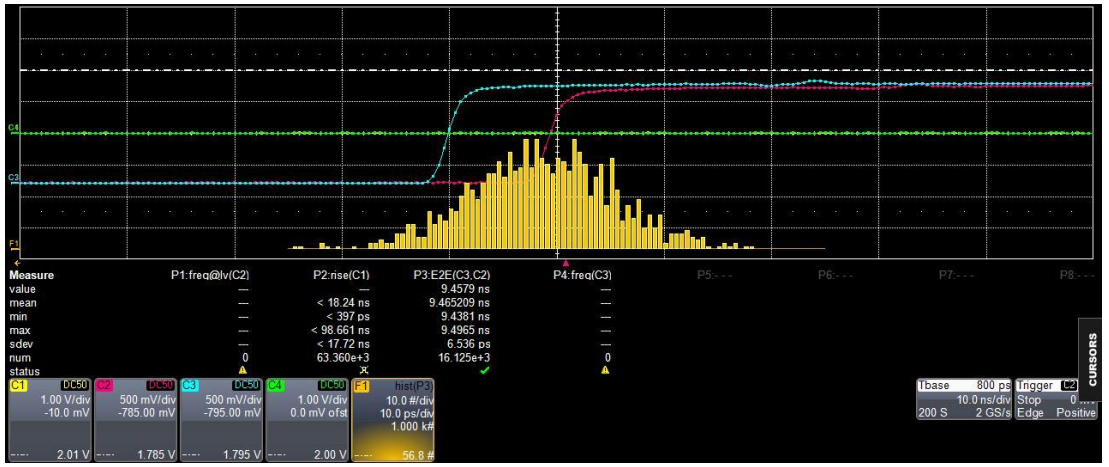
Distribution of pedestal of each channel



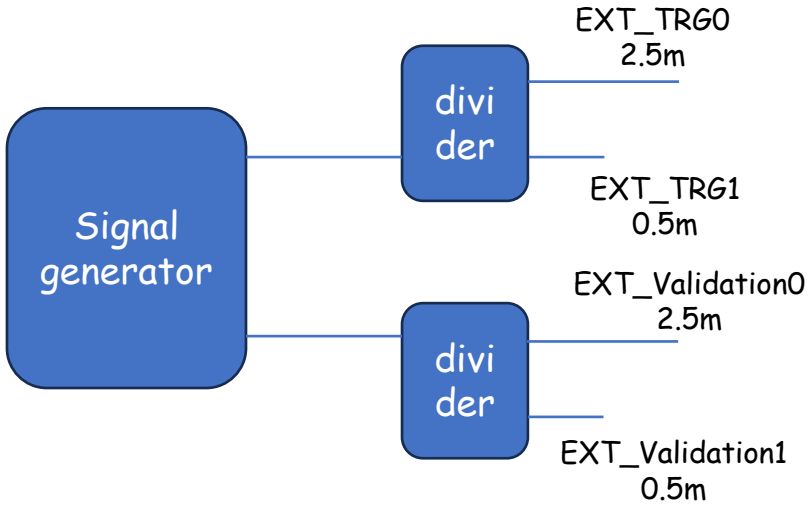
Charge spectrum of each channel

Test Results - TDC performance

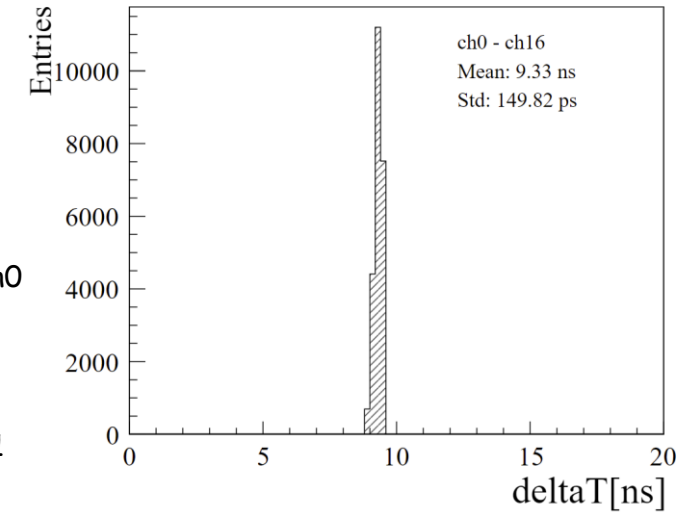
- Cable delay method
  - The difference of the length of two cable is 2m
  - Time difference
    - oscilloscope: 9.47 ns
    - MPT2321: 9.33 ns
- Time resolution: ~150 ps
- Frequency of TDC clock: 80MHz



Cable delay measured by oscilloscope



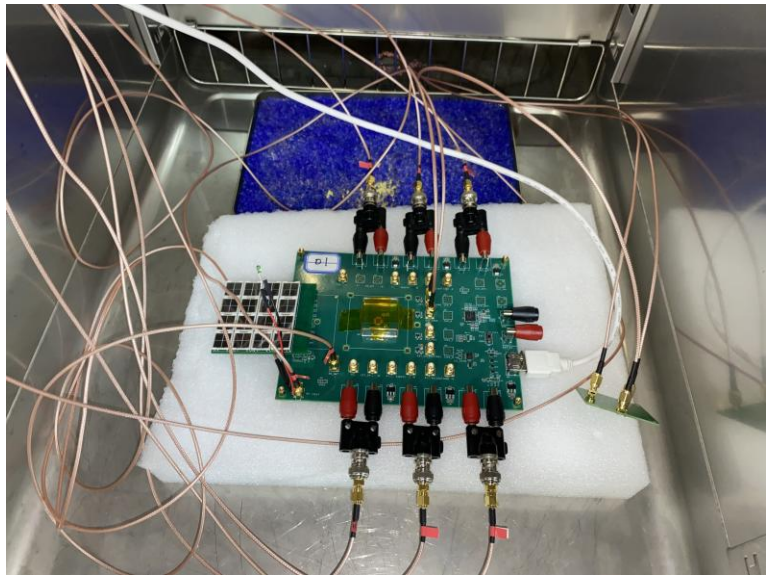
Setup



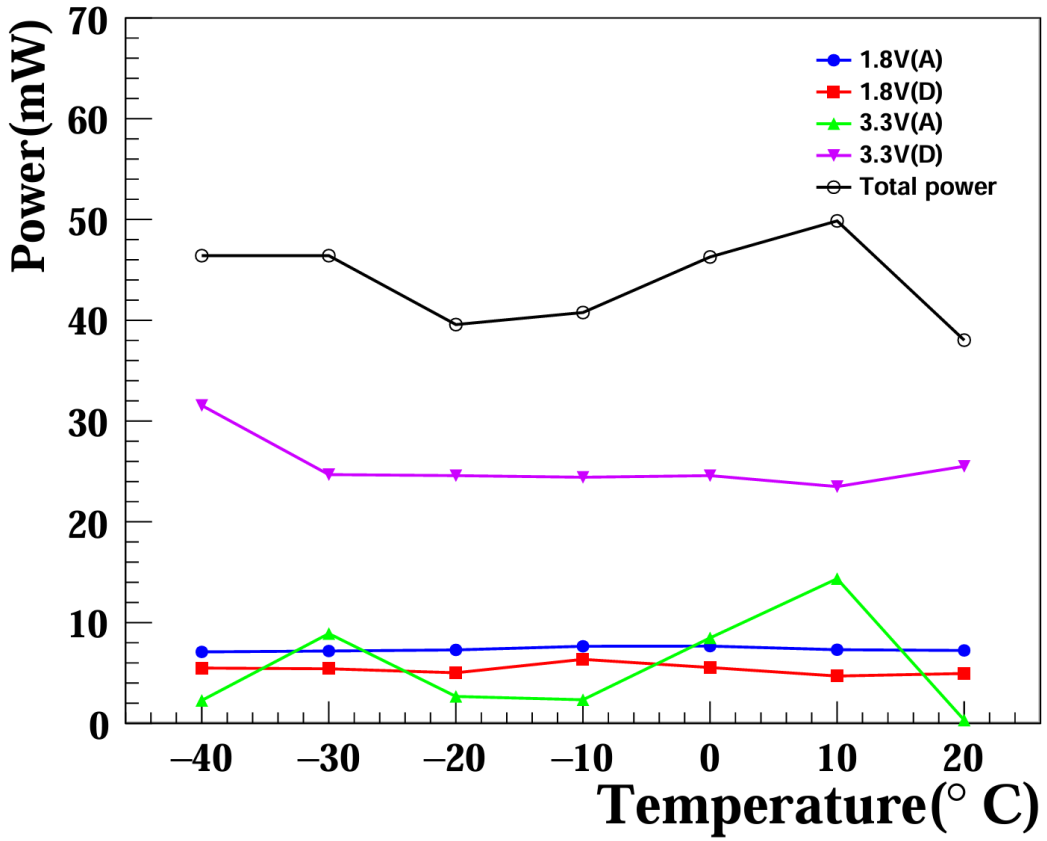
Cable delay measured by MPT2321

Test Results - Power consumption

- Measurement method
  - The board is set in a thermostat
  - Monitor the current of power supply interface
- The Power consumption is stable at -40 ℃ ~ 20 ℃



Setup



Power consumption vs Temperature

Summary & Plan

Summary:

- ✓ Test of Basic performance of MPT2321
  - ✓ Charge inject linearity
  - ✓ Charge spectrum
  - ✓ Signal to noise ratio
  - ✓ Power consumption

Plan:

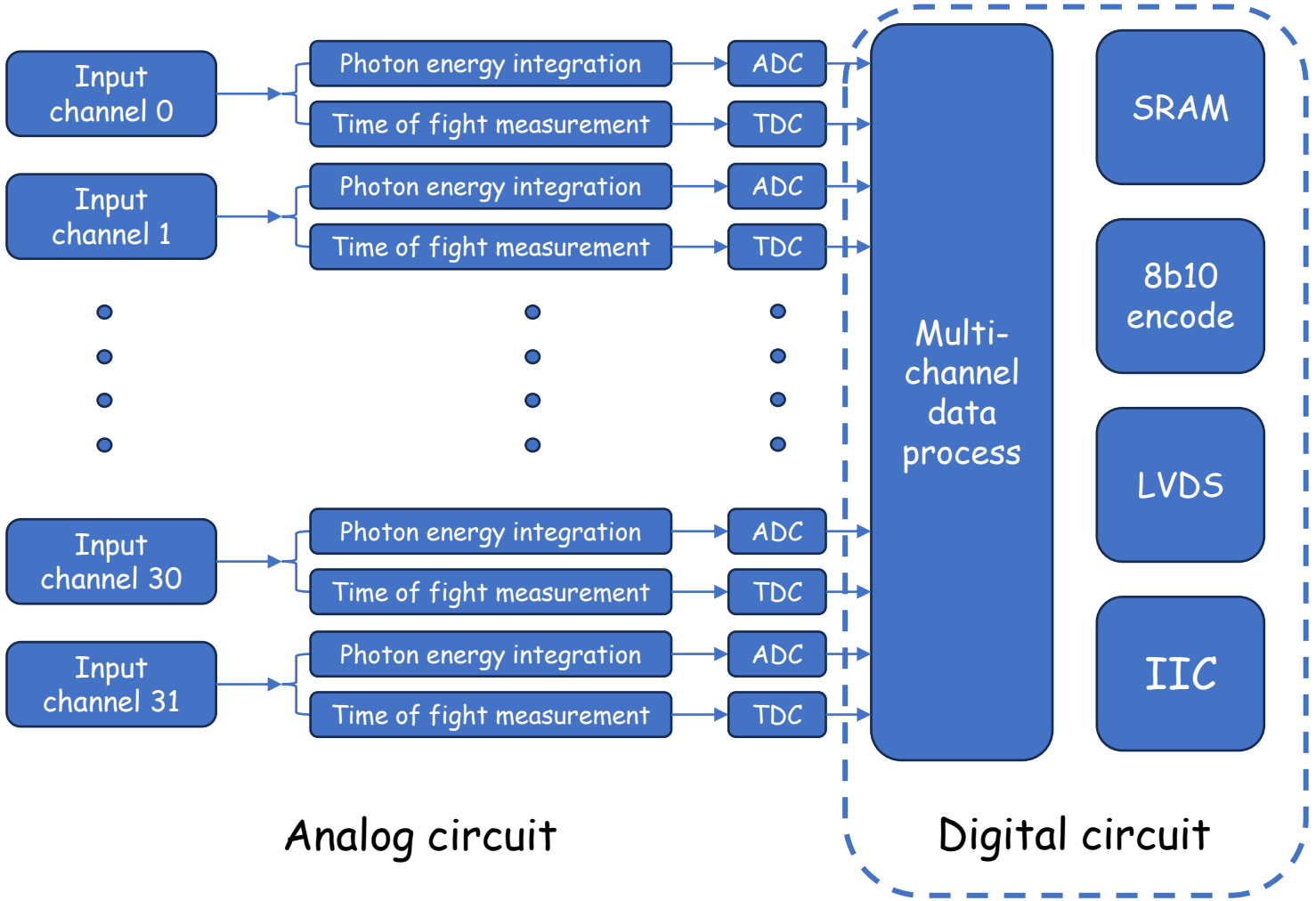
- ☐ Fix known bug of firmware (decode module)
- ☐ Develop trigger logic

Thanks for your attention!!!

Backup

Structure of MPT2321 chip

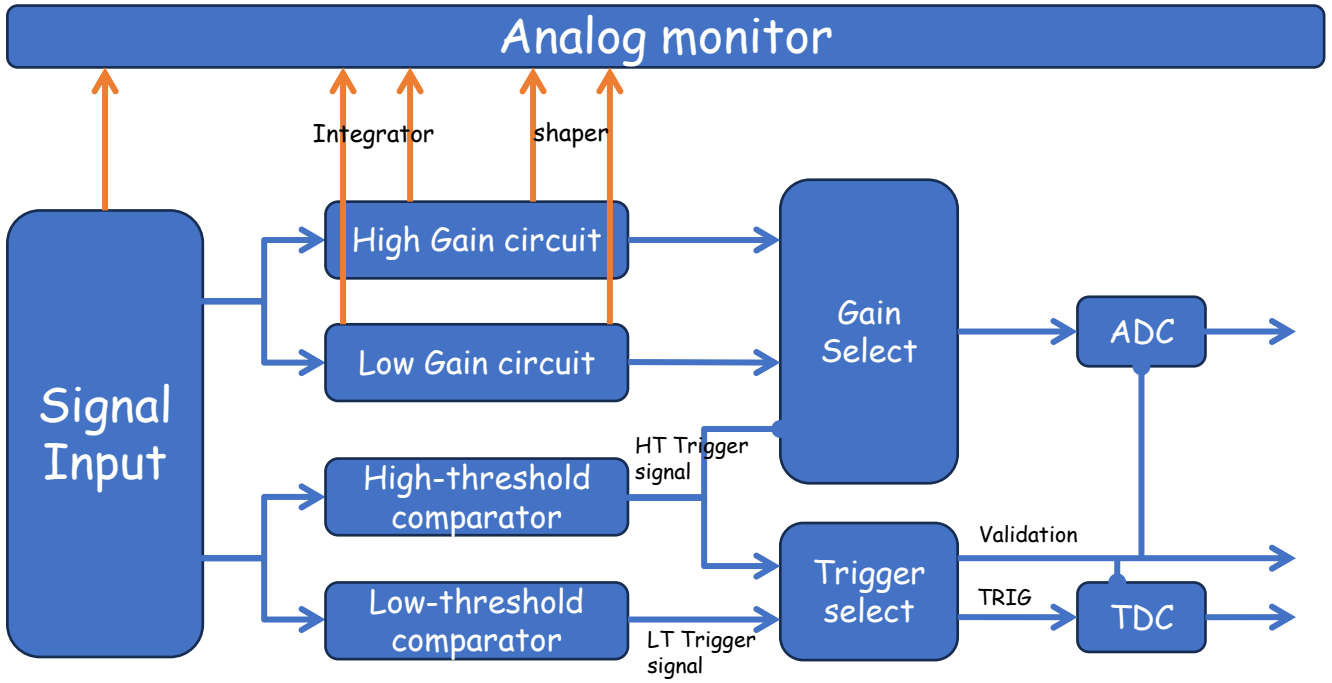
- Analog circuit
  - 12bits ADC module
  - 50ps precision TDC
- Digital circuit
  - Control of chip status
  - Data processing, compression and output



Signal process procedure of MPT2321

Analog signal process

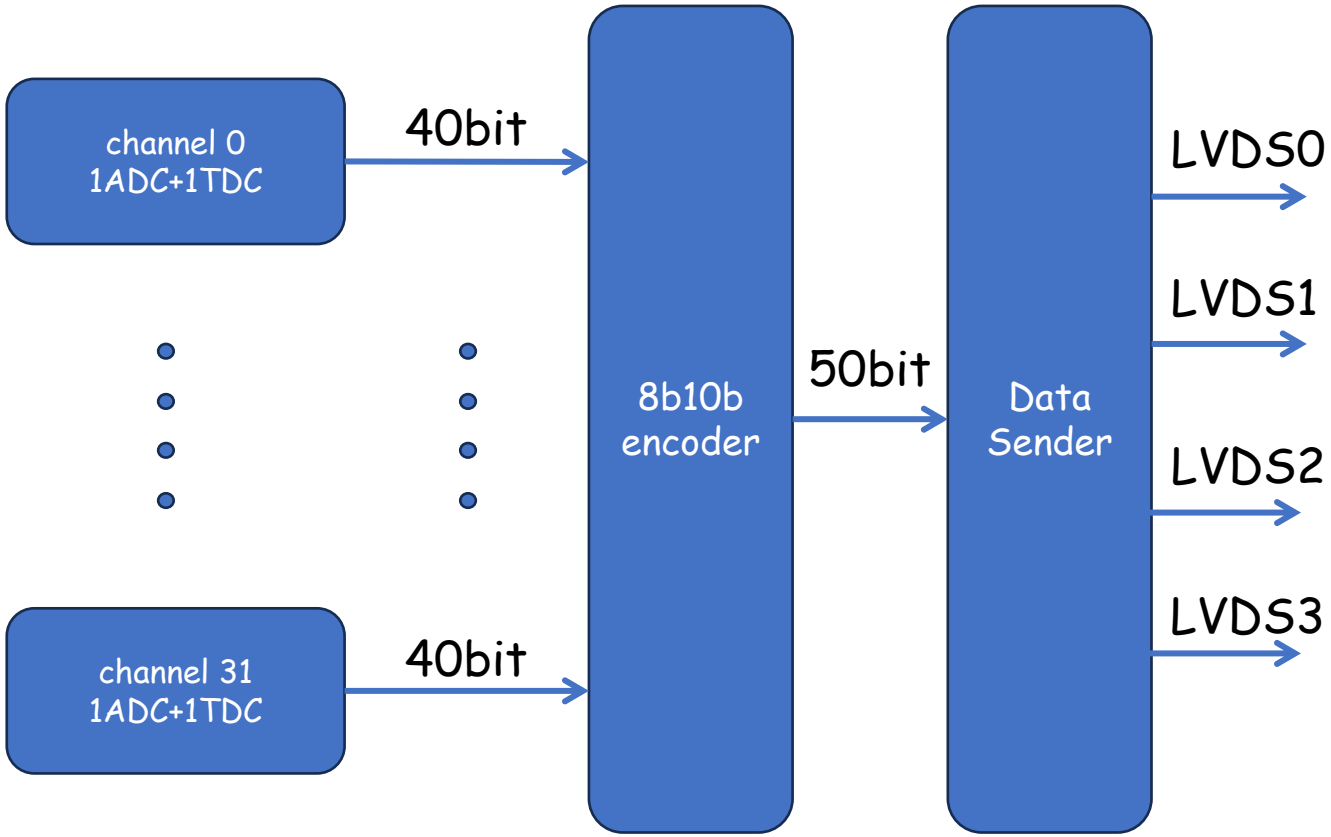
- Two Gain circuit
  - Four mode for high gain
  - Four mode for low gain
- Two threshold comparator
  - High-threshold comparator determine gain
  - Low-threshold comparator determine arrival time and trigger
- Event validity flag (Validation)
- TDC trigger signal (TRIG)
- Analog monitor (AM)



Signal process procedure of MPT2321

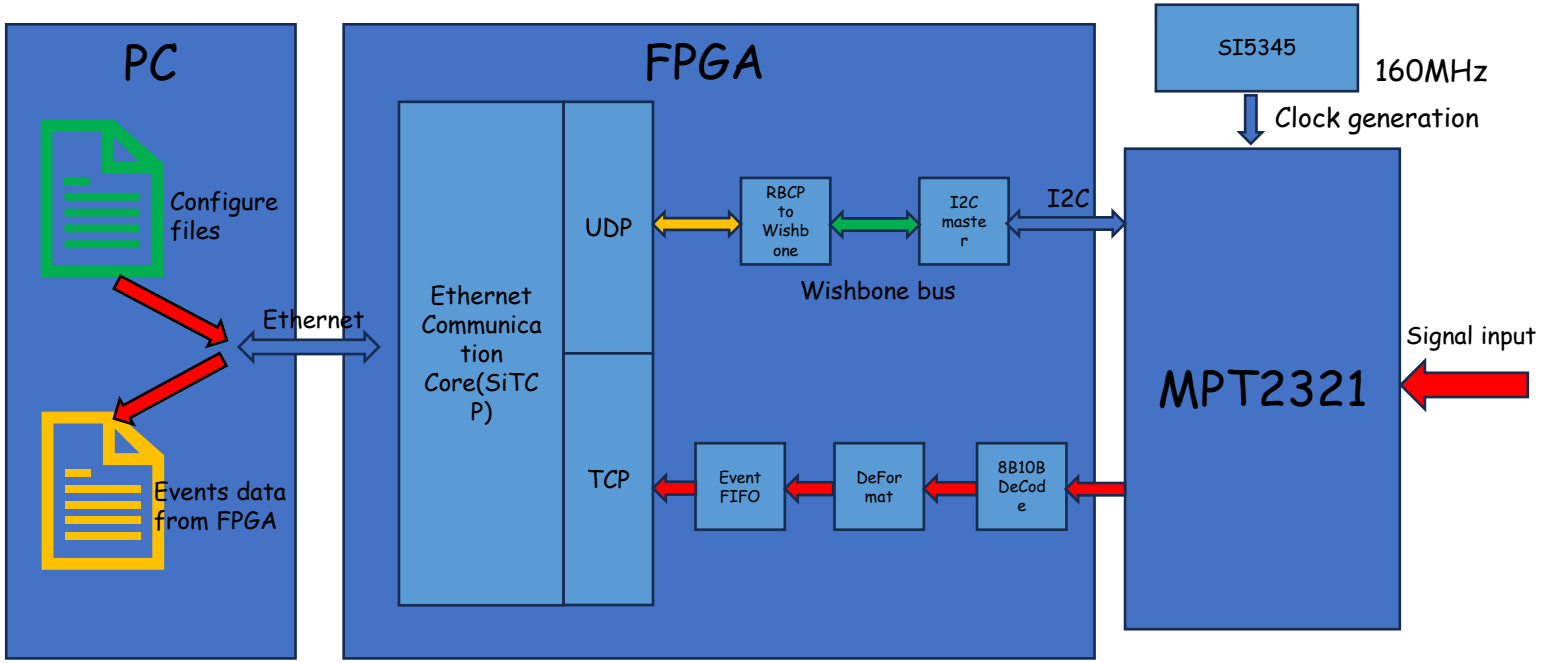
Digital signal process

- ADC and TDC data from each channel
  - 40 bits
- 8b10b encoder
  - 40 bits to 50 bits
- LVDS data transmission
  - Three transmission mode
  - Maximum event rate: ~ 1/(60 Tsys)



Structure of MPT2321 test system

- MPT2321 test board
  - 160 MHz Clock by SI5345
  - Important pin can be monitored through SMA interface
- FPGA
  - Communication Core: SiTCP
  - Configure MPT2321 through UDP
  - Decode, deformat and receive data through TCP
- PC
  - Configure script
  - DAQ script (Multithread)
  - Language: Python



IEEE transactions on nuclear science, 2008, 55(3): 1631-1637.

MPT2321 readout development

Optimization of configure parameter

- 基线调整
  - 调节SH_ped，高增益整形输出基线为300mV左右
  - 调节DIFF_ped，选择后N输出基线为1.7V左右
  - 调节CM_ped，选择后P输出基线为300mV左右
- 扫描最优低阈值
- 扫描hold delay参数
- 自动化脚本进行扫描

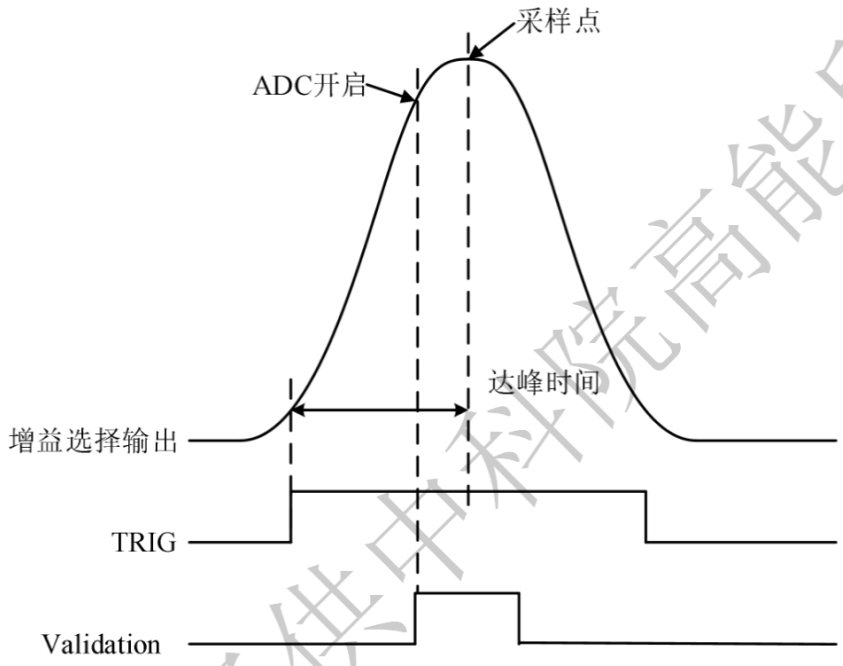
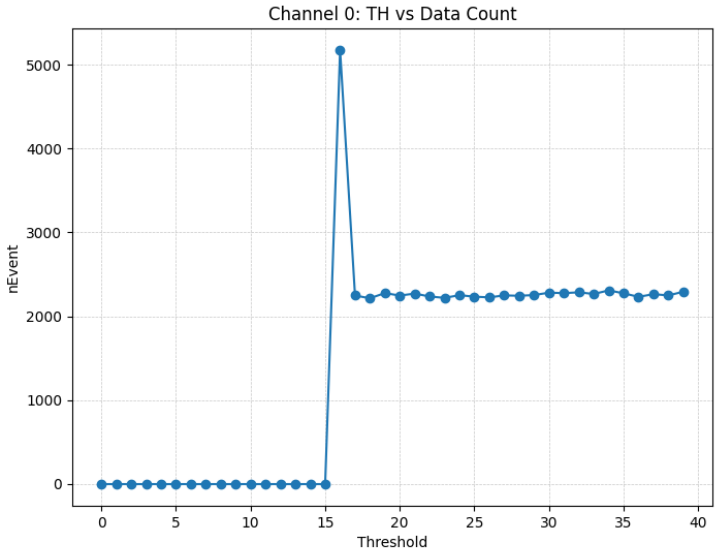


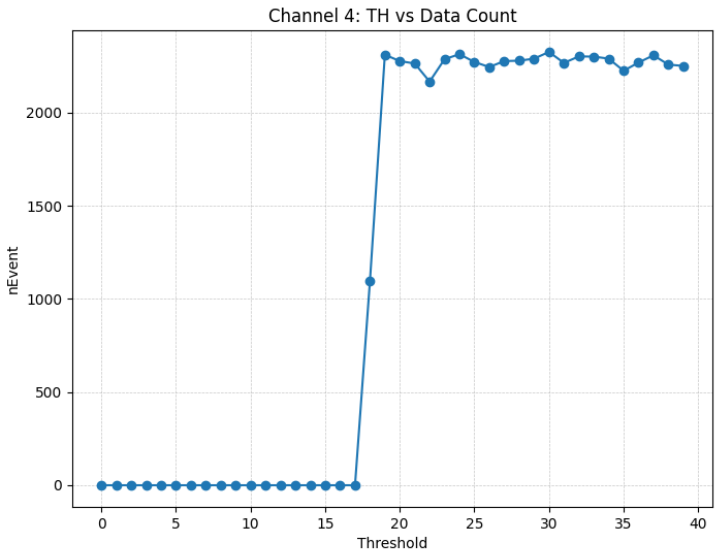
图 2.3 ADC 信号采样示意图

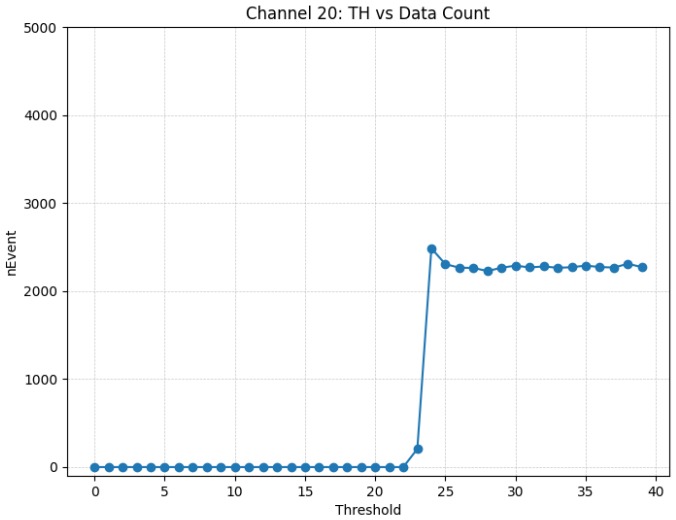
MPT2321 readout development

Optimization of configure parameter

- 低阈值扫描
  - 通过电荷注入板注入信号
  - 逐个通道设置一个阈值
    - 其他通道阈值设为最大
  - 每次采集数据时间固定
    - 注入频率2kHz
    - 采集2s
    - Python脚本中数据解析丢包
  - 采集数据跳变处为基线对应阈值



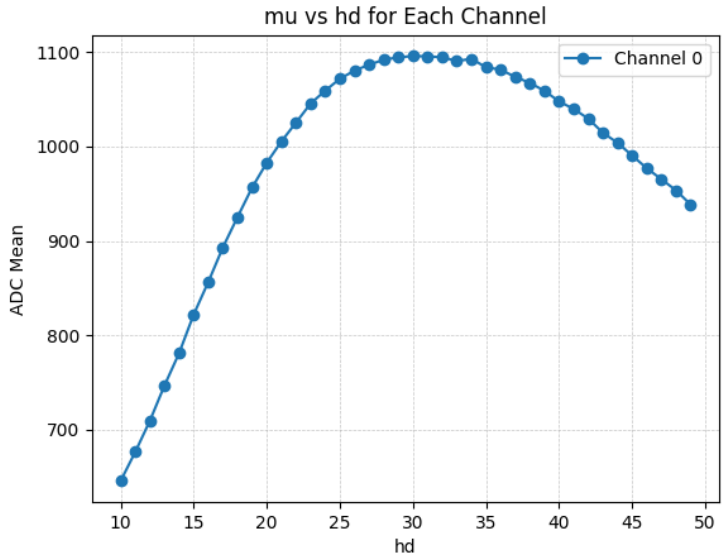




MPT2321 readout development

Optimization of configure parameter

- Hold delay扫描
  - 通过电荷注入板注入信号
  - 逐个打开每个通道
    - 低阈值设定为基线+5
  - 计算每次采集数据的ADC均值



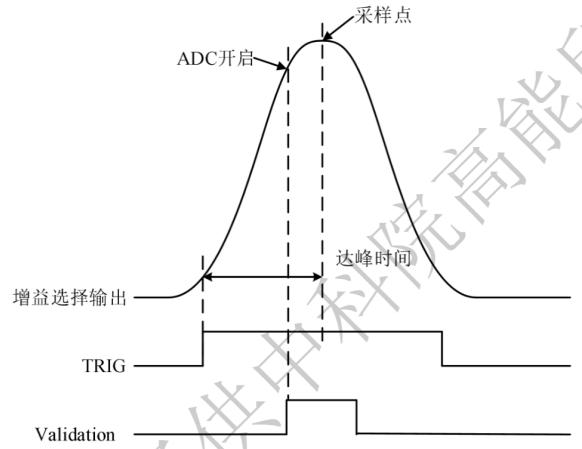
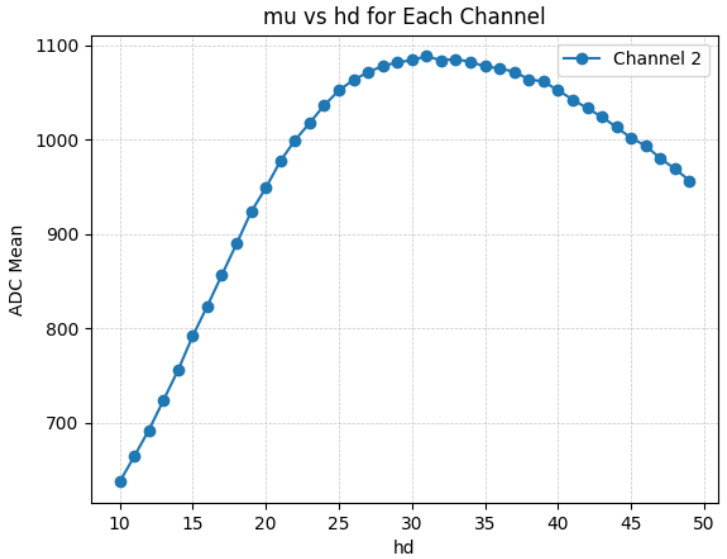
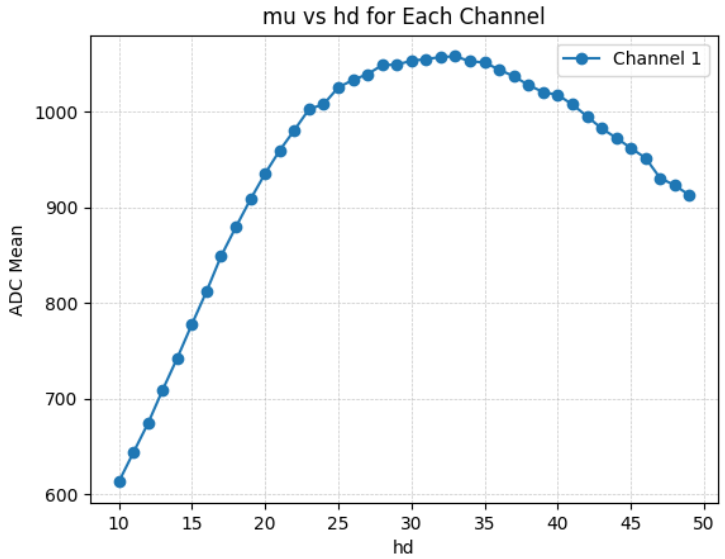


图 2.3 ADC 信号采样示意图

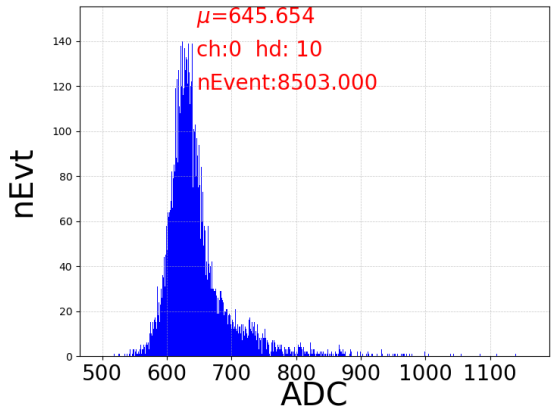


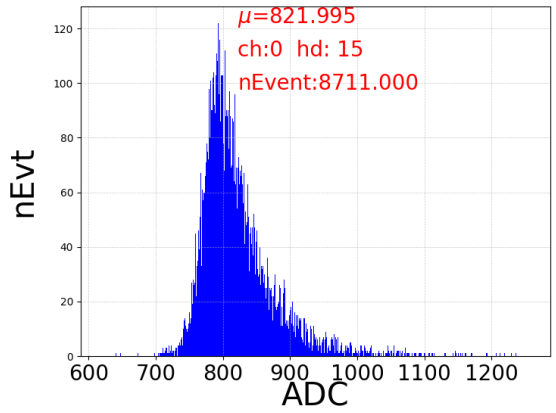


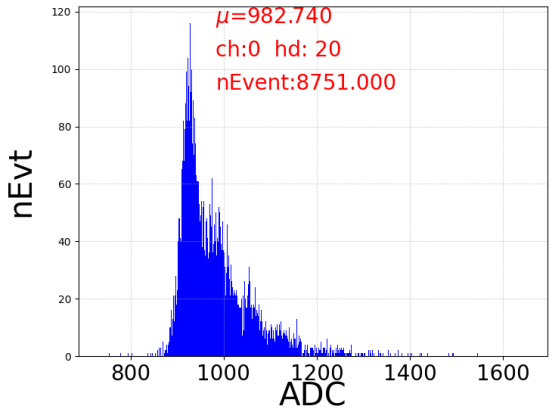
MPT2321 readout development

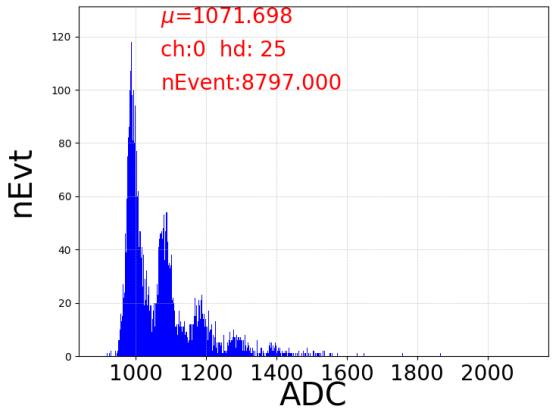
Optimization of configure parameter

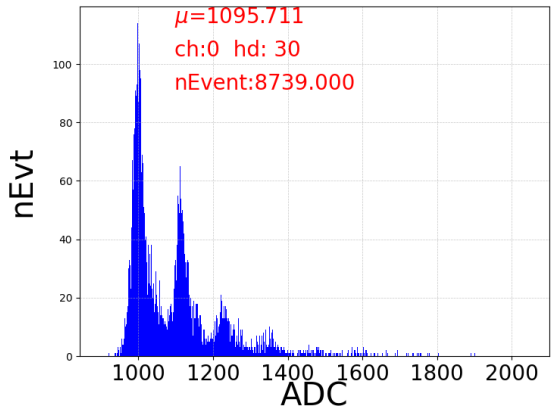
- Hold delay扫描

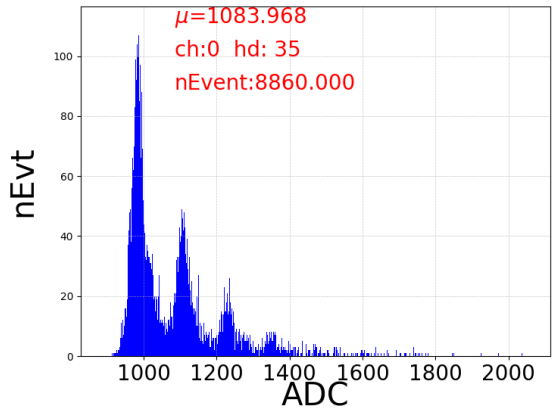


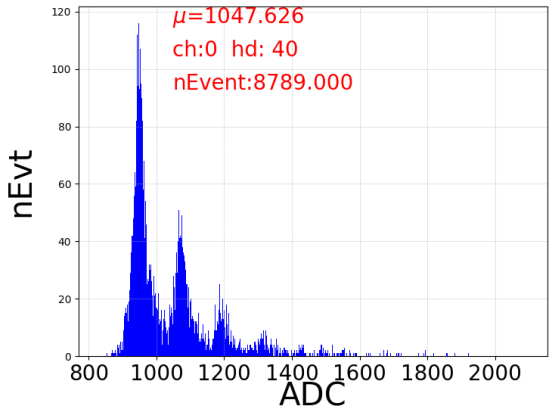


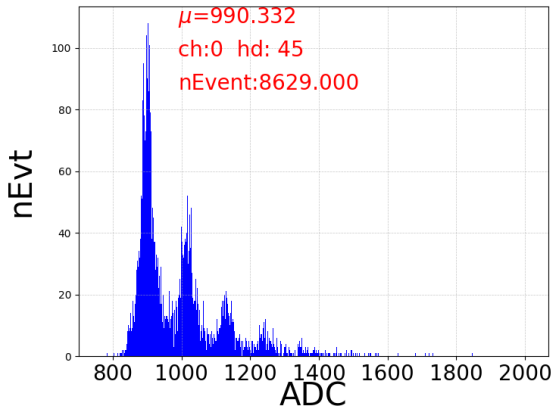


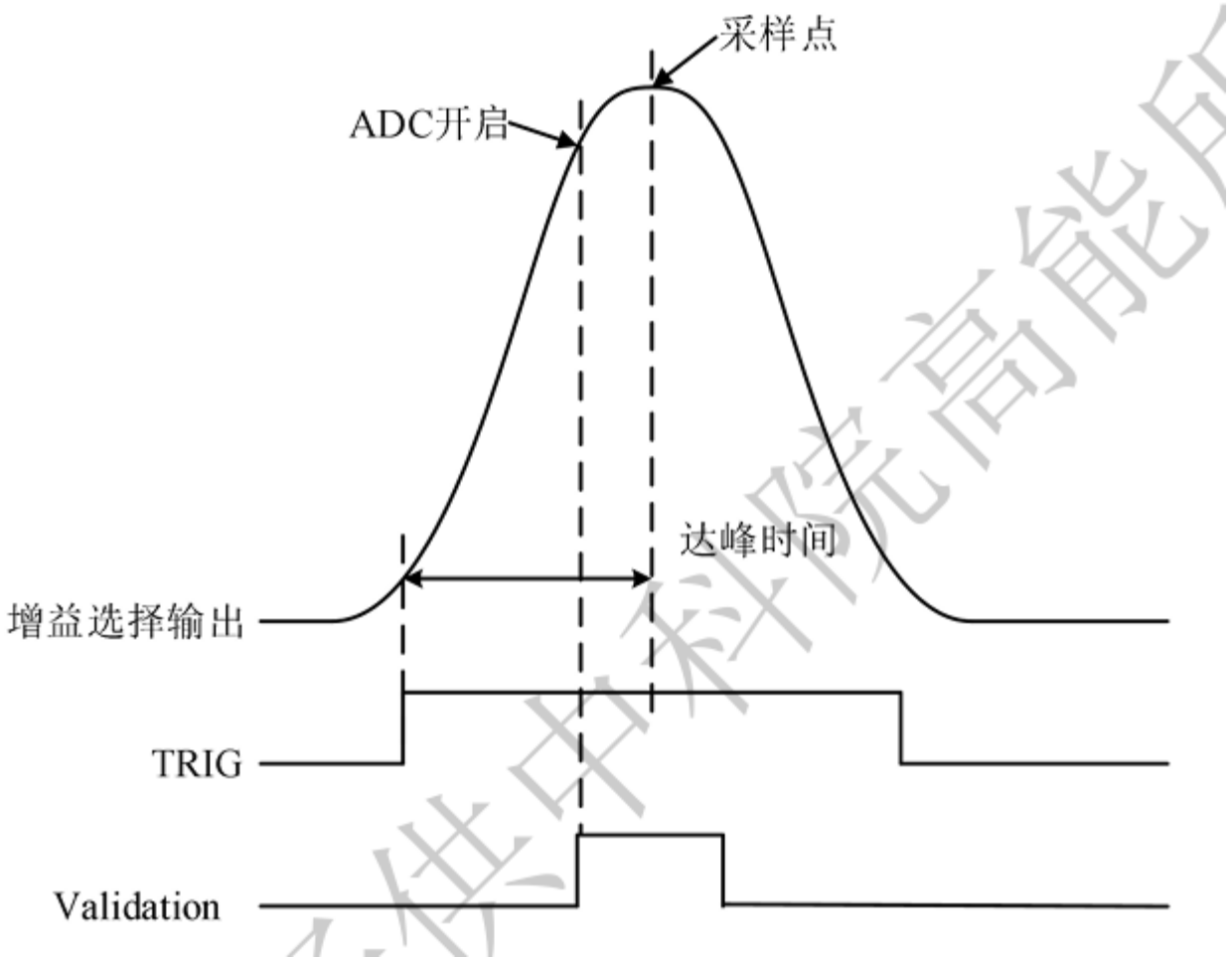


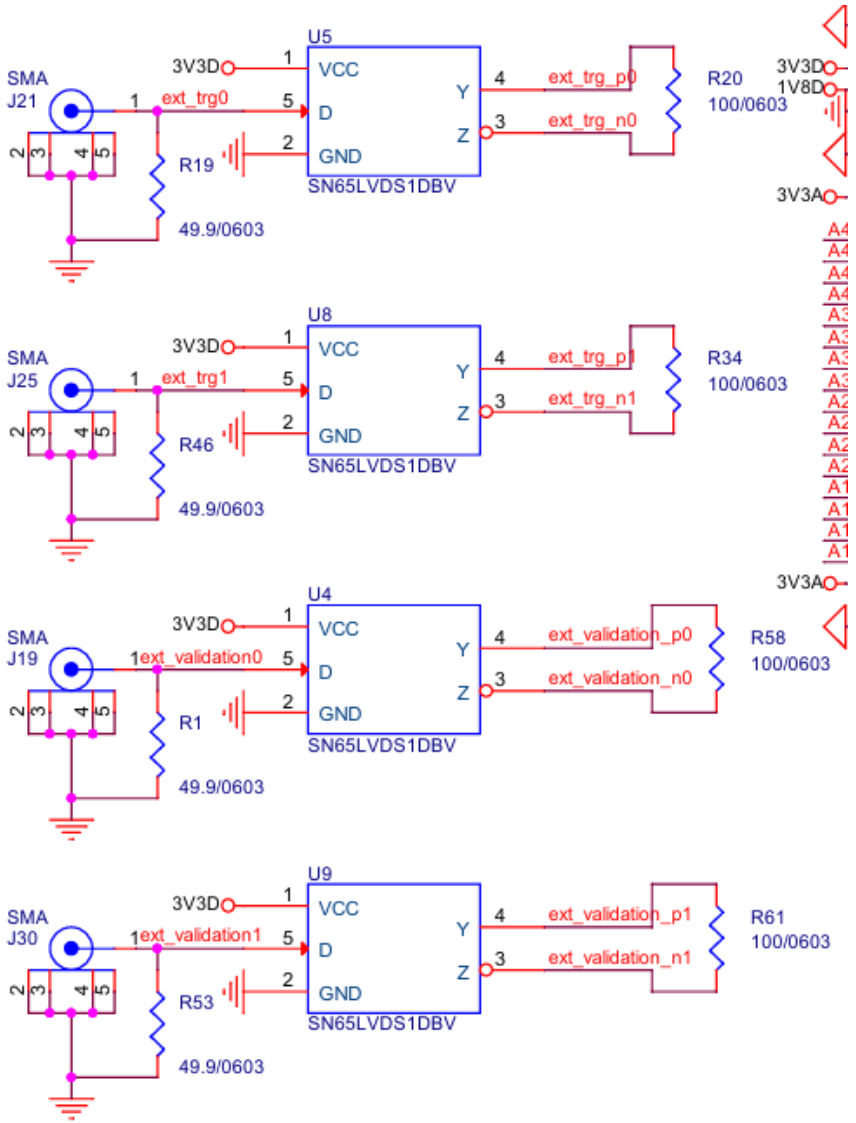








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SMA
J21
3V3D
ext_trg0
R19
49.9/0603
VCC
D
GND
Y
Z
SN65LVDS1DBV
ext_trg_p0
ext_trg_n0
R20
100/0603
3V3D
1V8D
3V3A
U8
SMA
J25
3V3D
ext_trg1
R46
49.9/0603
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ext_trg_n1
R34
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SMA
J19
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R1
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R58
100/0603
3V3A
U9
SMA
J30
3V3D
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R53
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R61
100/0603