Preparing for COFFEE3 Test

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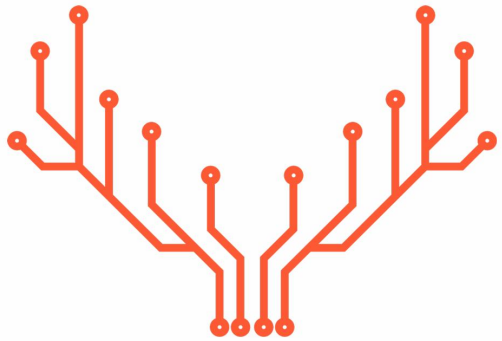
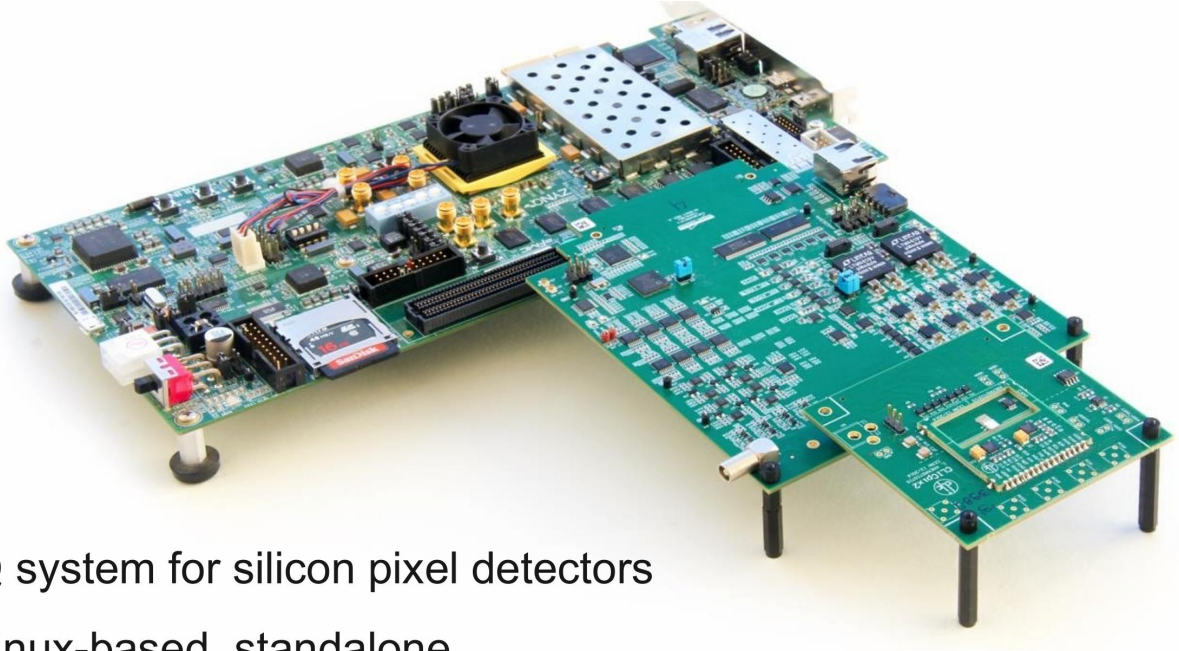
徐子骏, 张晓旭, 曾程, 周扬, ……

2025-Jun-27

Setup for Chip test: Caribou DAQ





- Caribou is:
  - A versatile DAQ system for silicon pixel detectors
  - Open source, Linux-based, standalone
  - Proving excellent operation on many detector prototypes
  - Entering its upgrade phase with many improvements to come

Application examples

- Support for various readout schemes
  - Digital interface via GTx or LVDS
  - Analogue waveforms (ADC or oscilloscope)

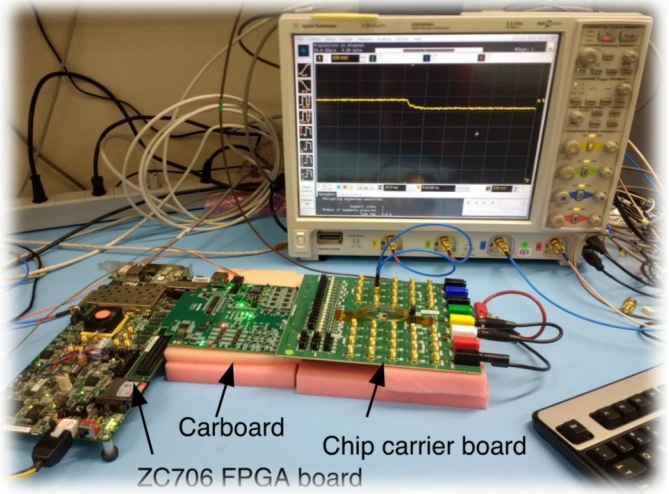
- Integration in beam telescope setups
  - FEI4, Timepix3, Mimosa, ALPIDE

Telescope integration

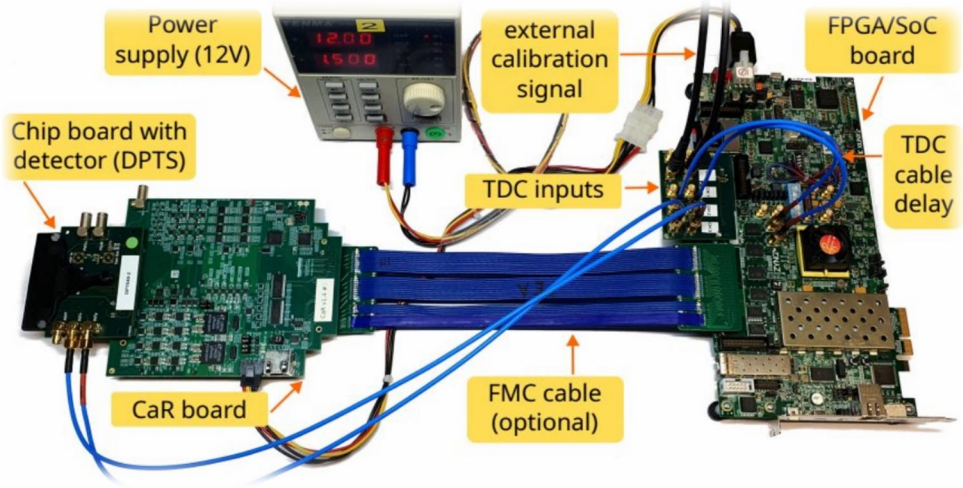
CLICdp Timepix3 @ CERN

MIMOSA @ DESY

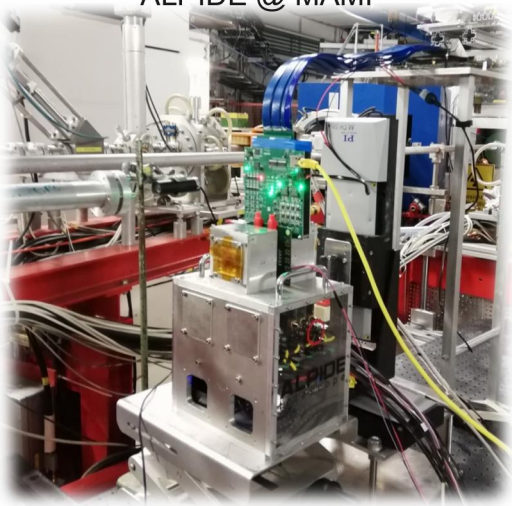
FASTpix with oscilloscope readout



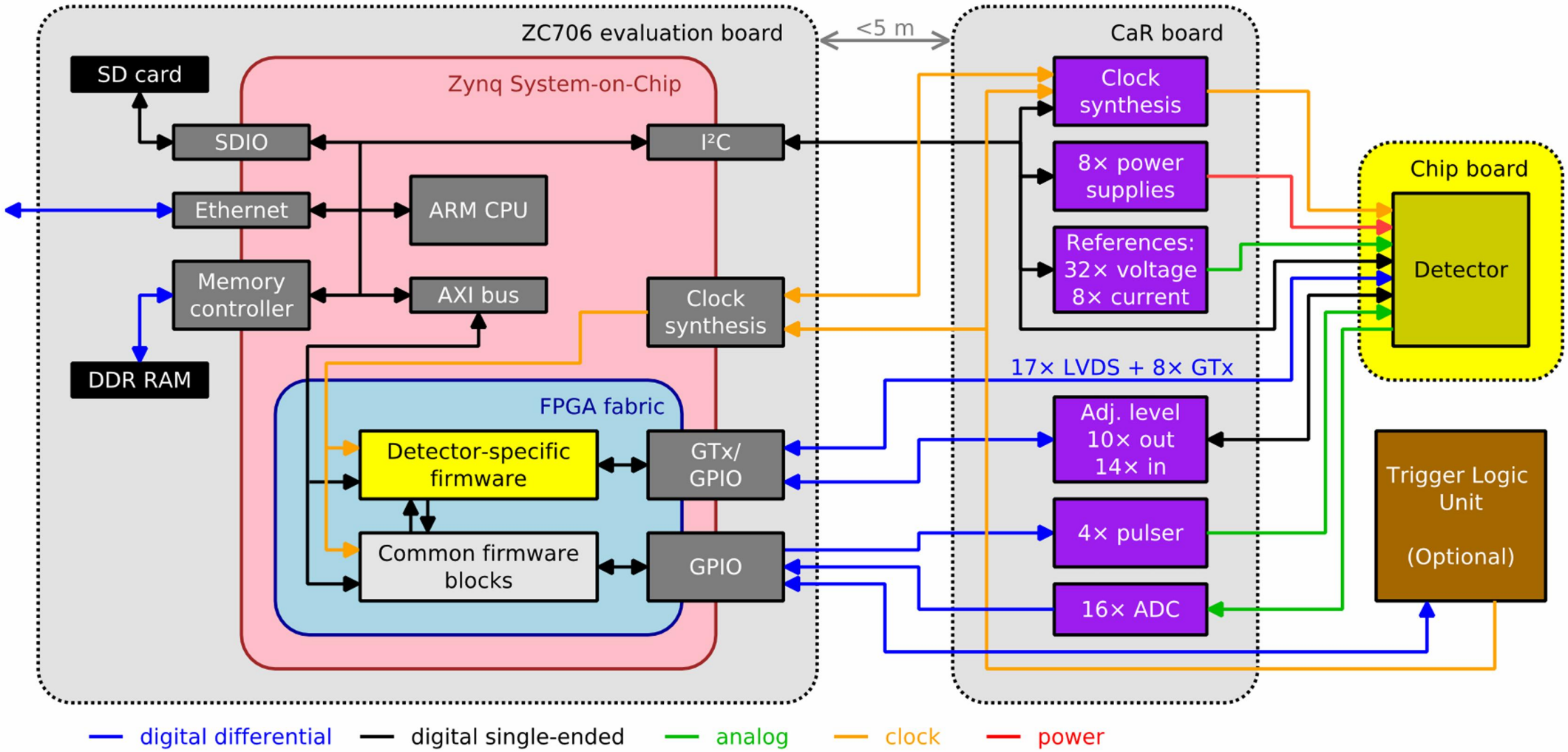
DPTS with TDC in FPGA readout



ALPIDE @ MAMI

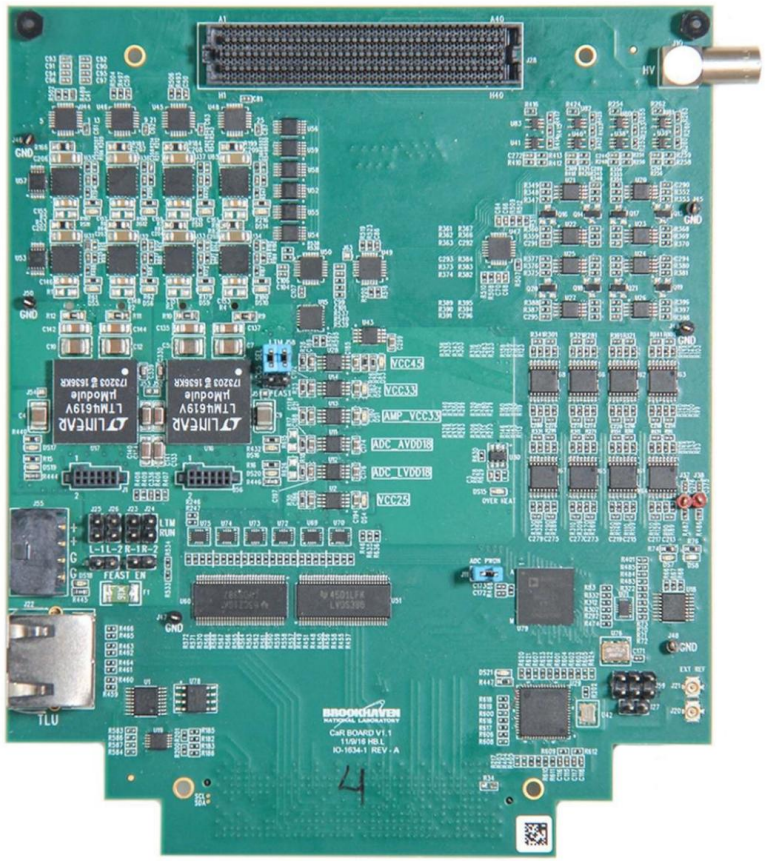


Caribou system architecture



Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector



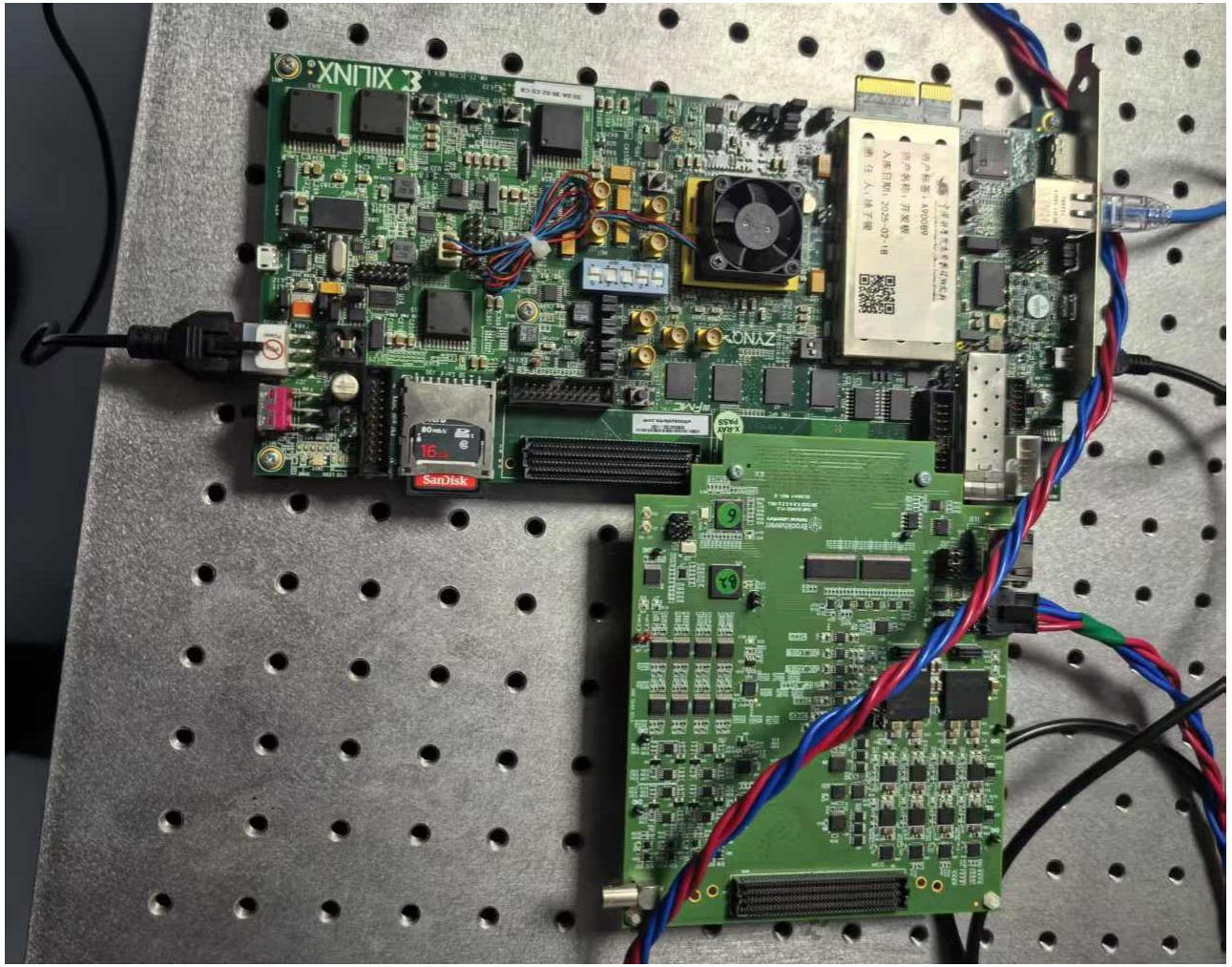
https://gitlab.cern.ch/Caribou/hardware/carboard

Resources for various target applications

20 CaR boards v1.4 produced and distributed within RD50 common project

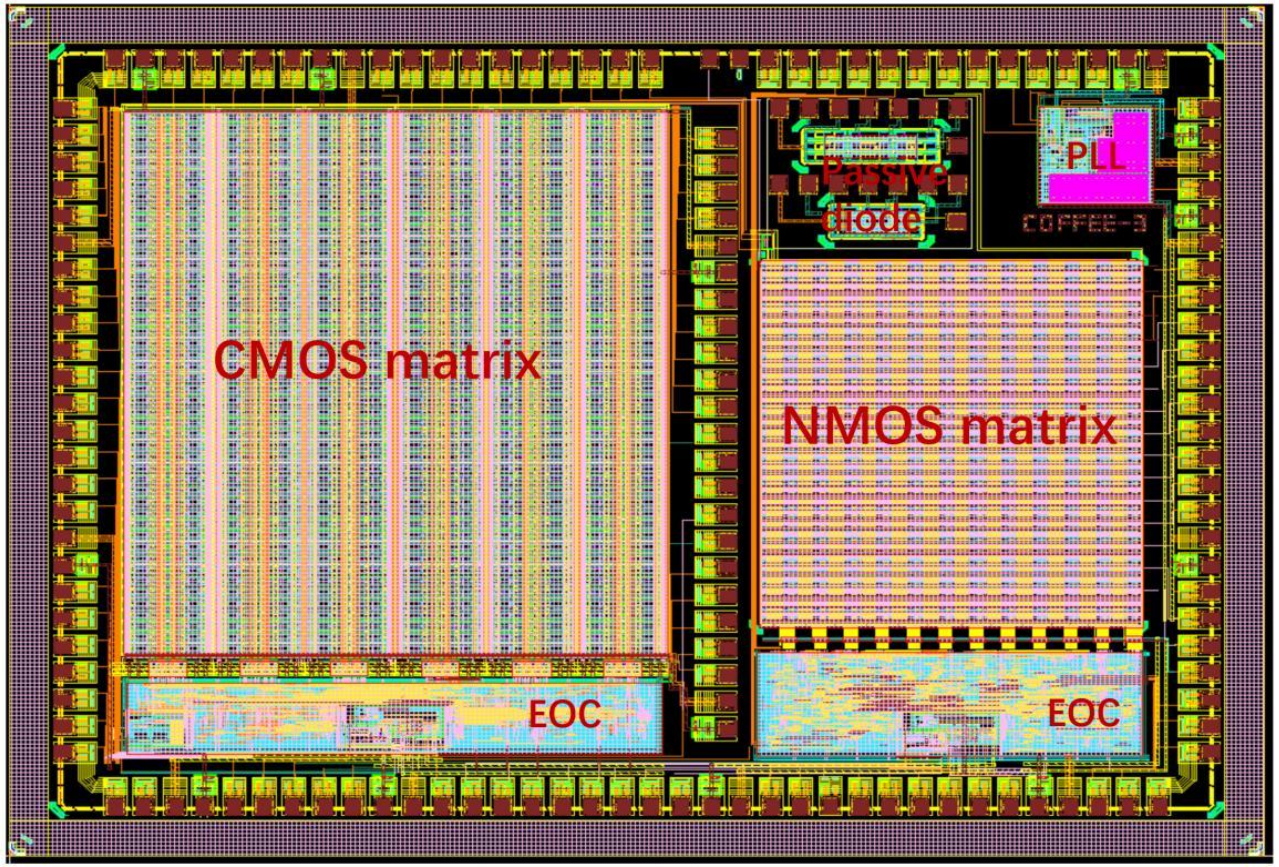
Caribou DAQ at IHEP

- both ZC706 and ZCU102 running fine with CaR boards



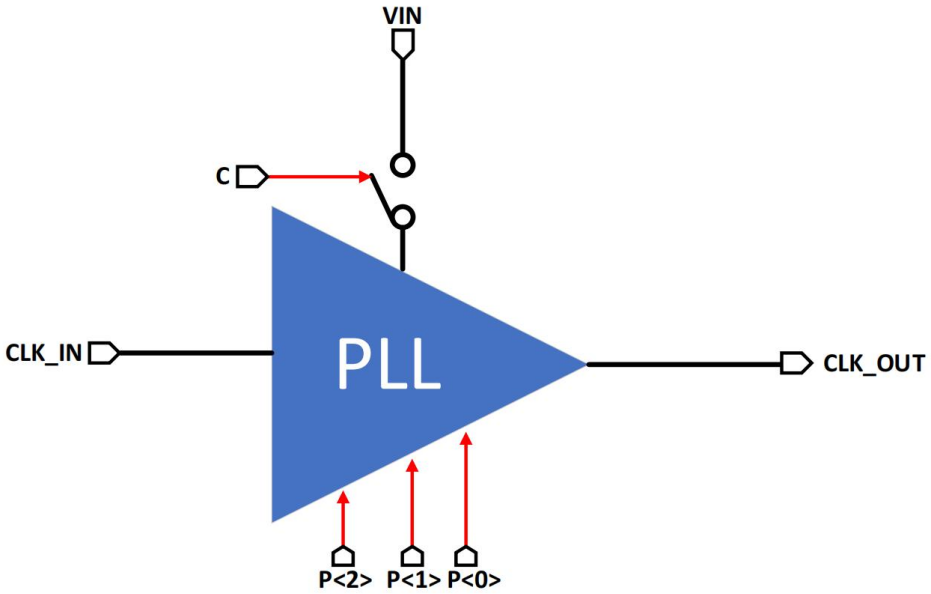
COFFEE3 Design

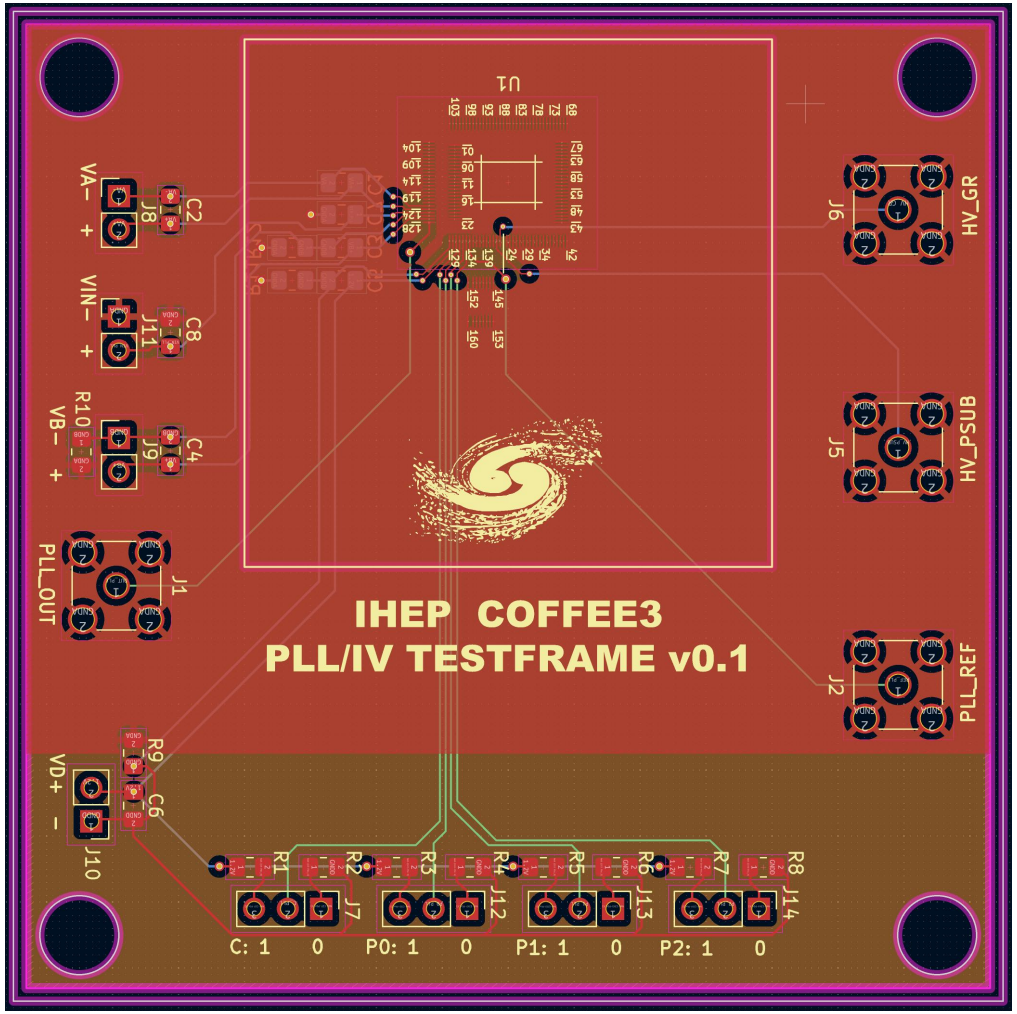
- see Yang's talk today
- CMOS and NMOS matrix
  - diff. in analog circuits and in-pixel circuits design
- EOC
  - same/similar in data serializer, LVDS driver
- PLL
  - standalone block
- Passive sensing diode only
  - massive tests done with COFFEE2 chips
- 160 pads for chip testing



PLL (and IV) Test Board

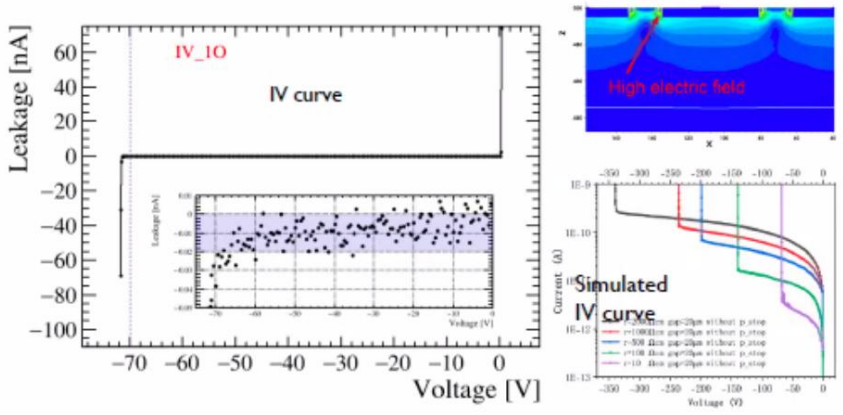
- Mostly for PLL block only

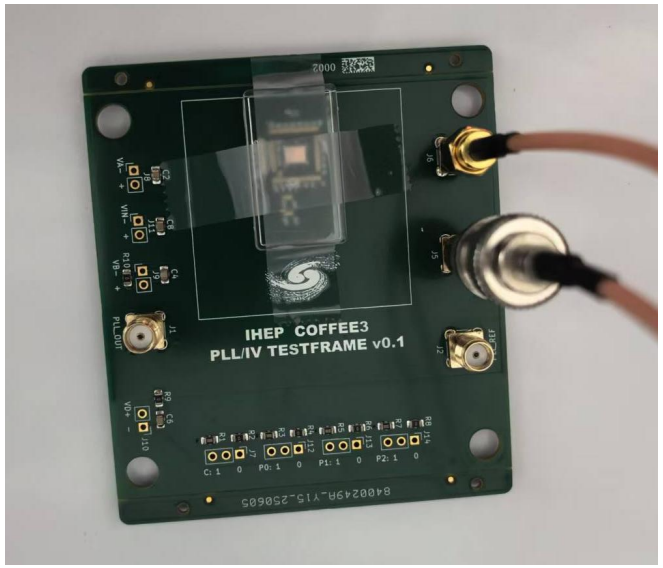




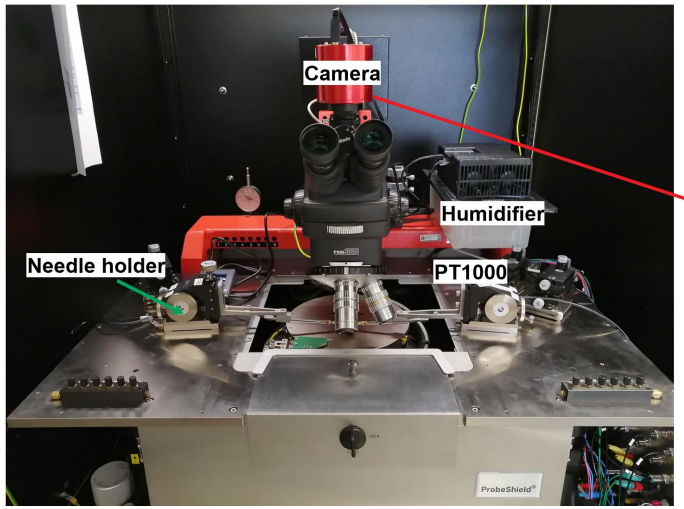
PLL (and IV) Test Board

- PLL test in next weeks
- 2 test point available for P-sub and right matrix Guard-Ring at this board
- IV test: -71.8V breakdown
  - highly consistent with COFFEE2





Imaging Setup



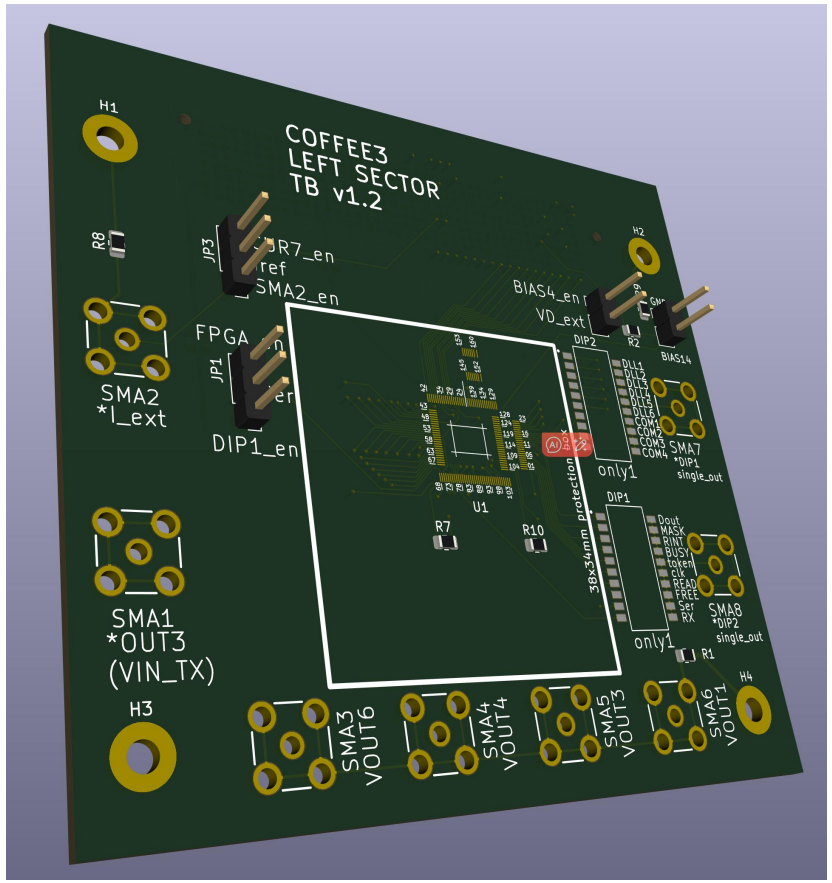
- ZWO CMOS camera: astronomy camera (~1K Euro)
- Camera: attached to the probe station microscope

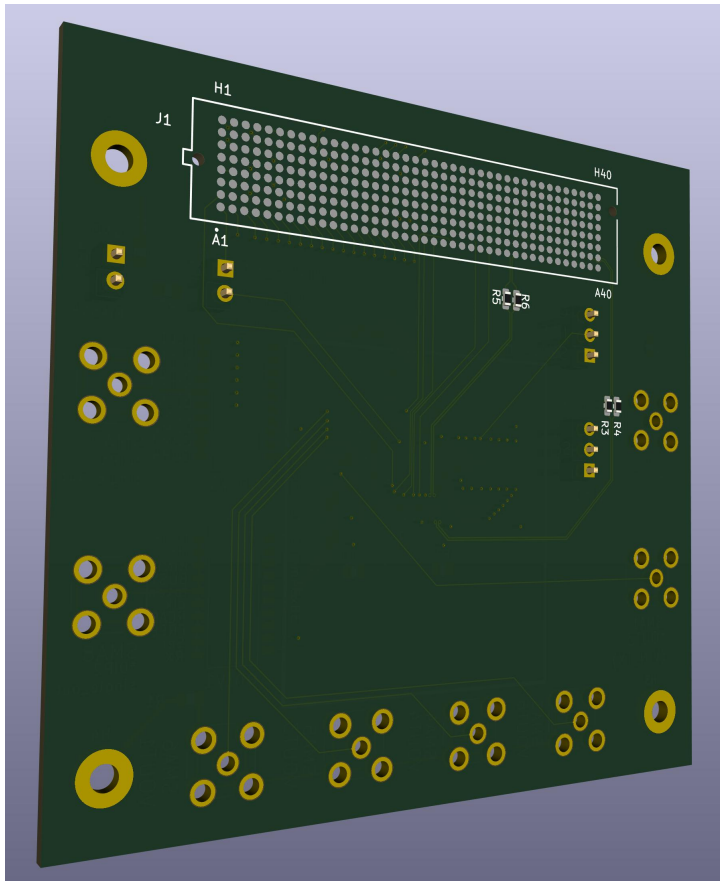
Image of the ASI183MM Pro (mono) [3].

from DESY ATLAS ITk strip sensor test

Left Matrix Test Board

- TB v1.2 Board in production, will arrive early next week
- COFFEE3 left matrix test will starting immediately



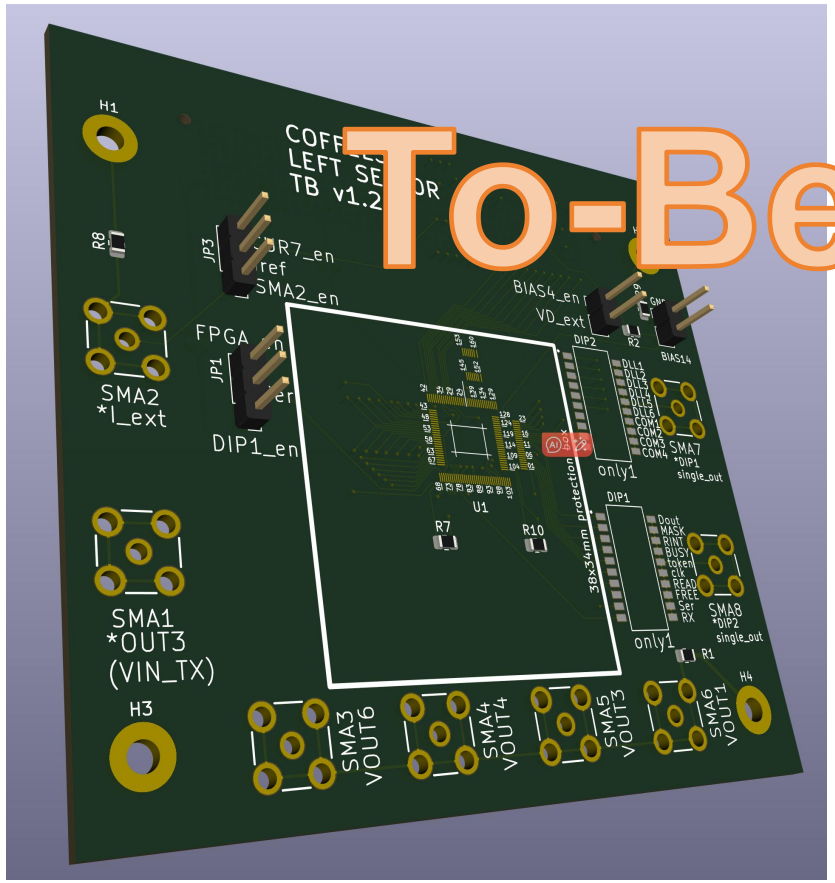


COFFEE3 left matrix test

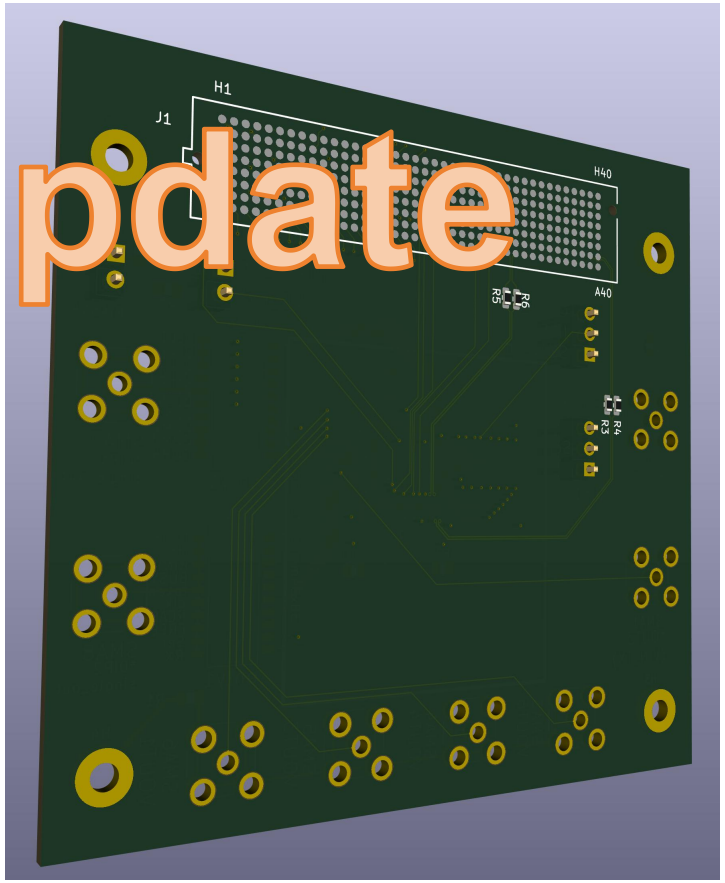
- SPI config between the FPGA and the CMOS matrix EOC
- power supply from Caribou DAQ
- reference voltage/current from Caribout to CMOS matrix
- 4 pixel CSA output from CMOS matrix => SMA cable => osc. scope
- ~10 Digitial signal output from EOC
- 6 DLL output
- LVDS Transceiver test between EOC and DAQ
  - Tx and Rx driver study
  - digital circuits for data serializer

Right Matrix Test Board

- Board in desigh



To-Be-Update



Working List

设计人员及配合测试的联络人（2025.6）待补充

	功能区域	设计人员	联络人（for 测试）
	模拟前端+比较器		
	4-bit 阈值调节 DAC		
	Colum-drain 优先级读出结构		
	TDC 结构		
	存储单元 RAM/ROM		
	整体集成		
	EoC		
	DLL		
	数字前端、仿真验证		
	数字后端		
	模拟前端+比较器		
	4-bit 阈值调节 DAC		
	像素内 SPI 配置		
	整体集成		
	数字前端、仿真验证		
	数字后端		
	LVDS driver/transmitter	陈洋（已毕业）	张子音 or 李乐怡
	PLL	王雨颉 （已毕业）	王小龙 or 李乐怡
	PASSIVE diode array		
	Guard ring		
	TOP integration		

-50C 制冷柜 for COFFEE2/3 test