课题三：ALICE探测器升级

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课题承担单位：华中师范大学
课题参与单位：中国原子能科学研究院

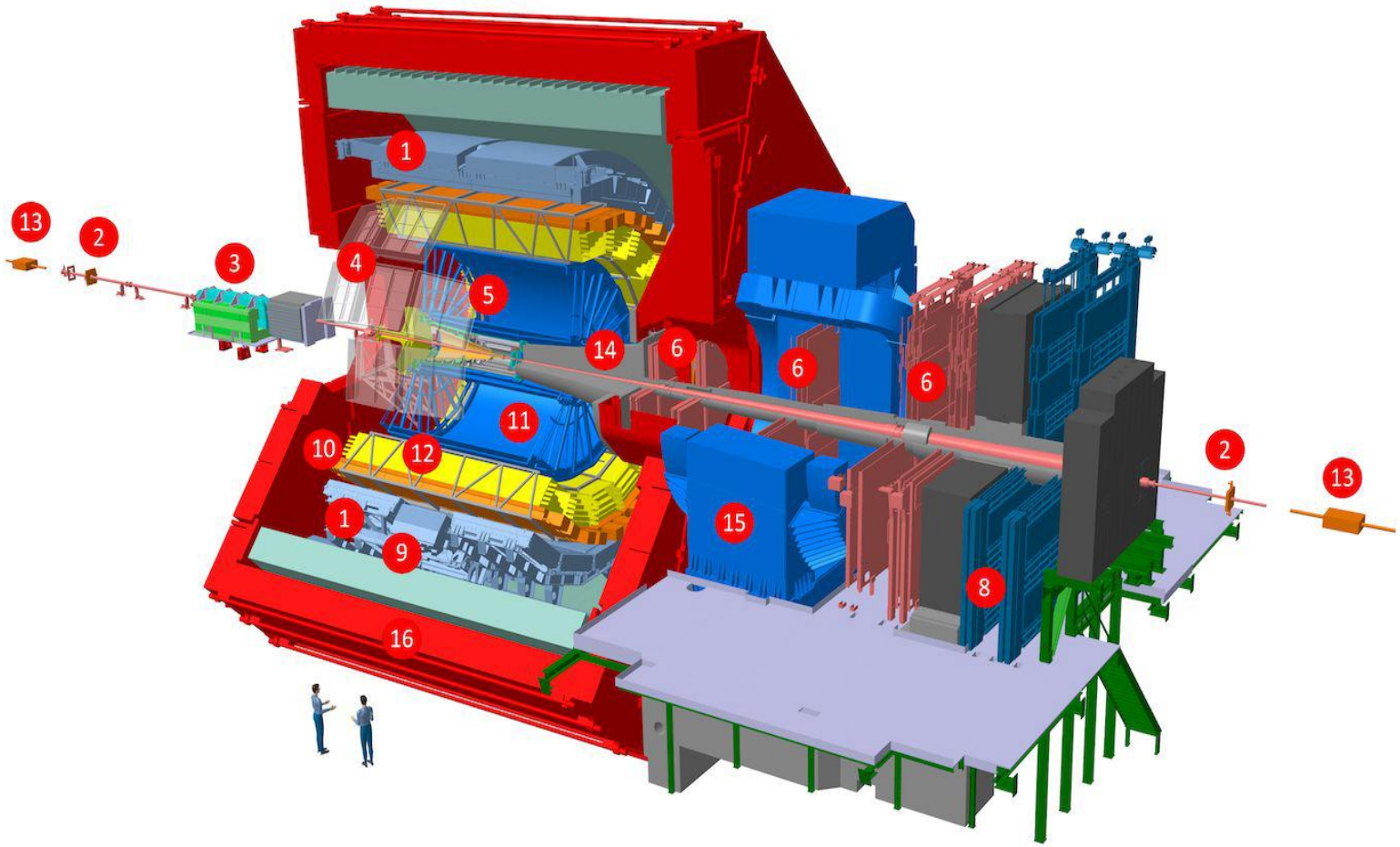
汇报内容

- 研究内容、考核指标、研究进度
- 课题研究的主要进展
  - ITS3硅像素芯片
  - FoCal硅像素层
  - FoCal读出电子学系统
- 经费执行、文章发表和人才培养情况
- 存在的问题
- 总结

升级后的ALICE探测器（~~2029~~2030年）

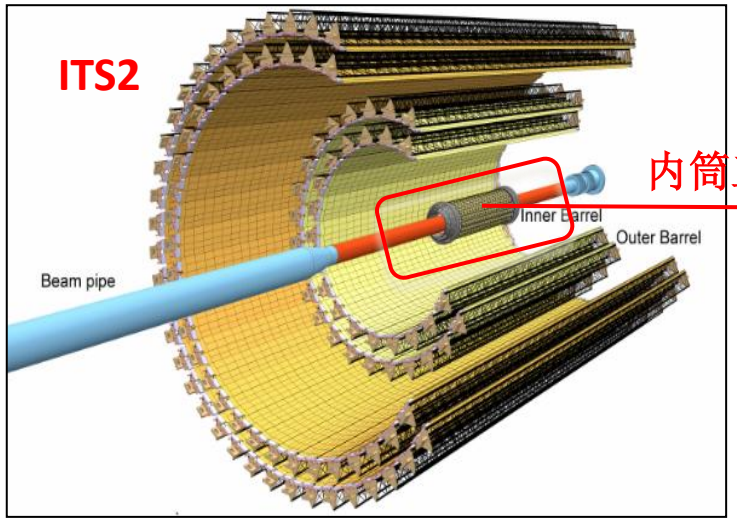
LS3 （~~2026-2028~~）期间

2026.7-2030.6

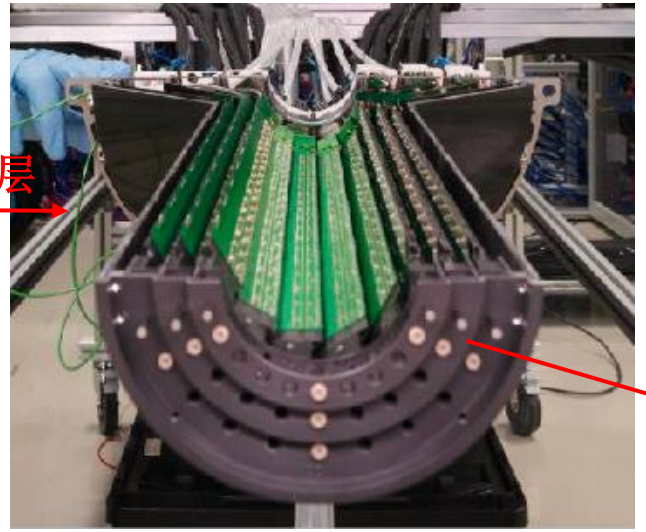


1. **EMCAL** | Electromagnetic Calorimeter
2. **FIT** | Fast Interaction Trigger
3. **FoCal** | Forward Calorimeter — 新增
4. **HMPID**| High Momentum Particle Identification Detector
5. **ITS**| Inner Tracking System — 更新
6. **MCH**| Muon Tracking Chambers
7. **MFT**| Muon Forward Tracker
8. **MID**| Muon Identifier
9. **PHOS/CPV**| Photon Spectrometer
10. **TOF**| Time Of Flight
11. **TPC**| Time Projection Chamber
12. **TRD**| Transition Radiation Detector
13. **ZDC**| Zero Degree Calorimeter
14. **Absorber**
15. **Dipole Magnet**
16. **L3 Magnet**

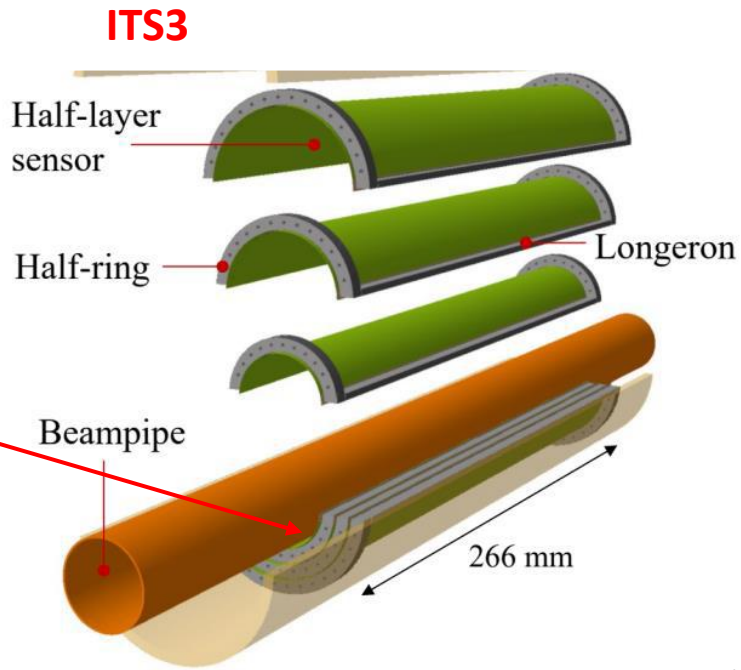
ITS3



内筒三层



替换为



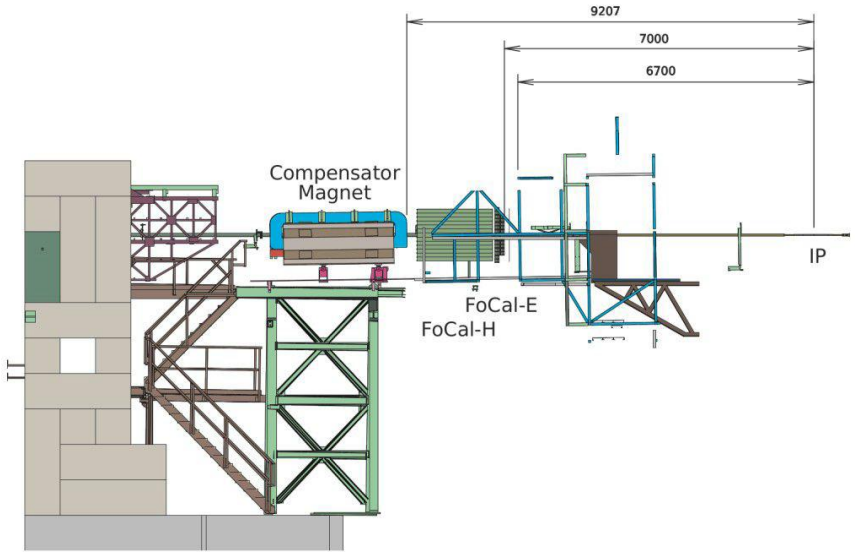
	ITS2	ITS3
到碰撞点的径向距离 （mm）	22	19
最内层辐射长度（%X_0）	~0.35	~0.09
像素大小 （μm²）	30×30	*O*(~~15×15~~22.8 ×20.8)
芯片大小 （cm²）	1.5×3.0	O(90×280)
芯片厚度 （μm）	50	50

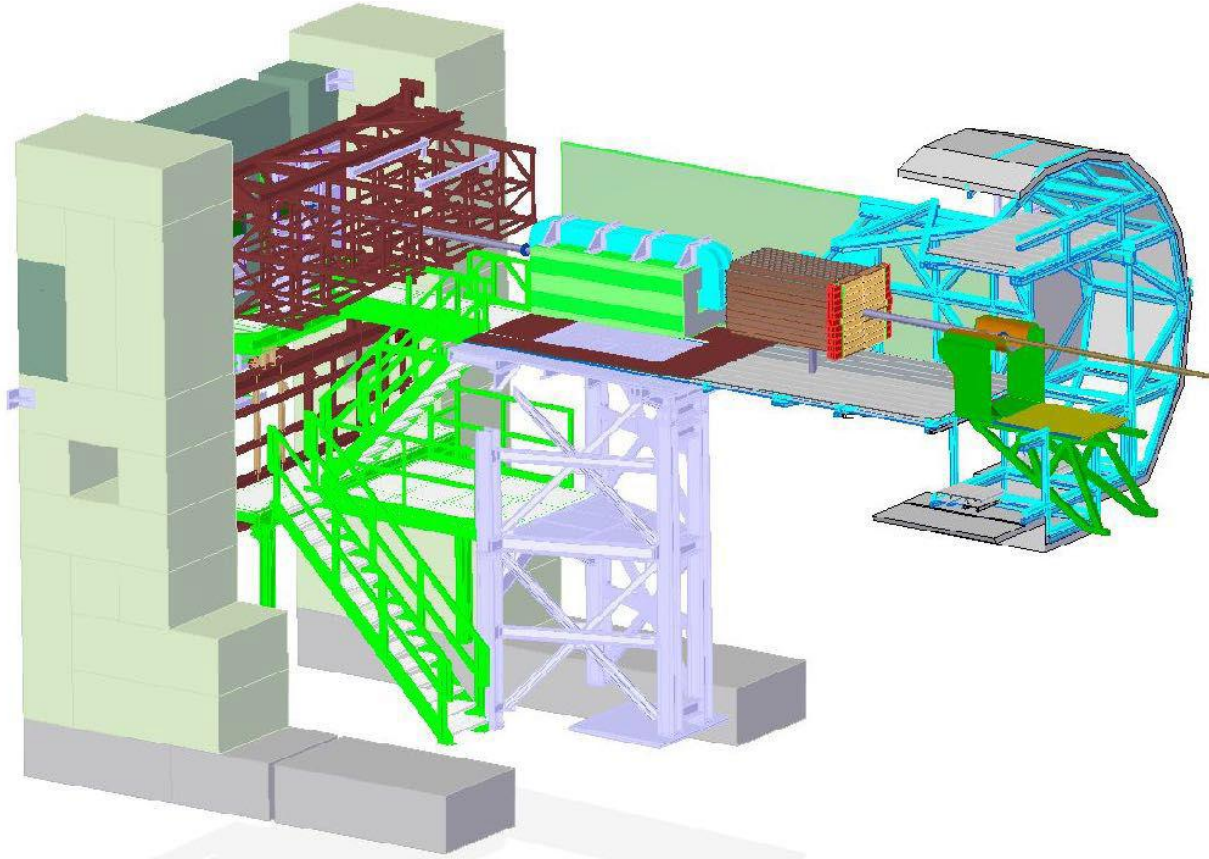
整个探测器几乎仅由6片大面积超薄传感器芯片组成

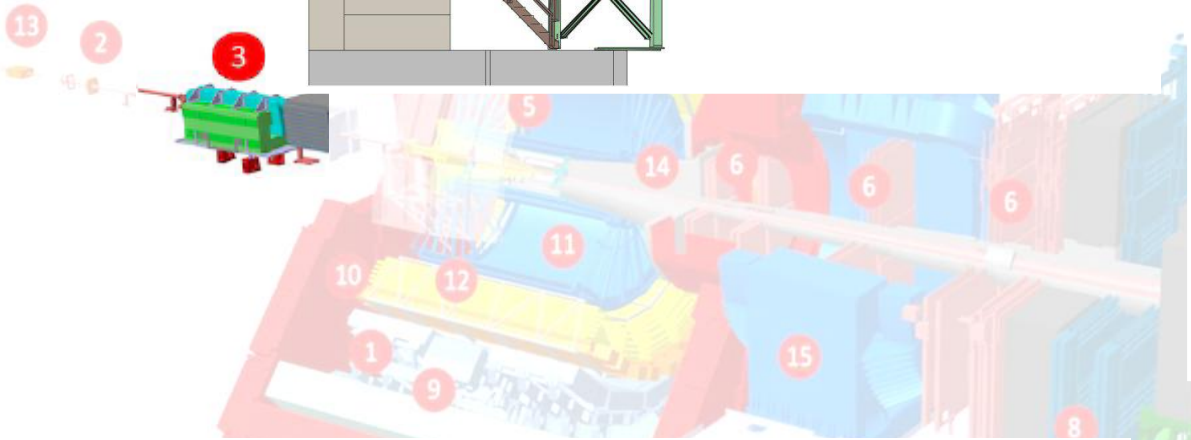
- 非常小的探测器材料辐射长度
- 非常均匀的材料分布，减小系统误差
- 更细的束流管，探测器最内层半径更小

- 会极大地提升在重离子碰撞中测量低横动量粲强子和底强子以及低质量双电子的能力

Forward Calorimeter (FoCal)



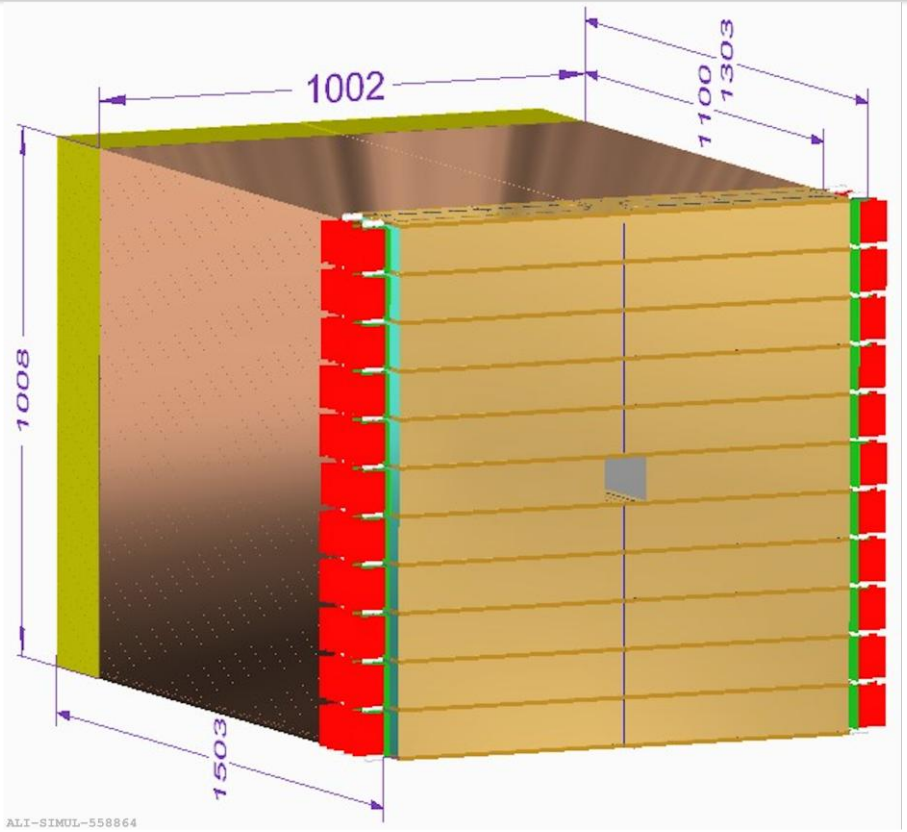




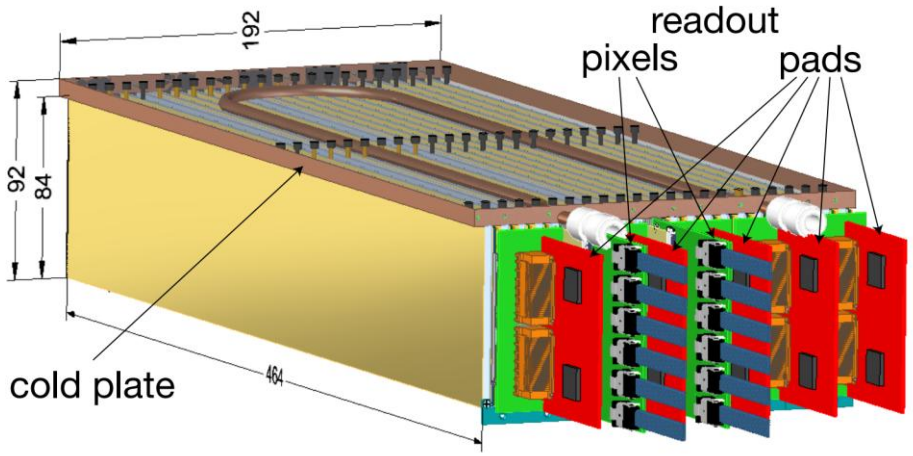
- 离碰撞点的距离为7米
- 覆盖赝快度：3.4 - 5.8

- 小 x 物理

FoCal探测器的构造

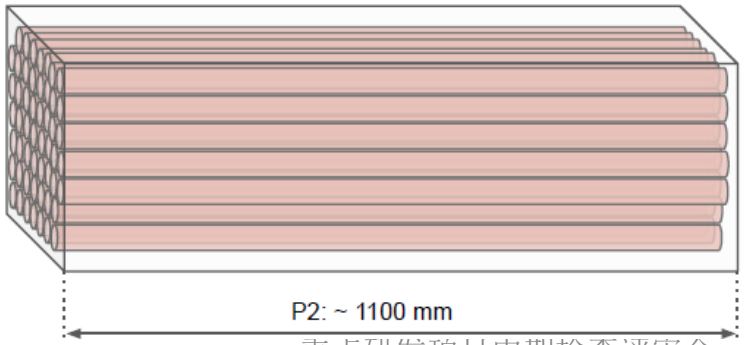


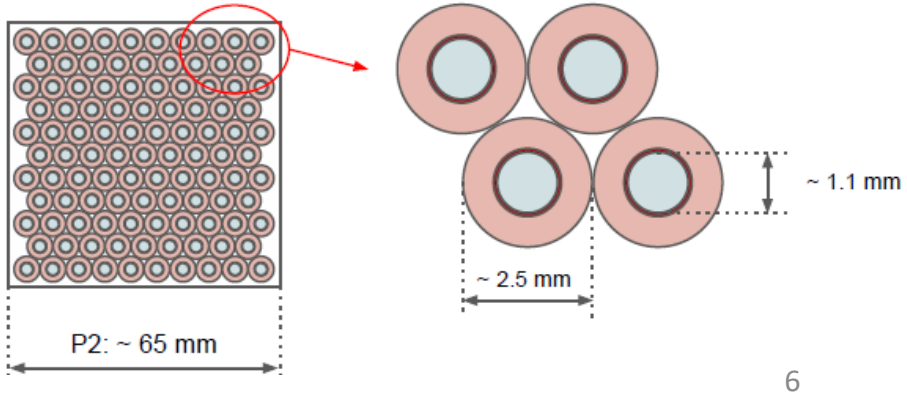
- FoCal-E: 18层粒度为1×1 cm^2硅片+2层硅像素层取样型**电磁量能器**



共含22个FoCal-E模块

- FoCal-H: 毛细铜管+闪烁光纤意大利面型**强子量能器**





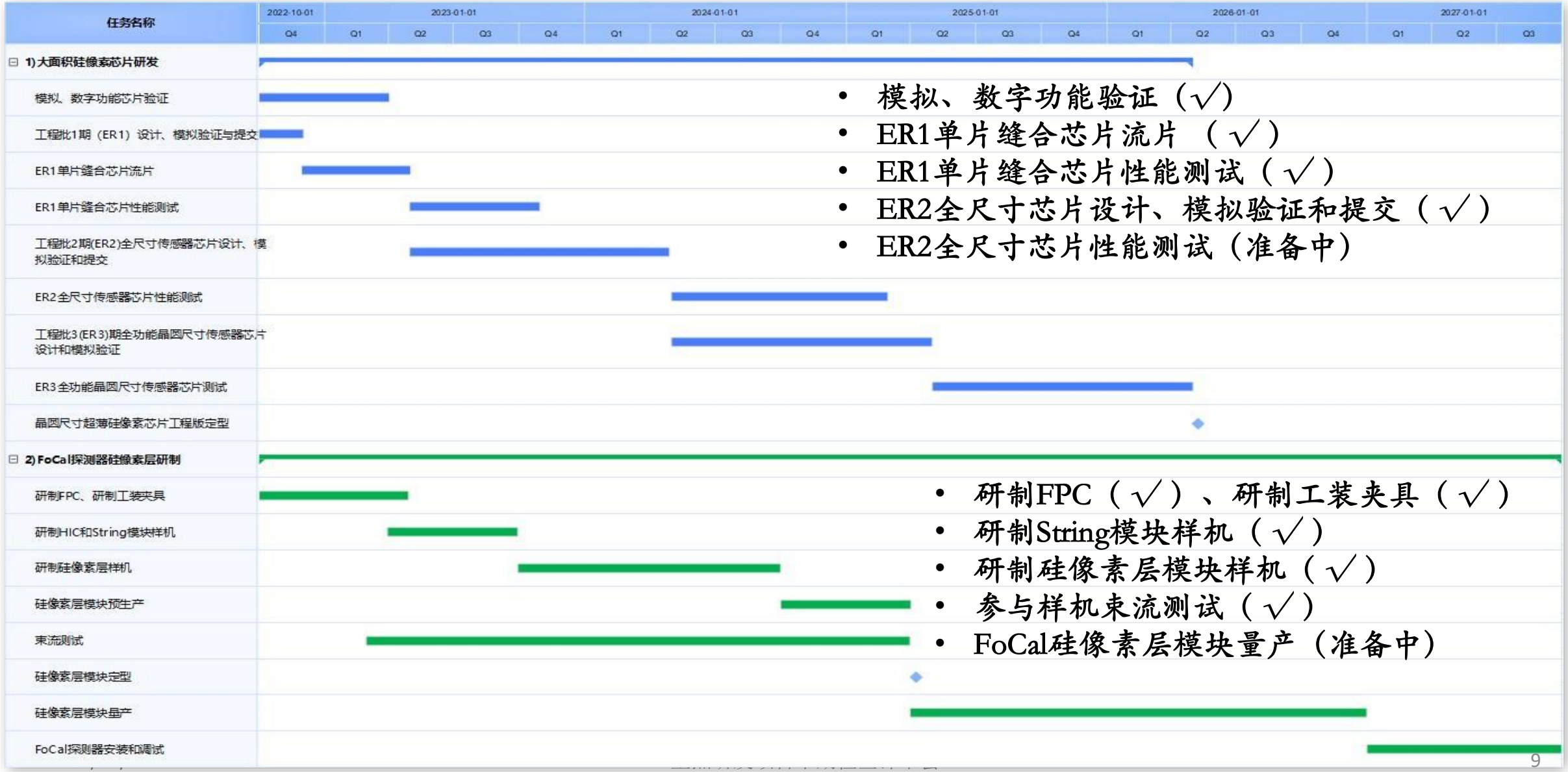
课题研究内容

- 合作研发晶圆尺寸的超薄硅像素芯片
  - 与CERN合作，利用拼接缝合技术，研发晶圆尺寸的超薄硅像素芯片
  - 参与芯片设计、模拟验证和测试等工作
- FoCal探测器的硅像素层研制
  - 与挪威卑尔根大学等单位合作，研制出FoCal探测器的硅像素层及其读出电子学系统
  - 参与束流测试，研究硅像素层模块的性能
  - 通过探测器模拟，优化FoCal的构造和像素层的位置
  - 设计开发探测器读出单元，结合系统模拟，优化固件架构设计，提高探测器性能
  - 基于束流测试结果，优化MC模拟参数，研究探测器物理性能，建立分析框架

考核指标

课题目标[1]	预期成果				考核指标[2]				考核方式（方法）及评价手段[4]
	预期成果名称			预期成果类型	指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态	
（限500字以内。）参与研发用于ALICE第三代硅像素探测器的晶圆尺寸硅像素芯片，掌握其研发关键技术；完成FoCal探测器的硅像素层的研制任务，掌握研制基于硅像素芯片的高粒度量能器及其读出电子学的关键技术。发表论文1-2篇；培养研究生2-3名。	主要成果	1	合作研发出大面积硅像素芯片	□新理论 □新原理 □新产品 □新技术 □新方法 ■关键部件 □数据库 □软件 □应用解决方案 □实验装置/系统 □临床指南/规范 □工程工艺 □标准 □论文 □发明专利 □其他_____	指标1.1 芯片技术指标-面积、功耗等	无	芯片面积达90 mm x 140 mm	芯片面积达90 mm×140 mm，像素大小约15 um×15 um，功耗低至20 mW/cm^2	合作组安排测试，提供测试结果
		2	合作研制出FoCal硅像素层模块及其读出电路板	□新理论 □新原理 □新产品 □新技术 □新方法 ■关键部件 □数据库 □软件 □应用解决方案 ■实验装置/系统 □临床指南/规范 □工程工艺 □标准 □论文 □发明专利 □其他_____	指标2.1 FoCal技术指标-位置分辨本领	～10 mm	样机位置分辨率～5 mm	～5 mm	合作组安排测试，提供测试结果
	其他成果								

进度安排

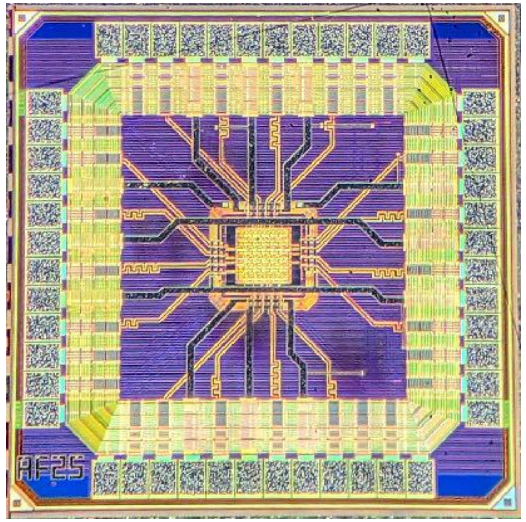


- 模拟、数字功能验证（√）
- ER1单片缝合芯片流片 （√）
- ER1单片缝合芯片性能测试（√）
- ER2全尺寸芯片设计、模拟验证和提交（√）
- ER2全尺寸芯片性能测试（准备中）

- 研制FPC（√）、研制工装夹具（√）
- 研制String模块样机（√）
- 研制硅像素层模块样机（√）
- 参与样机束流测试（√）
- FoCal硅像素层模块量产（准备中）

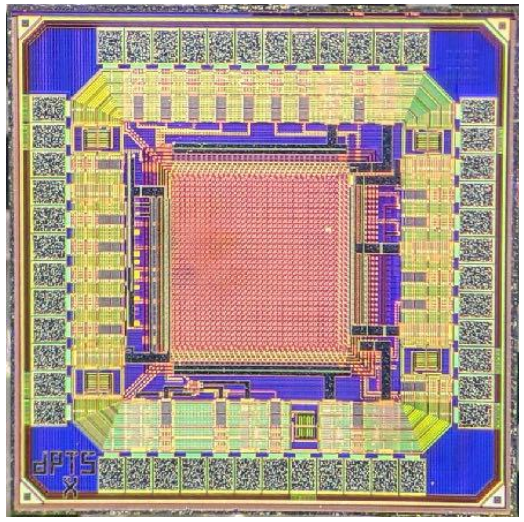
ITS3芯片研发：模拟、数字功能验证

APTS



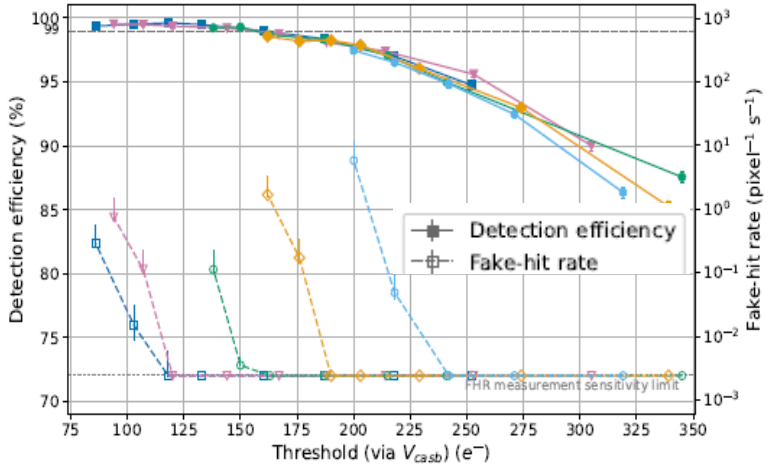
Matrix: 6x6 pixels
Readout: direct analog readout of central 4x4
Pitch: 10, 15, 20, 25 µm
Total: 34 dies

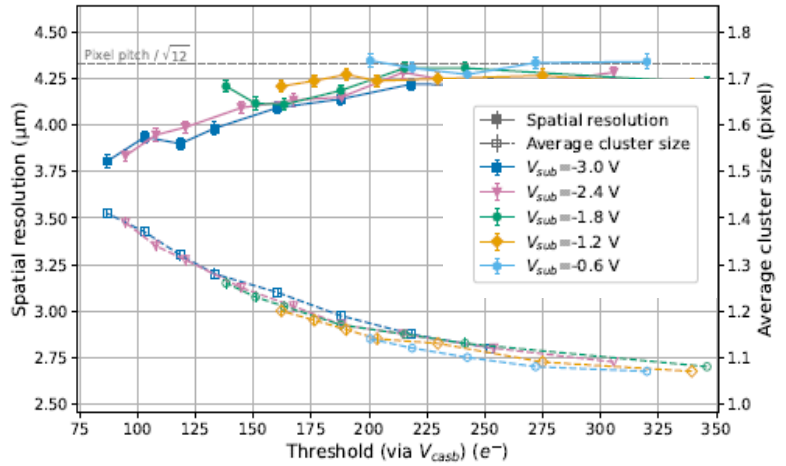
DPTS



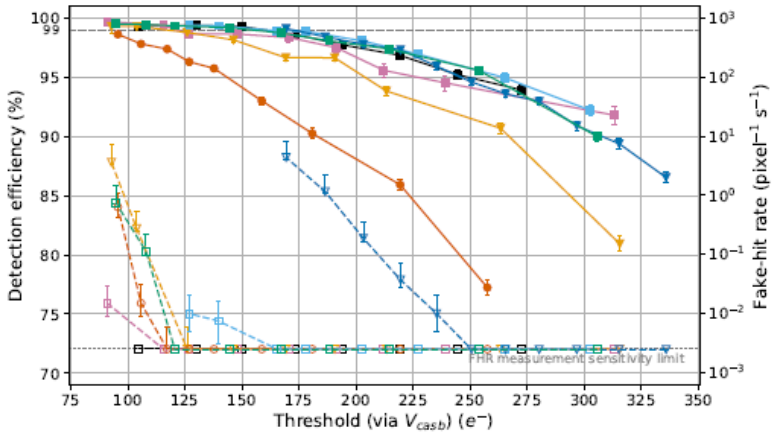
Matrix: 32x32 pixels
Readout: async. digital with ToT
Pitch: 15 µm
Total: 3 dies

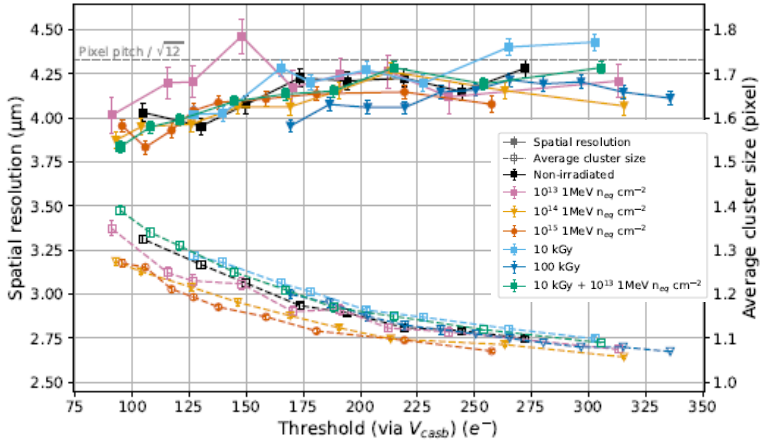
NIMA 1056 (2023) 168589 (arXiv:2212.08621)





Sensor irradiated to a dose of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} at different $V_{sub} = V_{pwell}$.

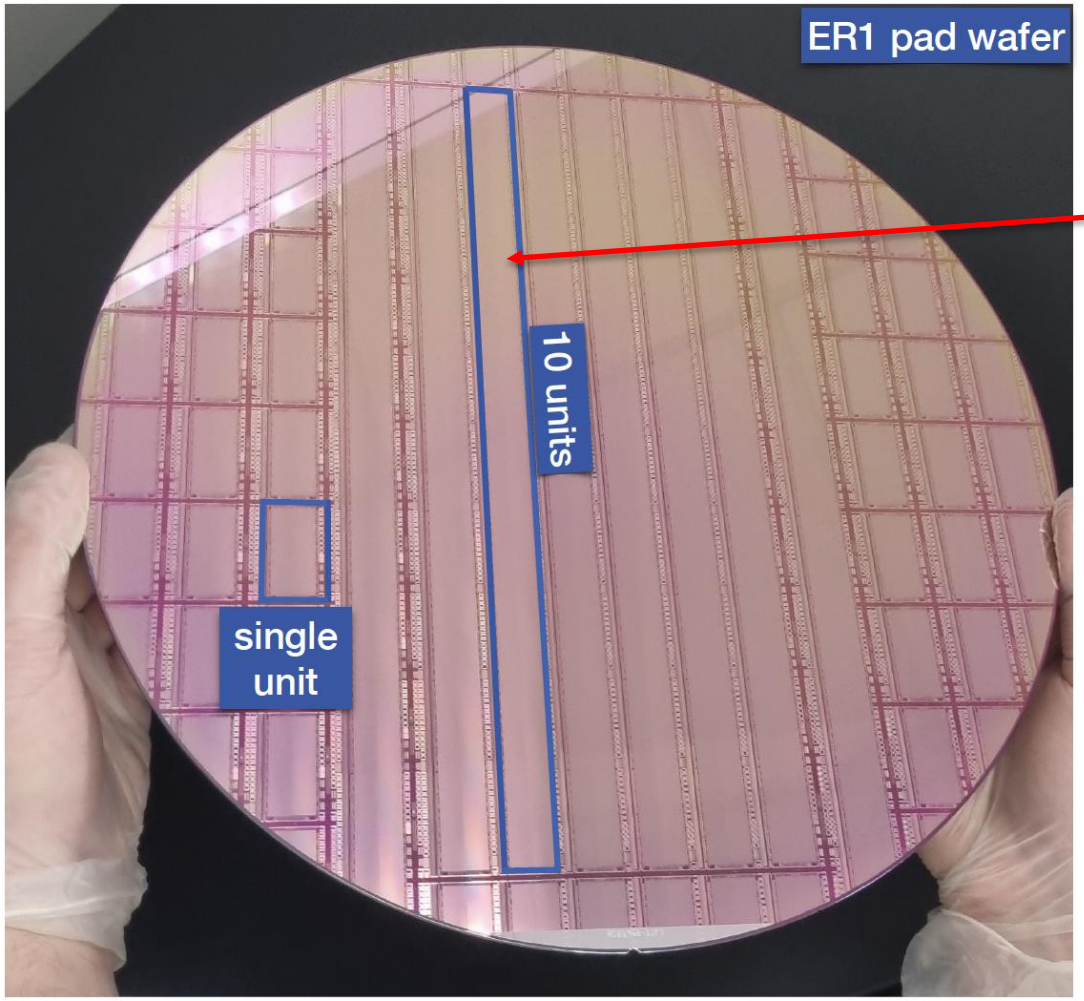


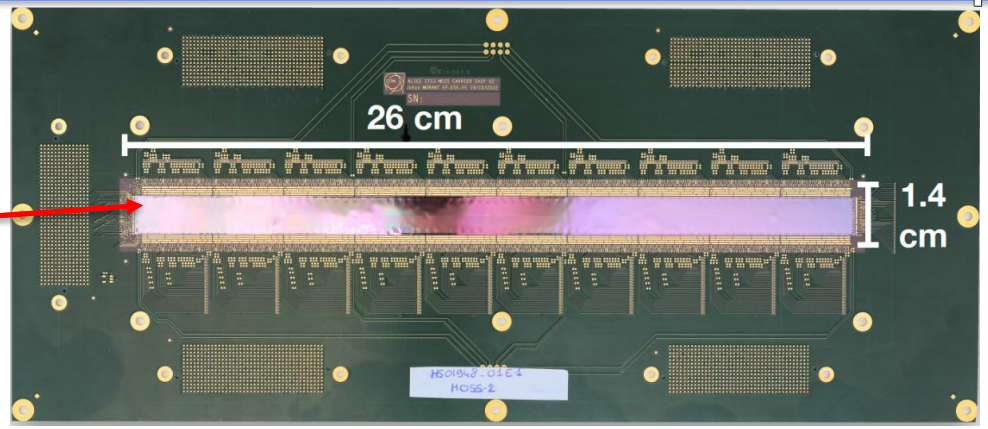


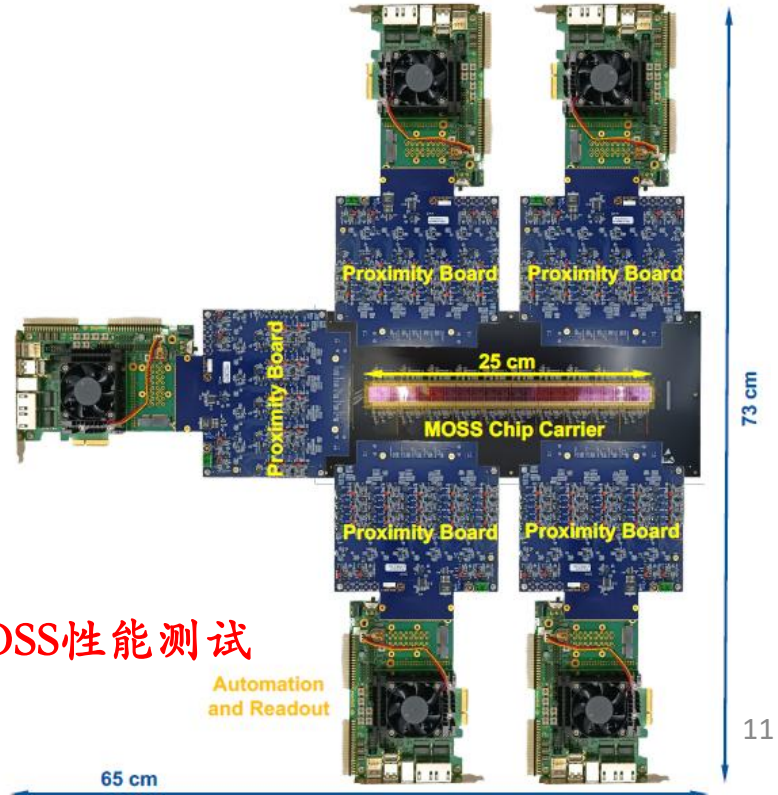
Sensors irradiated to different levels.

验证了基于65 nm工艺生产的芯片的探测器效率、位置分辨、抗辐照本领等性能指标满足ITS3要求

ER1单片缝合芯片MOSS性能测试





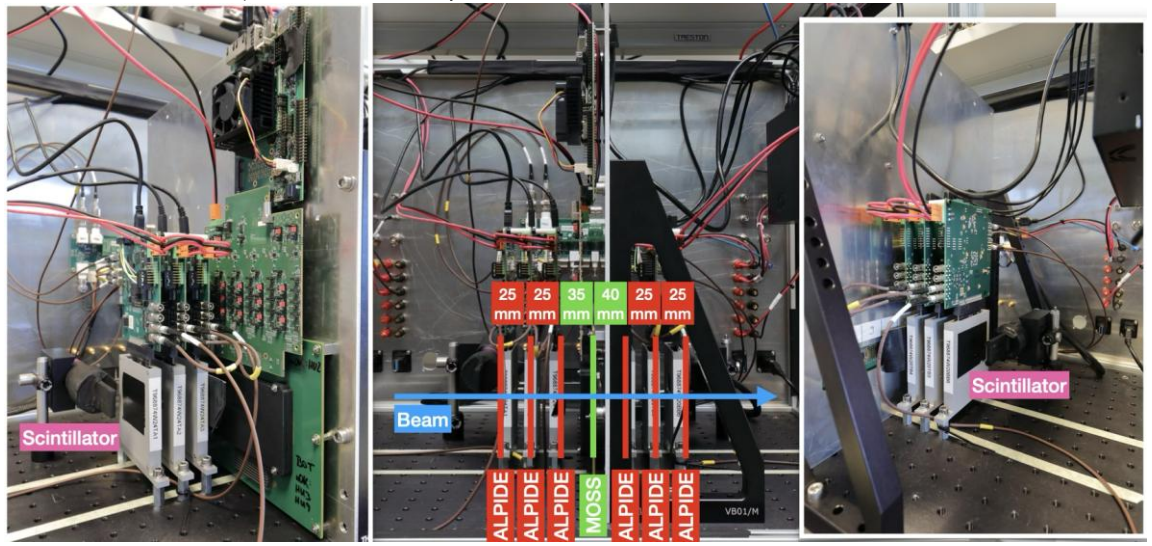


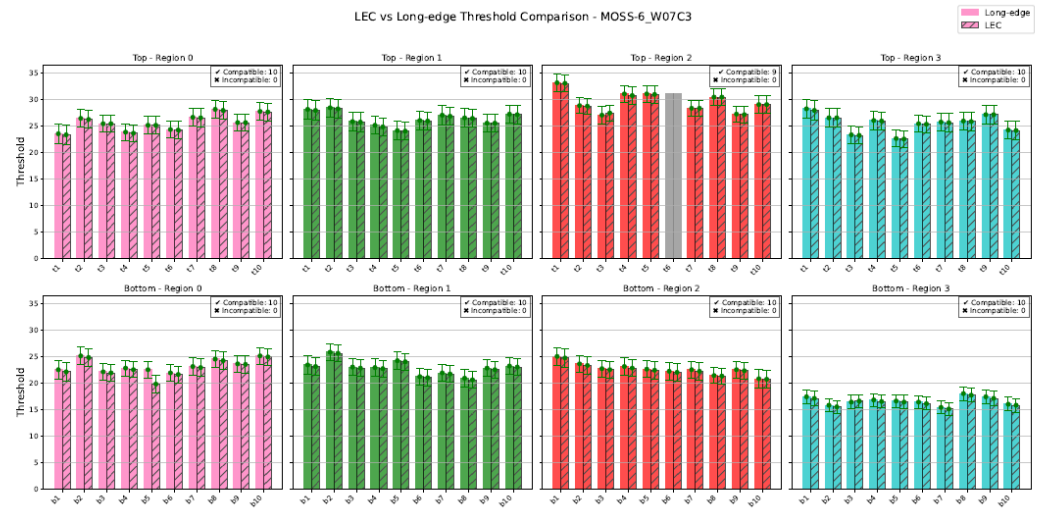
邓文静参与MOSS芯片的设计

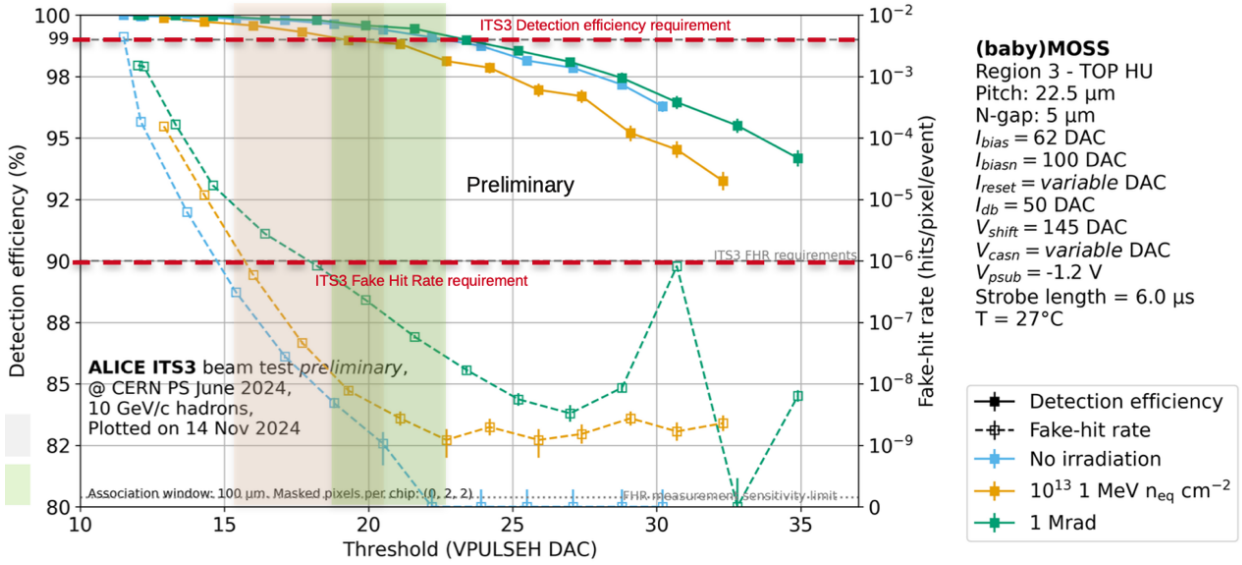
王淳正、赵子俊参与MOSS性能测试

MOSS芯片性能测试

- 实验室测试
  - ✓ 阻抗测试
  - ✓ 逐步上电-稳定性测试
  - ✓ 阻抗再测量
  - ✓ 成套功能测试
    - 供电，寄存器，位移寄存器，数模转换器，阈值和假击中率扫描
- 束流测试
  - ✓ 探测效率
  - ✓ 位置分辨率
  - ✓ 抗辐照能力

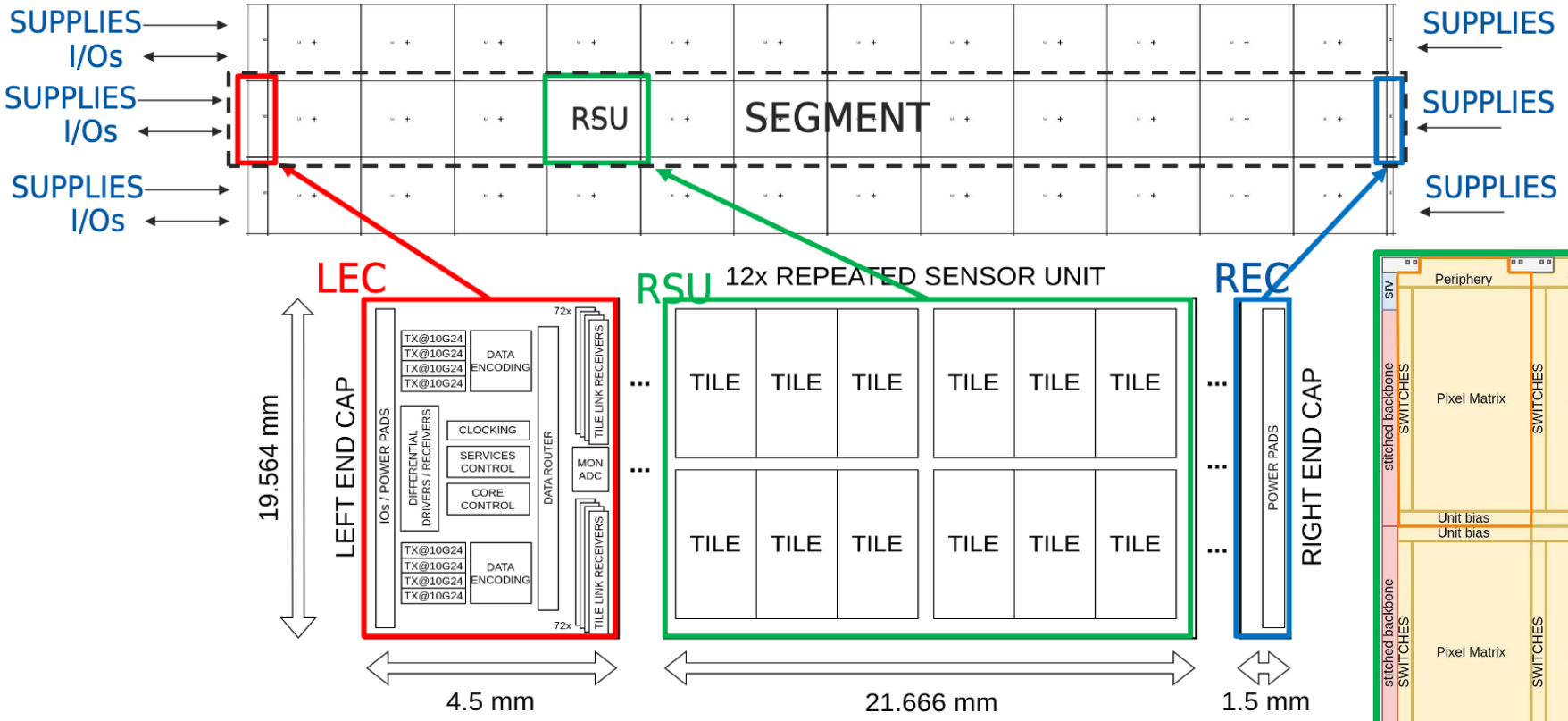






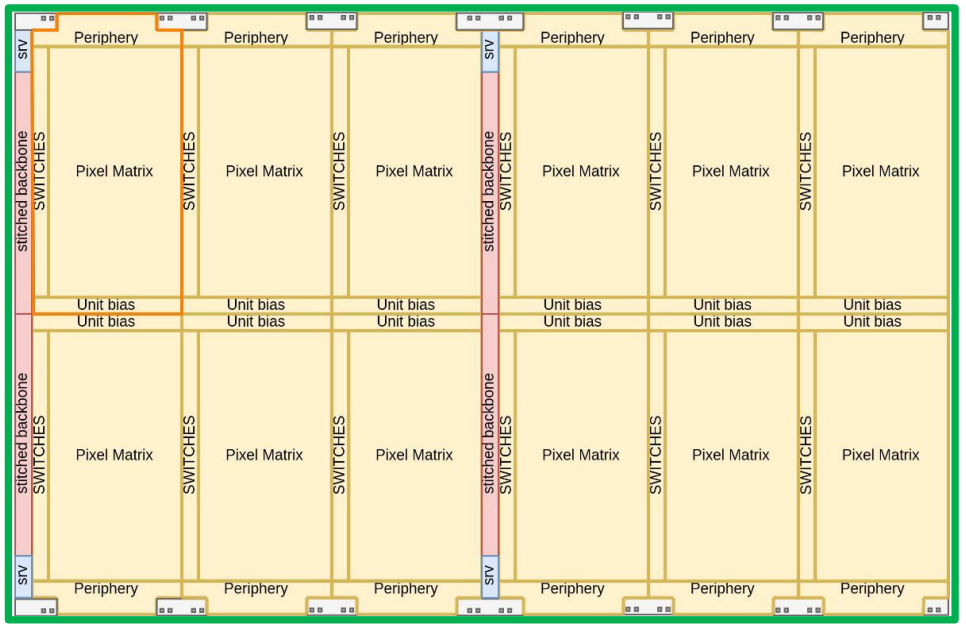
验证了MOSS芯片的性能符合设计预期，满足ITS3的需求

ER2芯片： MOSAIX总体结构



设计的硅像素传感器芯片的面积达97.8×266 mm^2, 达到中期考核指标

RSU组件及平面布局图



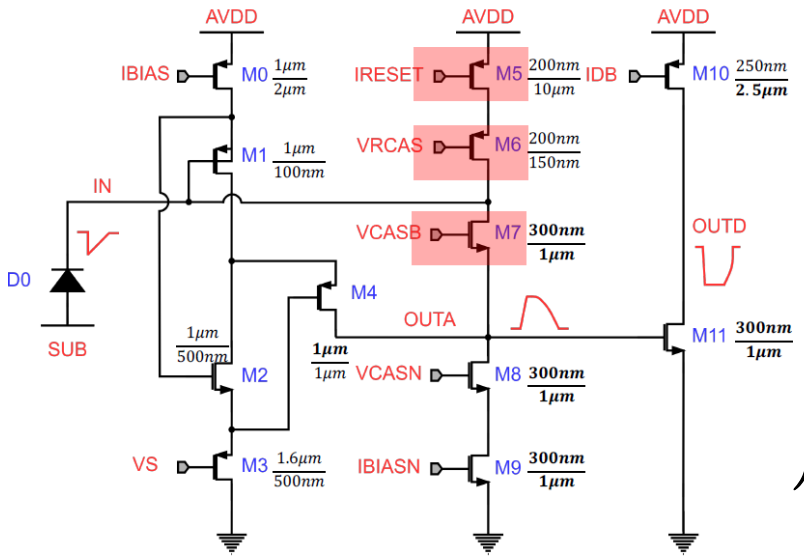
每个MOSAIX段由12各重复传感器单元(RSU)组成，每个RSU含12个瓦片 （TILE）

一个瓦片占L0层的1/864=0.116%

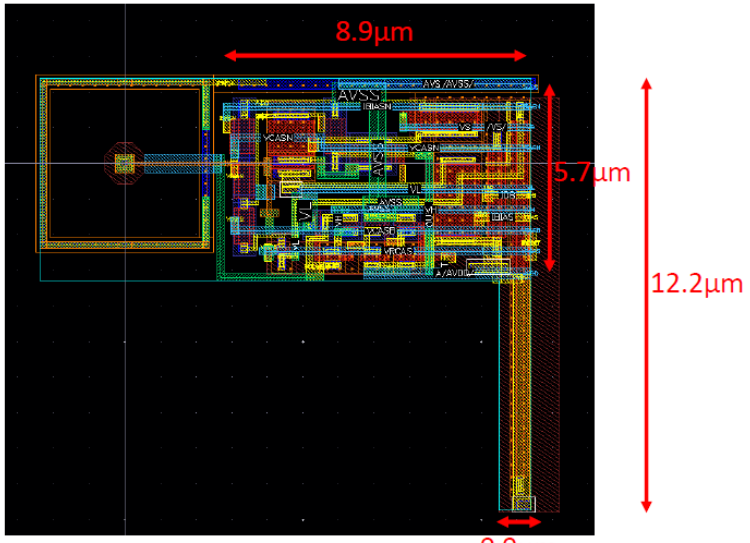
每个像素矩阵TILE分配独立的电源开关和外围传输电路，开关模块占用1个像素列约20微米，由四组的接骨架和标识对称排列构成

仝乔木参与MOSAIX芯片的设计与模拟验证

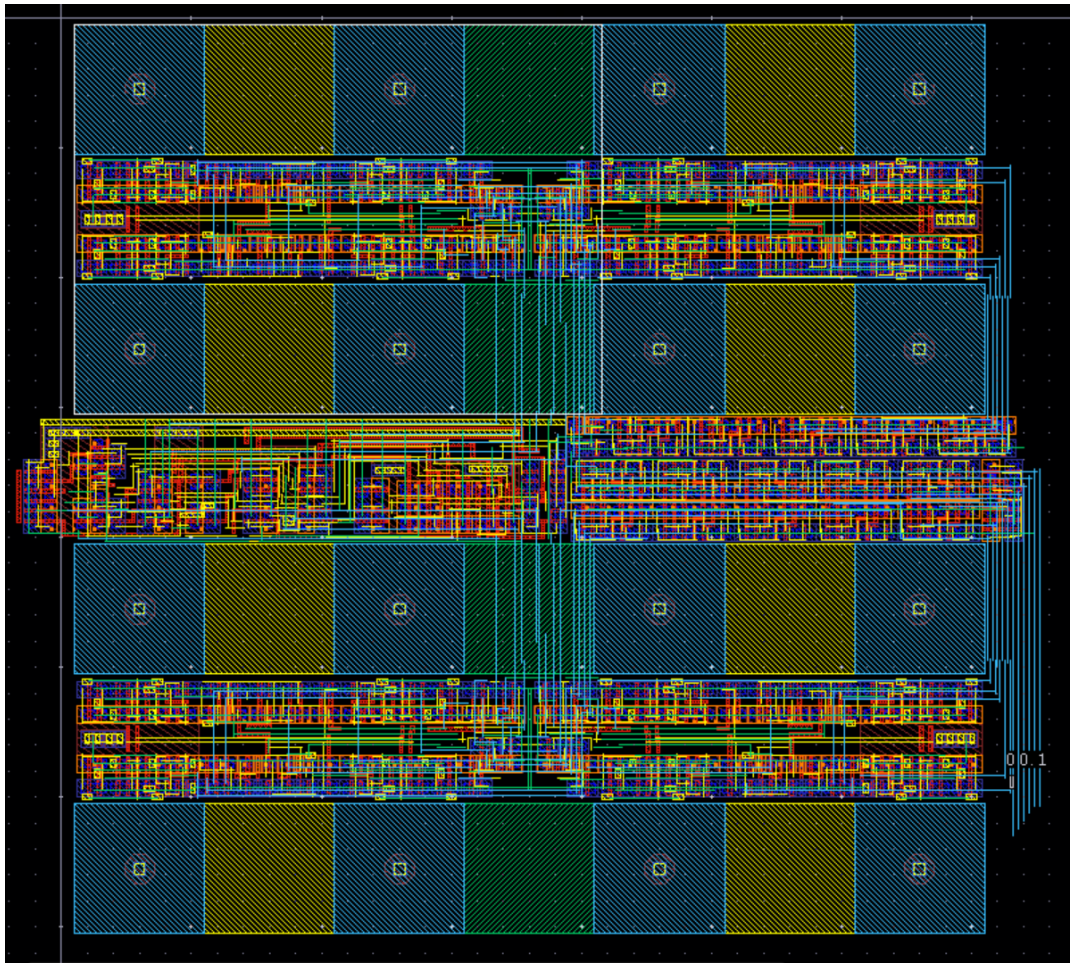
MOSAIX前端



原理图



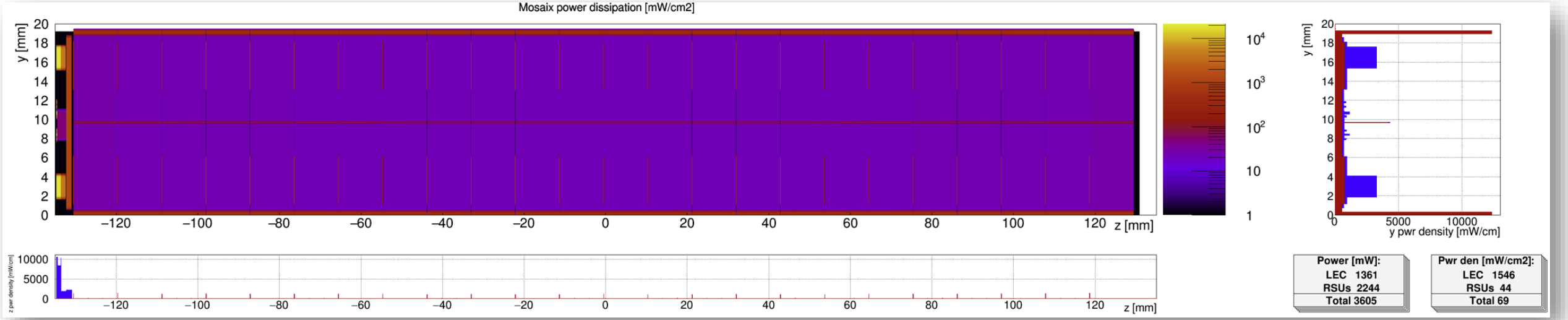
版图



数字前端读出结构布局布线

MOSAIX模拟验证

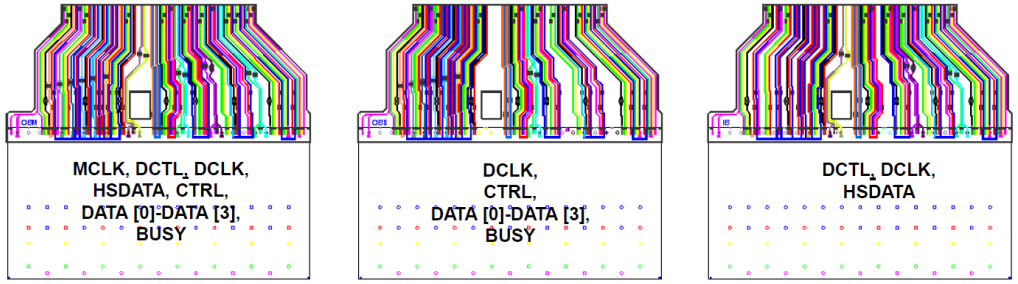
- MOSAIX的连线、设计规则检查、电气规则检查、天线效应检查、静电放电、高低压设计检查等物理验证与可靠性检查均已通过。
- 其余可能的设计规则检查（DRC）缺陷由代工厂进行审查。
- 对 MOSAIX 供电瞬态的模拟进行了全面的审核确认，以确保各种可能的改进随时都能为批量生产做好准备。

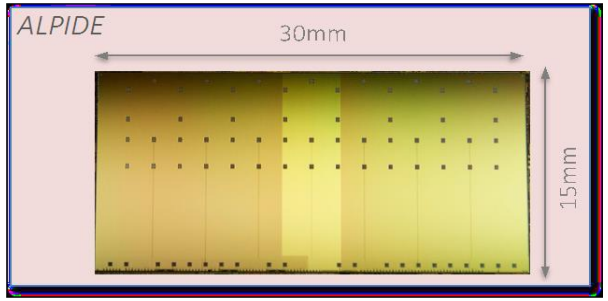


功率仿真分析

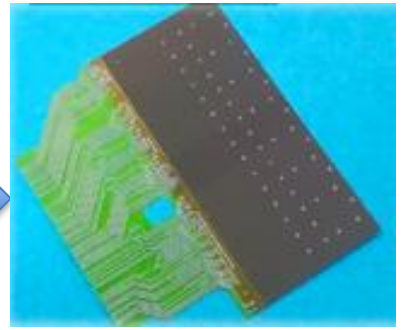
FoCal探测器硅像素层制作流程

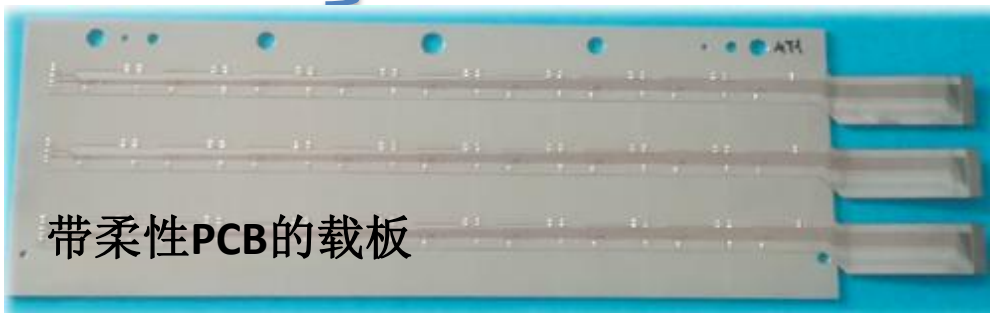
3 types of chip-cables





SpTAB





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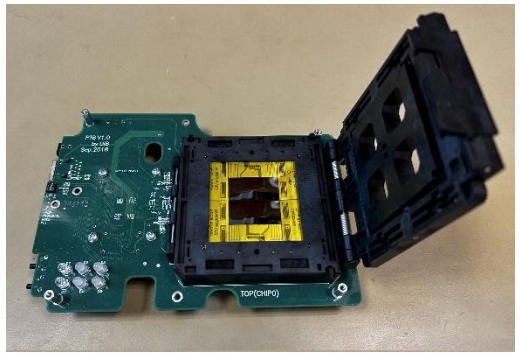
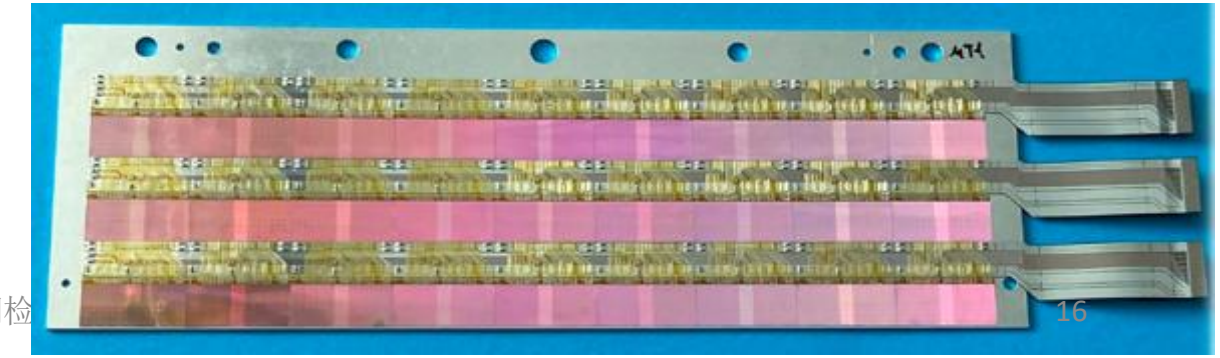


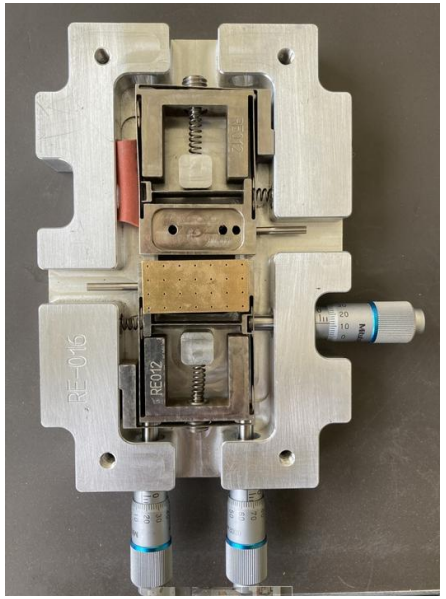
功能测试盒

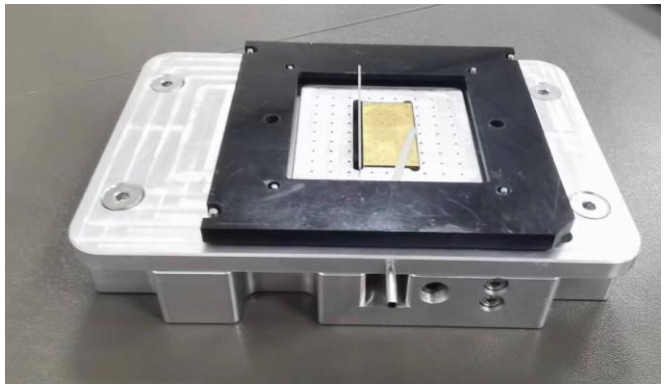


- 研制各种夹具
- 承担部分组装任务

FoCal硅像素层研制进展: 组装夹具研制

单芯片组装夹具研制

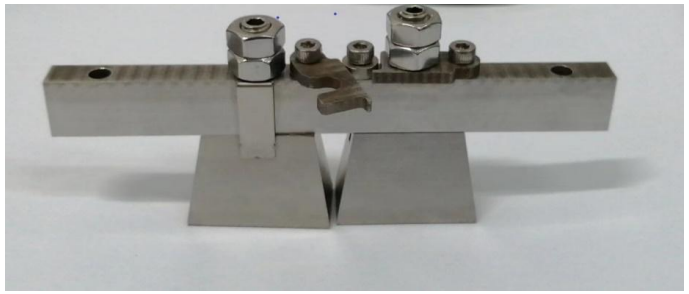




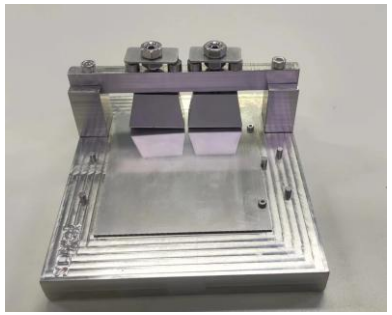
首次加工失败
通过热处理释放应力得以解决

- 2023 年 5 月 带 到 CERN进行验证
- 通过验证后，生产了3套，寄往各实验室
- 真空密闭性检验
- 用千分头进行功能测试

硅像素层模块组装夹具研制



在2023年底生产的第一次夹具测试样（含两种结构）

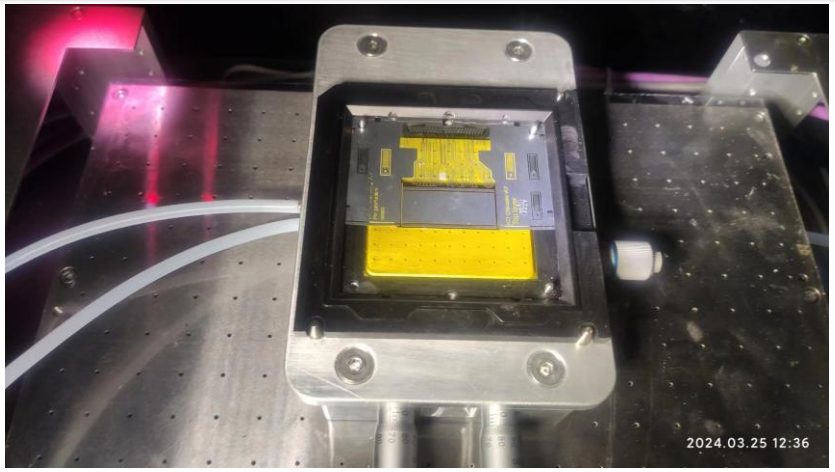


2024年4月生产的第二个夹具测试样

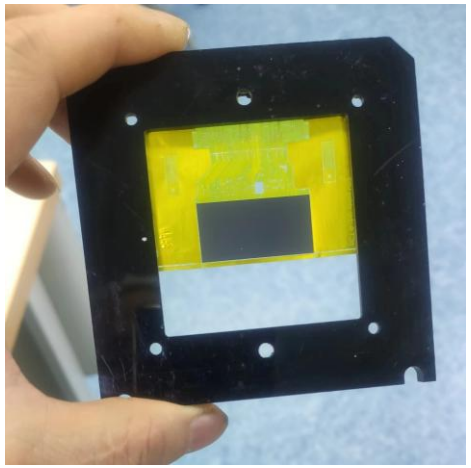
2024年8月生产的最终的组装夹具

2024年11月底寄到挪威奥斯陆

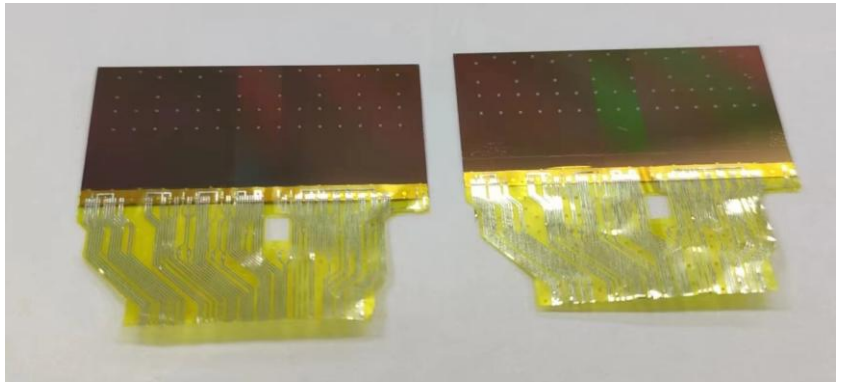
FoCal硅像素层研制进展: 组装流程测试



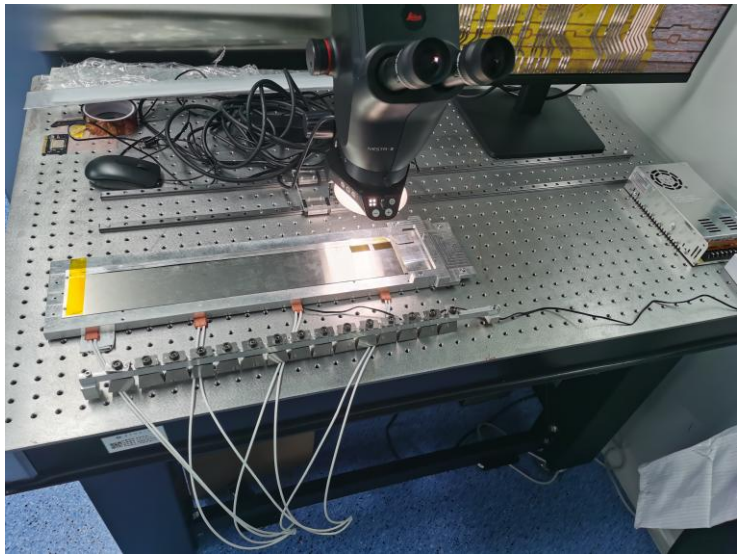
用F&K Delvotec G5 64000绑线机实现 SpTAB绑定



用手术刀裁下待组装部分

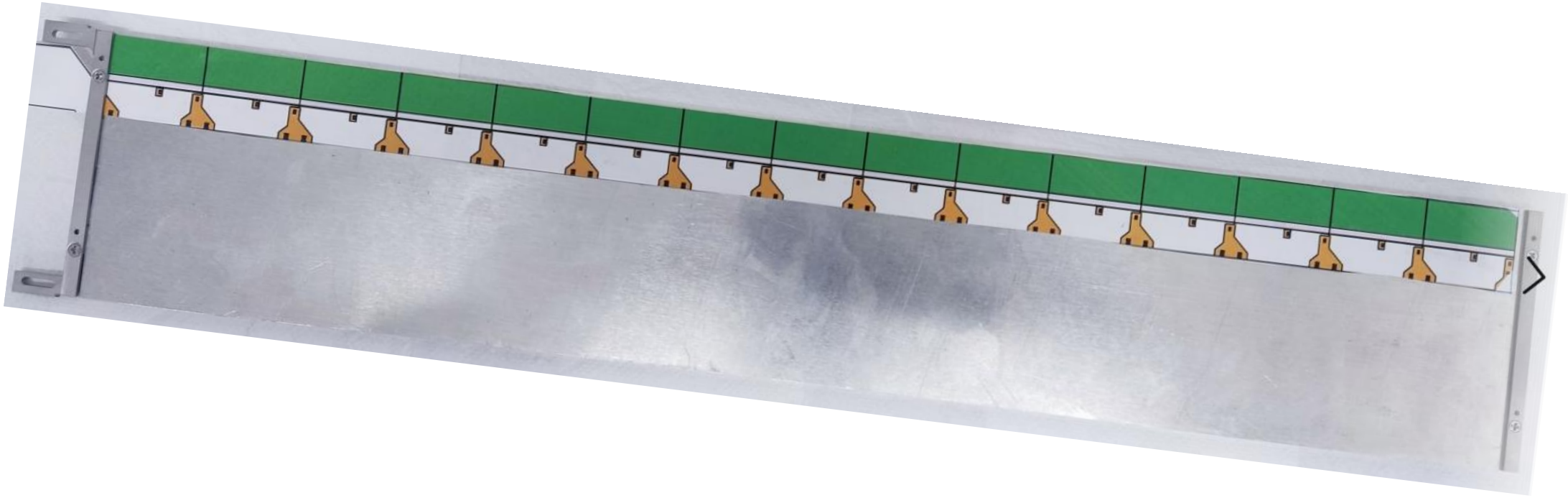


裁下的待组装部分



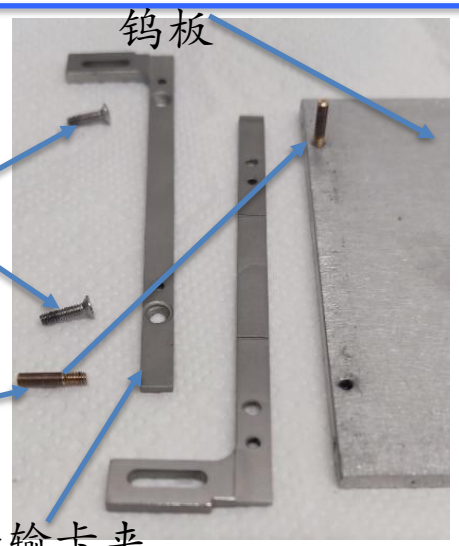
用工装夹具在带柔性条的载板上摆放待组装的芯片

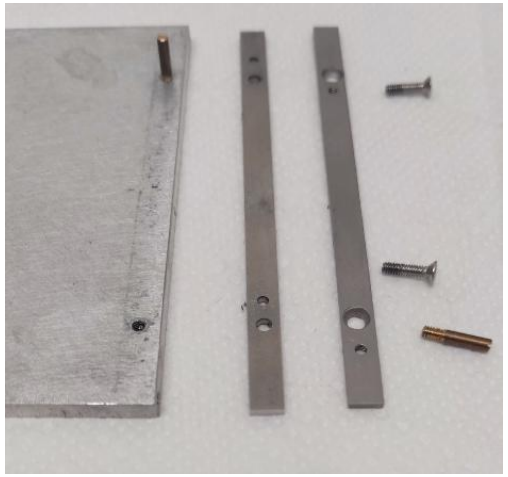
硅像素层模块机械实体样生产



- 生产了两套模块实体样组件
- 一套是铝合金的，一套是不锈钢的

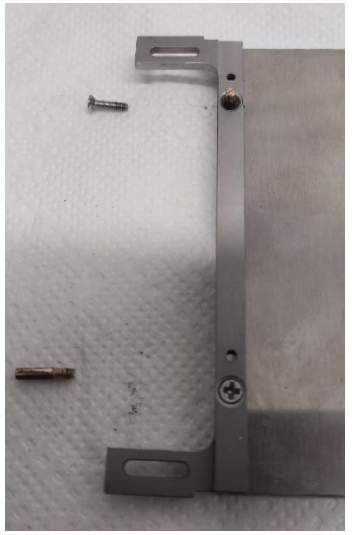
硅像素层模块机械件组装流程





所有部件

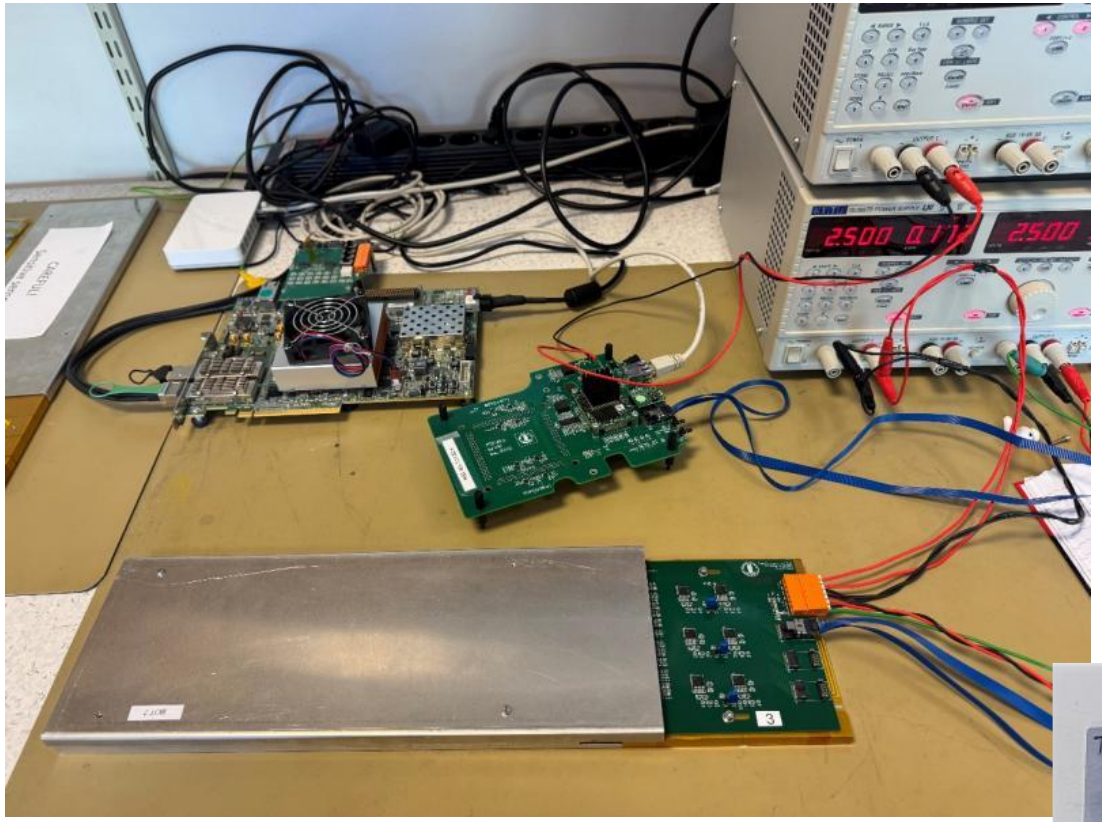
安装垫片



安装两个载板
和顶部垫片

固定所有部件，定位销
用于组装下一个模块

硅像素层样机实验室测试



测试清单:

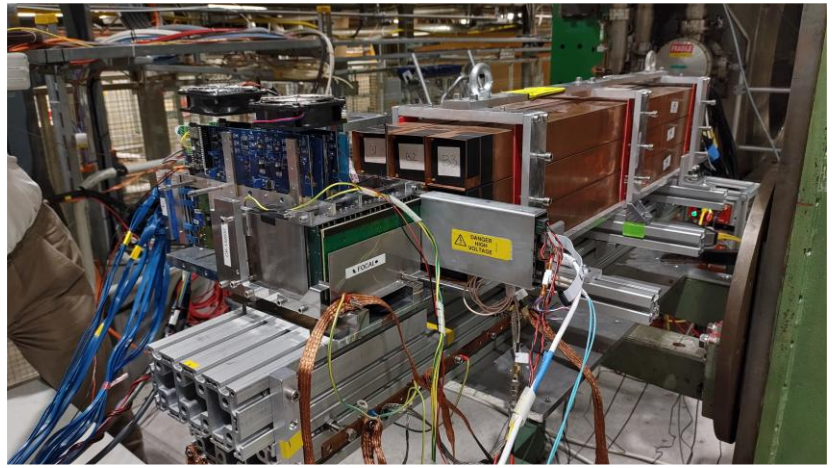
- 上电(AVDD, DVDD)
- 寄存器
- 高速传输链路
- FIFO
- 模拟电路扫描
- 数字电路扫描
- 阈值扫描
- ……

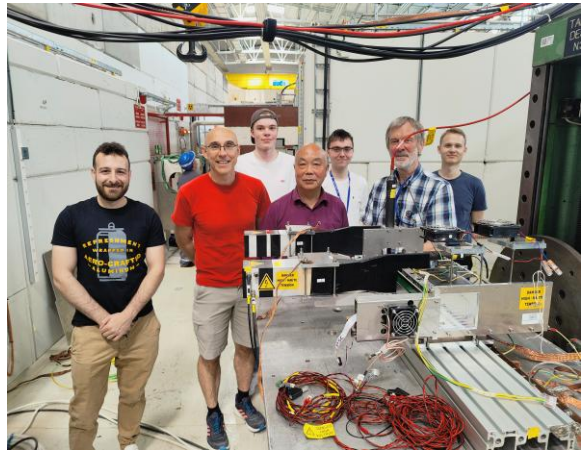
易杰在卑尔根大学参与硅像素层测试

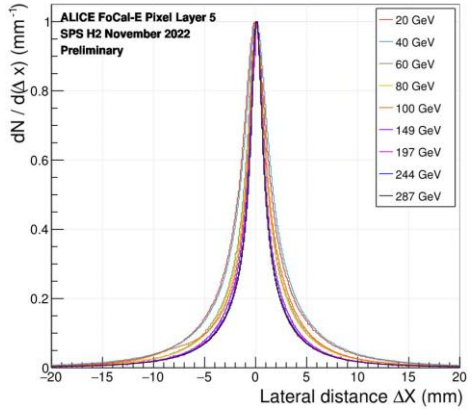
✓ 开发测试代码

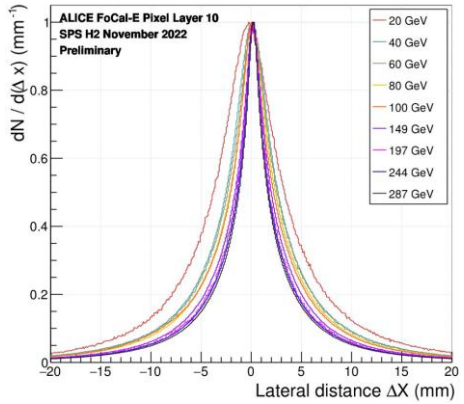
✓ 建立质控标准

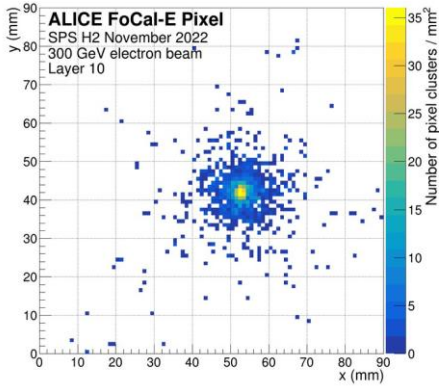
FoCal硅像素层研制进展: 束流测试及其数据分析

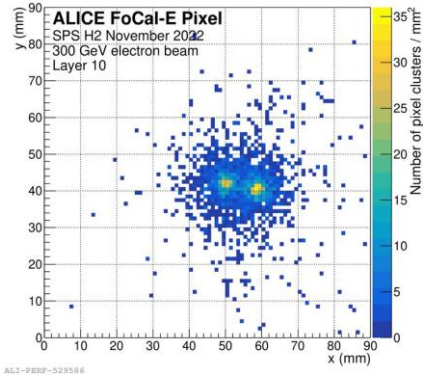












JINST 19 （2024）P07006 arXiv:2311.07413

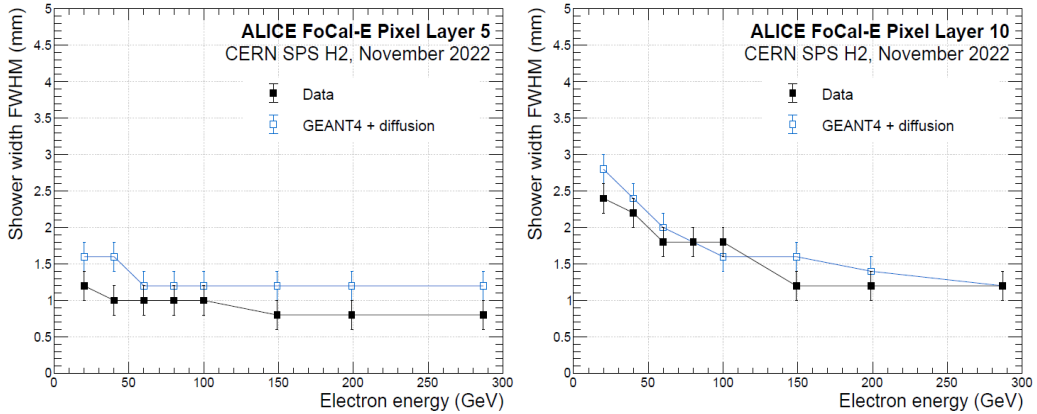
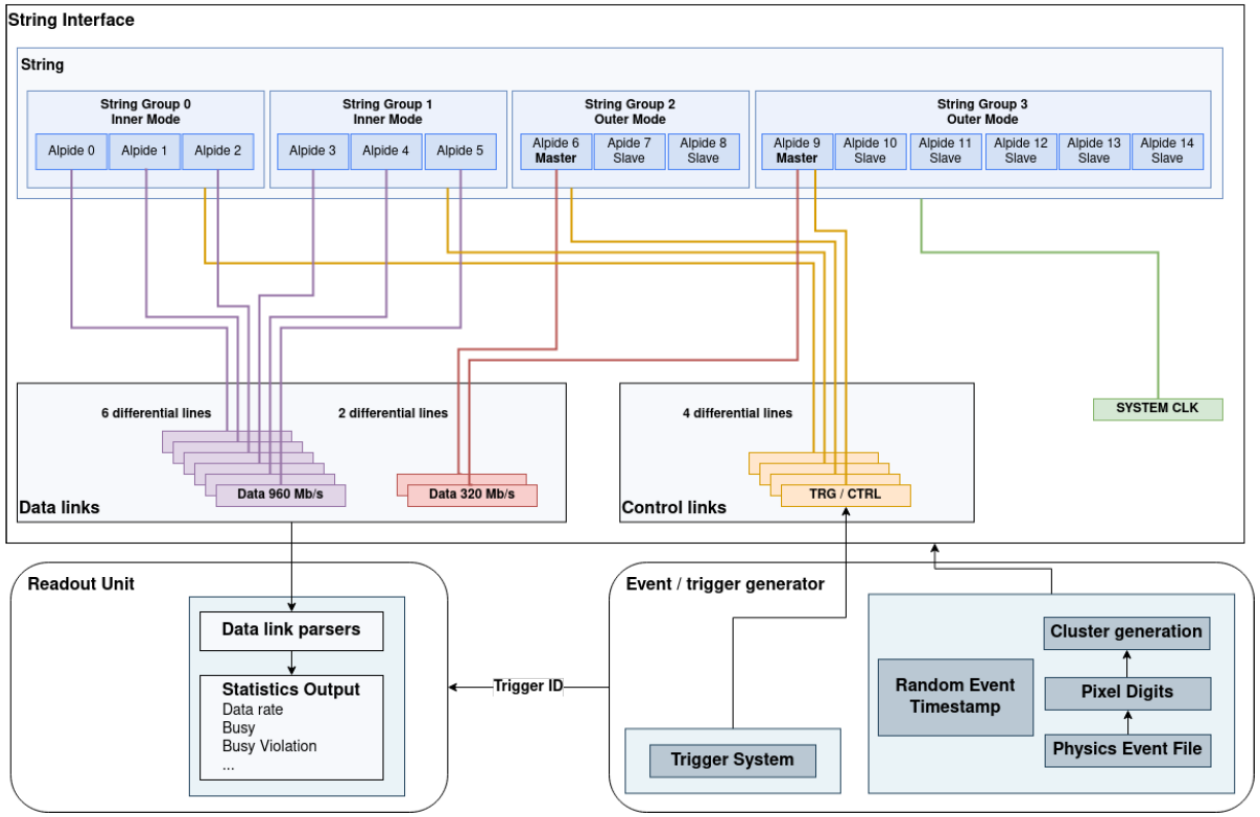


Figure 33. Measured and simulated FWHM for layer 5 (left panel) and 10 (right panel) versus electron energy. The error bars represent an uncertainty of 0.2 mm.

- 何柳参与了2022年9月份的束流测试
- 易杰和周老师参与了2023年6月份的束流测试
- 何柳负责分析了硅像素层束流测试数据，结果已发表在JINST上
- 簇射横向分布半高宽度可达 1 mm 左右，达到中期考核指标

SystemC 模拟

易杰负责完善了SystemC 模拟框架



- SystemC 模拟结果已经包含在2024年3月批准的技术设计报告TDR中.

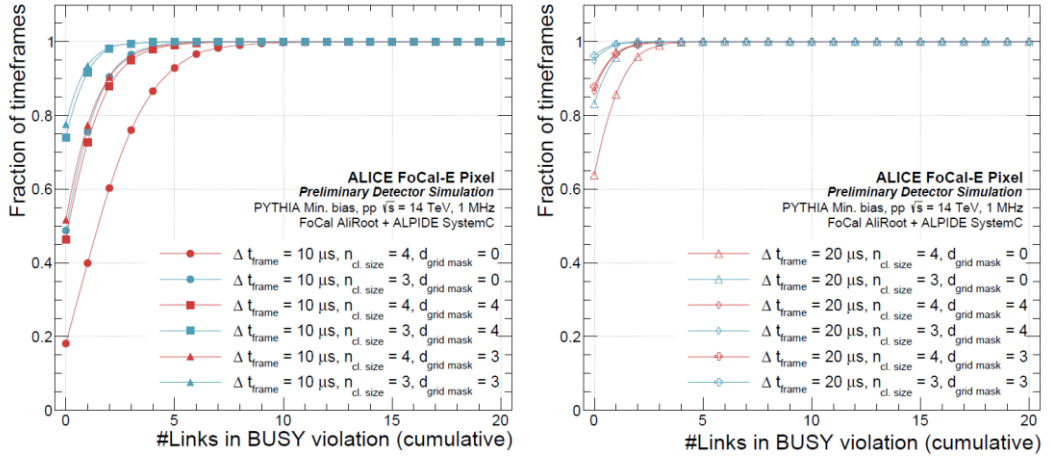
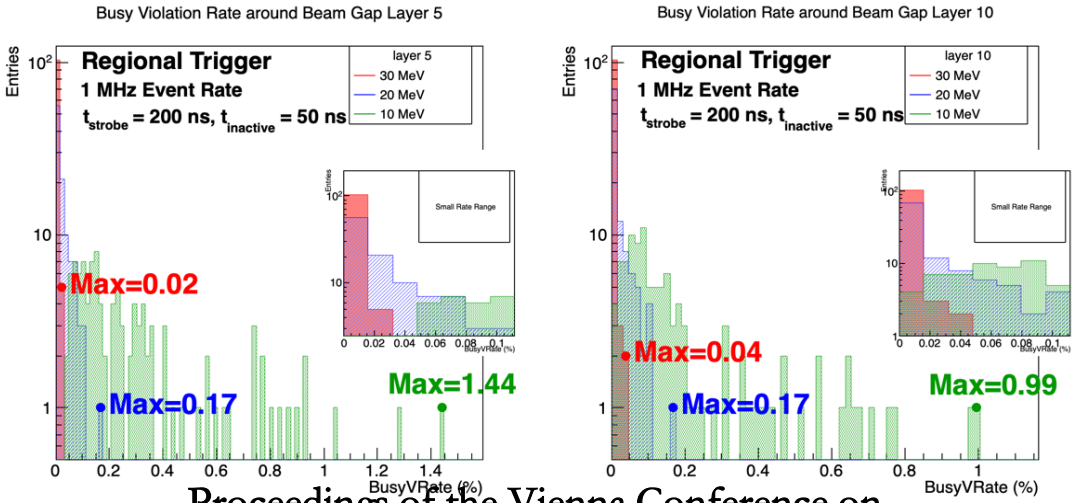
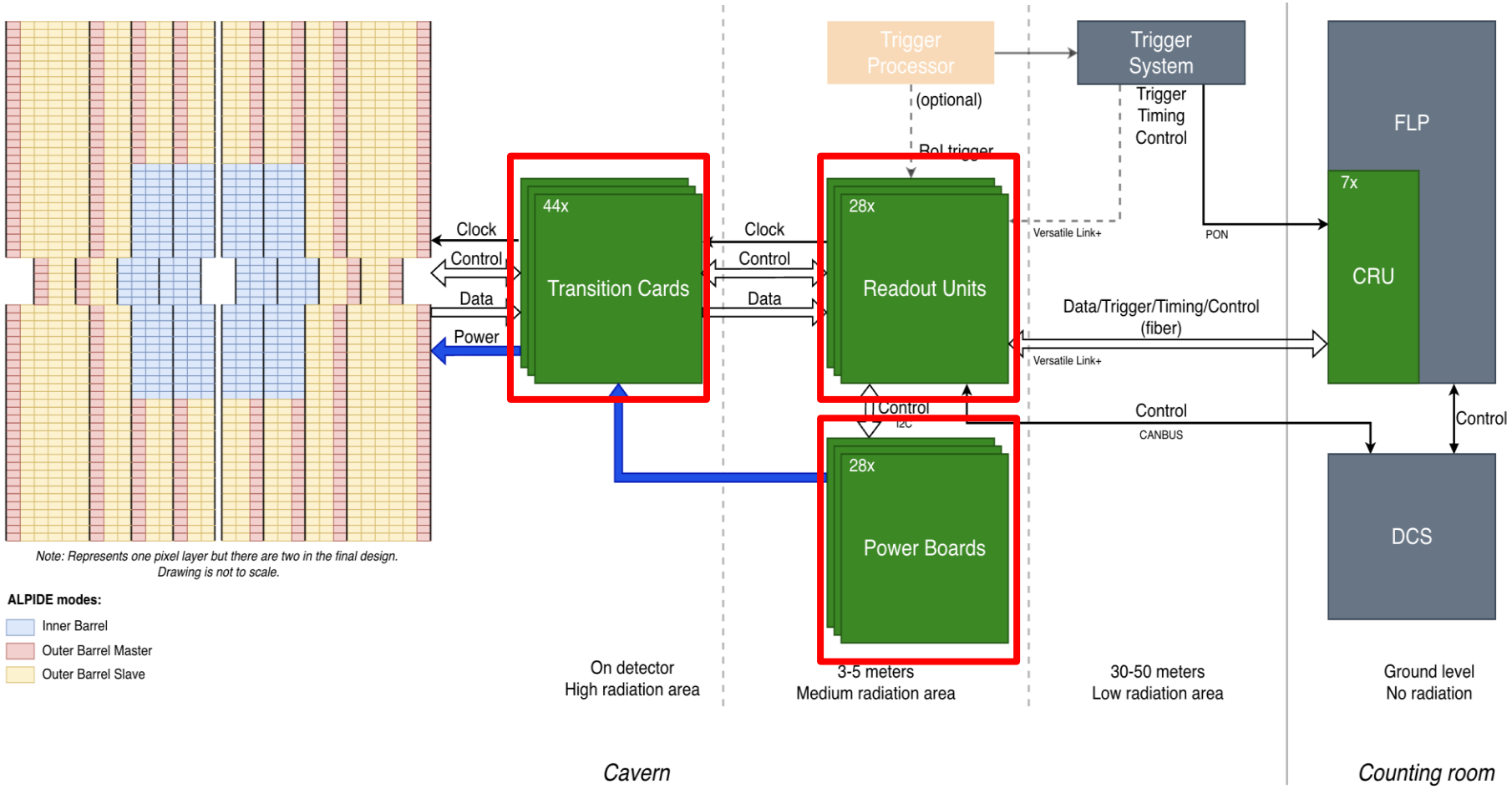


Fig. A.19: Fraction of frames with the cumulative number of links in BUSY violation for pp collisions, i. e. #Links with grid mask of $d_{\text{grid mask}} = 4$ and $d_{\text{grid mask}} = 3$, with two different timeframe lengths $\Delta t_{\text{frame}} = 10\,\mu\text{s}$ (left) and $\Delta t_{\text{frame}} = 20\,\mu\text{s}$ (right). The cumulative curves show the probability to encounter a timeframe with a maximum of #Links in BUSY violations.



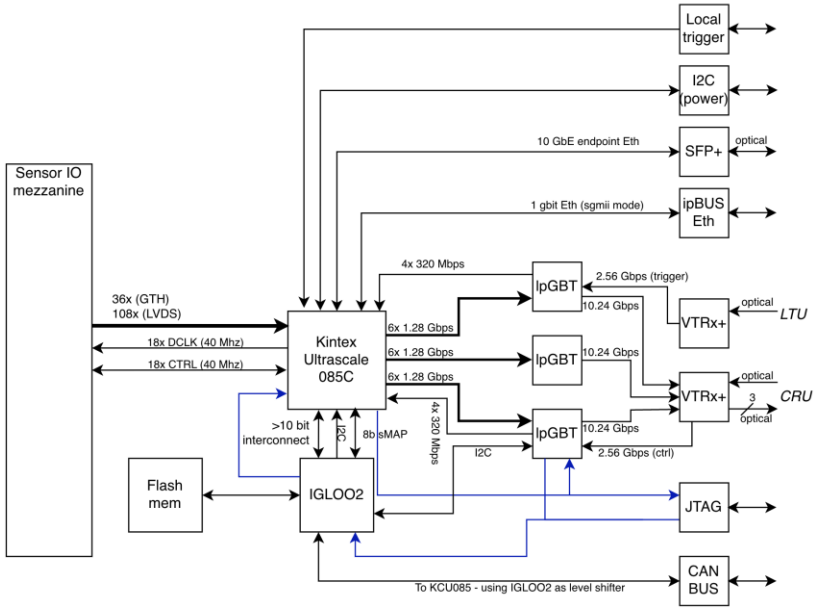
Proceedings of the Vienna Conference on Instrumentation 2025

硅像素层读出电子学系统

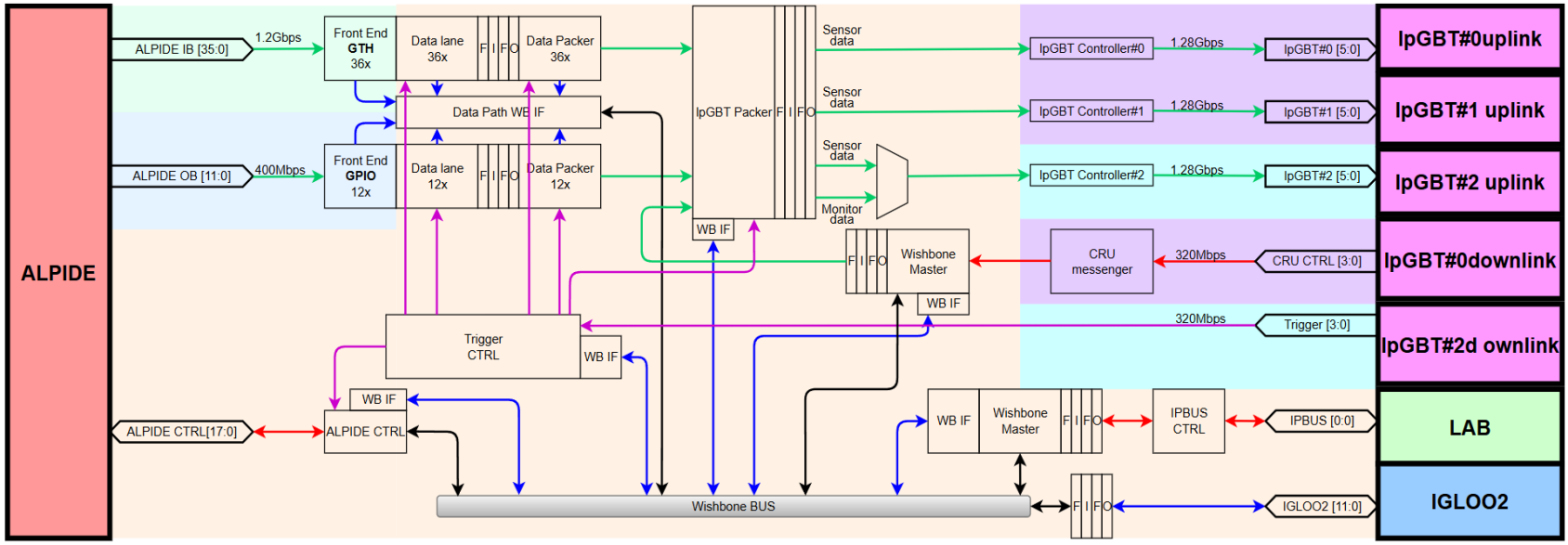


- ✓ 参加像素层读出系统设计
- ✓ 负责像素层读出单元主FPGA固件开发
- ✓ 负责转接板，背板设计与生产
- ✓ 参加电源板设计，负责电源板生产

硅像素层读出单元（RU）



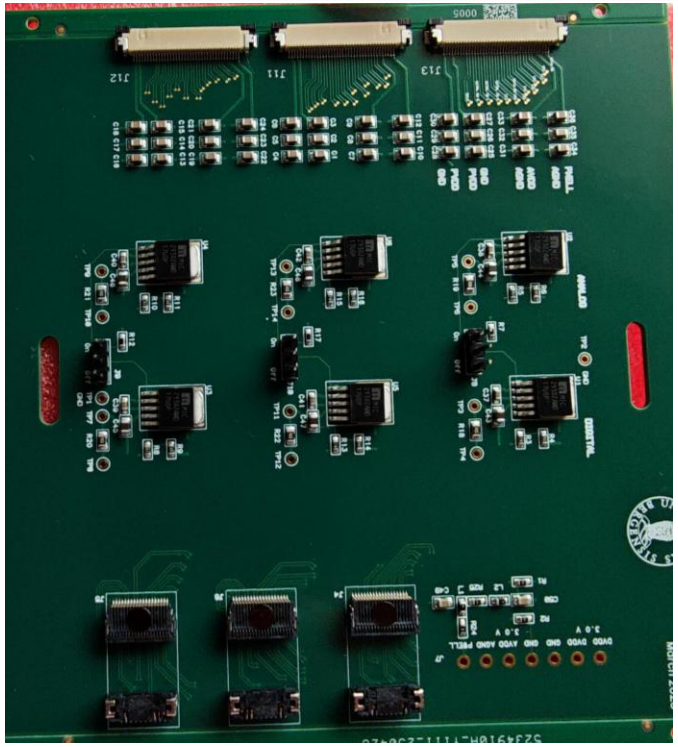
读出单元框图



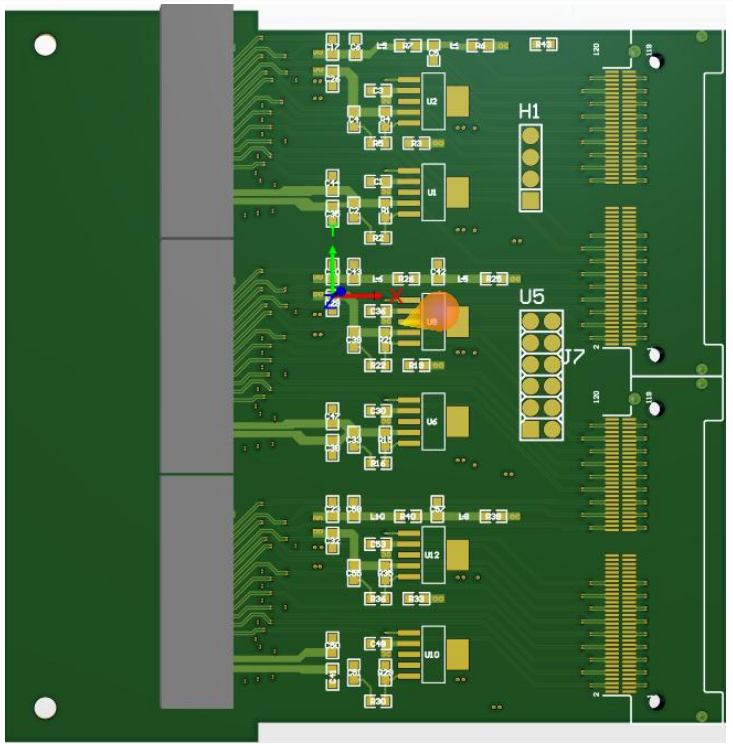
主FPGA固件逻辑模块图

- ✓ 参与了读出单元器件选型，功能定义，系统设计
- ✓ 确定主、辅FPGA，和数据传输链路（采用lpGBT和VTRX+）
- ✓ 参与了HPIO数据链路测试，HPIO-lpGBT-VTRX+测试
- ✓ 完成了主FPGA功能定义，模块划分，资源、功耗估计以及第一版测试固件设计
- ✓ 提出了三种lpGBT数据打包方案，正在进行数据传输效率模拟

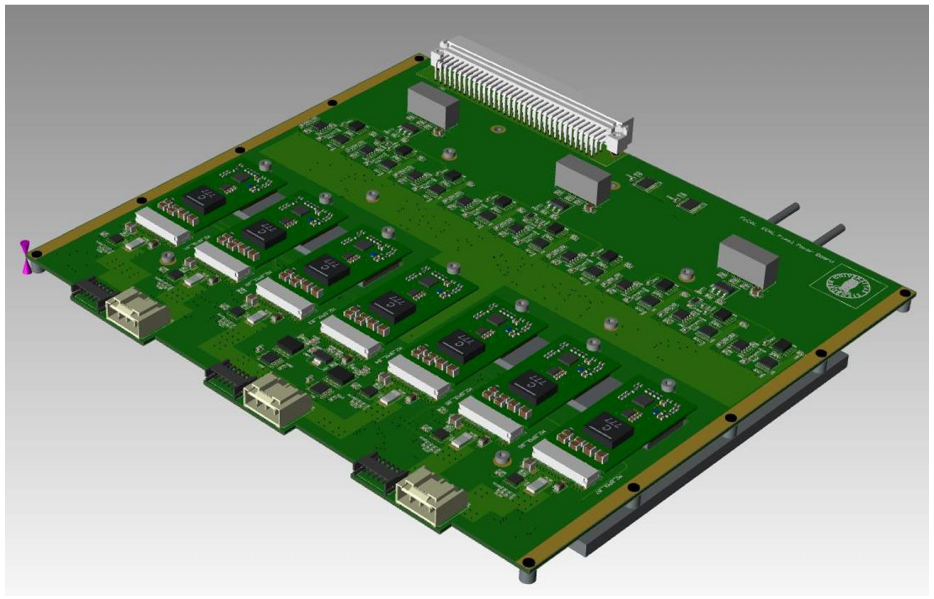
硅像素层读出电子学设计与生产



转接板测试板



FoCal转接板



FoCal电源板

- ✓ 设计了转接板测试板，五月份在国内生产后送至卑尔根大学进行测试
- ✓ 完成了转接板原理图和layout设计，等待检查和在中国生产
- ✓ 参与了电源板设计，等待最终检查和在中国生产

经费执行、文章发表和人才培养情况

经费执行情况（万元）

预算数	到位数	执行数	拨付课题承担单位
660	530	153	130

尚未开始量产

发表科技论文：7篇，其中SCI、EI收录5篇
学术会议报告：25人次
培养研究生毕业：9名，其中博士生2名

博士毕业2人：邓文静、智宇

硕士毕业7人：易杰、何柳、吝守龙、王浩桢、郭佳承、许天驹、唐倩

存在的问题

- “俄-乌冲突”导致乌克兰LTU不能如期交付铝基柔性电路板。（今年已经恢复正常生产，预期不会影响整个硅像素层的量产。）
- LHC运行计划发生了改变，第三次长停机（LS3）调整为2026年7月-2030年6月，这可能会致使ALICE升级项目的时间线的调整。目前预期其对本课题探测器研制任务的完成影响不大。
- ALICE合作组已对用于ALICE 第三代硅像素探测器的晶圆尺寸硅像素芯片的技术指标进行了调整。为此，需要对课题及项目考核指标进行相应的调整。

技术指标调整发言人证明信

ALICE Collaboration
https://alice-collaboration.web.cern.ch

Dr. Marco van Leeuwen
ALICE Experiment Spokesperson
EP Department - CERN
CH-1211 GENEVE 23
Tel. direct: + 41 22 767 8423
Tel.Secretariat: + 41 22 766 2525
Email: marco.van.leeuwen@cern.ch

Our reference: ALICE/MvL/mk/06-11-2024/093

Geneva, 6 November 2024

in the Letter of Intent, the impact on the overall performance was evaluated to be very small. A more detailed discussion can be found in the Technical Design Report (ALICE-TDR-021).

The design of the final prototype sensor is progressing well and we expect to submit the design for production in 2025. ALICE and the ITS3 project welcome the contributions of the CCNU group to the design and testing of prototypes and look forward to the continued collaboration in the coming years.

Yours sincerely,

Dr. Marco van Leeuwen
ALICE collaboration Spokesperson

The CCNU group is participating the design and characterization of the ITS3 sensors with 3 students who are stationed at CERN to work together with the design and characterization teams. The goal of the final design is to design a large-scale stitched pixel sensors with integrated readout circuits. Based on the R&D experience and the requirements of the geometry of the final detector, the final design will use a pixel size of 20.8 μm x 22.8 μm, which is expected to give a space point resolution of better than 5 μm and a power density below 50 mW/cm^2. While the pixel size is slightly larger than the goal that was originally formulated

area to a minimum. R&D on mechanical integration and air cooling solutions has demonstrated that the detector can cooled effectively with (average) power density up to about 50 mW/cm^2 over the full sensor area. The project is now moving towards the final design phase.

The CCNU group is participating the design and characterization of the ITS3 sensors with 3 students who are stationed at CERN to work together with the design and characterization teams. The goal of the final design is to design a large-scale stitched pixel sensors with integrated readout circuits. Based on the R&D experience and the requirements of the geometry of the final detector, the final design will use a pixel size of 20.8 μm x 22.8 μm, which is expected to give a space point resolution of better than 5 μm and a power density below 50 mW/cm^2. While the pixel size is slightly larger than the goal that was originally formulated

总结

- 课题组按计划在实施承担的ALICE在LS3期间的升级任务，达到预期目标
  - ✓参与研发的ITS3晶圆级超薄柔性硅像素芯片已通过验证、提交流片
  - ✓参与研制的FoCal探测器硅像素层样机的双光子位置分辨已达到mm量级
- 课题组开展的相关工作
  - ✓参与完成了模拟、数字测试芯片和ER1 MOSS芯片性能表征
  - ✓参与完成了ER2 MOSAIX芯片设计和模拟验证
  - ✓已研制出单ALPIDE芯片工装夹具和硅像素层的工装夹具
  - ✓参与研制了硅像素层模块样机及其实验室和束流测试
  - ✓合作完成了像素层读出系统级设计
  - ✓完成了读出单元第一版测试固件开发，等待测试
  - ✓完成了测试转接板生产，完成了转接板、电源板设计，等待检查和在中国生产
  - ✓负责分析了硅像素层束流测试数据，结果已经发表在JINST上
  - ✓对硅像素层读出系统进行了系统模拟，结果被包含在TDR之中

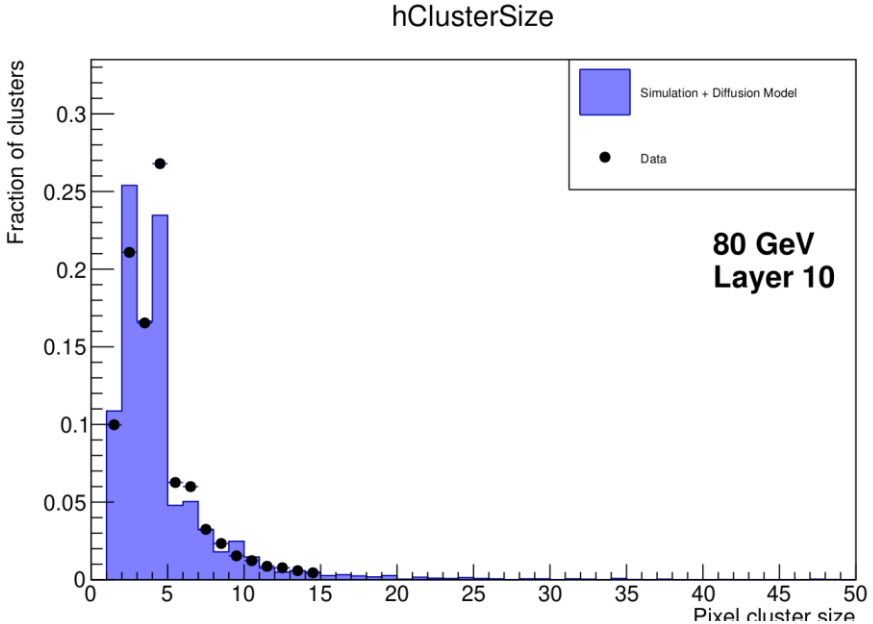
谢谢各位专家的指导!

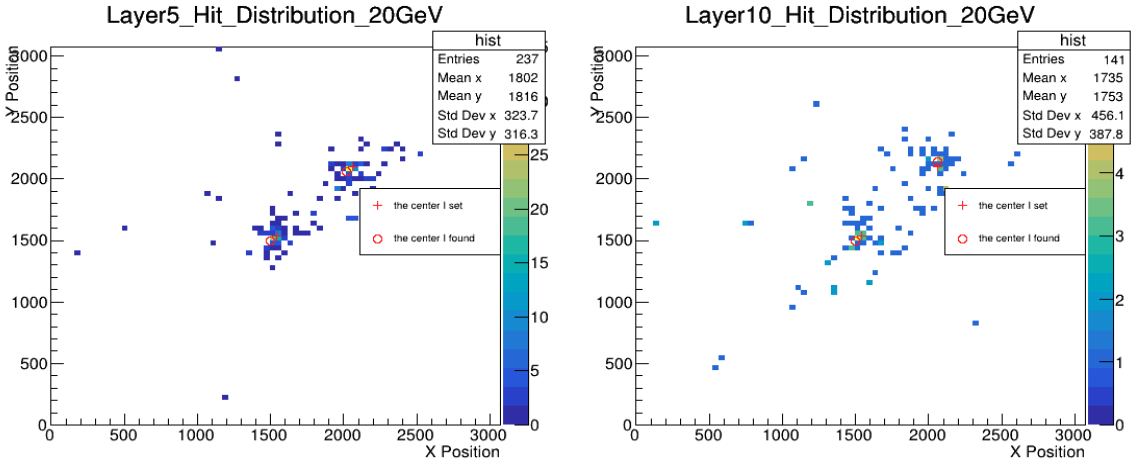
发表论文列表

1. Digital pixel test structures implemented in a 65 nm CMOS process，Gianluca Aglieri Rinella et al., Nuclear Instruments and Methods in Physics Research A 1056 (2023) 168589.
2. 单片型像素探测器及其应用研究进展. 邓文静，殷中宝，王亚平，等. 中国科学: 物理学力学天文学, 2023, 53: 290019.
3. Performance of the electromagnetic and hadronic prototype segments of the ALICE Forward Calorimeter, M. Aehle et. al, JINST 19 (2024) P07006.
4. A 14-Bit Digital to Analog Converter for a Topmetal-CEE Pixel Readout Chip, Yunqi Deng, Ping Yang, Guangming Huang, Jun Liu, Zhongguang Ren, Yan Fan and Zixuan Song, Electronics 13 (2024) 3074.
5. A 14-bit 100 MS/s two-step split SAR ADC with a low-power high-linearity residue amplifier，P. Yang et. al, JINST 20 (2025) C05036.

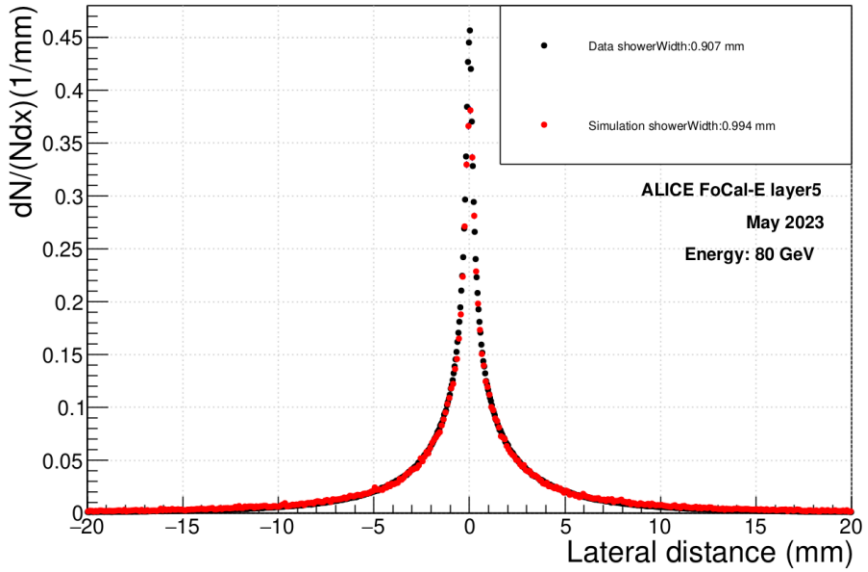
6. 用于FoCal量能器的高精度电荷读出电子学研究，吝守龙，李笑梅等，航天器环境工程, 第42卷, 2025年2月.
7. 硅像素探测器X 射线探测效率实验研究，刘军，杨晨飞等，实验科学与技术, 第22卷第4期，2024年8月.
8. 粒子探测器基于分立元件的多用途宽动态范围前端电子学研究，郭佳承，王浩祯，吝守龙，贾世海等，核电子学与探测技术（已接收）.
9. Expected performance of the ALPIDE pixel layers in ALICE FoCal, J.Yi and M. P. Rauch (for the ALICE Collaboration), Nuclear Instruments and Methods in Physics Research A（已接收）.
10. 紧凑型闪烁光纤探测系统研究，许天驹，吝守龙，智宇等，核电子学与探测技术（已接收）.

探测器GEANT4模拟

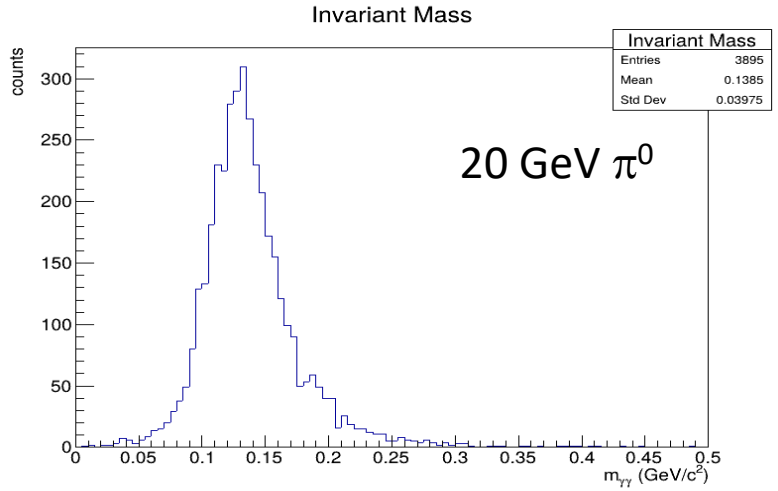




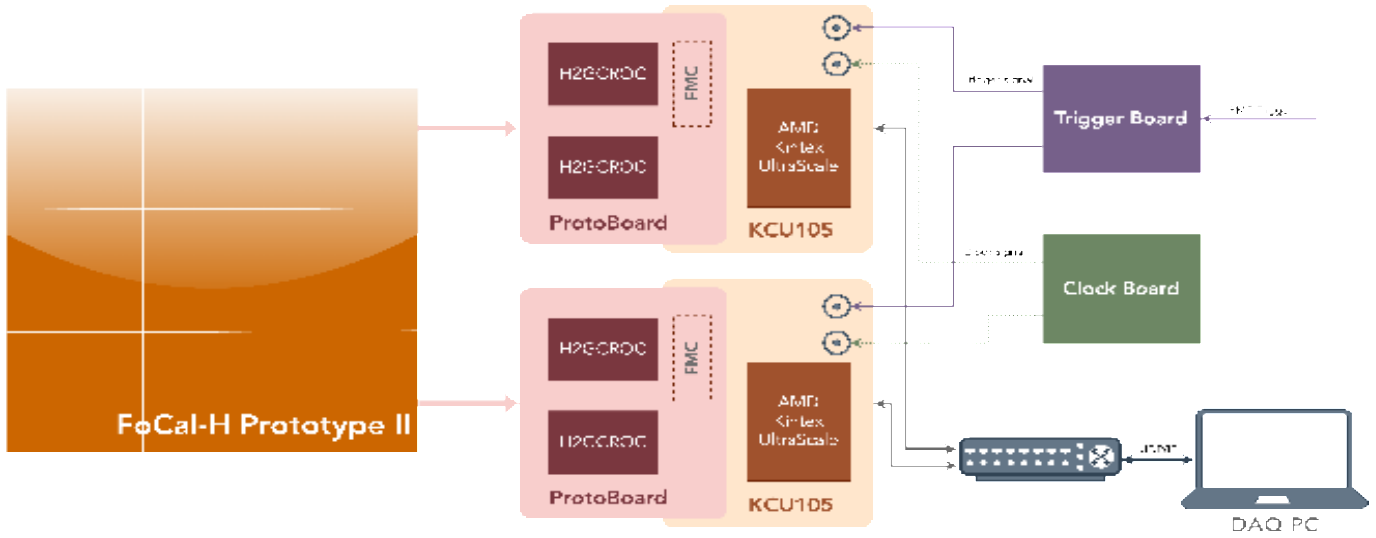
- 用像素层确定PAD层簇射的中心位置
- 基于簇射的径向分布，分解有交叠的簇团
- 将源于同一粒子的各层簇团能量相加
- 计算双簇团的不变质量

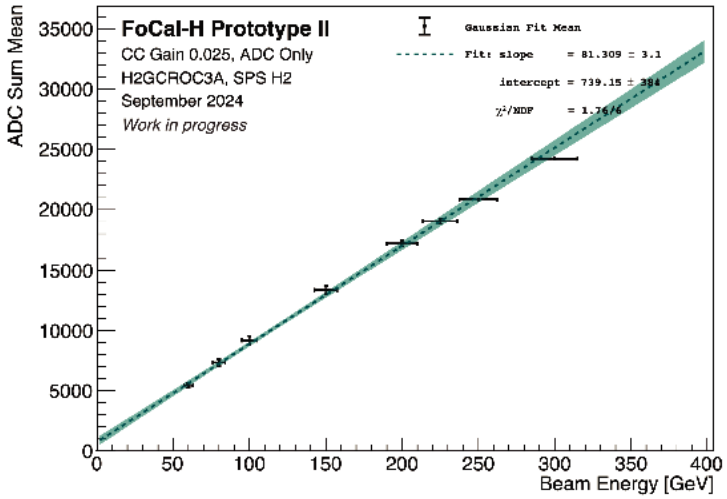


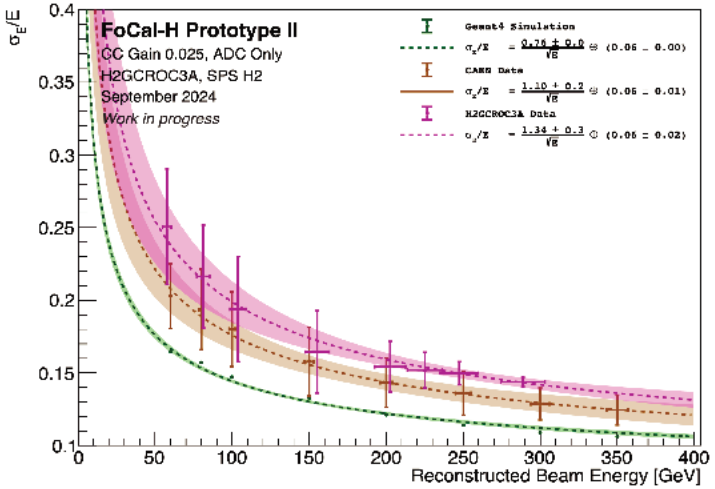
引入扩散效应，
模拟数据能够比
较好地符合束流
测试结果



FoCal强子量能器读出电子学系统

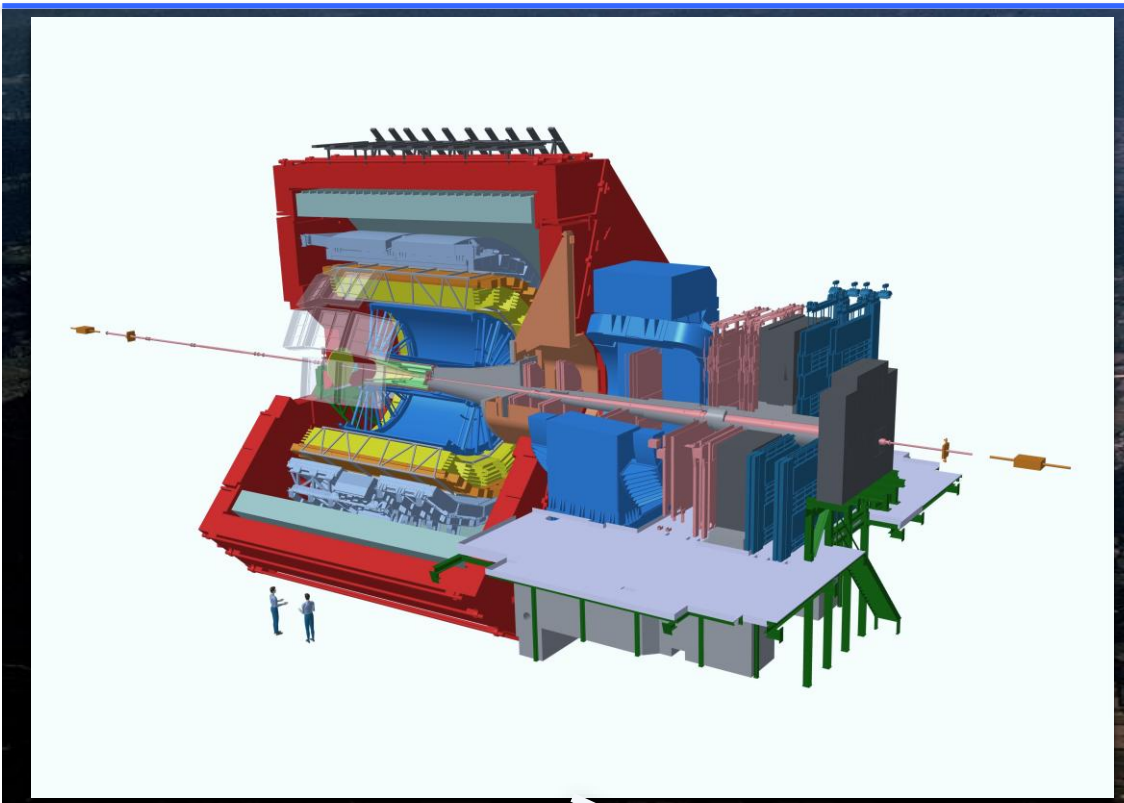






- ✓ 参与了基于HGCROC芯片的读出电子学系统的搭建。
- ✓ 参与了2024 年在SPS H4进行的束流测试，负责开发了读出软件系统，并主导了测试数据分析。
- ✓ 对基于 H2GCROC 芯片的电子学读出系统进行性能评估。
  - ✓ 在最小增益下，系统在 60 – 300 GeV 能量扫描中有良好的响应线性。
  - ✓ 能量分辨率为 $(1.34 \pm 0.3)/\sqrt{E} \oplus (0.06 \pm 0.02)$，与 2023 年使用商业读出系统获得的分辨率相当。

课题简介



- ALICE是LHC上唯一致力于重离子碰撞物理的大科学装置。
- 研究夸克-胶子等离子体（QGP）的性质及其演化规律，以深入理解由量子色动力学（QCD）主导的多粒子系统的特性，认识早期宇宙及其演化规律。

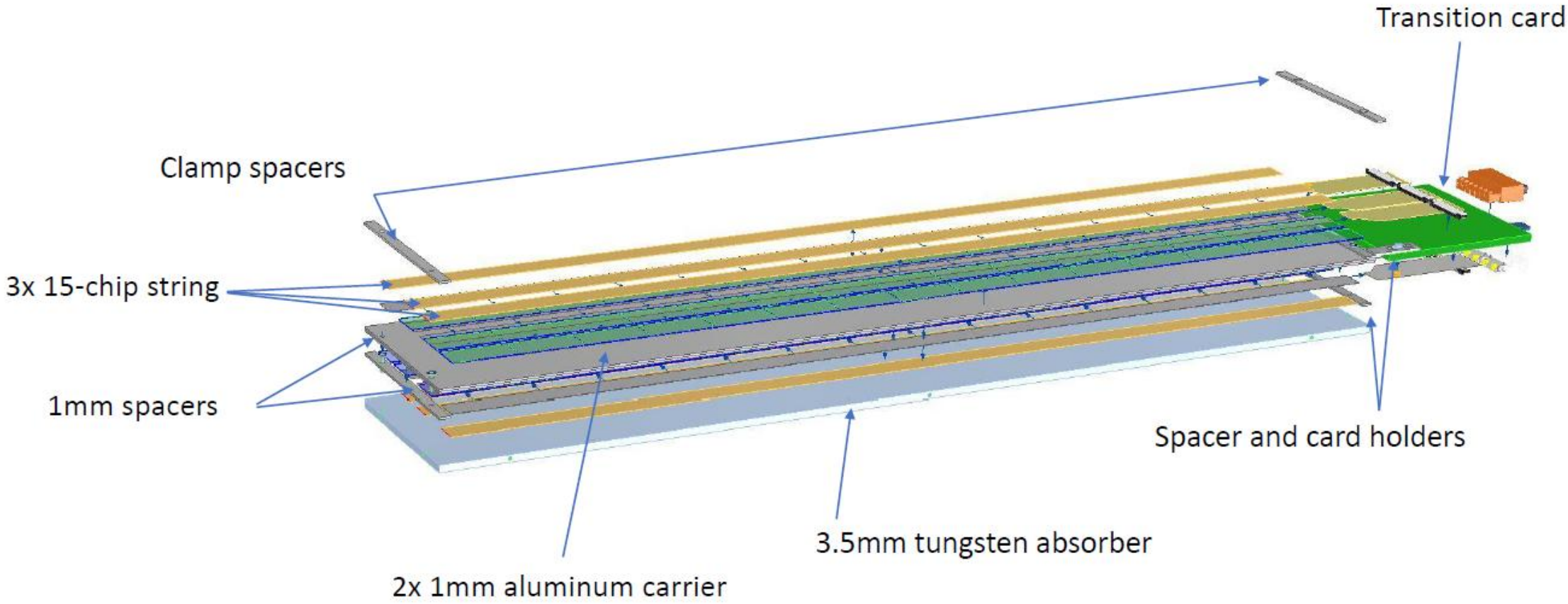
~40个国家，~172个大学和研究机构，~2000名科学家和工程技术人员

探测器建造费用： 200 M 瑞郎

本次升级总经费：18 M 瑞郎

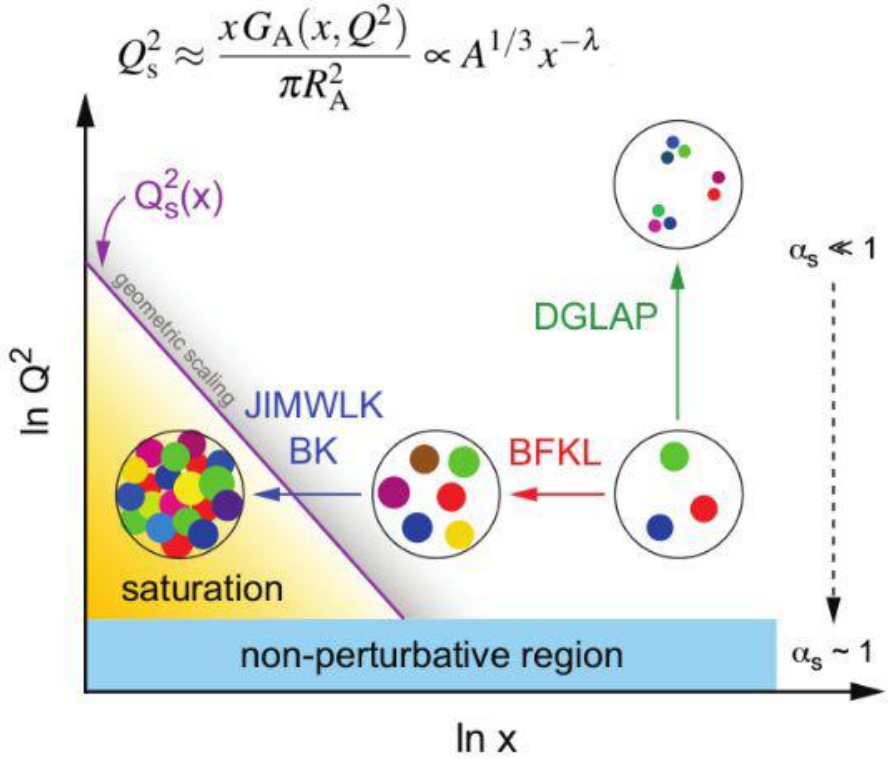
→ 中国组预期贡献：~2.8 %

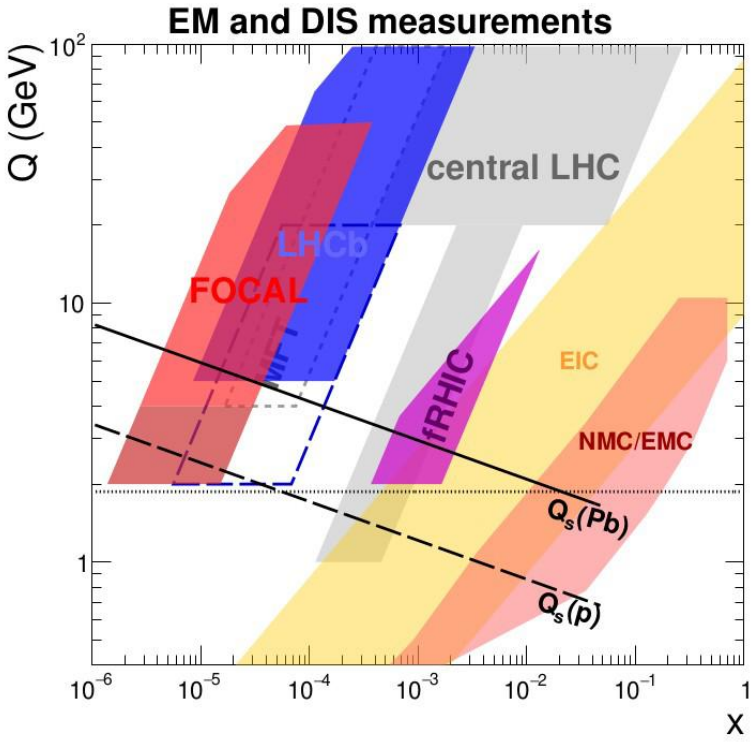
FoCal硅像素层的结构

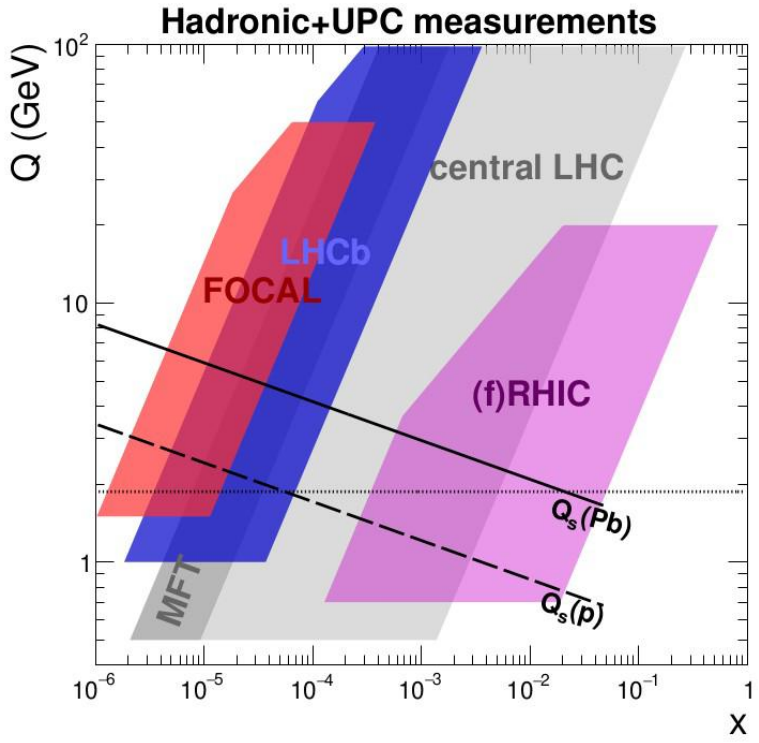


Total thickness = 3.5 (absorber) + 1.0 (spacer) + 1.0 (carrier) + 1.0 (carrier) + 1.0 (spacer) + 1.0 (spacer) = **8.5mm**

FoCal的物理目标





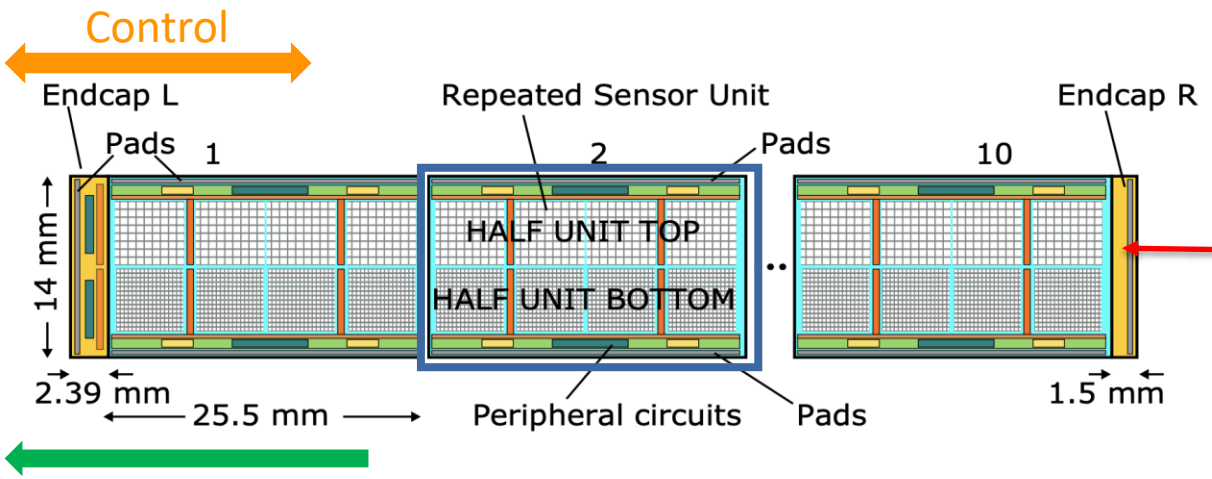


- FoCal将拓展*Q*-*x*探测区域，x低至10^{-6}，*Q*达4 GeV→测量质子-质子碰撞中前向快度区直接光子的横动量谱
- 研究小*x*物理及QCD非线性动力学→测量π^0-π^0和γ-π^0方位角关联

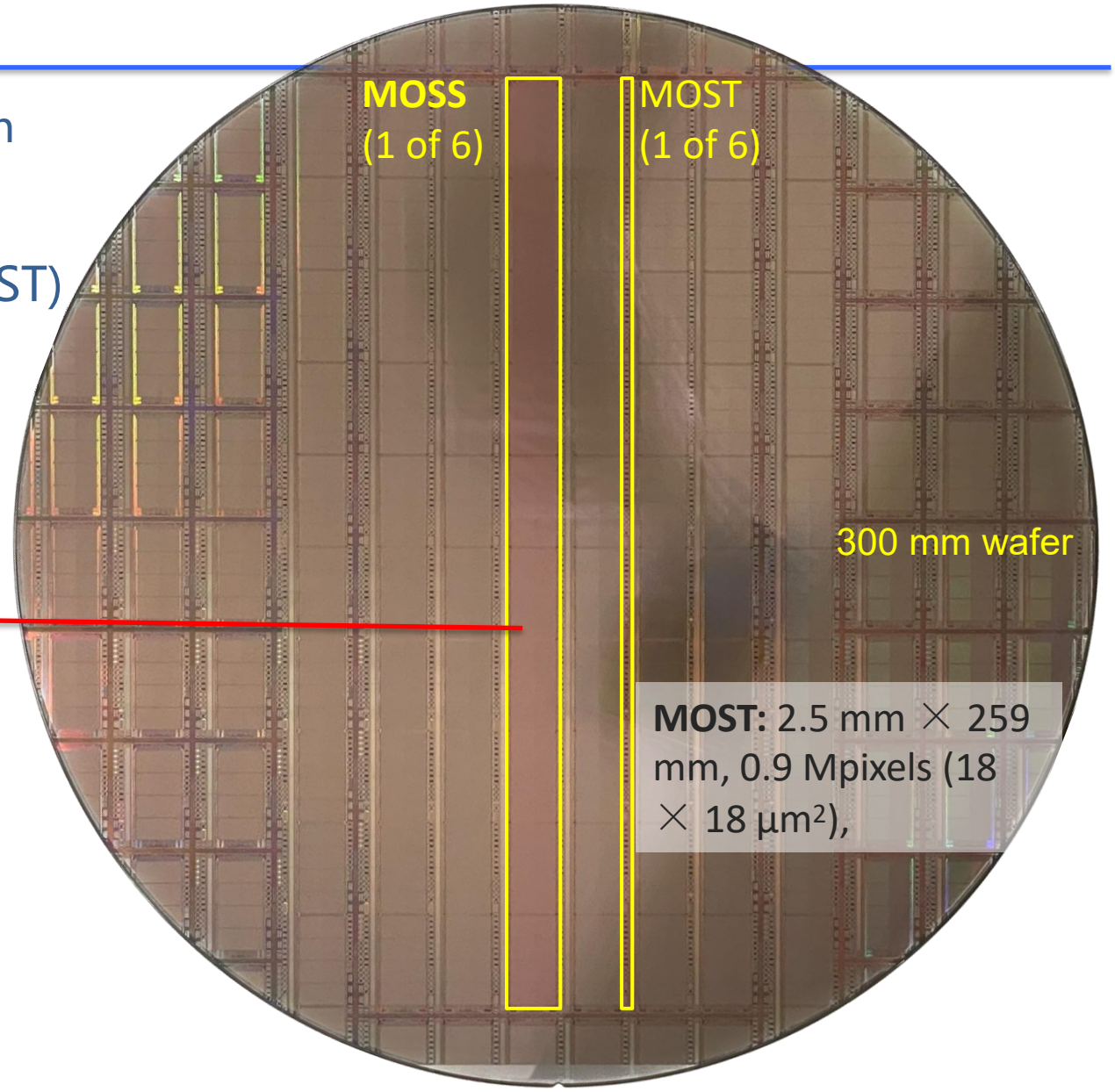
ER1 MAPS Chip

Aim at learning and proving **stitching**, submitted in December 2022

Two wafer scale stitched sensor chips (MOSS, MOST)

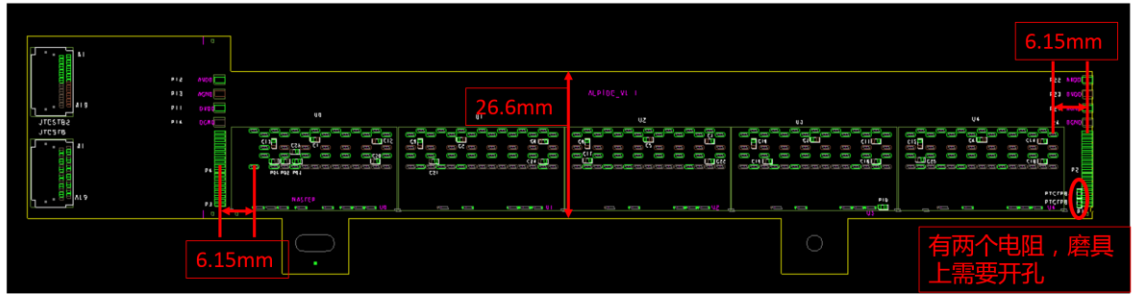


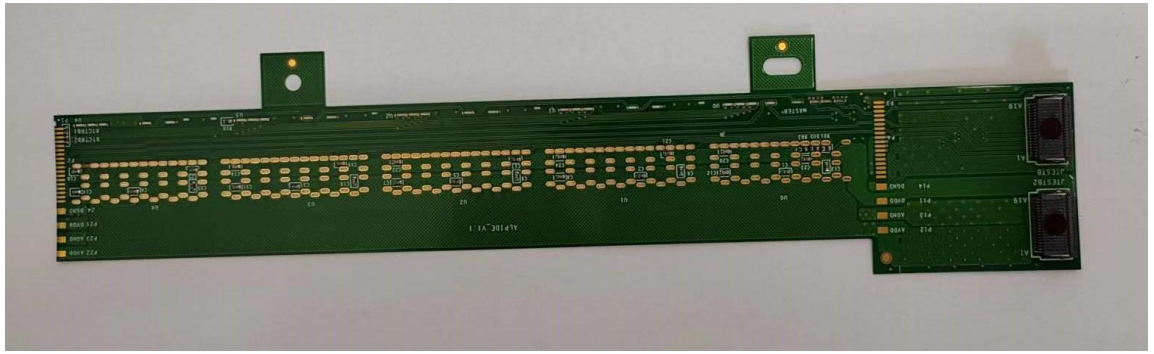
	Pixel matrix	Pixel size
Matrices on the top	256 × 256	22.5 μm
Matrices on the bottom	320 × 320	18 μm

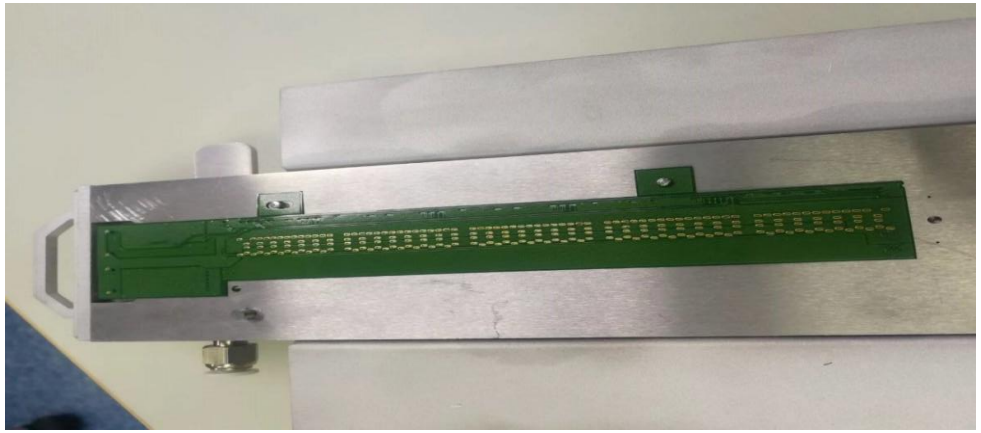


The MOSS chip contains 20 half units and 6.72 million pixels.

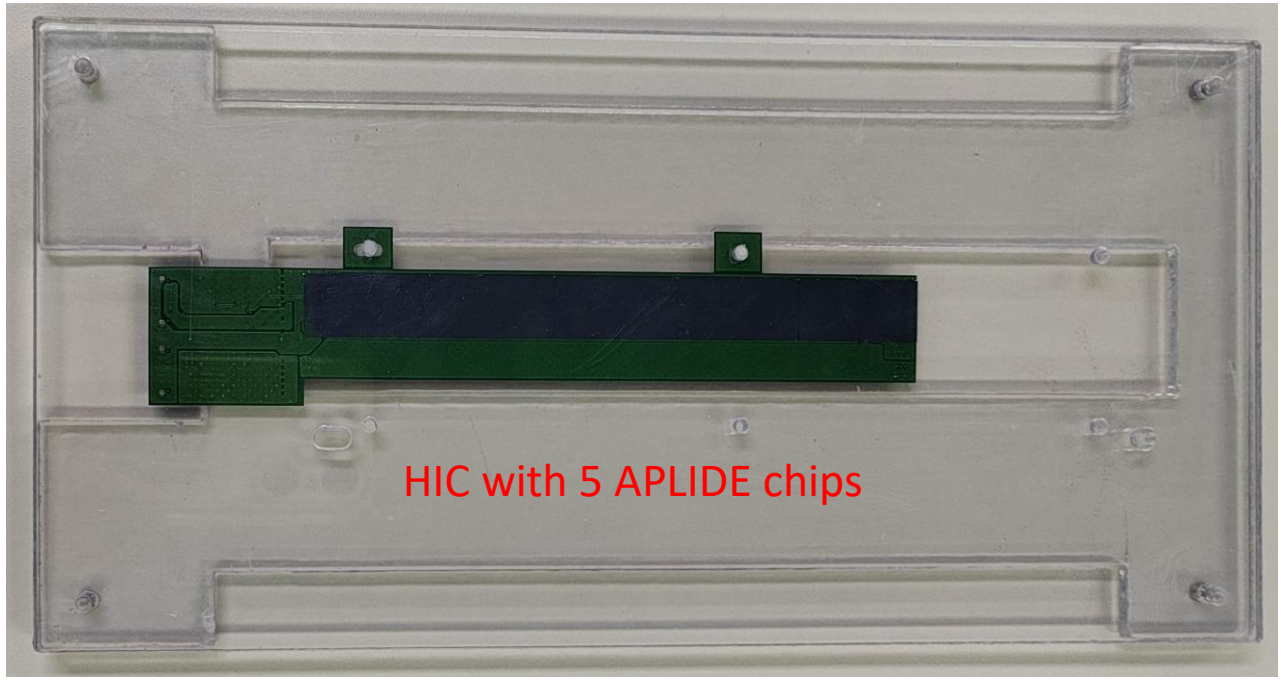
FoCal硅像素层研制进展: FPC、夹具研制





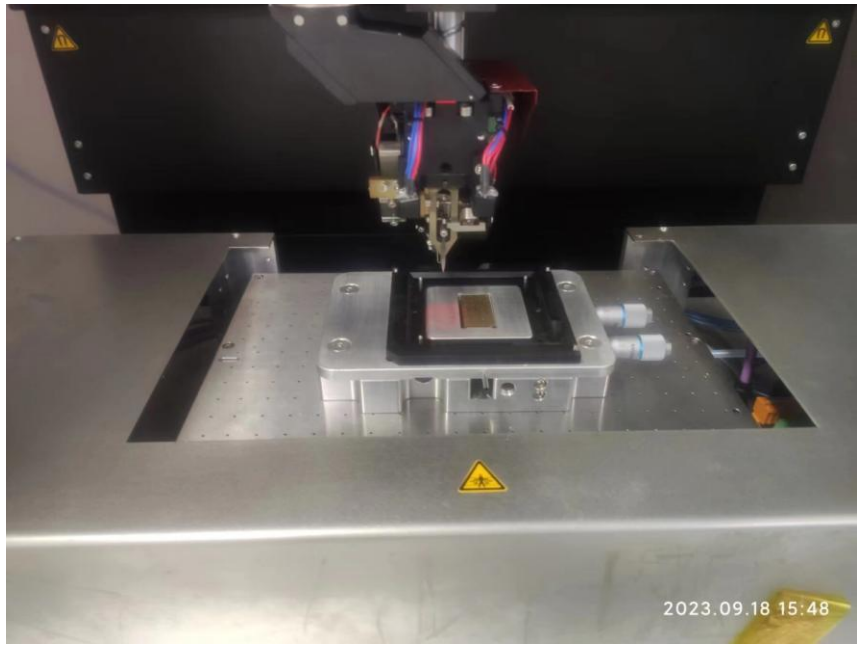


FPC gripper

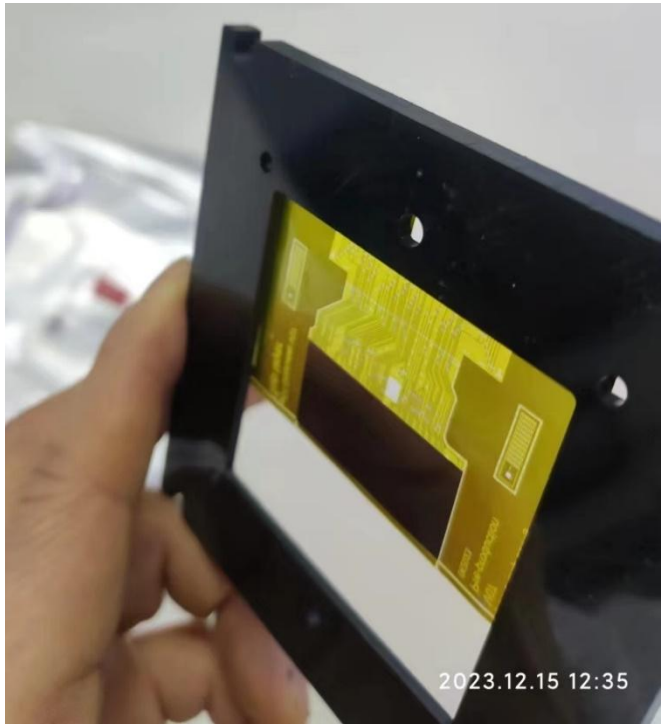


- R&D on HIC as backup solution is ended as chips have to be returned to CERN by the end of March,2023
- We are suggested to join the effort on string-based pixel layer R&D and production.

FoCal硅像素层研制进展: ALPIDE2Chipcable

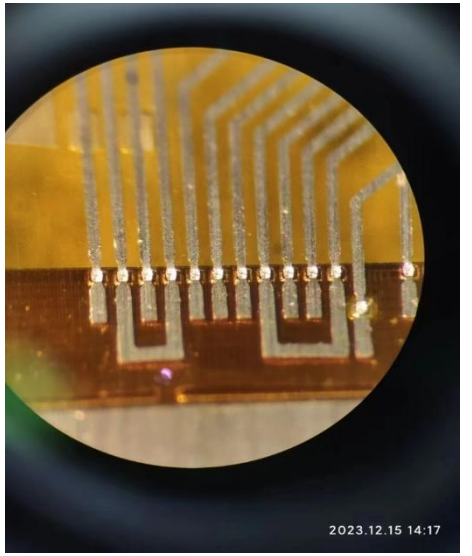


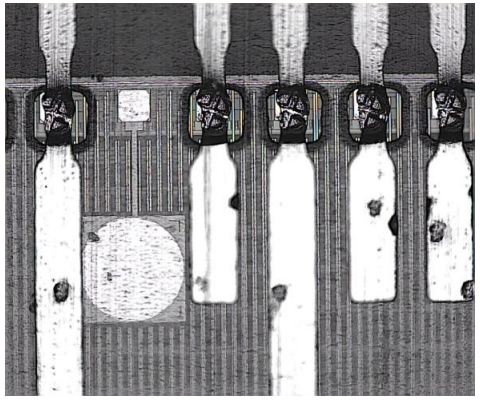
为放置单芯片组装夹具，绑线机平台需调低 2 cm

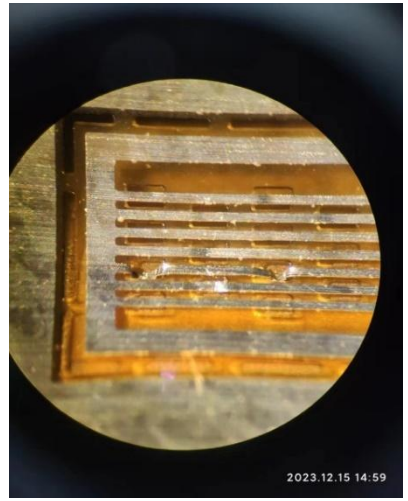


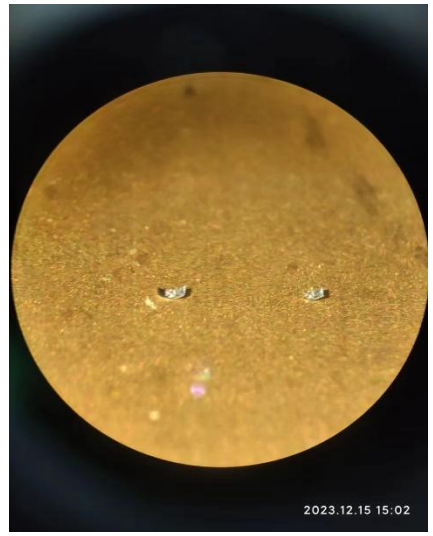
ALPIDE绑定到chip-cable

显微镜下检查绑定效果



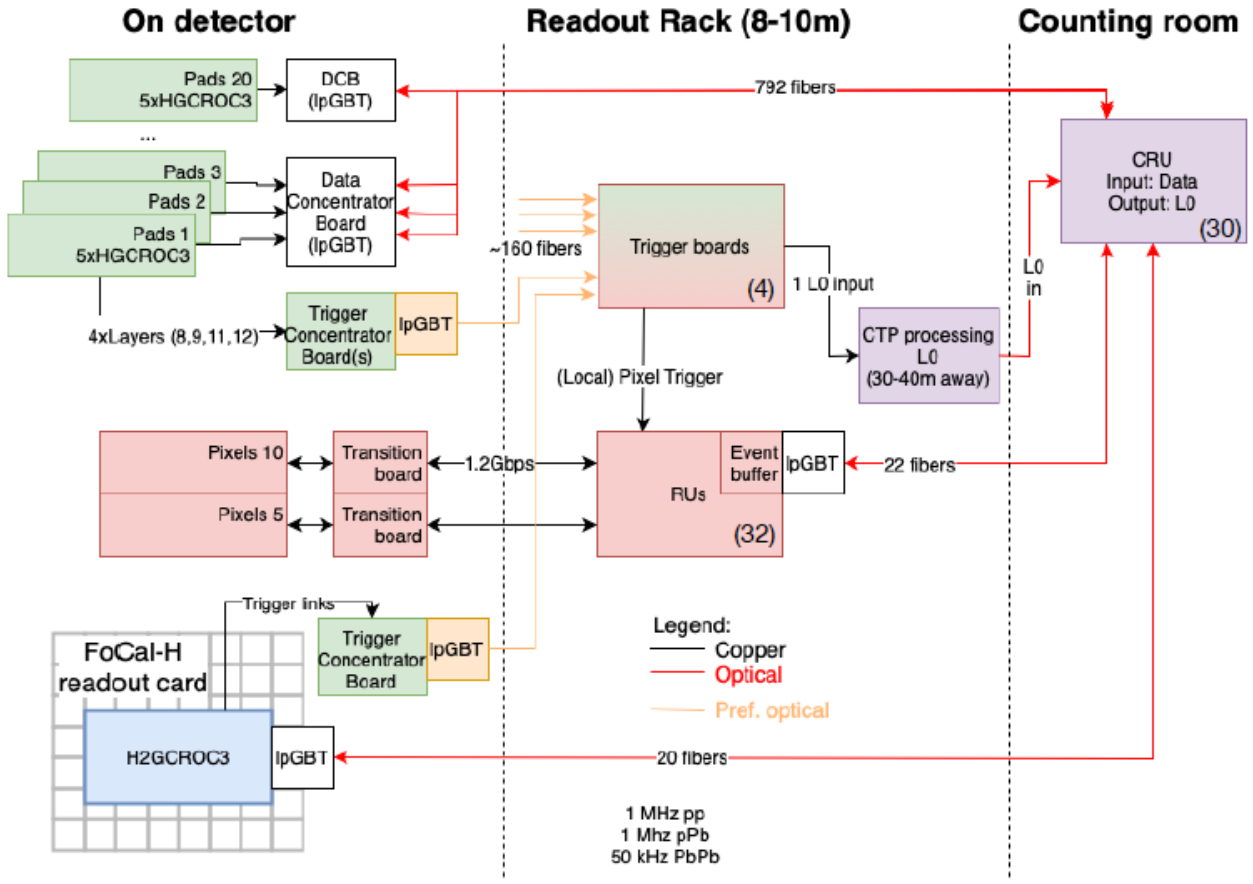




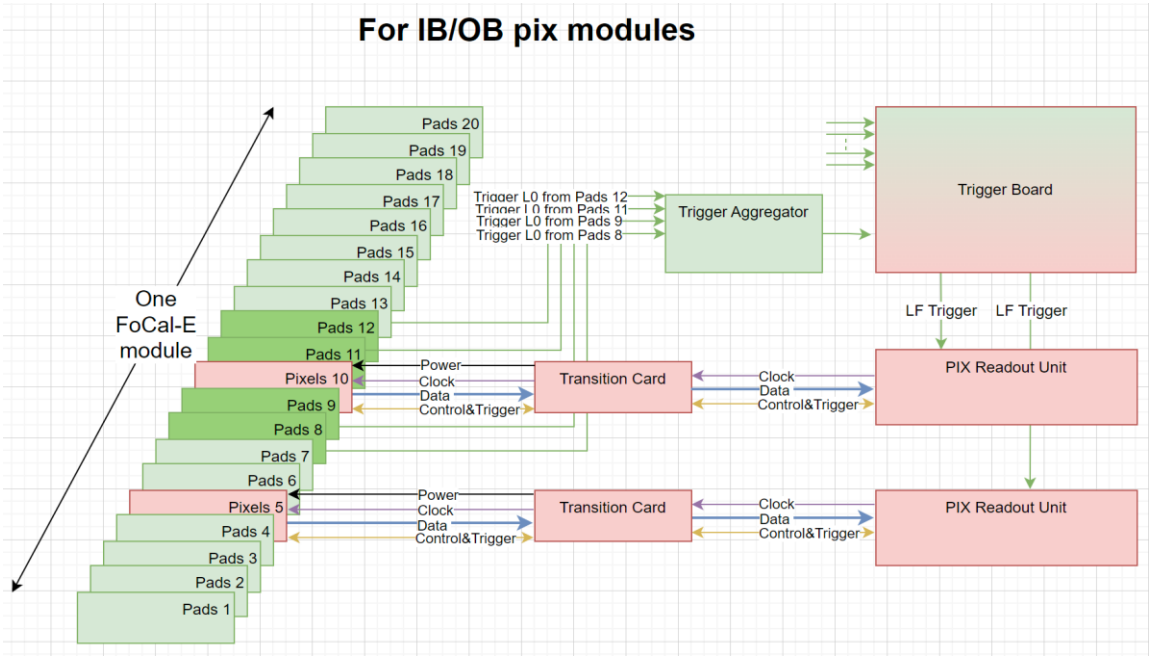


剥离测试

FoCal探测器硅像素层读出电子学系统



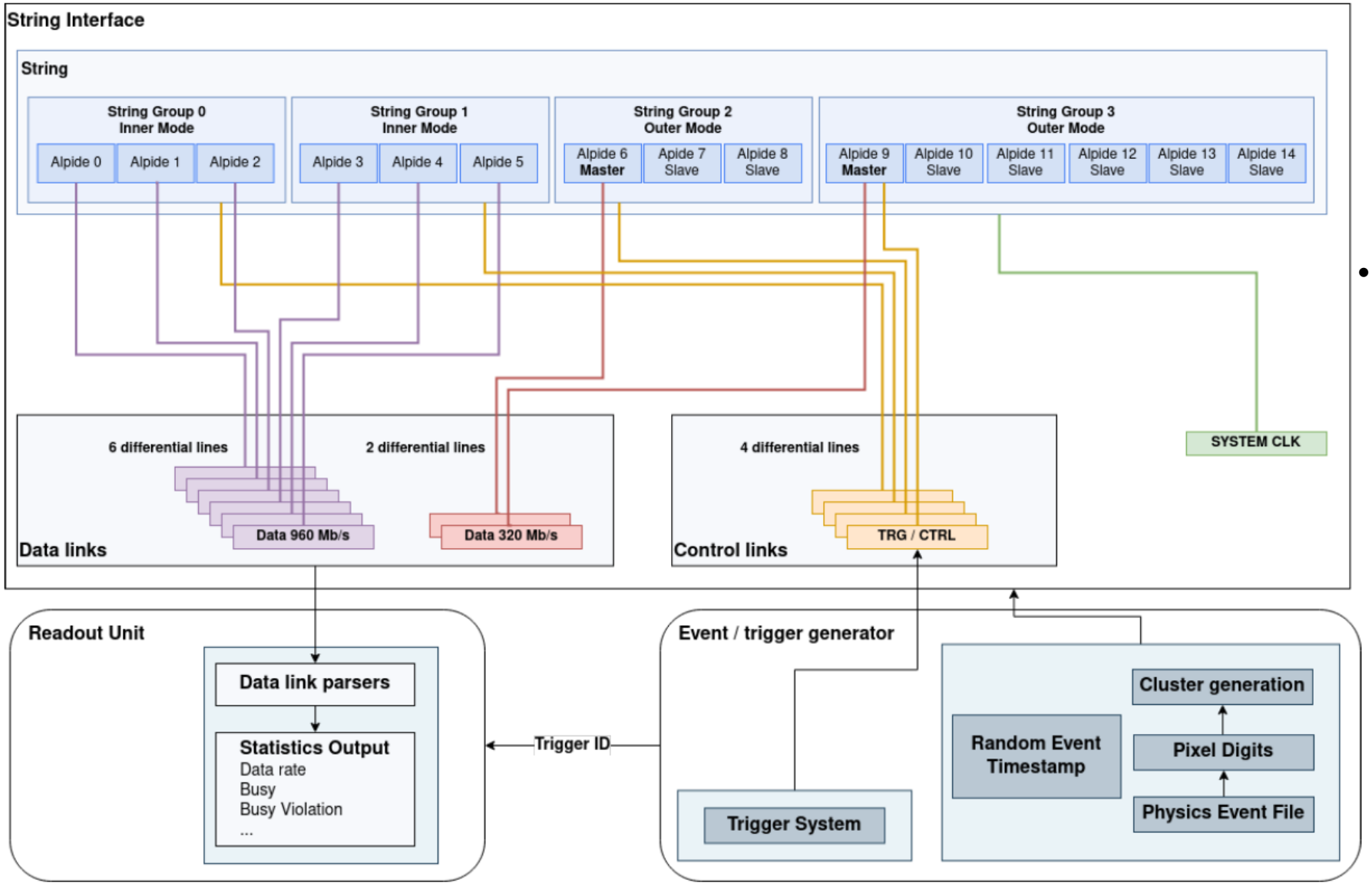
FoCal读出系统



硅像素层读出系统

- 将合作研制硅像素层读出单元

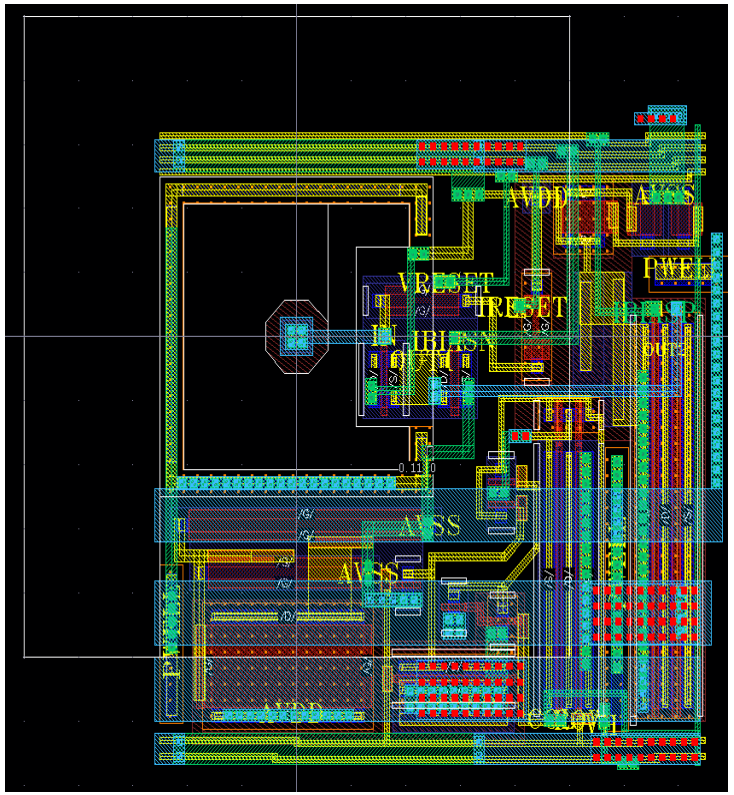
SystemC模拟框架



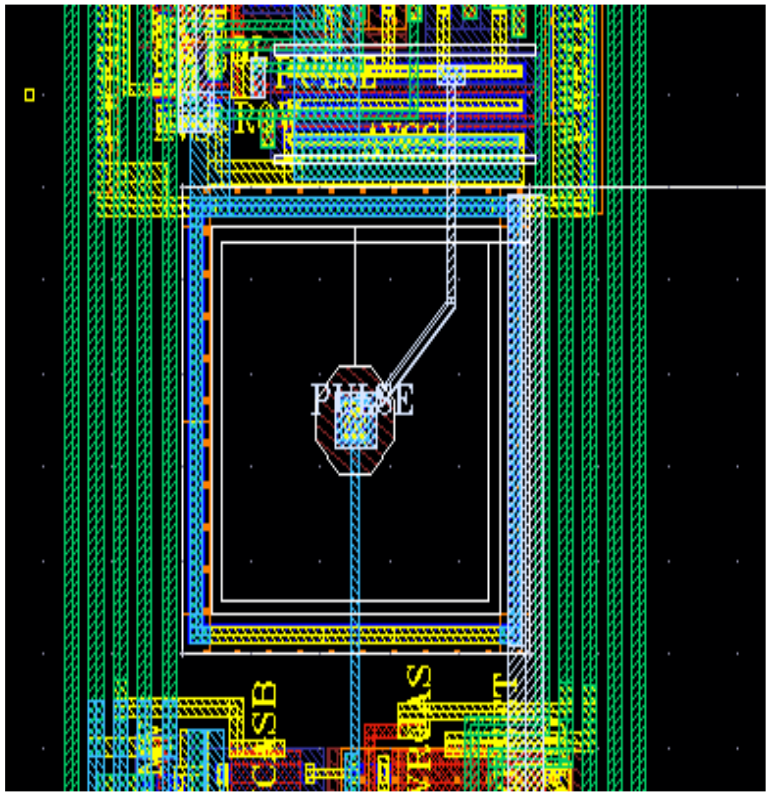
- 通过系统模拟，优化FoCal的构造和像素层的位置，在实现有效分离高能π^0衰变光子的同时，减小读出带宽和读出死（忙）时间。

ER2芯片设计：功能优化

- Reduce the input capacitance while balance current leakage



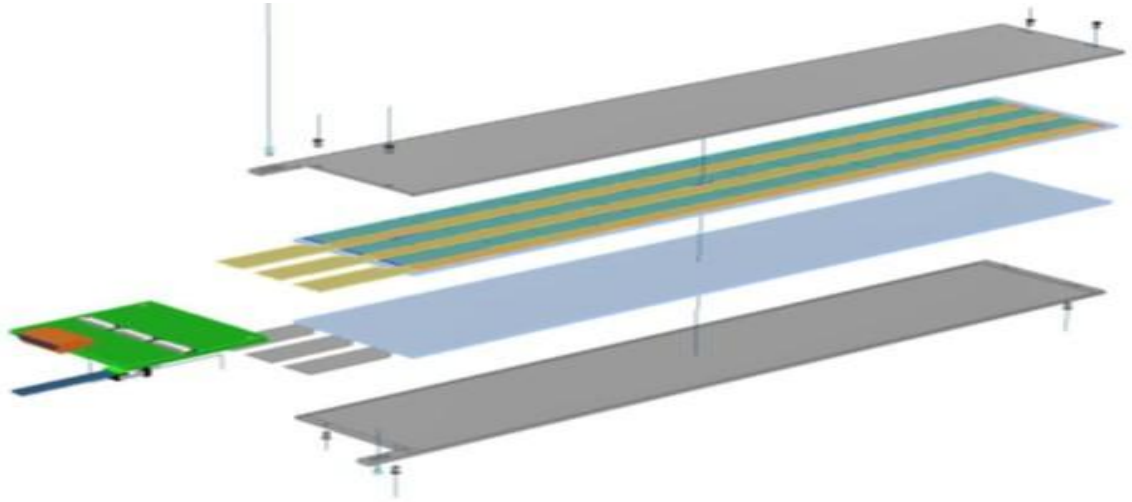
APTS



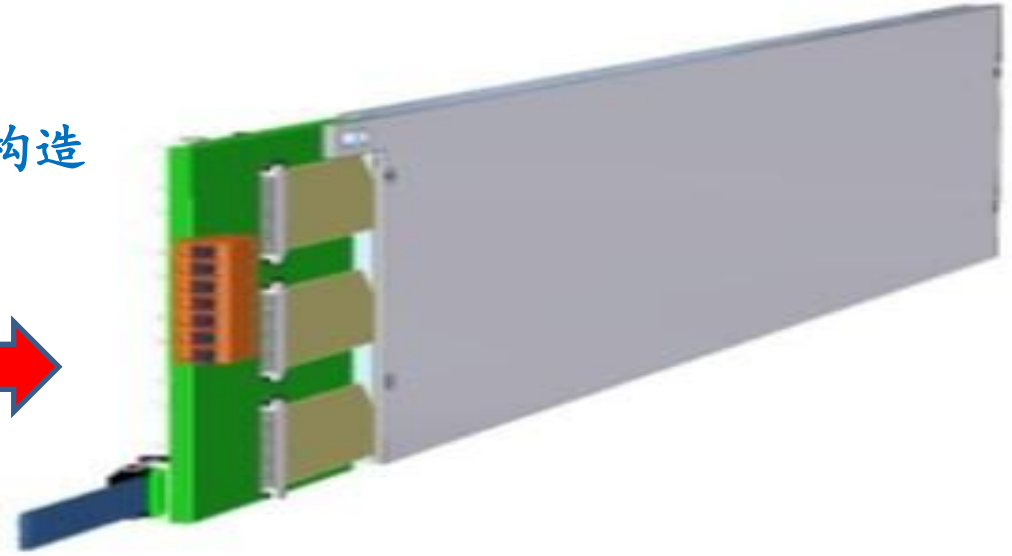
DPTS

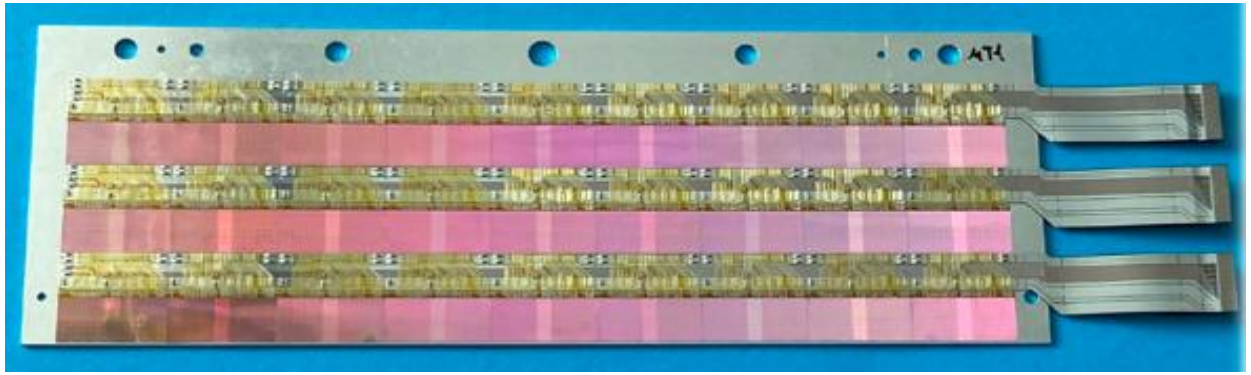
- The length of the metal lines at the input terminal has a negligible impact on its own capacitance, approximately from 0.01 to 0.05fF.
- Concerning coupling capacitance, shortening the metal lines significantly reduces the coupling capacitance between the input terminal and the substrate PWELL, while changes in other areas are minor.
- Optimizing the layout of power lines and isolation rings can reduce some coupling capacitance.
- Additionally, removing the PULSE covering the M4 metal portion on the input terminal can decrease the coupling capacitance by approximately 0.1fF.

FoCal探测器硅像素层的研制

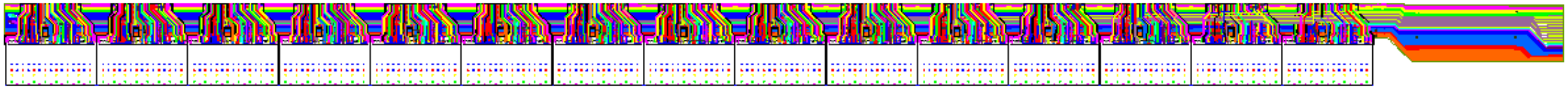


硅像素层构造





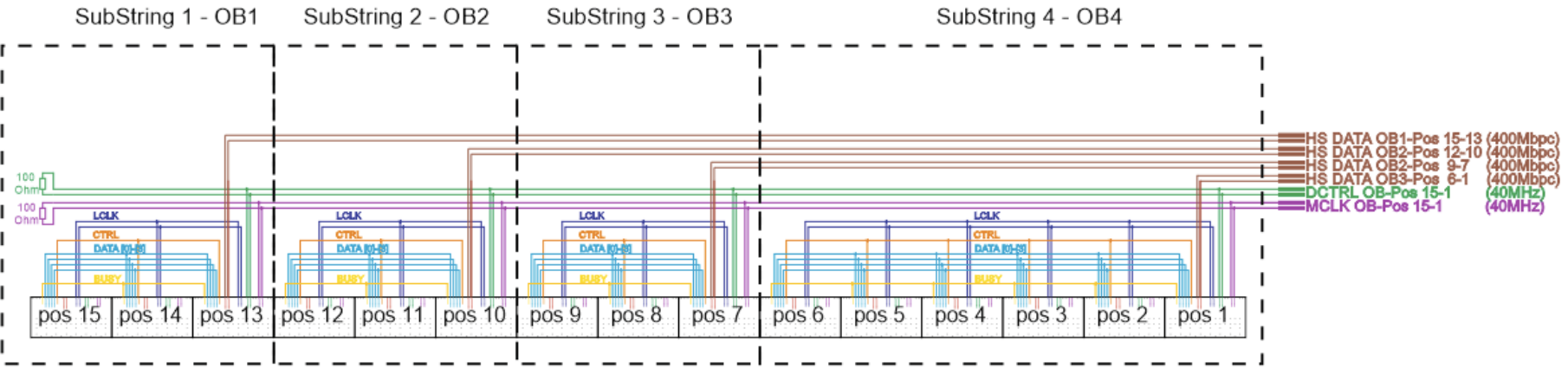
- 每个模块含 2 × 3 个长条，每个长条由15 个ALPIDE芯片及其读出柔性电路组成
- 每个模块含90个 ALPIDE芯片
- FoCal共44 个像素层模块, 需要3960个ALPIDE芯片



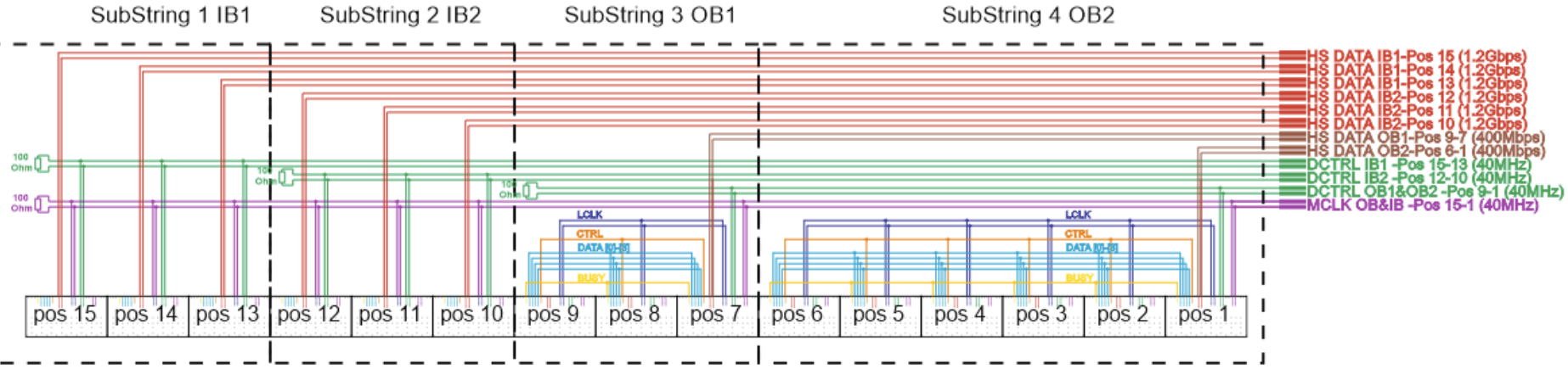
由15个ALPIDE组成的长条

FoCal硅像素层研制进展: String研制

Schematic diagram of strings



OB string



IB/OB string

- 1个由IB/OB ALPIDE芯片构成的模块 含6个长条 → 1个RU:
  - 36 IB chips @ 960 Mbps
  - 12 OB 主芯片 @ 320 Mbps

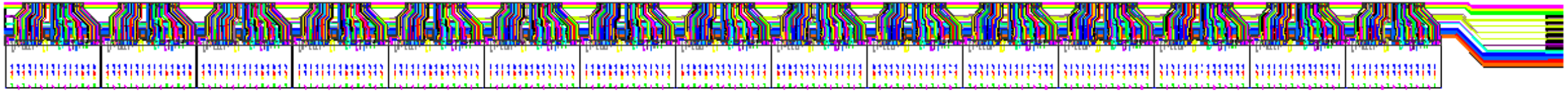
  带宽: 38.4 Gbps
- 3 个由OB ALPIDE 芯片构成的模块 → 1个RU:
  - 每个模块含24个OB主芯片
  - → 72 个OB 主芯片 @ 320 Mbps

  带宽: 23.4 Gbps

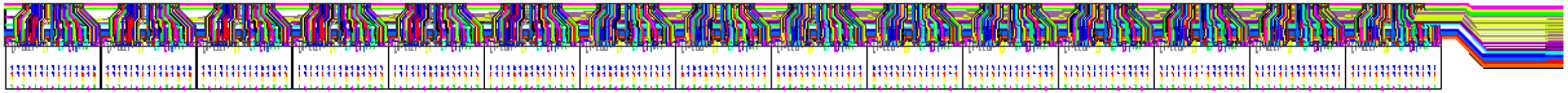
FoCal硅像素层研制进展: String研制

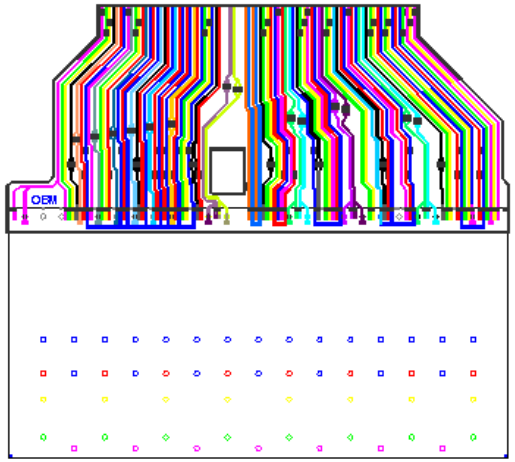
Layout of the strings

IB/OB string

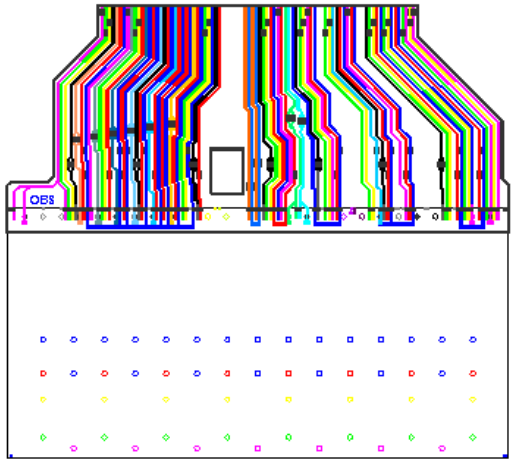


OB string

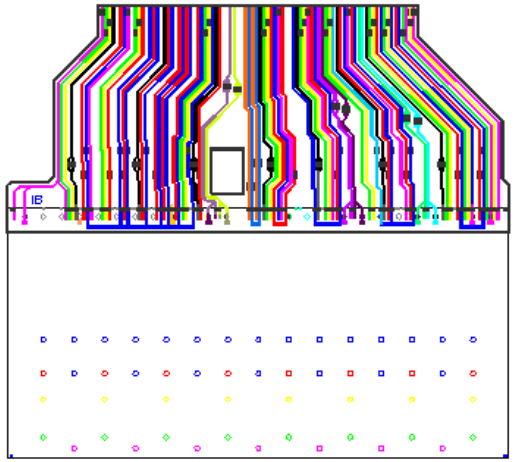




OB-M



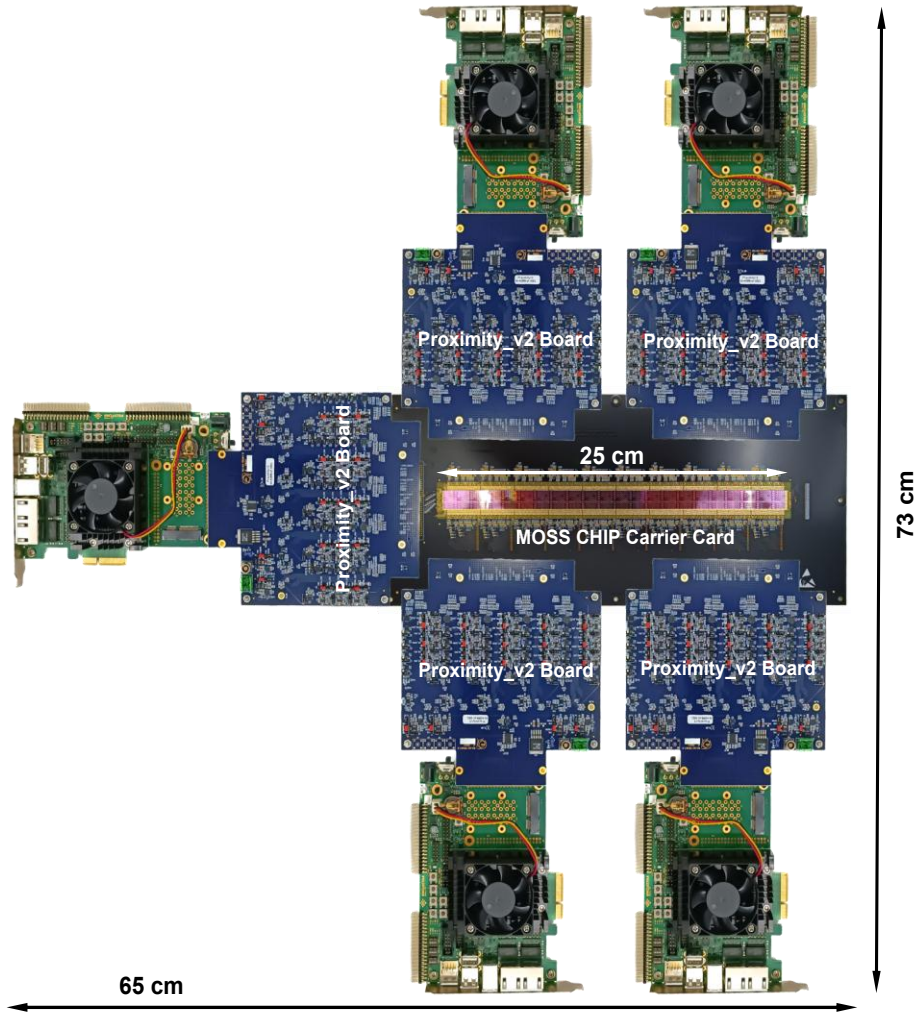
OB-S



IB

Three different types of chip-cables are designed as similar as possible

ER1单片缝合芯片性能测试: 产率



ER1 test system

Yields

		RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10
Wafer 20	1-TOP	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - II	OK - II	OK - I	OK - II
	1-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - II	OK - I
	2-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	2-BOT	OK - II	OK - I	OK - I	LIMIT	OK - II	OK - I	OK - I	OK - I	OK - I	OK - II
	3-TOP	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I
	3-BOT	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - II	OK - I	LIMIT	OK - I	OK - II
	4-TOP	OK - I	OK - I	LIMIT	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I
	4-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - II	OK - I
	5-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I
	5-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	6-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - II	OK - II
	6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
Wafer 21	1-TOP	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - II	OK - II
	1-BOT	OK - II	OK - II	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I
	2-TOP	OK - I	OK - II	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I
	2-BOT	LIMIT	OK - II	OK - I	OK - II	OK - I	LIMIT	LIMIT	OK - I	OK - I	OK - II
	3-TOP	OK - II	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	3-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	4-TOP	OK - I	OK - II	OK - I	OK - I	OK - II	LIMIT	OK - I	OK - II	OK - I	OK - I
	4-BOT	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - II	OK - II	LIMIT	LIMIT
	5-TOP	LIMIT	OK - I	OK - I	OK - II	OK - I	OK - I	OK - II	OK - II	OK - I	OK - II
	5-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - II
	6-TOP	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	LIMIT	OK - II	OK - I	OK - II
	6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	LIMIT	OK - I
Wafer 22	1-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	1-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	2-TOP	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II
	2-BOT	LIMIT	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I
	3-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	3-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	4-TOP	OK - I	OK - I	OK - I	OK - II	OK - II	OK - I	OK - II	OK - II	OK - II	OK - I
	4-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I
	5-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I
	5-BOT	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	6-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I
	6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - II	OK - I	OK - I

115/120 'OK' (95.8%)
19 HUs 'OK-II'
5 HUs 'LIMIT'

109/120 'OK' (90.8%)
29 HUs 'OK-II'
11 HUs 'LIMIT'

116/120 'OK' (96.7%)
11 HUs 'OK-II'
4 HUs 'LIMIT'

ER2芯片设计：ASIC框图

设计指标

Simulation parameters	Value	Unit	Conditions
Particle Rates			
Pb-Pb Interaction Rate	164	kHz	Safety factor 2
Particle flux (Hadronic)	2.55	MHz cm^{-2}	z=0 cm, all centralities.
Particle flux (QED)	3.20	MHz cm^{-2}	z=0 cm.
Total particle flux	5.75	MHz cm^{-2}	z=0 cm, all centralities.
Geometry, timing, encoding, data transfer capacity			
Pixel dimensions	20.8 × 22.8	µm × µm	
Tile pixel array size	442 × 156		
Pixels per Tile	68952		
Sensitive Area of the tile	0.328	cm^2	
Tiles per segment	144		
Readout regions per tile	3 or 4		
Frame Interval Duration (FD)	2 or 5	µs	
Minimum average cluster size	2.1		$\Delta z = 0$ cm, Fig. 3.43.
Pixel hit encoding time	25	ns	
Bits per pixel hit	16	bit	
Capacity of tile link	160	Mbit s^{-1}	
Aggregated capacity (Segment)	23.04	Gbit s^{-1}	
Simulation results			
Average pixel occupancy	$< 2.0 \times 10^{-4}$		z=0 cm.
Average pixel occupancy	$< 5.0 \times 10^{-4}$		z=0 cm, FD=5 µs.
Data throughput	120	Mbit s^{-1} Tile^{-1}	z=0 cm.
Data throughput	15.55	Gbit s^{-1} Segment^{-1}	
Data throughput per unit area	365	Mbit s^{-1} cm^{-2}	z=0 cm.
Data throughput per unit area	329	Mbit s^{-1} cm^{-2}	Average over z.
Data throughput per link	2.58	Gbit s^{-1}	
Incomplete event probability	$< 6 \times 10^{-5}$		Layer 0 segment.
Incomplete event probability	$< 2 \times 10^{-4}$		Full layer 0.

One tile (total 6) of the half of one repeated sensor unit (total 12)