CEPC Common Trigger Board Design

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Introduction

What is Common Trigger Board

- An ATCA Development Platform
- Core component of L1 trigger system, the implementation of trigger algorithms and the testing of data readout bandwidth are both based on this

Requirements

- High-Speed Data Transfer Performance
- High-Performance Data Processing Capability
- High-Capacity Data Buffering
- Scalability

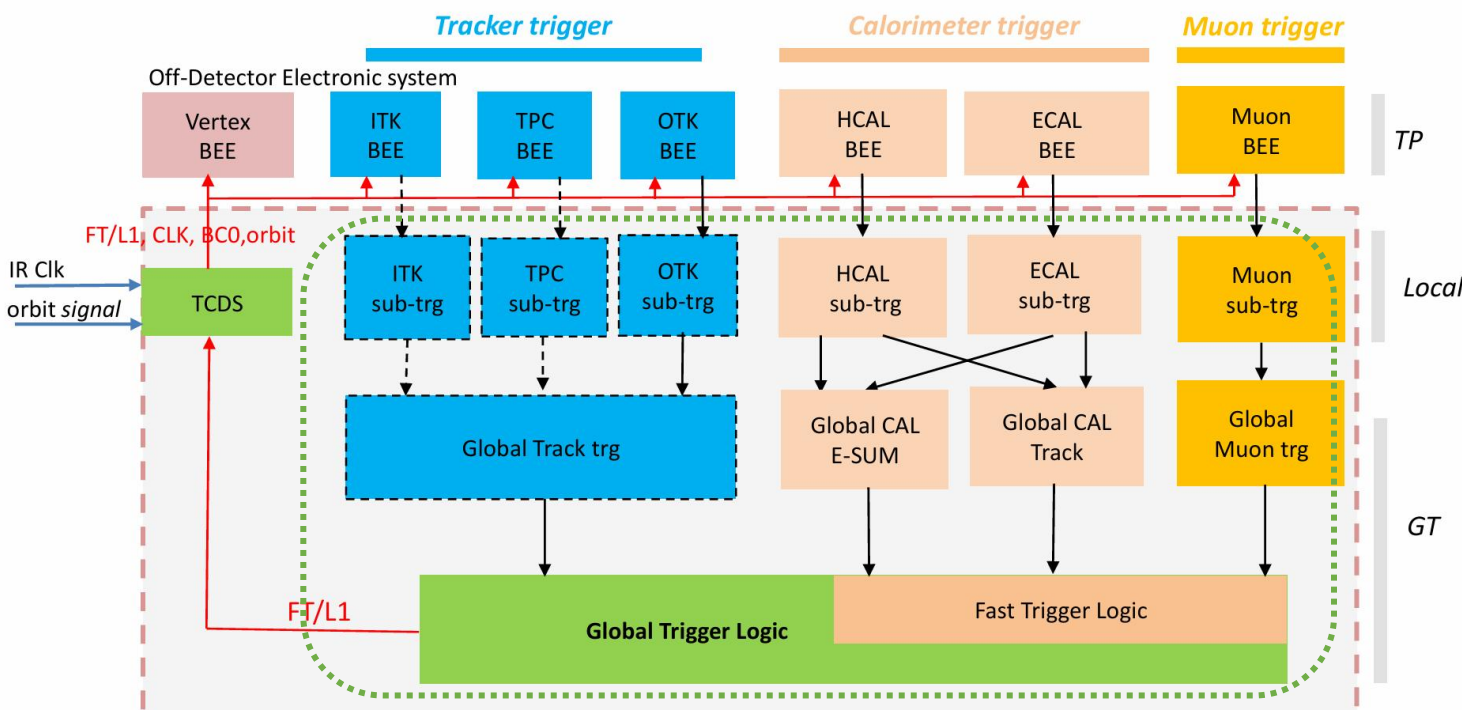


Figure 1 .CEPC Trigger structure

Introduction

Investigation Outcomes

Hardware structure should include:

- Board Infrastructure
  - SoM
  - Clock, power
  - Storage
- ATCA Infrastructure
  - Backplane connectors
  - IPMC
  - Power input
  - Ethernet switch
- Payload
  - Optical transceivers
  - FPGA
  - Clocks

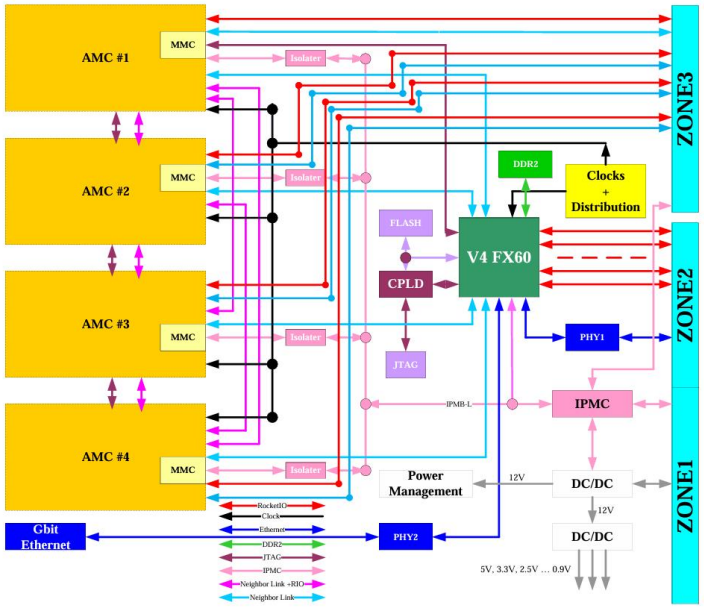


Figure 2.HPCN V4 structure(BelleII PXD)

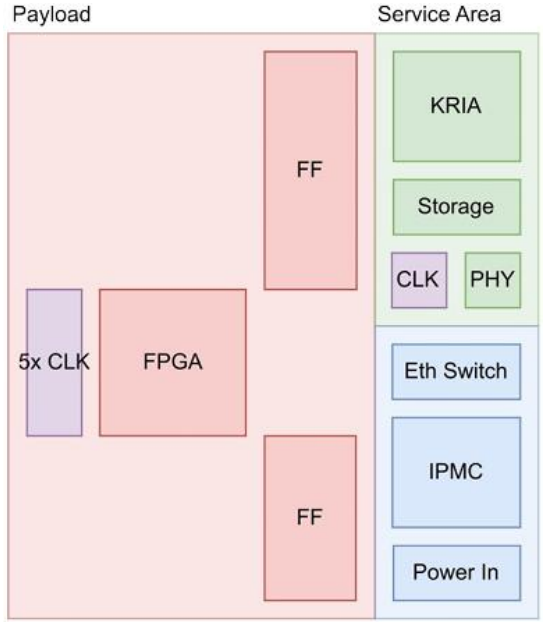


Figure 3.Serenity board overview (CMS BEE and Trigger)

- High-Speed Data Transfer
  - Rocket IO +Optical transceivers
  - QSFP,Firefly ,Minipod
- High-Performance Data Processing
  - FPGA
- High-Capacity Data Buffering
  - FPGA RAM (tens to hundreds of Mb)
  - DDR4(8GB-64GB)
- Board management
  - SOM
  - IPMC

Design progress

Hardware structure design

- FPGA for data process
- Optical channel: 10-25 Gbps/ch
- Channel number:36-48 channels
- Optical Ethernet port: 40-100GbE
- DDR4 for mass data buffering
- SoC module for board management
- IPMC module for Power management

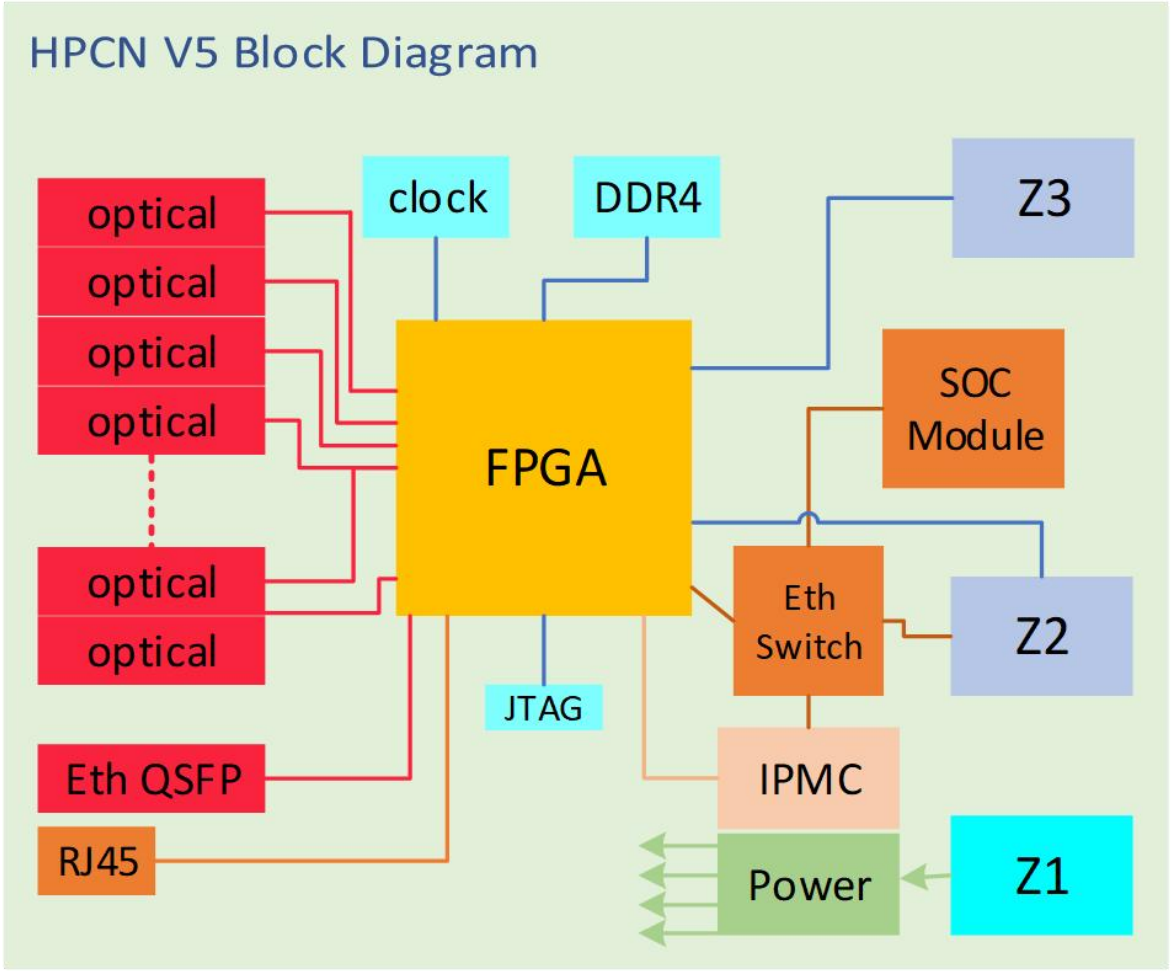


Figure 4. CEPC Common Trigger Board overview

Design progress

Component Selection

Table 12: **Virtex UltraScale+ Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU23P	VU27P	VU29P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, HD, GTY	HP, HD, GTY, GTM	HP, GTY, GTM	HP, GTY, GTM
VSVA1365	35x35								364, 0, 34(7), 4		
FFVC1517	40x40	520, 40									
FSVJ1760	42.5x42.5								572, 72, 34, 4		
FLGF1924(5)	45x45					624, 64					
FLVA2104	47.5x47.5		832, 52	832, 52							
FLGA2104	47.5x47.5				832, 52						
FHGA2104	52.5x52.5(6)						832, 52				
FLVB2104	47.5x47.5		702, 76	702, 76							
FLGB2104	47.5x47.5				702, 76	572, 76					
FHGB2104	52.5x52.5(6)						702, 76				
FLVC2104	47.5x47.5		416, 80	416, 80							
FLGC2104	47.5x47.5				416, 104	416, 96					
FHGC2104	52.5x52.5(6)						416, 104				
FSGD2104	47.5x47.5				676, 76	572, 76					
FIGD2104	52.5x52.5(6)						676, 76			676, 16, 30	676, 16, 30
FLGA2577	52.5x52.5				448, 120	448, 96	448, 128				
FSGA2577	52.5x52.5						448, 128			448, 32, 48	448, 32, 48
FSVA3824	65x65							1976, 96, 48			
FSVB3824	65x65							1664, 96, 80			

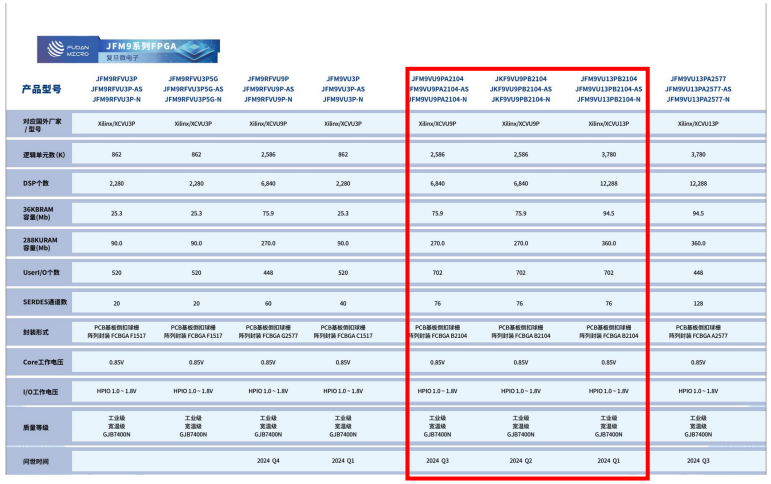
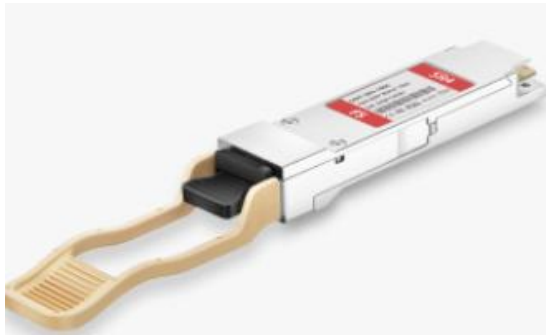


Figure 5 .FPGA selection investigation



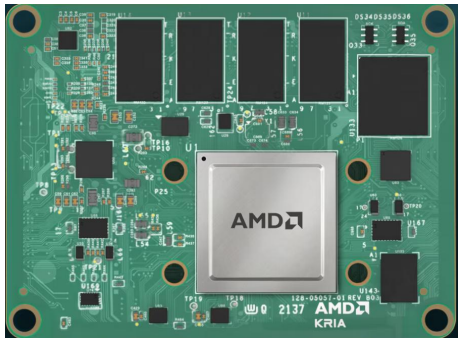


Figure 6 .QSFP(left),K26 SOM(right)

Requirement

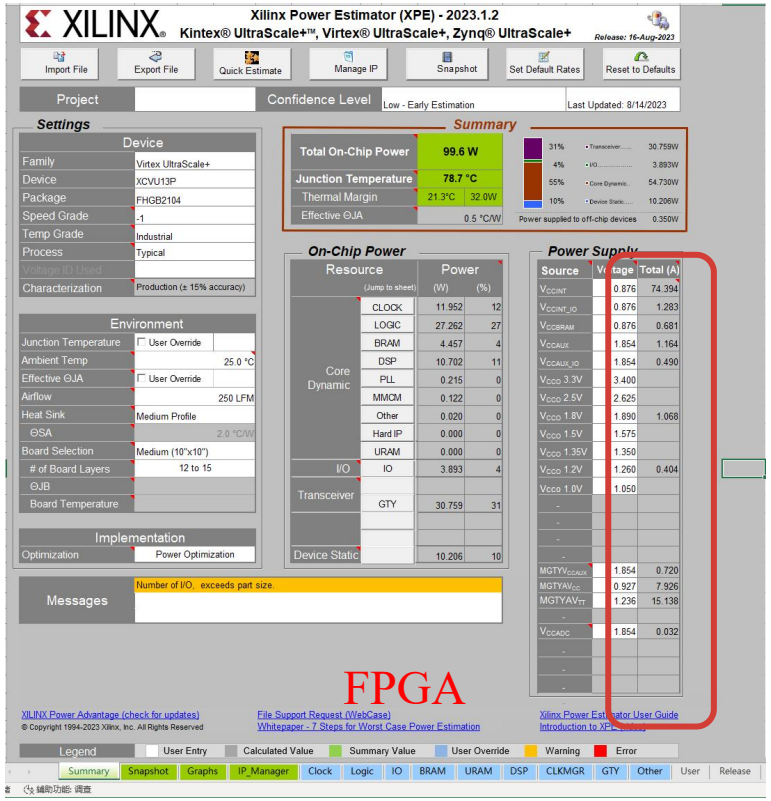
- Optical transceiver :36-48 channels
- ETH Switch :5 or more ports
- Clock:12 channels at least

Recommand

- QSFP*10 (40 channels)
- KSZ9897R(7 ports)
- ZL30274 *2 (8*2)
- K26 SOM

Design progress

- Power design



IV. Electrical Characteristics

Parameter	Symbol	Unit	Min	Type	Max	Notes
Supply Voltage	Vcc	V	3.135		3.465	
Supply Current	Icc	A			1.5	
Module Total Power	P	W		1.8		

QSFP

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V_{CC_SOM}	5V (4.75V – 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on-board power regulators.
V_{CC_BATT}	1.20 – 1.50V	150 nA – 3650 nA	External battery input for the RTC
V_{CCO_HPA}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 66
V_{CCO_HPB}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 65
V_{CCO_HPC}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 64
V_{CCO_HDA}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 45
V_{CCO_HDB}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 43
V_{CCO_HDC}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 44

SOM

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Current - Full 1000 Mbps Operation						
I_{DD_AH}	**AVDDH** supply current	**VDDIO** @ 3.3V Ports 1-5 in 1000BASE-T Ports 6 & 7 in RGMII (1000 Mbps) All ports 100% utilization		330		mA
I_{DD_IO}	**VDDIO** supply current			80		mA
I_{DD_CA}	**AVDDL** supply current			460		mA
I_{DD_CD}	**DVDDL** supply current			750		mA

ETH Switch

ParameterSymbol 24002133 Units				
One bank ACTIVATE-PRECHARGE current	DD0	512	480	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I_{PP} current	PP0	3232	mA	
One bank ACTIVATE-READ-PRECHARGE current	DD1	544	520	mA
Precharge standby current	DD2N	400	368	mA
Precharge standby ODT current	DD2NT	464	432	mA
Precharge power-down current	DD2P	256	240	mA
Precharge quiet standby current	DD2Q	328	312	mA
Active standby current	DD3N	536	504	mA
Active standby I_{PP} current	PP3N	2424	mA	
Active power-down current	DD3P	352	352	mA
Burst read current	DD4R	1280	1200mA	
Burst write current	DD4W	1440	1280mA	
Burst refresh current (1x REF)	DD5B	1536	1520mA	
Burst refresh I_{PP} current (1x REF)	PP5B	176	176	mA
Self refresh current: Normal temperature range (0°C to 85°C)	DD6N	160	160	mA
Self refresh current: Extended temperature range (0°C to 95°C)	DD6E	216	216	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	DD6R	8080	mA	
Auto self refresh current (25°C)	DD6A	7272	mA	
Auto self refresh current (45°C)	DD6A	8080	mA	
Auto self refresh current (75°C)	DD6A	128	128	mA
Auto self refresh I_{PP} current	PP6X	2424	mA	
Bank interleave read current	DD7	1680	1480mA	
Bank interleave read I_{PP} current	PP7	112	96	mA
Maximum power-down current	DD8	144	144	mA

DDR4

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units
Total power, two CMOS REF inputs, Synth1 and six LVDS outputs enabled	P_{noise}	—	0.8	—	W
Total current, 3.3V supply (VDD33+VDDOx pins)	I_{DD33}	—	160	322	mA
Total current, 1.8V supply (VDD18 pins)	I_{DD18}	—	207	519	mA

CLK Fanout

Figure 7 .Power Consumption Analysis of On-board Devices

Design progress

Power design

Table 1: Summary of Power Consumption Evaluation

Component	Quantity	Voltage (V)	5	3.3	2.5	1.8	1.2	0.85	0.6	MGT_1.8	MGT_1.2	MGT_0.9
SOM	1	Current (A)	4	3		3				1	16	8
QSFP	10	Current (A)		15								
DDR4(8GB)	1	Current (A)			0.4		3.4		1			
FPGA	1	Current (A)				3	0.5	76				
CLK_FAN	3	Current (A)		1.8		3						
SWITCH	1	Current (A)			0.4	0.1	1.3					
PHY	1	Current (A)		0.2								
BUFFER	2	Current (A)		0.6								
Total Current			4	20.6	0.8	9.1	5.2	76	1	1	16	8
Power Consumption			20	67.98	2	16.38	6.24	64.6	0.6	1.8	19.2	7.2

Power Consumption in total : 206W

Design progress

- Power structure design

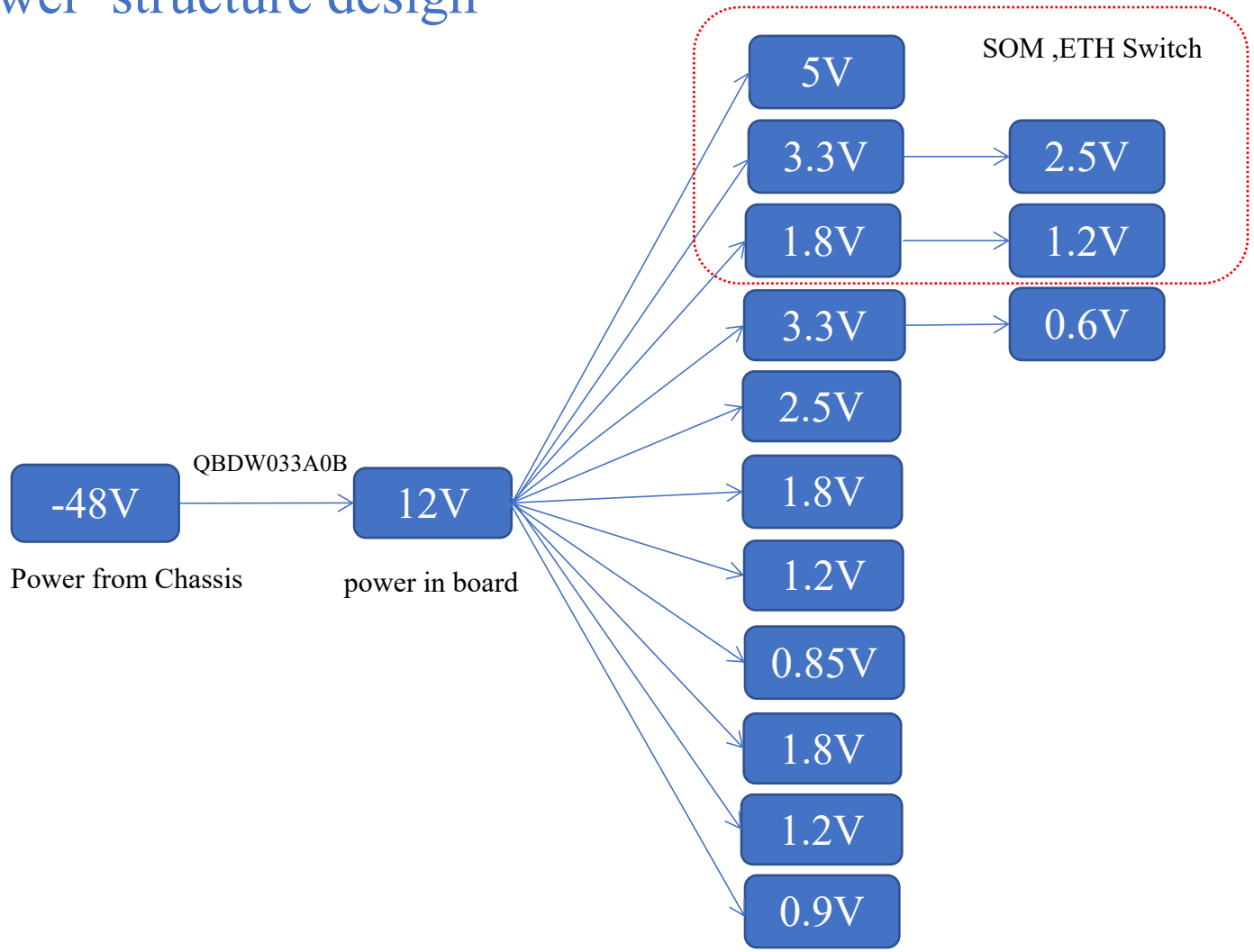


Figure 8.Power structure

Applications in board

QSFP, PHY, Clock fan out,DDR4

DDR4

FPGA , CLOCK fan out ....

DDR4,FPGA

FPGA_VCCINT

MGTVCCAUX

MGTAVTT

MGTAVCC

Design progress

Clock distribution design

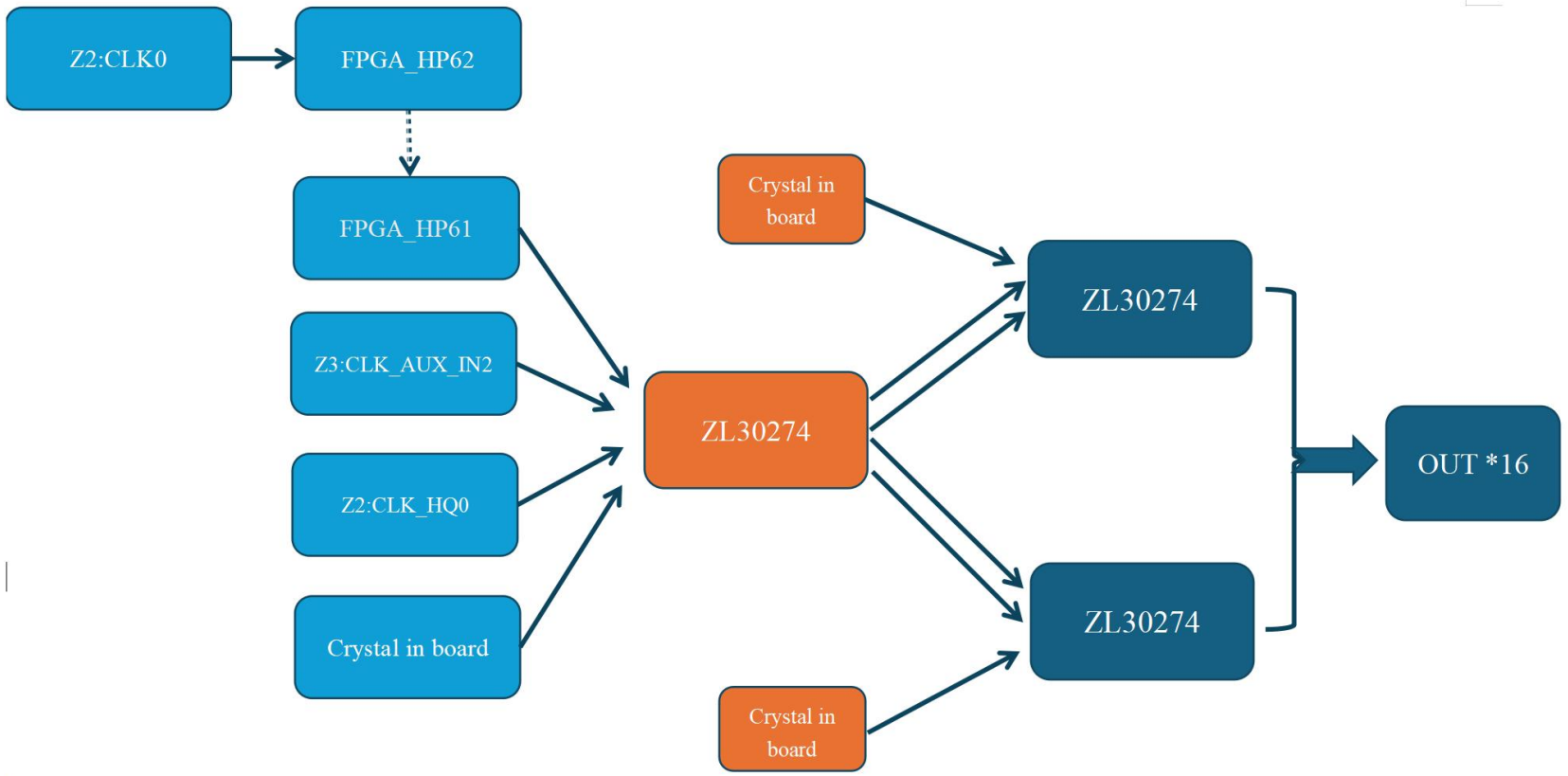


Figure 9.Clock Distribution structure

Design progress

Schematic Design

Schematic design progress

Component	Status	Details
Power	Basic Completion	12->2.5V need to be refined
Clock Distribution	In Progress	Schematic for clock fanout device done
DDR4	Basic Completion	
Ethernet Switch	Basic Completion	
Z1,Z2,Z3 Connector	Basic Completion	
IPMC	In Progress	Interface signals require definition and refinement
QSFP	Basic Completion	
FPGA	In Progress	
SOM	In Progress	Interface signals require definition and refinement
Test and Configuration Interface	Not Started	
System Integration	Not Started	

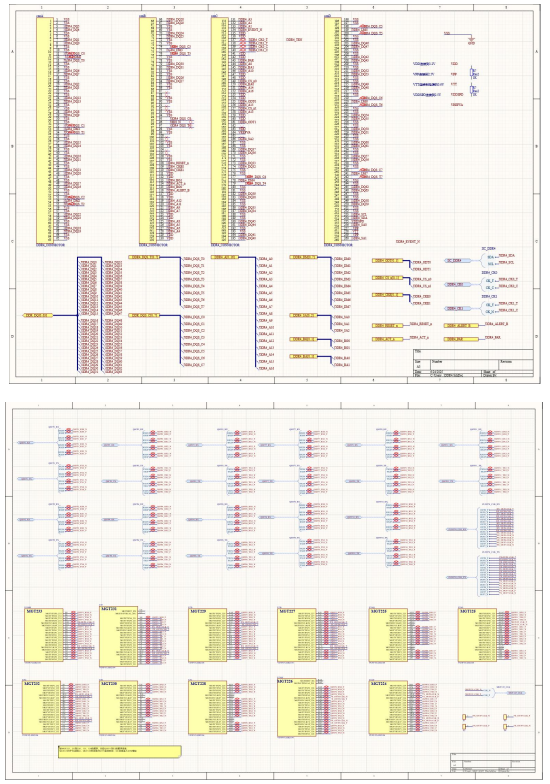


Figure 10: Schematic Design - Top (DDR4), Bottom (QSFP)

Design progress

PCB layout

- FPGA Positioning（Centralized placement）
- High-Speed Interface Arrangement
  - QSFP connector
  - DDR4 connector
  - ETH Switch
- Power
  - -48V-12V Converter Power
  - MGT Power
- IO
  - Backplane connectors
  - RJ45， QSFP

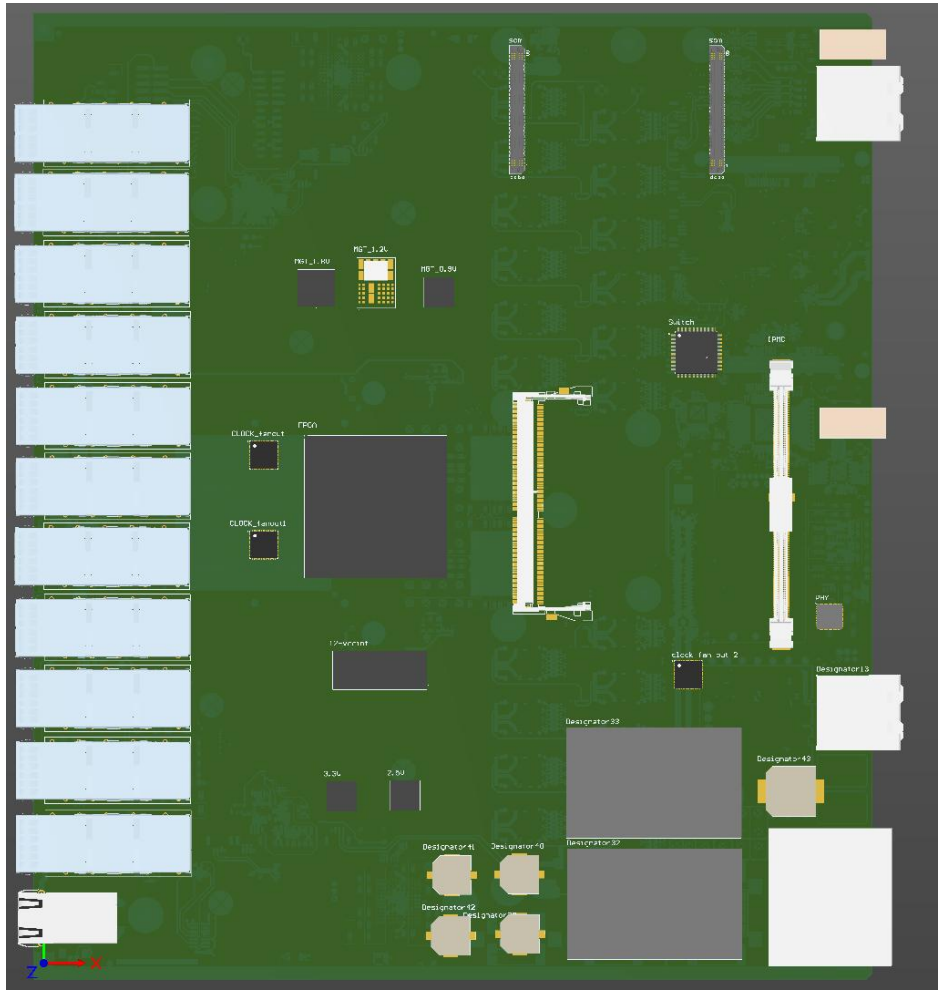
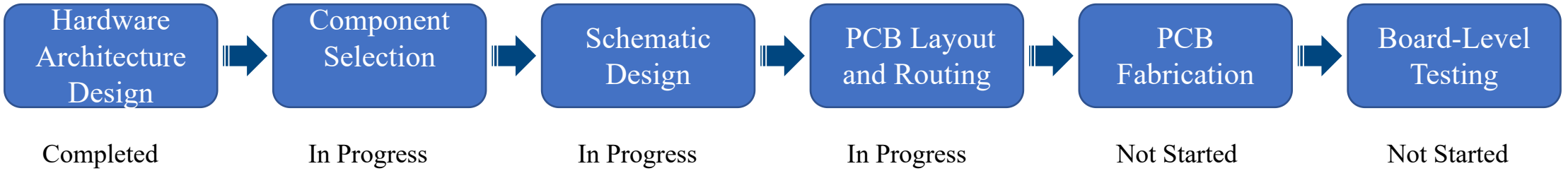


Figure 11 .PCB layout overview

Summary & Outlook



- The hardware architecture design has been completed
- Primary Components Selection in Progress
  - Clock fan out ,PHY,Eth switch,Power have been selected and validated against design requirements.
  - Some components(e.g., oscillators, sensors,DDR4,) require further specification alignment.
- Schematic Design in Progress
  - Detailed schematic design is underway, with the power subsystem designed .
- Next Phase: PCB Layout & Routing
  - PCB layout and routing shall commence following schematic design sign-off.

Analysis of ECAL Barrel Cluster

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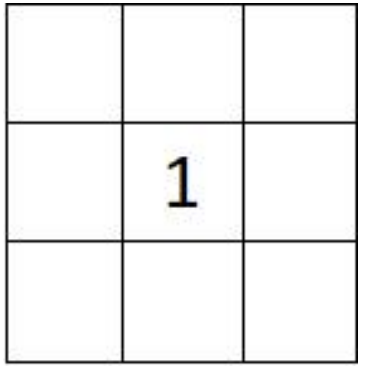
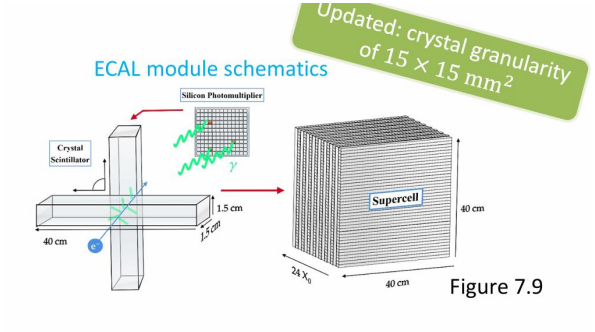
Cluster Definition

Cluster: groups of contiguous and adjacent calorimeter units with energy deposition above threhold



- Adjacency : 8-connected neighborhood .
- Unit : Supercell
- Seed : A high-energy fired module with a threshold of 0.6 GeV.
- Member : Low-energy fired modules with a threshold of 0.2681 GeV



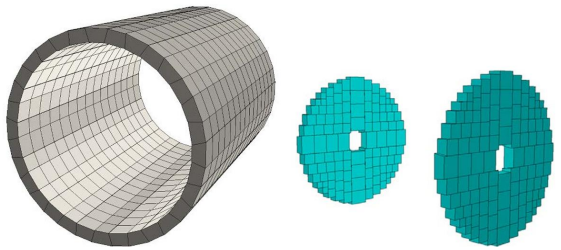
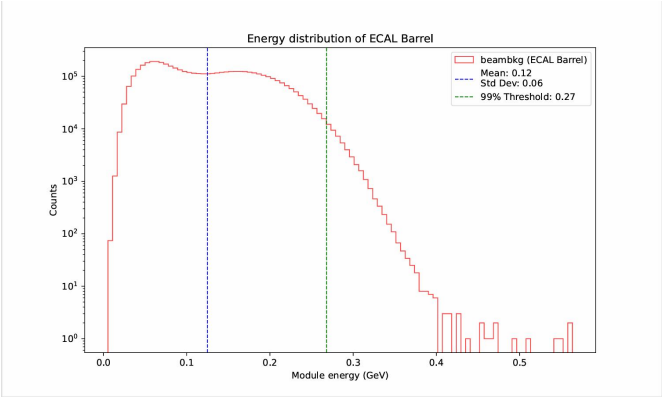


Figure 1: Schematic of ECAL



Cluster Analysis Process

- Seed Identification

  Locate modules with deposited energy greater than 0.6 GeV as seeds.

- Seed Merging

  Merge adjacent seeds into a single set, serving as the starting point for cluster identification.

- Cluster Expansion

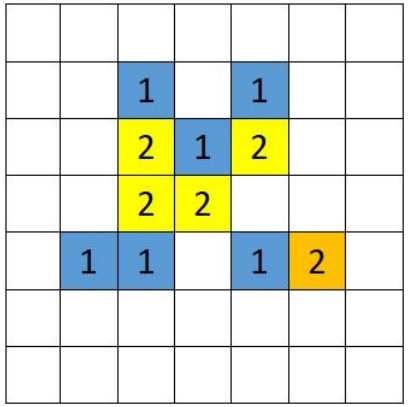
  Starting from the seeds, merge adjacent fired modules (above 0.2681 GeV) into the cluster.

- Conflict Resolution

  In cases where multiple clusters compete for the same module, assign the module to the cluster whose centroid is closest to the conflicting module.

$$X_C = \frac{\sum X_i \times E_i}{\sum E_i}$$

$$Y_C = \frac{\sum Y_i \times E_i}{\sum E_i}$$



Seeds are labeled as 2, members are labeled as 1.

- Cluster Characteristics
  - Cluster Size
  - Cluster Energy Total energy
  - Number of Clusters
  - Cluster Energy Sum per Event

.

- Physical Processes
  - ZH → νν$\bar{\nu}$γγ(5,000 events)
  - ZH → νν$\bar{\nu}$bb (10,000 events)

Cluster Analysis Results

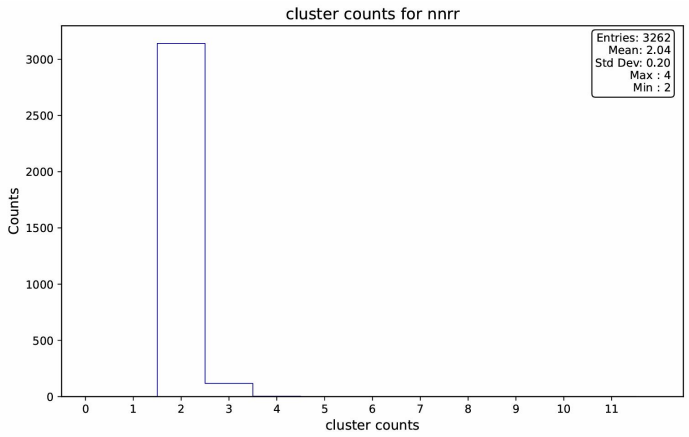


Figure 3.Distribution of cluster counts per event for the ZH → νν̄γγ process

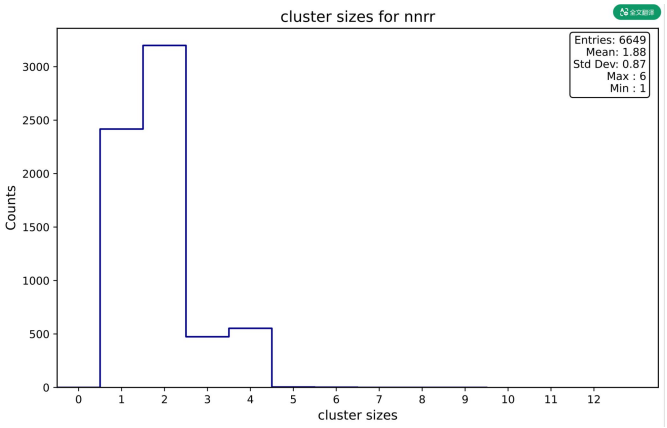


Figure 4.Distribution of cluster size per cluster for the ZH → νν̄γγ process

Out of 5,000 events, 3,262 satisfy the requirement that the photons from H → γγ are directed toward the barrel region.

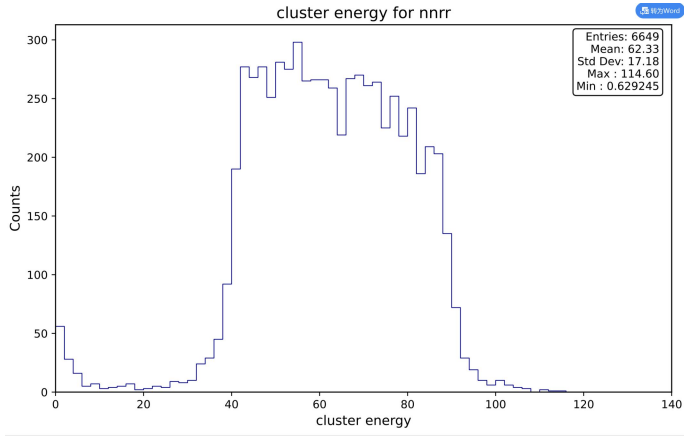


Figure 5.Distribution of cluster energy per cluster for the ZH → νν̄γγ process

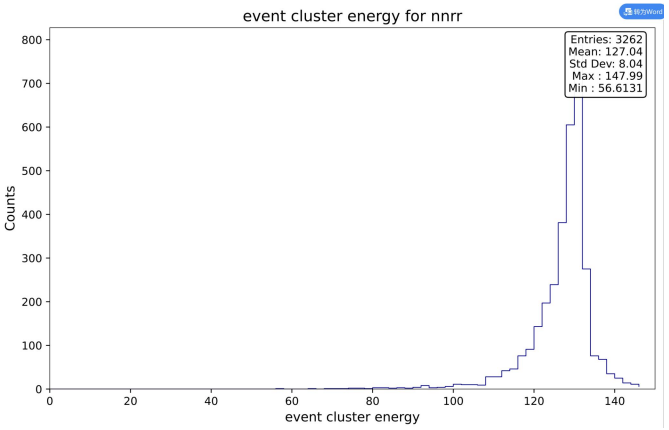


Figure 6.Distribution of total cluster energy per event for the ZH → νν̄γγ process

Cluster Analysis Results

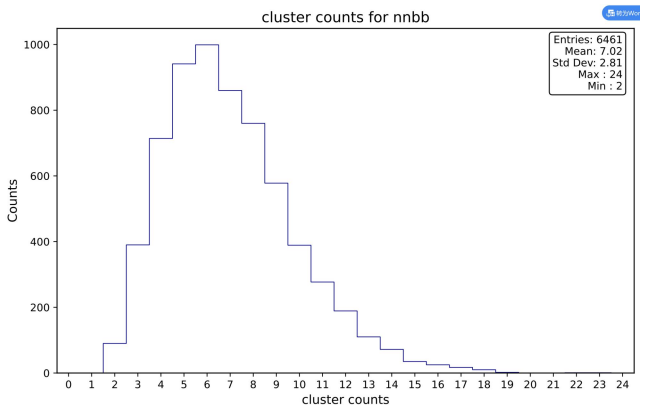


Figure 7.Distribution of cluster counts per event for the ZH → νvbb process

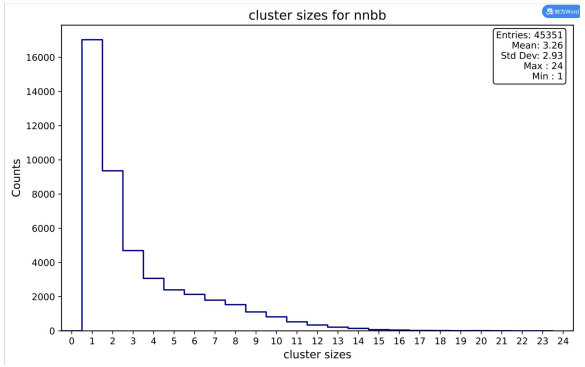


Figure 8.Distribution of cluster size per cluster for the ZH → νvbb process

Out of 10,000 events, 6,461 satisfy the requirement that the photons from H → bb are directed toward the barrel region.

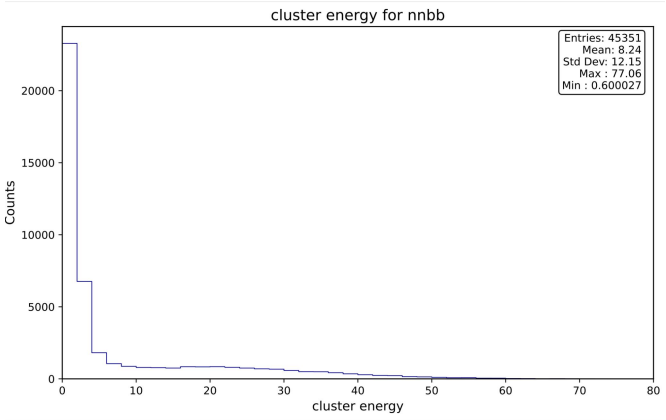


Figure 9.Distribution of cluster energy per cluster for the ZH → νvbb process

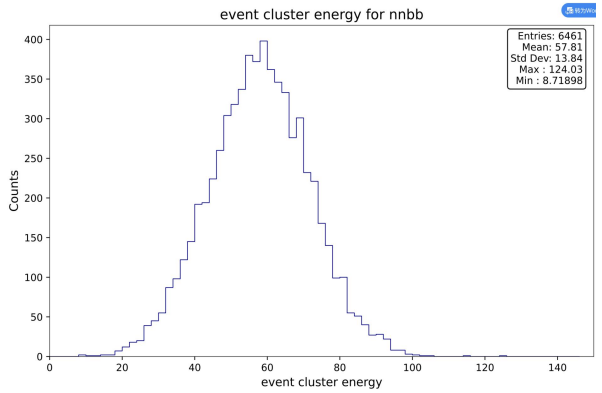


Figure 10.Distribution of total cluster energy per event for the ZH → νvbb process

Summary & Outlook

- Preliminary analysis results of the clusters in the barrel region have been obtained
- next step is to analyze the clusters in the endcap region
- The varying sizes of clusters in the endcap region pose significant challenges

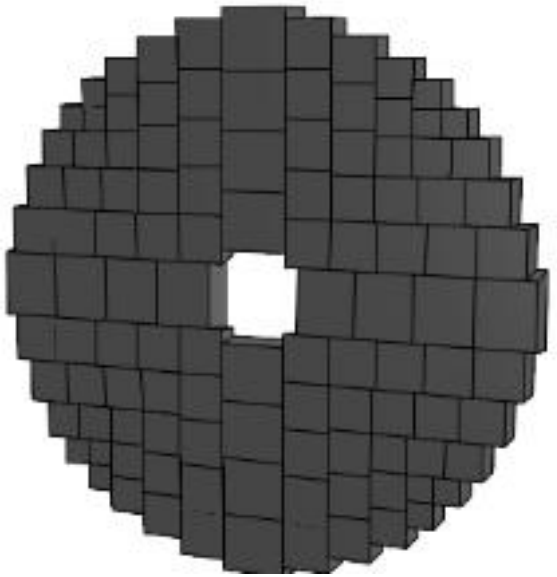


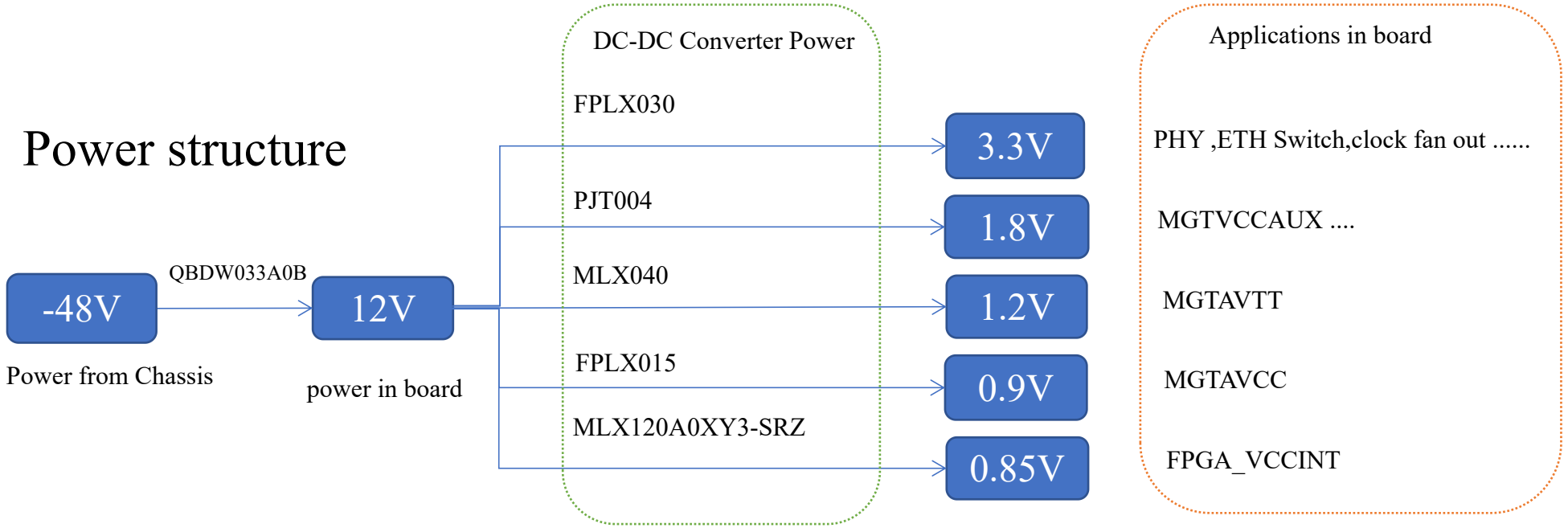
Figure 11: Schematic of ECAL endcap

Design progress

Power design

Power Consumption Evaluation Summary

Voltage (V)	3.3	1.8	1.2	0.9	0.85
Estimated Current (A)	20	4	16	8	80
Design Maximum Current (A)	30	8	40	15	120



Design progress

Power design

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V_{CC_SOM}	5V (4.75V – 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on-board power regulators.
V_{CC_BATT}	1.20 – 1.50V	150 nA – 3650 nA	External battery input for the RTC
V_{CCO_HPA}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 66
V_{CCO_HPB}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 65
V_{CCO_HPC}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 64
V_{CCO_HDA}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 45
V_{CCO_HDB}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 43
V_{CCO_HDC}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 44

SOM 功耗评估

供电电压（V）	5	3.3	1.8
电流(A)	4	3	3

IV. Electrical Characteristics

Parameter	Symbol	Unit	Min	Type	Max	Notes
Supply Voltage	Vcc	V	3.135		3.465	
Supply Current	Icc	A			1.5	
Module Total Power	P	W		1.8		

QSFP:

供电电压（V）	3.3
电流(A)	1.5*10

DDR4

供电电压（V）	2.5	1.2	0.6
电流(A)	0.2	1.7	0.5

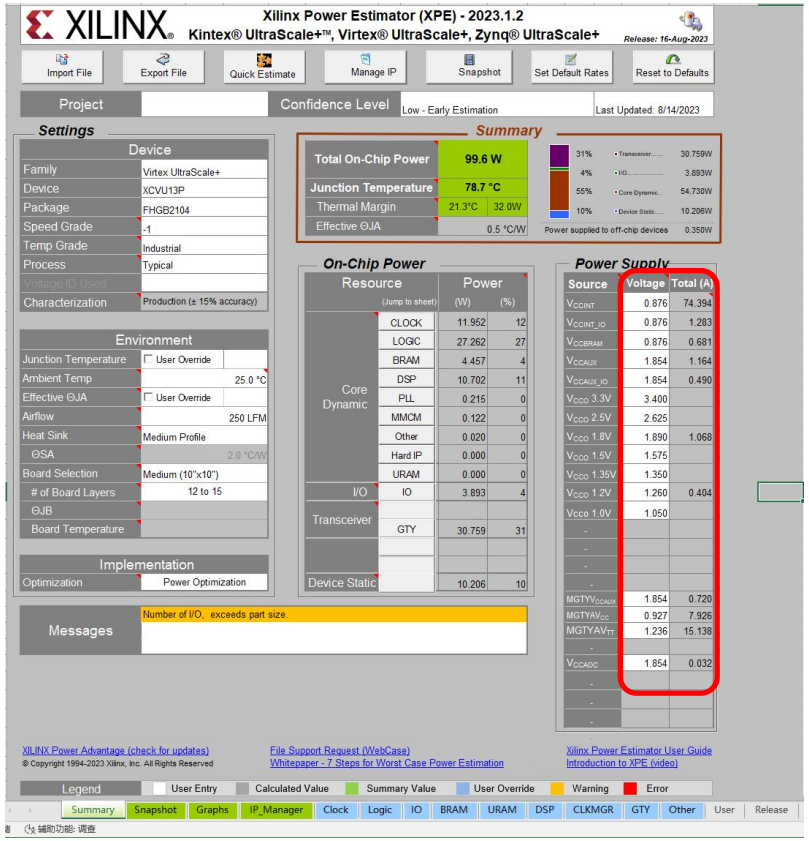
Table 13: DDR4 I_{DD} Specifications and Conditions – 4GB (Die Revision A)

Values are for the MT40A512M8 DDR4 SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

ParameterSymbol	24002133	Units		
One bank ACTIVATE-PRECHARGE current	DD0	512	480	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I_{PP} current	PP0	3232	mA	
One bank ACTIVATE-READ-PRECHARGE current	DD1	544	520	mA
Precharge standby current	DD2N	400	368	mA
Precharge standby ODT current	DD2NT	464	432	mA
Precharge power-down current	DD2P	256	240	mA
Precharge quiet standby current	DD2Q	328	312	mA
Active standby current	DD3N	536	504	mA
Active standby I_{PP} current	PP3N	2424	mA	
Active power-down current	DD3P	352	352	mA
Burst read current	DD4R	1280	1200	mA
Burst write current	DD4W	1440	1280	mA
Burst refresh current (1x REF)	DD5B	1536	1520	mA
Burst refresh I_{PP} current (1x REF)	PP5B	176	176	mA
Self refresh current: Normal temperature range (0°C to 85°C)	DD6N	160	160	mA
Self refresh current: Extended temperature range (0°C to 95°C)	DD6E	216	216	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	DD6R	8080	mA	
Auto self refresh current (25°C)	DD6A	7272	mA	
Auto self refresh current (45°C)	DD6A	8080	mA	
Auto self refresh current (75°C)	DD6A	128	128	mA
Auto self refresh I_{PP} current	PP6X	2424	mA	
Bank interleave read current	DD7	1680	1480	mA
Bank interleave read I_{PP} current	PP7	112	96	mA
Maximum power-down current	DD8	144	144	mA

Design progress

Power design



供电电压（V）	0.85	1.2	1.8	MGT_0.9	MGT_1.2	MGT_1.8
电流（A）	76	0.5	3	8	16	1

TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units
Total power, two CMOS REF inputs, Synth1 and six LVDS outputs enabled	P_{DISS}	—	0.8	—	W
Total current, 3.3V supply (VDD33+VDDOx pins)	I_{DD33}	—	160	322	mA
Total current, 1.8V supply (VDD18 pins)	I_{DD18}	—	207	519	mA

供电电压（V）	3.3	1.8
电流(A)	0.6*2	1*2

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Design progress

Power design

SWITCH

Symbol	Parameter	Conditions	Min	Typ	Max	U
Supply Current - Full 1000 Mbps Operation						
I_{DD_AH}	**AVDDH** supply current	**VDDIO** @ 3.3V Ports 1-5 in 1000BASE-T Ports 6 & 7 in RGMII (1000 Mbps) All ports 100% utilization		330		
I_{DD_IO}	**VDDIO** supply current			80		mA
I_{DD_CA}	**AVDDL** supply current			460		mA
I_{DD_CD}	**DVDDL** supply current			750		mA

供电电压（V）	2.5	1.8	1.2
电流(A)	0.4	0.1	1.3

PHY

4.6.2 Current Consumption when using Internal Regulators

Table 153: Current Consumption REG_IN
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{REG_IN}	3.3V Internal Regulator Supply	REG_IN	SGMII to 1000BASE-T with traffic		92		mA
			SGMII to 100BASE-TX with traffic		53		mA
			SGMII to 10BASE-T with traffic		43		mA
			Energy Detect		25		mA
			IEEE Power Down		13		mA

供电电压（V）	3.3
电流(A)	0.2

Table 154: Current Consumption AVDD33
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{AVDDR}	Analog 3.3V supply	AVDD33	SGMII to 1000BASE-T with traffic		58		mA
			SGMII to 100BASE-TX with traffic		16		mA
			SGMII to 10BASE-T with traffic		32		mA
			Energy Detect		2		mA
			IEEE Power Down		1		mA

SUPPLY CURRENT (Static)						
I_{CC}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-. PEM = L		175	215	mA
I_{CCZ}	Supply Current - Power Down Mode	$\overline{PWDN}$ = L, PEM = L		20	200	µA

供电电压（V）	3.3
电流(A)	0.3*2

Design progress

Power design

Table 1: Summary of Power Consumption Evaluation

Component	Quantity	Voltage (V)	5	3.3	2.5	1.8	1.2	0.85	0.6	MGT_1.8	MGT_1.2	MGT_0.9
SOM	1	Current (A)	4	3		3				1	16	8
QSFP	10	Current (A)		15								
DDR4(8GB)	1	Current (A)			0.4		3.4		1			
FPGA	1	Current (A)				3	0.5	76				
CLK_FAN	3	Current (A)		1.8		3						
SWITCH	1	Current (A)			0.4	0.1	1.3					
PHY	1	Current (A)		0.2								
BUFFER	2	Current (A)		0.6								
Total Current			4	20.6	0.8	9.1	5.2	76	1	1	16	8
DESIGN			?	30	?	4/个	40/个	120	2	4	40	15
Power Consumption			20	67.98	2	16.38	6.24	64.6	0.6	1.8	19.2	7.2
			LTM4705	LTM4630 18*2	LTM4644	LTM4637	LTM4644	mlx120	tps51200	PJT004	mlx040	fplx015

待确定:

5*2 20 4*3+4

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