



# **CEPC Common Trigger Board Design**

Dong Liu, Jingzhou Zhao, Sheng Dong IHEP











# Introduction



## What is Common Trigger Board

- An ATCA Development Platform
- Core component of L1 trigger system, the
  implementation of trigger algorithms and the testing
  of data readout bandwidth are both based on this

## Requirements

- High-Speed Data Transfer Performance
- High-Performance Data Processing Capability
- High-Capacity Data Buffering
- > Scalability



Figure 1 .CEPC Trigger structure

# Introduction



## Investigation Outcomes

Hardware structure should include:

### Board Infrastructure

- SoM
- Clock, power
- Storage
- ATCA Infrastructure
  - Backplane connectors
  - IPMC
  - Power input
  - Ethernet switch

### ➢ Payload

- Optical transceivers
- FPGA
- Clocks





- High-Speed Data Transfer
- Rocket IO +Optical transceivers
- **QSFP**,Firefly ,Minipod
- High-Performance Data Processing
  Board management
- FPGA



Figure 3.Serenity board overview (CMS BEE and Trigger)

- High-Capacity Data Buffering
- FPGA RAM (tens to hundreds of Mb)
- DDR4(8GB-64GB)
- SOM
- IPMC

- Optical Ethernet port: 40-100GbE
- DDR4 for mass data buffering ۲
- SoC module for board management ۲
- ۲

## Hardware structure design

- FPGA for data process ۲
- Optical channel: 10-25 Gbps/ch
- Channel number: 36-48 channels

- IPMC module for Power management



**HPCN V5 Block Diagram** 





### Component Selection

#### Table 12: Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Package	Package	VU3P	VUSP	VU7P	VU9P	VU11P	VU13P	VU19P	VU23P	VU27P	VU29P
(1)(2)(3)(4)(5)	(mm)	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, HD, GTY	HP, HD, GTY, GTM	HP, GTY, GTM	HP, GTY, GTM
VSVA1365	35x35								364, 0, 34(7), 4		
FFVC1517	40x40	520, 40									
FSVJ1760	42.5x42.5								572, 72, 34, 4		
FLGF1924(5)	45x45					624, 64					
FLVA2104	47.5x47.5		832, 52	832, 52				1			
FLGA2104	47.5x47.5				832, 52						
FHGA2104	52.5x52.5(6)						832, 52				
FLVB2104	47.5x47.5		702, 76	702, 76							
FLGB2104	47.5x47.5				702, 76	572, 76					
FHGB2104	52.5x52.5(6)						702, 76				
FLVC2104	47.5x47.5		416, 80	416, 80							
FLGC2104	47.5x47.5				416, 104	416, 96					
FHGC2104	52.5x52.5(6)						416, 104				
FSGD2104	47.5x47.5				676, 76	572, 76					
FIGD2104	52.5x52.5(6)						676, 76			676, 16, 30	676, 16, 30
FLGA2577	52.5x52.5				448, 120	448, 96	448, 128				
FSGA2577	52.5x52.5						448, 128			448, 32, 48	448, 32, 48
FSVA3824	65x65							1976, 96, 48			
EC1/02024	65v65							1664 06 90			

- (W) =	JFM9系列 SCRO 复旦政电子	PGA						
产品型号	JFM9RFVU3P JFM9RFVU3P-AS JFM9RFVU3P-N	JFM9RFVU3P5G JFM9RFVU3P5G-AS JFM9RFVU3P5G-N	JFM9RFVU9P JFM9RFVU9P-AS JFM9RFVU9P-N	JFM9VU3P JFM9VU3P-AS JFM9VU3P-N	JFM9VU9PA2104 FM9VU9PA2104-AS JFM9VU9PA2104-N	JKF9VU9P82104 JKF9VU9P82104-AS JKF9VU9P82104-N	JFM9VU13PB2104 JFM9VU13PB2104-AS JFM9VU13PB2104-N	JFM9VU13PA2577 JFM9VU13PA2577-AS JFM9VU13PA2577-N
对应国外厂家 /型号	Xilinx,XXVU3P	Xilinx/XCVU3P	Xilinx/XCVU9P	Xilinx/XCVU3P	Xilinx/XCVU9P	Xilina/XXVU9P	Xilinx/XCVU13P	Xilina/XXVU13P
逻辑单元数(K)	862	862	2,595	862	2,586	2,585	3,780	3,780
DSP个数	2,280	2,280	6,840	2,280	6,840	6,840	12,288	12,288
36KBRAM 容量(Mb)	25.3	25.3	75.9	25.3	75.9	75.9	94.5	94.5
288KURAM 容量(Mb)	90.0	90.0	270.0	90.0	270.0	270.0	360.0	360.0
Userl/0个数	520	520	448	520	702	702	702	448
SERDES通道数	20	20	60	40	76	76	76	128
ntanist	PCBMALMIKINAM PRPUNK FCBGA F1517	PCB基板的IDI和種 時列時期 FCBGA F1517	PCB-8645-01101848 P67918188 FCBGA G2577	PCB基板的DIR# 种列时的 FCBGA C1517	PCB基级的1218相 转列目前第 FCBGA 82104	PC8基板例化除栅 阵列时装 FCBGA 82104	PCB基础组织的建築 同时间接 FCBGA B2104	PCB基板倒扣球槽 用列IIII装 FCBGA A2577
CoreIfFIEE	0.85V	0.85V	0.854	0.89V	0.85V	0.85V	0.85V	0.85V
1/0工作电压	HPI0 1.0 ~ 1.8V	HPI0 1.0 ~ 1.8V	HPIO 1.0 ~ 1.8V	HPI0 1.0 ~ 1.8V	HPIO 1.0 ~ 1.8V	HPID 1.0 ~ 1.8V	HPI0 1.0 ~ 1.8V	HPIO 1.0 ~ 1.8V
质量等级	工业级 宽温级 GJ87400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJ87400N	工业级 宽温级 GJ87400N	工业级 変進级 GJ87400N	工 新規 克道級 GJB7400N
问世时间			2024 Q4	2024 Q1	2024 Q3	2024 Q2	2024 Q1	2024 Q3

Figure 5 .FPGA selection investigation

C C C

### Requirement

- Optical transceiver :36-48 channels
- ETH Switch :5 or more ports
- Clock:12 channels at least

### Recommand

- QSFP\*10 (40 channels)
- KSZ9897R(7 ports)
- ZL30274 \*2 (8\*2)
- K26 SOM







## Power design

말 <mark>랐</mark> Import File	Export File	Quick Estima	te Mana	ge IP	E Snapsł	not	Z Set Default Ra	tes R	aset to l	<u>⊾</u> Defaults
Project		C	Confidence Lev	vel <sub>Low - Ea</sub>	rly Estimatio	on		Last Update	ed: 8/14	/2023
Settings					SI	ımma	ry			
	Device		Total On C	hin Power	00.6	w/	31%	Transceiv		30.759W
	Virtex UltraScale+		Total Oni-Ci	inp i owei	33.0		4%	• 10		3.893W
	XCVU13P		Junction Te	mperature	78.7	°C	55%	Core Dyn	anic.	54.730W
ackage	FHGB2104		Thermal Ma	argin	21.3°C	32.0W	10%	• Device St	tetic	10.206W
beed Grade	-1		Effective OJ	A	(	0.5 °C/W	Power supplie	d to off-chip d	levices	0.350W
mp Grade	Industrial									
ocess	Typical		On-Chip	Power			Po	wer Sup	phy	_
			Reso		Pow	er	Sour	ce Vr 1	tage T	otal (A)
iaracterization	Production (± 15%	accuracy)		(Jump to sheet)	(W)	(%)	VCCINT		0.876	74.394
				CLOCK	11.952	12	V <sub>CCINT</sub>	.10	0.876	1.283
En	vironment			LOGIC	27.262	27	VCCBRA	w	0.876	0.681
	User Override			BRAM	4.457	4	VCCAUX		1.854	1.164
		25.0 °C	Coro	DSP	10.702	11	VCCAUX	00	1.854	0.490
	🗆 User Override		Dynamic	PLL	0.215	0	V <sub>cco</sub> 3	.3V	3.400	
low		250 LFM		MMCM	0.122	0	Vcco 2	.5V	2.625	
	Medium Profile			Other	0.020	0	V <sub>cco</sub> 1	.8V	1.890	1.068
		2.0 °C/W		Hard IP	0.000	0	V <sub>cco</sub> 1	.5V	1.575	
	Medium (10"x10")			URAM	0.000	0	V <sub>cco</sub> 1	.35V	1.350	
	12 to 1	5	/O	10	3.893	4	V <sub>cco</sub> 1	.2V	1.260	0.404
ЭJВ			Transceiver				Vcco 1	.0V	1.050	
loard Temperature				GTY	30.759	31	· ·			
Lorente							<u> </u>			
Imple	Rever Ontin	instian	Device Chalie				<u> </u>	_		
urnizauon	Power Optim		Device Static	1l	10.206	10	- MGTYV		1 854	0.720
	Number of I/O, ex	ceeds part size.					MGTYA	Vcc	0.927	7.926
Messages							MGTY	AVTT	1.236	15.138
								_		
							VCCADO		1.854	0.032
							-			
			Т	TDC	AF					
				1PC	IA					
VX Power Advantage (o pyright 1994-2023 Xilinx, k	check for updates) Ic. All Rights Reserved	File Whi	Support Request (W tepaper - 7 Steps for	ebCase) Worst Case Po	ower Estimat	tion	Xilinx F Introdu	Power Est	ator Us	er Guide
						-			-	

IV. Electrical Characteristics

Parameter		Symbol	Unit	Min	Туре	Max	Notes
Supply Voltage	OGED	Vcc	v	3.135		3.465	
Supply Current	QSFP	lec	A			1.5	
Module Total Power		Ρ	w		1.8		

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V <sub>CC_SOM</sub>	5V (4.75V – 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on- board power regulators.
V <sub>CC_BATT</sub>	1.20 - 1.50V	150 nA – 3650 nA	External battery input for the RTC
V <sub>CCO_HPA</sub>	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 66
V <sub>CCO_HPB</sub>	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 65
V <sub>CCO_HPC</sub>	1.00V - 1.80V SOV	1.0A	Voltage rail for HPIO bank 64
V <sub>CCO_HDA</sub>	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 45
V <sub>CCO_HDB</sub>	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 43
V <sub>CCO_HDC</sub>	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 44

Symbol	Parameter	Conditions N		Тур	Max	Units
Supply Co	urrent - Full 1000 Mbps Oper	ation IH SW1tc	h			
I <sub>DD_AH</sub>	AVDDH supply current	<b>VDDIO</b> @ 3.3V		330		mA
I <sub>DD_IO</sub>	VDDIO supply current	Ports 1-5 in 1000BASE-T		80		mA
I <sub>DD_CA</sub>	AVDDL supply current	(1000 Mbps)		460		mA
I <sub>DD_CD</sub>	DVDDL supply current	All ports 100% utilization		750		mA

Figure 7 .Power Consumption Analysis of On-board Devices

ParameterSymbol 24002133 Units				
One bank ACTIVATE-PRECHARGE currentI	DD0	512	480	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, pp currentl	PPO	3232	mA	
One bank ACTIVATE-READ-PRECHARGE currentl	DD1	544	520	mA
Precharge standby currentl	DD2N	400	368	mA
Precharge standby ODT currentl	DD2NT	464	432	mA
Precharge power-down currenti	DD2P	256	240	mA
Precharge quiet standby currentl	DD2Q	328	312	mA
Active standby currentl	DD3N	536	504	mA
Active standby Ipp currentI	PP3N	2424	mA	
Active power-down current	DD3P	352	352	mA
Burst read currenti	DD4R	1280	1200mA	0
Burst write currentl	DD4W	1440	1280mA	
Burst refresh current (1x REF)I	DD58	1536	1520mA	
Burst refresh Ipp current (1x REF)I	PP58	176	176	mA
Self refresh current: Normal temperature range (0°C to 85°C)I	DD6N	160	160	mA
Self refresh current: Extended temperature range (0°C to 95°C)I	DD6E	216	216	mA
Self refresh current: Reduced temperature range (0°C to 45°C)I	DD6R	8080	mA	
Auto self refresh current (25°C)I	DD6A	7272	mA	
Auto self refresh current (45°C)I	DD6A	8080	mA	
Auto self refresh current (75°C)I	DD6A	128	128	mA
Auto self refresh Ipp currentI	PP6X	2424	mA	
Bank interleave read currentl	DD7	1680	1480mA	
Bank interleave read Ipp currentl	PP7	112	96	mA
Maximum power-down currentl	DD8	144	144	mA

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units
Total power, two CMOS REF-inputs, Synth1 and sx LVDS outrats enable	ລະຄະຄາ	1f	0.8	-	w
Total current, 3:3V supply (VDD33+VDDOx pins)	IDD33	<u>-</u>	160	322	mA
Total current, 1.8V supply (VDD18 pins)	I <sub>DD18</sub>		207	519	mA







## Power design

Quantity Component Voltage (V) 5 3.3 2.5 1.8 1.2 0.85 0.6 **MGT 1.8 MGT 1.2 MGT 0.9** SOM Current (A) 3 3 16 8 4 1 1 **QSFP** 10 Current (A) 15 DDR4(8GB) Current (A) 0.4 3.4 1 1 FPGA Current (A) 0.5 76 3 1 CLK FAN Current (A) 1.8 3 3 SWITCH Current (A) 0.4 0.1 1.3 1 PHY Current (A) 0.2 1 BUFFER Current (A) 0.6 2 Total Current 20.6 0.8 9.1 5.2 76 16 8 4 1 1 **Power Consumption** 20 67.98 16.38 6.24 0.6 1.8 19.2 7.2 2 64.6

Table 1: Summary of Power Consumption Evaluation

Power Consumption in total : 206W



Power structure design







## Clock distribution design







## Schematic Design

#### Schematic design progress

Component	Status	Details
Power	Basic Completion	12->2.5V need to be refined
Clock Distribution	In Progress	Schematic for clock fanout device done
DDR4	Basic Completion	
Ethernet Switch	Basic Completion	
Z1,Z2,Z3 Connector	Basic Completion	
IPMC	In Progress	Interface signals require definition and refinement
QSFP	Basic Completion	
FPGA	In Progress	
SOM	In Progress	Interface signals require definition and refinement
Test and Configuration Interface	Not Started	
System Integration	Not Started	





Figure 10: Schematic Design - Top (DDR4), Bottom (QSFP)

## High-Speed Interface Arrangement

FPGA Positioning (Centralized placement)

- QSFP connector
- DDR4 connector
- ETH Switch
- > Power

PCB layout

- -48V-12V Converter Power
- MGT Power
- ≻ IO
  - Backplane connectors
  - RJ45, QSFP





# Design progress

## **Summary & Outlook**





- The hardware architecture design has been completed
- Primary Components Selection in Progress
- Clock fan out ,PHY,Eth switch,Power have been selected and validated against design requirements.
- Some components(e.g., oscillators, sensors, DDR4,) require further specification alignment.
- Schematic Design in Progress
- Detailed schematic design is underway, with the power subsystem designed .
- Next Phase: PCB Layout & Routing
- PCB layout and routing shall commence following schematic design sign-off.





# **Analysis of ECAL Barrel Cluster**

Dong Liu, Boping Chen IHEP

Analysis of ECAL Barrel Cluster 2025.06.26

## **Cluster Definition**

Cluster: groups of contiguous and adjacent calorimeter units with energy deposition above threhold

- Adjacency : 8-connected neighborhood .
- Unit : Supercell
- Seed : A high-energy fired module with a threshold of 0.6 GeV.
- Member : Low-energy fired modules with a threshold of 0.2681 GeV







Figure 1: Schematic of ECAL





#### Analysis of ECAL Barrel Cluster 2025.06.26

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# **Cluster Analysis Process**

• Seed Identification

Locate modules with deposited energy greater than 0.6 GeV as seeds.

• Seed Merging

Merge adjacent seeds into a single set, serving as the starting point for cluster identification.

• Cluster Expansion

Starting from the seeds, merge adjacent fired modules (above 0.2681 GeV) into the cluster.

• Conflict Resolution

In cases where multiple clusters compete for the same module, assign the module to the cluster whose centroid is closest to the conflicting module.



- Cluster Characteristics
  - Cluster Size
  - Cluster Energy Total energy
  - Number of Clusters
  - Cluster Energy Sum per Event



Seeds are labeled as 2, members are labeled as 1.

- Physical Processes
  - $ZH \rightarrow vv\gamma\gamma(5,000 \text{ events})$
  - $ZH \rightarrow vvbb (10,000 \text{ events})$



## **Cluster Analysis Results**





Figure 3.Distribution of cluster counts per event for the ZH  $\rightarrow \nu\nu\gamma\gamma$  process



Figure 5.Distribution of cluster energy per cluster for the  $ZH \rightarrow vv\gamma\gamma$  process



Out of 5,000 events, 3,262 satisfy the requirement that the photons from  $H \rightarrow \gamma \gamma$  are directed toward the barrel region.





Figure 6.Distribution of total cluster energy per event for the ZH  $\rightarrow \nu\nu\gamma\gamma$  process

## **Cluster Analysis Results**





Figure 7.Distribution of cluster counts per event for the  $ZH \rightarrow vvbb$  process



Figure 9.Distribution of cluster energy per cluster for the  $ZH \rightarrow vvbb$  process



Figure 8.Distribution of cluster size per cluster for the  $ZH \rightarrow vvbb$  process



Figure 10.Distribution of total cluster energy per event for the  $ZH \rightarrow vvbb$  process

Out of 10,000 events, 6,461 satisfy the requirement that the photons from  $H \rightarrow bb$  are directed toward the barrel region.

## **Summary & Outlook**

Preliminary analysis results of the clusters in the barrel region have been obtained

Analysis of ECAL Barrel Cluster

2025.06.26

- next step is to analyze the clusters in the endcap region
- The varying sizes of clusters in the endcap region pose significant challenges







## Power design

Power Consumption Evaluation Summary





## Power design

### SOM 功耗评估

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V <sub>CC_SOM</sub>	5V (4.75V – 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on-
			board power regulators.
V <sub>CC_BATT</sub>	1.20 - 1.50V	150 nA – 3650 nA	External battery input for the RTC
V <sub>CCO_HPA</sub>	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 66
V <sub>CCO_HPB</sub>	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 65
V <sub>CCO_HPC</sub>	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 64
V <sub>CCO_HDA</sub>	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 45
V <sub>CCO_HDB</sub>	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 43
V <sub>CCO_HDC</sub>	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 44

供电电压(V)	5	3.3	1.8
电流(A)	4	3	3

#### IV. Electrical Characteristics

Parameter	Symbol	Unit	Min	Туре	Max	Notes
Supply Voltage	Vcc	V	3.135		3.465	
Supply Current	lcc	A			1.5	
Module Total Power	P	w		1.8		

QSFP:	供电电压(V)	3.3
	电流(A)	1.5*10

	供电电压 (V)	2.5	1.2	0.6
DR4	电流(A)	0.2	1.7	0.5

#### Table 13: DDR4 IDD Specifications and Conditions – 4GB (Die Revision A)

Values are for the MT40A512M8 DDR4 SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

ParameterSymbol 24002133 Units				
One bank ACTIVATE-PRECHARGE currentl	DD0	512	480	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, bp currentl	PPO	3232	mA	
One bank ACTIVATE-READ-PRECHARGE currentl	DD1	544	520	mA
Precharge standby currentl	DD2N	400	368	mA
Precharge standby ODT currentl	D02NT	464	432	mA
Precharge power-down currentl	DD2P	256	240	m,A
Precharge quiet standby currentl	DD2Q	328	312	mA
Active standby currentl	DD3N	536	504	mA
Active standby Ipp currentI	PP3N	2424	mA	
Active power-down currentl	DD3P	352	352	mA
Burst read currentl	DD4R	1280	1200mA	
Burst write currentl	DD4W	1440	1280mA	
Burst refresh current (1x REF)	D058	1536	1520mA	
Burst refresh Ipp current (1x REF)I	PP58	176	176	m.A
Self refresh current: Normal temperature range (0°C to 85°C)I	DD6N	160	160	mA
Self refresh current: Extended temperature range (0°C to 95°C)I	DD6E	216	216	mA
Self refresh current: Reduced temperature range (0°C to 45°C)I	DD6R	8080	mA	
Auto self refresh current (25°C)I	DD5A	7272	mA	
Auto self refresh current (45°C)I	DD5A	8080	mA	
Auto self refresh current (75°C)I	DD6A	128	128	mA
Auto self refresh Ipp currenti	PP6X	2424	mA	
Bank interleave read currentl	DD7	1680	1480mA	
Bank interleave read Ipp currentl	PP7	112	96	mA
Maximum power-down currentl	DOB	144	144	mA

2025.06.26

#### CEPC Common Trigger Board Design Report 2025.06

供电电压(V)

6.26			

#### XILINX = XIIInx Power Estimator (XPE) - 2023.1.2 Kintex® UltraScale+™, Virtex® UltraScale+, Zynq® UltraScale+ 1 Release: 16-Aug-2023 Import File Export File Quick Estimate Set Default Rates Manage IP E Snapshot Confidence Level Low - Early Estimation Last Updated: 8/14/2023 Settings Summary 30,759V Total On-Chip Power 99.6 W Virtex UltraScale+ 3.893V 78.7 °C XCVU13P 54.730W FHGB2104 21.3°C 32.0W 10.206W 10% Device Static 0.5 \*C/W Power supplied to off-chip devices 0.350 Industrial **On-Chip Power** Power Supply Typical Resource Voltage Total (A aracterization Production (± 15% accuracy) 0.876 74.394 0.876 1.283 11.952 CLOCK 12 Environment LOGIC 27.262 0.876 0.681 27 User Override BRAM 4.457 1,854 1,164 4 DSP 10.702 1.854 0.490 25.0 °C 11 User Override PLL 0.215 3.400 250 LFM MMCM 0.122 2.625 Medium Profile Other 0.020 1.890 1.068 Hard IP 0.000 1.575 URAM Medium (10"x10") 0.000 1.350 12 to 15 ю 3.893 1.260 0.404 1.050 GTY 30.759 31 Power Optimization 10.206 10 1.854 0.720 mber of I/O exceeds part size 0.927 7.926 1.236 15.138 1.854 0.032

File Support Request (WebCase) Whitepaper - 7 Steps for Worst Case Power Estimation

Clock Logic

Legend User Entry Calculated Value Summary Value User Override

Xilinx Power Estimator User Guid Introduction to XPE (video) Warning Error

Other User Release

IO BRAM URAM DSP CLKMGR GTY

Power design

XILINX Power Advantage (check for updates) © Copyright 1994-2023 Xilinx, Inc. All Rights Reserved

者 (火辅助功能:调查

Summary Snapshot Graphs IP\_Manager

电流(A)	76	0.5	3	8	16

1.8

#### **TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS**

1.2

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units
Total power, two CMOS REF inputs, Synth1 and six LVDS outputs enabled	P <sub>DISS</sub>		0.8		W
Total current, 3.3V supply (VDD33+VDDOx pins)	I <sub>DD33</sub>	<u>10</u>	160	322	mA
Total current, 1.8V supply (VDD18 pins)	I <sub>DD18</sub>		207	519	mA

供电电压(V)	3.3	1.8
电流(A)	0.6*2	1*2

时钟

0.85

Design	progress	



MGT\_1.2

MGT\_1.8

1

MGT\_0.9



## Power design

### SWITCH

Symbol	Parameter	Conditions	Min	Тур	Мах	└ 供电电压 (∨)	2.5	1.8	1.2
Supply Cu	urrent - Full 1000 Mbps Opera	ation				I. N.N. (			
I <sub>DD_AH</sub>	AVDDH supply current	<b>VDDIO</b> @ 3.3V		330		= 电流(A)	0.4	0.1	1.3
I <sub>DD_IO</sub>	VDDIO supply current	Ports 1-5 in 1000BASE-T		80		ma			
I <sub>DD_CA</sub>	AVDDL supply current	(1000 Mbps)		460		mA			
I <sub>DD_CD</sub>	DVDDL supply current	All ports 100% utilization		750		mA			

### PHY

#### 4.6.2 Current Consumption when using Internal Regulators

#### Table 153: Current Consumption REG\_IN

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Тур	Max	Units
I <sub>REG_IN</sub>	G_IN 3.3V Internal REG_IN	SGMII to 1000BASE-T with traffic		92		mA	
	Regulator	gulator pply	SGMII to 100BASE-TX with traffic		53		mA
	Supply		SGMII to 10BASE-T with traffic		43		mA
		Energy Detect		25		mA	
		IEEE Power Down		13		mA	

#### Table 154: Current Consumption AVDD33

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Тур	Max	Units
IAVDDR	Analog 3.3V	AVDD33	SGMII to 1000BASE-T with traffic		58		mA
	supply		SGMII to 100BASE-TX with traffic		16		mA
			SGMII to 10BASE-T with traffic		32		mA
			Energy Detect		2		mA
					4		0

供电电压	(V)	3.3	
电流(A)		0.2	

SUPPLY CURRENT (Static)									
I <sub>CC</sub>	Supply Current	All inputs and outputs enabled and active, terminated with differential load of $100\Omega$ between OUT+ and OUT PEM = L	175	215	mA				
I <sub>CCZ</sub>	Supply Current - Power Down Mode	PWDN = L, PEM = L	20	200	μΑ				

3.3



供电电压

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## Power design

Table 1: Summary of Power Consumption Evaluation

Component	Quantity	Voltage (V)	5	3.3	2.5	1.8	1.2	0.85	0.6	MGT_1.8	MGT_1.2	MGT_0.9
SOM	1	Current (A)	4	3		3				1	16	8
QSFP	10	Current (A)		15								
DDR4(8GB)	1	Current (A)			0.4		3.4		1			
FPGA	1	Current (A)				3	0.5	76				
CLK_FAN	3	Current (A)		1.8		3						
SWITCH	1	Current (A)			0.4	0.1	1.3					
РНҮ	1	Current (A)		0.2								
BUFFER	2	Current (A)		0.6								
Total Current			4	20.6	0.8	9.1	5.2	76	1	1	16	8
DESIGN			?	30	?	4/个	40/个	120	2	4	40	15
Power Consumption			20	67.98	2	16.38	6.24	64.6	0.6	1.8	19.2	7.2
		I	_TM4705	LTM4630 18*2	LTM4644	LTM4637	LTM4644	mlx120	tps51200	PJT004	mlx040	fplx015
待确定:			5*2			20	4*3+4					

ltm4671