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CEPC Reference Detector

Technical Design Report

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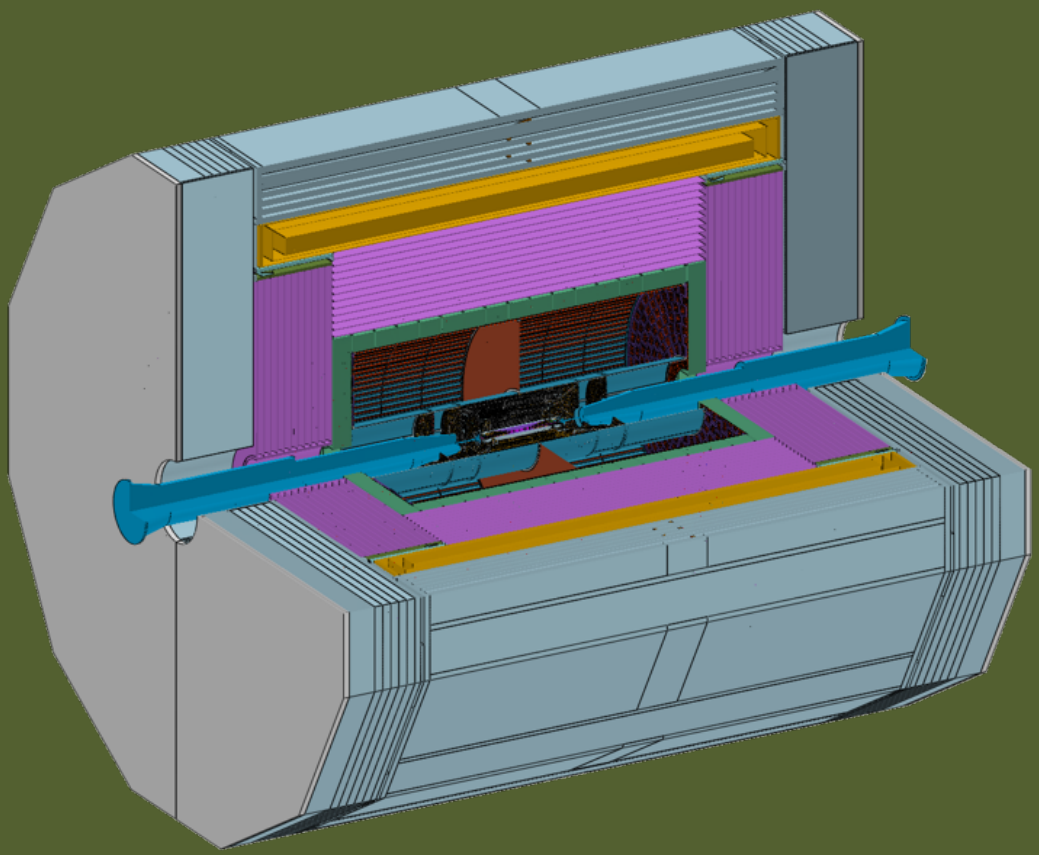


Chapter 4 Vertex Detector

The CEPC vertex detector is a crucial component of the tracking system, designed to provide excellent spatial resolution and ultra-low material budget for precision vertexing and flavor tagging.

A high-granularity low-mass design based on Monolithic Active Pixel Sensor (MAPS) has been proposed and selected as the CEPC vertex detector baseline, in order to achieve an excellent impact parameter resolution while maintaining low power consumption and air cooling compatibility. The MAPS technology allows for sub-5 μm spatial resolution and minimal dead zones, with a target material budget of less than 0.15% radiation length (X_0) per layer, ensuring high tracking performance without compromising the calorimeter and timing detector coverage.

The CEPC vertex detector consists of several concentric cylindrical layers surrounding the interaction point and is finely segmented in both the longitudinal and transverse directions. This layout is optimized to provide full solid angle coverage and to ensure efficient reconstruction of secondary and tertiary vertices.

This chapter is organised in the following structure: the overall design considerations are outlined in Sec. 4.1, followed by the design on detector layout along with estimates of the background rate and radiation dose in this layout. Detailed sensor and readout technologies are presented in Sec. 4.2, Mechanics and cooling design as well as service design are presented in Sec. 4.3. R&D of key technology are presented in Sec. 4.5 to support the baseline design of the CEPC vertex detector. The detailed simulation of expected detector performance and detector alignment strategy are presented in Sec. 4.6. Finally, The summary and future plan are presented in Sec. 4.7.

4.1 Detector overall design

4.1.1 Vertex detector design specification

The CEPC is designed to operate at higher collision frequencies, accommodating multiple collision modes. In its initial 10 years, the plan includes running at 240 GeV in the Higgs boson factory mode and at 90 GeV in the Z boson factory mode. Specifically, the collision frequency for the Higgs factory is approximately 1.7 MHz, while the Zboson factory mode operates at about 14.5 MHz during the initial low-luminosity phase and increases to 43 MHz in the later high-luminosity phase. These frequencies significantly exceed the 100 kHz collision frequency of the A Large Ion Collider Experiment (ALICE) experiment, posing challenges in maintaining low power consumption at higher operational frequencies - a critical aspect of the vertex detector chip development for this project. To

balance power efficiency and timing performance, the CEPC vertex detector is designed with a power consumption limit of below 40 mW $\cdot$ cm^{-2} while maintaining a time stamp precision within 100 ns for recorded hits.

Additionally, the CEPC requires the vertex detector to achieve higher spatial resolution, targeting levels between 3 to 5 μm, and to maintain a low material budget of less than 0.15% X_0 per layer. This capability is essential for studying the properties of the Higgs particle, particularly its decay channels involving bottom and charm quarks, and for exploring potential new physics phenomena. The performance of the vertex detector directly impacts the physics objectives of the CEPC.

To meet the requirements mentioned above, the vertex detector has selected 65 nm technology as the baseline for chip development. Preliminary simulations and tests based on the first CEPC vertex detector prototype indicate that the power consumption at low-luminosity Zmode operation for the 180 nm technology is larger than 60 mW/cm^2. This level of power dissipation exceeds the air cooling capacity of the vertex detector, resulting in sensor temperatures surpassing the operational upper limit of 30 °C. To address this critical issue, the vertex detector has adopted 65 nm technology as the baseline technology. This choice significantly reduces power consumption and also offers the potential for smaller pixel sizes, thereby enhancing spatial resolution.

During extended runs at the Z-pole, the vertex detector will be subjected to significant radiation exposure and intense beam-related backgrounds, requiring sensor technologies with high radiation tolerance, low noise, fast timing, and reliable long-term stability. Additionally, the readout electronics must handle high occupancy and deliver data at rates sufficient to cope with the demanding trigger and data acquisition requirements, all while operating under stringent power and cooling constraints to maintain mechanical stability and minimize distortions. In summary, the key requirements are listed in Table 4.1:

Table 4.1: Baseline Requirements and Overall Vertex Detector Design Parameters

Parameter	**Baseline Requirement / Design**
Operation Period	First 10 years (Higgs factory + low-luminosity Zrun)
Number of Barrel Layers	6 layers
Layer Radii	~11–40 mm
Material Budget per Layer	$\leq$ 0.15% X_0
Fluence	$\sim 2 \times 10^{14}$Neq/cm^2 (for first 10 years)
Operation Temperature	~ 5°C to 30°C
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures to minimize mass
Replacement Strategy	Replacement/upgrade after ~10 years
Spatial Resolution	~3–5 μm
Power Consumption	< 40mW/cm^2 (air cooling requirement)
Time stamp precision	± 100 ns

4.1.2 Detector layout

In the ~~baseline~~ layout, shown as Figure 4.1, the first four layers utilize stitching technology, with each layer composed of two semicircular structures spliced together. This technology employs wafer stitching techniques to fabricate large-area sensors that can be integrated directly into a curved geometry. By reducing or eliminating the need for multiple planar tiles and mechanical support frames, curved sensors significantly lower the overall material ~~budget~~. ~~There~~ is a mechanical gap between the two semicircular structures ranging from 0.2 to 0.5 mm, as shown in Table 4.2. The semicircular structure achieved through stitching technology requires the entire chip to be bent along the phi direction as a half arc corresponding to each radius. The position of different layers determines the arc length of the semicircle, which defines the width of the whole chip. Additionally, to satisfy the covering pole angle of 8.1°, the length of the whole chip is also determined. Due to wafer size limitations, stitching technology cannot be effectively applied to the large-area outer layers. Therefore, we employ conventional double-layer planar CMOS sensors with a ladder design for the 5th and 6th layers as Figure 4.2a shows. With the outter radius of the beam pipe in the CEPC-TDR set at 10.7 mm, the radius of the innermost layer in the vertex detector baseline is designed to be 11.06 mm based on the chip design of the stitching scheme.

A backup detector layout using 3 layers of double-sided ladders with planar CMOS sensors are also considered as Figure 4.2b shows. The backup layout represents a well-established, more conventional option. It serves as alternative ~~fallback~~ solution if the baseline layout with curved technology encounters unforeseen challenges. However, it introduces additional material and complexity due to the need for mechanical support, overlaps between ladders, and potentially thicker support elements.

Detailed parameters for baseline vertex detector layout and backup detector layout are provided in Table 4.2. The intrinsic single-point resolution of the chip is derived from the TaichuPix-3 beam current experiments, with a conservative resolution of 5 μm.

Stitching plan in baseline layout On a 300 mm wafer, the stitching plan is designed to meet the layout requirements of the four stitching layers in the ~~baseline~~ scheme. To enhance the design reticle utilization and streamline the process flow, the same chip is used to fulfill the baseline scheme requirements, and the same mask plate is employed. Due to the required arc length and the integer number of instances needed per layer, an instance with a dimensions of 17.277 × 20.000 mm^2 is used as the Repeated Sensor Unit (RSU)s (see Section 4.2.2). Three layouts are designed on a wafer, with the A/B/C regions of different lengths designed based on the required z-axis length. The preliminary stitching plan of the silicon wafer and the dimensions of each half layer are depicted in Figure 4.3. Each region is composed of repeated sensor units with different rows and columns, and

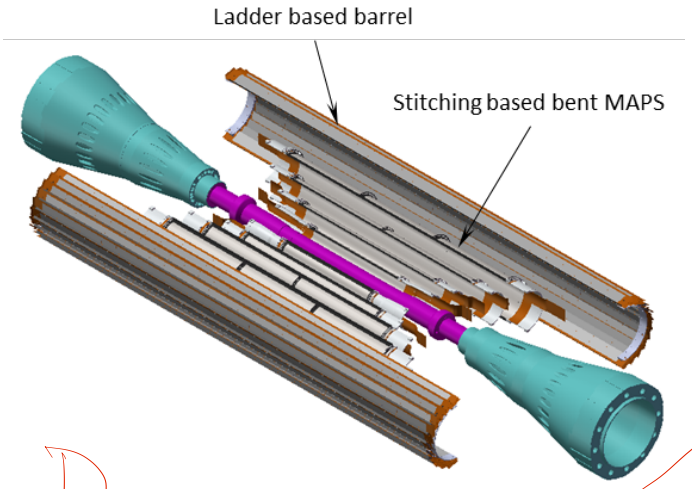
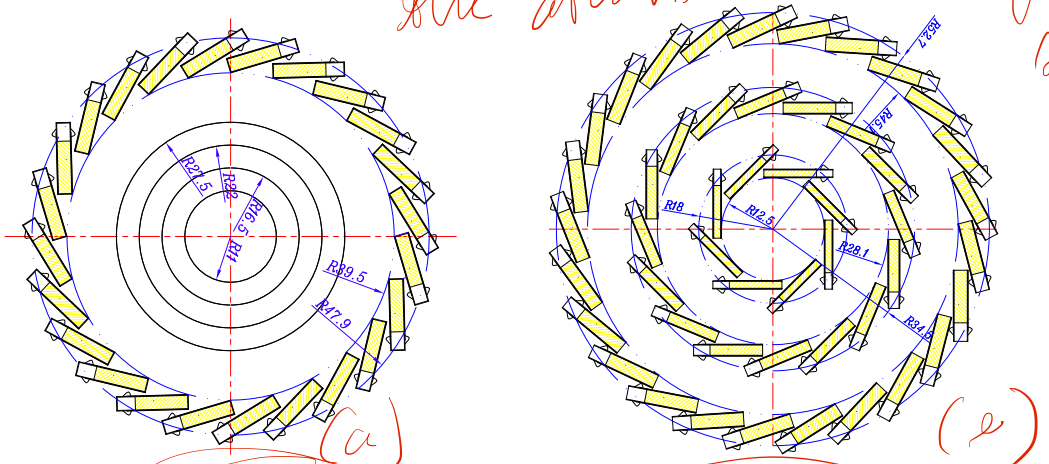


Figure 4.1: Baseline design diagram of the vertex detector. The first four layers are designed as single-layer structures (full-model cylindrical structure) using 65 nm Cmos Image Sensor (CIS) stitched sensors, while the last two layers are designed as double-layer structures (ladder structure) utilizing full size 65 nm CIS sensors.



(a) Sectional view of the VTX baseline layout.

(b) Sectional view of the VTX backup layout.

Figure 4.2: Sectional view of baseline and backup layout. (a) The inner four layers are bent MAPS with semicircular structure and for the 5th and 6th layers are double-layer planar CMOS sensors with ladder desgin. (b) All the 6 layers (3 layers of double sided ladders) are composed of planar CMOS sensors.

chip peripheral circuits and I/O pads at the left and right edges.

BVTX 1 and BVTX 3 share the C region, with BVTX 1 containing the two C region of the two modules. BVTX 2 utilizes the A region chip, consisting of two A region 3 modules arranged along the z-direction and two A region 3 modules arranged along ϕ-direction. BVTX 3 employs the C region chip, consisting of two C region 4 modules arranged along the z-direction and two C region 4 modules arranged along the ϕ-direction. BVTX 4 adopts the B region chip, consisting of two B region 5 modules arranged along

Table 4.2: Geometric configuration parameters. Bent Vertex Layer (BVTX) is used to denote the layer of VTX employing a curved stitching CMOS sensor, while Planar Vertex Layer (PVTX) is used to denote the layer of VTX employing a planar CMOS sensor. The effective thickness of the support structure in each layer in baseline layout and backup layout are also listed.

Layout	BVTX/ PVTX X	radius mm	length mm	arc length mm	height mm	support thickness µm
Baseline	BVTX 1	11.1	161.4	69.1	-	45
	BVTX 2	16.6	242.2	103.7	-	32
	BVTX 3	22.1	323.0	138.2	-	31
	BVTX 4	27.6	403.8	172.8	-	29
	PVTX 5-6	39.5	682.0	-	3.3	300
Backup	PVTX 1-2	12.5	260.0	-	1.7	300
	PVTX 3-4	27.9	494.0	-	2.6	300
	PVTX 5-6	43.8	749.0	-	3.3	300

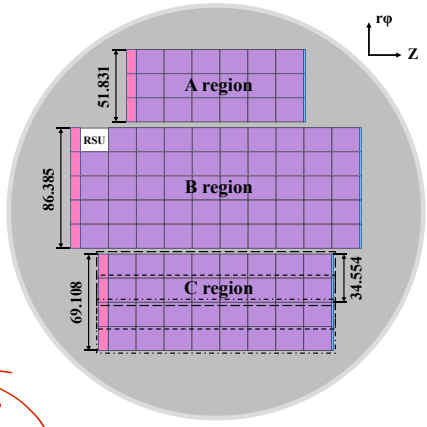


Figure 4.3: The arrangement of stitching frames on a 300 mm wafer. The purple part represents the RSUs, the pink represents the Left-End Block (LEB) (Left-End Block), and the blue represents the Right-End Block (REB) (Right-end Block). To meet the requirements of each layer of the vertex detector, the A/B/C regions are designed with different lengths and widths. The A and B regions are used to make one of the sensors for BVTX 2 and BVTX 4, respectively. The full C region can be used for one of the sensors for BVTX 3. The C region can be divided into four modules along the vertical direction. Using two modules of the C region can make a sensor for BVTX 1. The three possible groupings of two modules are indicated by long-dashed lines, short-dashed lines, and dash-dot lines, respectively.

the z-direction and two B region 5 modules arranged along the ϕ-direction. BVTXs 2, 3, and 4 are spliced in the z-direction, resulting in a 0.5 mm splicing seam at z = 0, also referred to as a mechanical gap, as shown in Figure 4.4.

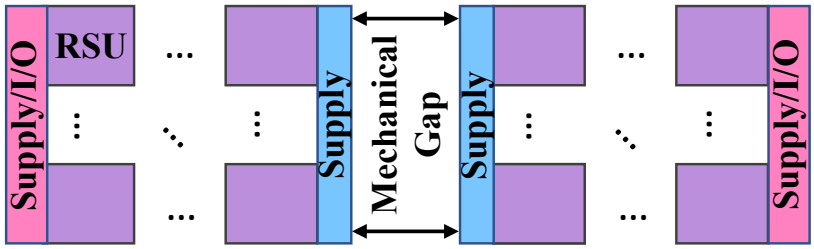


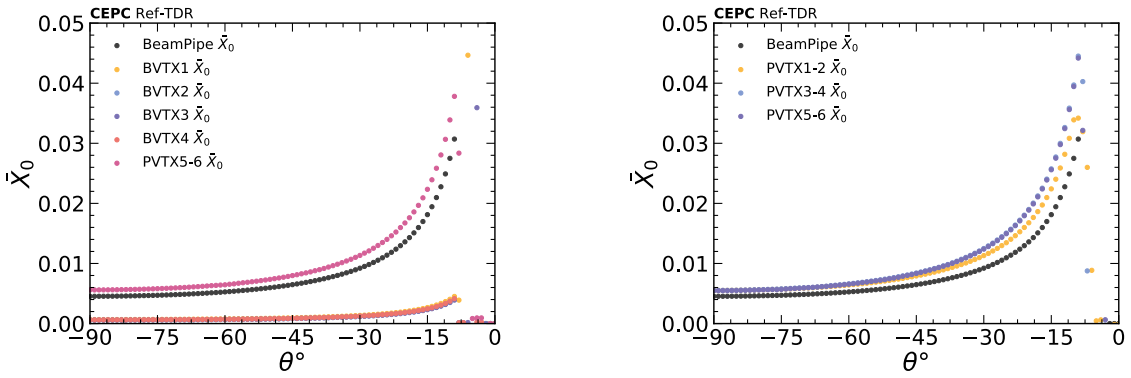
Figure 4.4: Schematic diagram of layer 2/3/4 assembly (not to scale).

Considering the mechanical dead zones in the ϕ direction and the dead zones in the width of the whole chip, the BVTX 1, BVTX 2, BVTX 3, and BVTX 4 of the vertex detector are rotated by an angle when mounted. This angular adjustment minimizes the occurrence of multiple dead zones at the same angle in the $r\phi$ plane. Each semicircular structure is supported by a Carbon Fiber Reinforced Polymer (CFRP) (Carbon Fibre-Reinforced Polymer) material with a specific thickness (see Section 4.3.1.3). The amount of the vertex detector material per layer is detailed in Table 4.3.

Double-sided Ladders in baseline layout The fifth and sixth layers are constructed using Taichu chips, each sized 15.9 × 25.7 mm^2 with a thickness of 40 µm. The back of the chip is affixed to the flex that transmits the signal using glue. The chip is treated as a unit, and the dead zones of the adhesive are arranged from the $-z/2$ region to the $z/2$ region at intervals of 0.1 mm. The flex is glued to both sides of the support structure CFRP to create a complete ladder cell as shown in Figure 4.6, where the effective thickness of the support structure CFRP hollow pipe is 300 µm, as described in the Section 4.3.1. The geometric center of the ladder unit rotates around the origin at a specific radius position from the $\phi = 0$ position, while maintaining the height of the wire, forming a barrel structure known as PVTX 5-6 to ensure that no particles leak out in the ϕ direction. A total of 24 ladder structures are utilized in the fifth and sixth layers.

Material budget for baseline and backup layout The backup layout replaces the first four layers of the stitching chip in the baseline layout with a structure similar to the PVTX 5-6. To optimize the material budget and accommodate the readout electronics, each ladder of PVTX 1-2, PVTX 3-4 and PVTX 5-6 consists of eight layers of aluminum, forming a symmetric ladder structure as shown in Figure 4.6. Additionally, the innermost layer of PVTX 1-2 has a radius of 12 mm, which differs from BVTX 1. Figure 4.5 shows

the variation of the average material budget X_0 with θ in the ϕ direction. Table 4.3 lists the material budget of each layer for the two configurations.



(a) Baseline layout. **(b)** Backup layout.

Figure 4.5: The average value $\bar{X}_0$ within the range of $\phi \in (0, 360)°$ of two configurations, the baseline layout 4.5a and the backup layout 4.5b, varies with θ.

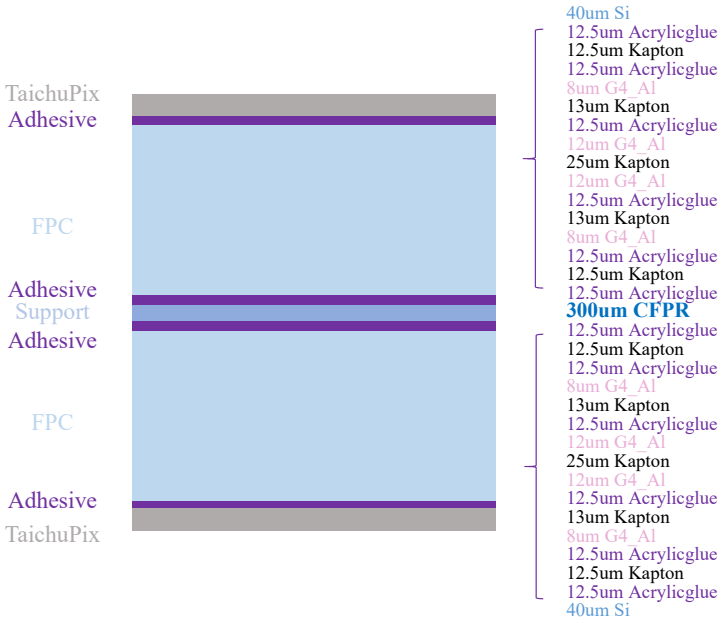


Figure 4.6: Longitudinal cross-section of a ladder in the backup layout, composed of two layers of chips and other materials, such as glue, carbon fiber, and aluminum. Each ladder of PVTX 1-2, PVTX 3-4 and PVTX 5-6 in the backup layout, as well as PVTX 5-6 in the baseline layout, utilizes this structure.

Table 4.3: The material budget parameters of the baseline layout and backup layout.

Layout	Beampipe	layer 1	layer 2	layer 3	layer 4	layer 5	layer 6
Baseline	0.454%	0.067%	0.059%	0.058%	0.061%	0.280%	0.280%
Backup	0.454%	0.276%	0.276%	0.276%	0.276%	0.287%	0.287%

4.1.3 Background estimation

As a kind of important information, the hit rate significantly affects the design specifications of the sensor. The details of each component's contribution to the VTX will be discussed in the Chapter 3 . In this subsection, we will only present the total hit rate, data rate, occupancy, and other relevant information for each mode.

Before we talk about these information, the definition of them should be declared. When a particle passes through a chip, several pixels on that chip may generate signals due to a series of physical effects. The collection of signals produced by the same particle on the same chip is referred to as a hit, and the number of pixels contained in this collection is known as the cluster size. The number of hits per unit time is termed the hit rate. For a given time window, the ratio of the number of active subunits within a cell to the total number of subunits in that cell is referred to as the occupancy of the cell during that time window. For example, when the cell is defined as a specific chip, the numerator is the total number of active pixels within that chip. When the cell is defined as a specific layer, the numerator is the total number of active chips within that layer.

In order to calculate the data rate, information about the cluster size is essential. To compute the data rate more accurately, we did not set the cluster size as a fixed value; instead, we referenced the results from the TaichuPix-3 beam test and calculated the cluster size based on the particle's incidence angle. The background hit rate and data rate are shown as Table 4.4, and the hit rate distributions of Higgs as well as Zmode are shown as Figure 4.7 and Figure 4.8.

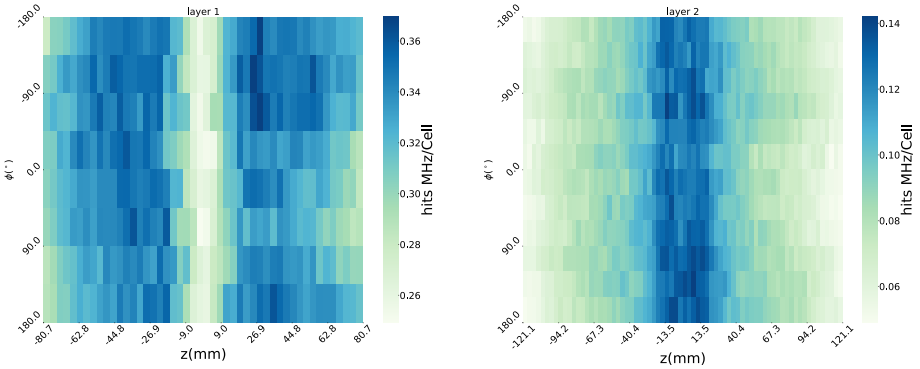


Figure 4.7: Hit rate distribution of Higgs mode. The shape of VTX is approximately cylindrical, where the x-axis can be equivalently regarded as the z-axis of the global coordinate, and the y-axis can be equivalently regarded as the polar angle ϕ of the global coordinate. Synchrotron radiation is not included.

For the VTX, the primary sources of beam background are synchrotron radiation and pair production. However, due to the excessive computational resources required for simulating and analyzing synchrotron radiation, we did not perform simulations and analyses with the same event statistics and granularity as those for other beam backgrounds.

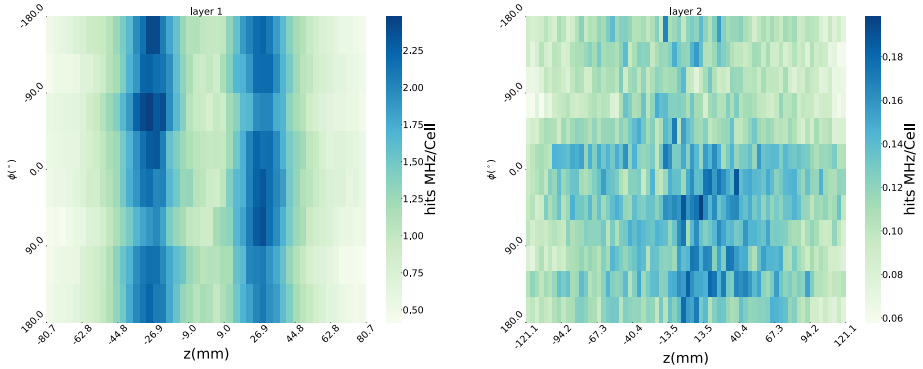


Figure 4.8: Hit rate distribution of Z mode. For we could not completely handle high-lumi Z mode now, as well as the major difference between high-lumi Z with Z mode is luminosity which means their hit rate distribution is similar, the hit rate distribution of high-lumi Z would not be shown here. Synchrotron radiation is not included.

Table 4.4: Summary of background estimation. Current detector scheme cannot completely handle high-lumi Z mode, so the result of high-lumi Z will not be shown here. For the results of high-lumi Z, based on accelerator parameters, a rough estimation can be made by simply multiplying the existing Z mode results by a factor of 3. Synchrotron radiation is included.

Layer	**Ave. Hit Rate MHz/cm^2**	**Max. Hit Rate MHz/cm^2**	**Ave. Hit Rate×C MHz/cm^2**	**Max. Hit Rate×C MHz/cm^2**	**Ave. Data Rate Mbps/cm^2**	**Max. Data Rate Mbps/cm^2**
Higgs: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 346ns, 53 %Gap, 25× 25 μm^2/ pixel)						
1	2.45	2.79	8.17	10.48	261.29	335.36
2	0.67	1.07	2.18	3.48	69.59	111.41
3	0.17	0.35	0.62	1.19	19.68	38.21
4	0.08	0.18	0.32	0.98	10.25	31.39
5	0.03	0.15	0.11	0.74	3.41	23.73
6	0.02	0.09	0.07	0.41	2.37	13.24
Zmode: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 69ns, 9 %Gap, 25× 25 μm^2/ pixel)						
1	9.35	18.68	42.45	88.23	1358.33	2823.36
2	0.89	1.47	3.73	7.54	119.24	241.36
3	0.31	0.75	1.45	5.99	46.49	191.75
4	0.19	0.47	0.95	4.86	30.50	155.50
5	0.05	0.10	0.20	0.45	6.40	14.38
6	0.04	0.07	0.15	0.38	4.80	12.17

Based on simulation results of approximately 1×10^9 synchrotron photons, we estimate that the beam background contribution from synchrotron radiation is comparable to that from pair production. Therefore, when presenting Table 4.4, to incorporate the synchrotron radiation results, we multiplied the pair production contribution by a factor of 2. However, it should be noted that the actual maximum value will be lower than simply doubling the pair production results.

We used a bunch crossing as a time window to calculate the occupancy of different modes at various levels, and the results are as Table 4.5.

Table 4.5: Occupancy estimation. †: Considering that the only difference between the two modes in the current simulation lies in the bunch settings, the occupancy in both modes should be similar. Therefore, they are combined and presented as *Z*mode. Synchrotron radiation is not included.

Layer	Mode	Ave. Occupancy@Pixel ($\times10^{-5}$ / BX)	Max. Occupancy@Pixel ($\times10^{-5}$ / BX)
1	Higgs	1.818	2.331
2		0.484	0.778
3		0.137	0.265
4		0.071	0.219
5		0.024	0.170
6		0.017	0.095
1	*Z* Mode	0.972	2.026
2		0.085	0.168
3		0.033	0.124
4		0.022	0.108
5		0.005	0.011
6		0.004	0.009

Considering all beam background effects, the maximum achievable data rates are 335 Mbps/cm^2 in Higgs mode and 2823 Mbps/cm^2 in *Z*mode, with corresponding average rates of 261 Mbps/cm^2 and 1358 Mbps/cm^2 respectively. The system demonstrates excellent compatibility with the current vertex detector design, particularly given the low occupancy of 2.331×10^{-5}/BX in Higgs mode and 2.026×10^{-5}/BX in *Z*mode. These favorable occupancy levels ensure efficient data handling within the existing scheme.

4.2 Sensors and electronics design

4.2.1 Sensor technology overview

The current design and development of the CEPC vertex detector are centered on utilizing state-of-the-art MAPS technology for chip design and manufacturing. This technology integrates the sensor and readout electronics onto a single chip, significantly reducing both pixel size and power consumption while delivering high-performance detection capabilities. Such features meet the stringent requirements for high resolution, low material budget, and rapid readout speeds.

The Solenoidal Tracker at RHIC (STAR) experiment at Relativistic Heavy Ion Collider (RHIC) (Relativistic Heavy Ion Collider) successfully employs MAPS technology in its vertex detector [1], and the STAR MAPS vertex detector features excellent spatial resolution [1, 2]. The Inner Tracker System (ITS)2 of CERN's ALICE experiment is the largest scale MAPS system among high energy physics experiments [3]. ITS2 is a full-pixel silicon detector based on TowerJazz 180 nm technology. It boasts exceptional technical parameters, including approximately 5 μm high resolution, an extremely low

material budget of less than 0.3 % X_0 per layer, stable readout support for collision frequencies up to 100 kHz, and power consumption as low as 40 mW·cm^{-2} [3, 4]. The upcoming ITS3 upgrade for the ALICE experiment introduces the concept of "curved wafer-level chips", aiming to achieve a self-supporting wafer structure [5, 6]. This development is based on TowerJazz Tower Partners Semiconductor Co. (TPSCo) 65 nm technology. This innovation could potentially reduce the material budget of the vertex detector by a factor of 3 to 5. The ITS3 project is currently in the research and development phase. The comparison of key parameters between different vertex detectors mentioned above is shown as Teble 4.6.

Table 4.6: Comparison of sensor technology in vertex detectors of different experiments: ALICE ITS2, ALICE ITS3, the first CEPC vertex detector prototype, and final CEPC vertex detector.

Detector	Technology Node	Power Consumption	Readout Speed	Spatial Resolution
ALICE ITS2 [3, 4]	180 nm	40mW/cm^2	Up to 100 kHz	5 µm
ALICE ITS3 [5]	65 nm	40mW/cm^2	164 kHz	5 µm
1st CEPC Vertex prototype [7–9]	180 nm	80 ~ 100mW/cm^2	40 MHz	5 µm
Final CEPC Vertex Detector	65 nm	≤ 40mW/cm^2	Up to 43 MHz	3-5 µm

4.2.2 Stitched sensor prototype design

The stitching technology enables the production of chips significantly larger than the dimensions of the design reticle. The design reticle is divided into sub-frames that align with the sub-frames of the photomasks. By selectively exposing these reticle sub-frames onto adjacent locations following the designed pattern, manufacturers can create large chips with dimensions nearing the wafer's diameter. This innovative approach expands the possibilities for chip design and production, allowing for more efficient utilization of wafer space. This technology is particularly advantageous for pixel sensor chips that feature a high number of repeated units (pixel matrices) and demand a large active area. Taking into account the difficulty and yield of stitching technology, the baseline design of the stitched sensor prototype involves using 1D stitching to achieve stitched-chip along the beam pipe direction. The feasibility of 2D stitching will also be continuously explored during research and development.

4.2.2.1 Sensor architecture and functional blocks

The idea of using a stitched sensor chip to construct half of the detector layer is inspired by the design of the ALICE ITS3[5][6] sensor. Thanks to the promising results obtained in the MOnolithic Stitched Sensor (MOSS) and MOnolithic Stitched sensor with Timing (MOST) prototypes for the ALICE ITS3 project, this consideration benefits from the scheme of the MOSS and MOST prototype. Detailed R&D on the stitching floor

plan for the vertex detector is under assessment at the time of writing. The preliminary stitching plan of the silicon wafer and the dimensions of each half layer are introduced in Figure 4.3.

Figure 4.9 illustrates the floor-plan of one RSU. One RSU is divided into several identical Sensor Block. Each sensor block is fully independent from the others with its own biasing generator, slow control and periphery readout circuit, shown in Figure 4.10. The sensor block has local power switches located at the right side of the sensor block that can be selectively switched on by the user control. This powering granularity reduces the sensitivity of the stitched sensor to possible manufacturing faults. In the case of a supply short in one of the sensor blocks, it allows to switch off the faulty sensor block and maintain the others functioning normally. Considering the sensitive area of a sensor block will introduce an extra dead area in the event of switching off, the dimension of the pixel matrix in a sensor block should be choose carefully. The scale of a sensor block will be optimized in the future design for a trade-off between the power granularity and the data transmission performance. In the preliminary design at the time of writing, one RSU contains 12 identical sensor blocks and 4 stitched interface blocks arranged in two rows. Each sensor block has a single output for data readout at 86.66 Mbps. Data of each sensor block has to be transmitted to the LEB through the one-to-one direct connection between the sensor block and the LEB. As the longest transmission distance reaches more than 20 cm for the rightmost sensor block of the module, the regeneration of the signal periodically over the link is necessary. This function is proposed to be implemented in the stitched data interface blocks. The stitched data interface block transmits control signals and data from/to the LEB. Table 4.7 provides plan of the dimensions of the LEB, REB and the main functional blocks that make up the Repeated Sensor Unit. Some values are derived from the experience gained from the design of TaichuPix prototypes. Table 4.7 provides the dimensions of individual functional blocks. As the RSU is divided into multiple sections internally, different functional blocks are repeated multiple times. An RSU contains 12 Pixel Matrices, Biasing Blocks, Power Switches Blocks, and Matrix Readout Blocks, and 4 Stitched Data interface Blocks.

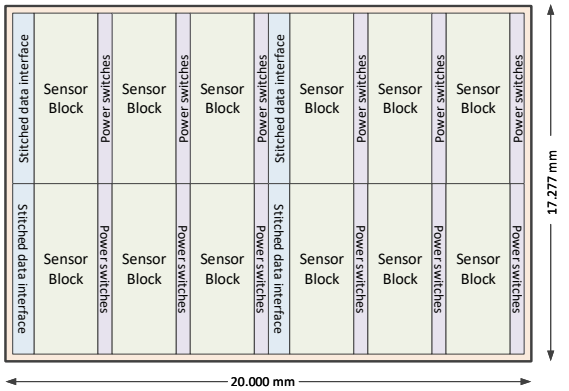


Figure 4.9: Proposed floor-plan for a RSU (not to scale). It contains several identical sensor blocks. Each of them has a pixel matrix with its own biasing generator, slow control and periphery readout circuit. Each sensor block can be selectively switched on/off. The stitched data interface blocks are used to transmit control signals and data to the edge of the stitching sensor.

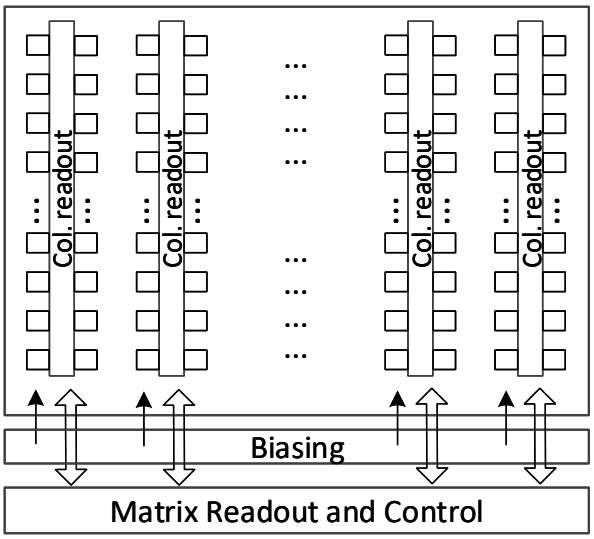


Figure 4.10: Architecture of the sensor block. It consists of a pixel matrix, a biasing generator block and a periphery readout and control.

Table 4.7: Plan of dimensions of the LEB, the REB, and the main functional blocks of one RSU.

	Pixel Matrix	**Biasing Block**	**Power Switches**	**Matrix readout**	**Stitched interface**	**RSU**	**LEB**	**REB**
Height [mm]	8.409	0.053	8.409	0.177	8.409	17.277	17.277	17.277
Width [mm]	3.296	3.333	0.019	3.333	0.055	20.000	4.154	1.385

4.2.2.2 Design of the repeated sensor unit

Each pixel cell integrates a sensing diode, a front-end amplifier, a discriminator and a digital pixel readout. The in-pixel digital readout benefited from the TaichuPix prototype. Each pixel contains a hit storage register and logic for pixel mask and test pulse configuration. A common threshold level is applied to all the discriminators of the pixels. Every pixel can be tested and calibrated individually, combining charge injection scans and threshold scans.

I. Sensing diode As depicted in Figure 4.11, the collection N-well electrode has an octagonal shape fabricated on a P-type epitaxial layer. The collection electrode is surrounded by the P-guard ring. The space between the collecting N-well and the surrounding P-well is introduced to increase the depletion region and thus enhance the charge collection efficiency. Footprint represents the total area defined by the surrounding P-well. The design of the sensing diode geometry is a compromise among the charge collection performance (i.e. charge collection efficiency and time, radiation tolerance), area, and sensor capacitance. As mentioned in Section 4.5.1, the optimization of sensor performance was previously addressed in the 180 nm TowerJazz CMOS technology. These studies offer valuable insights for enhancing sensor performance in the 65 nm TowerJazz CMOS technology. To further optimize the sensor geometry to align with the 65 nm CMOS process, pixel test structures are proposed to be designed in the initial phase of the stitched sensor R&D. Various sensor variants in the test structures encompass different electrode diameters, spacing between electrode and surrounding PWELL, PWELL shapes, and the method of applying reverse bias to the sensor diode.

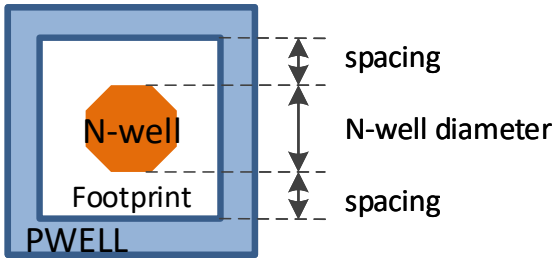
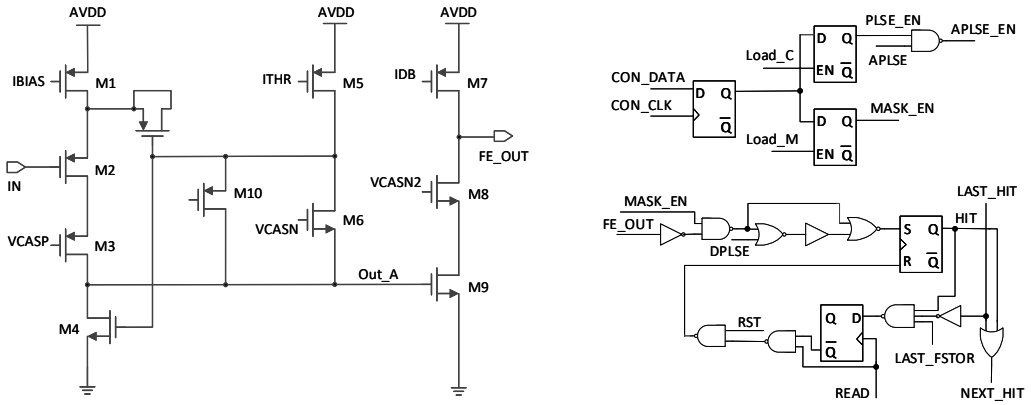


Figure 4.11: Geometry of the sensing diode. It consists of the collecting N-well and the surrounding P-well.

II. Pixel Front-end The simplified schematic of the analogue front-end is shown in Figure 4.12a, which had been verified in the TaichuPix prototype (see Section 4.5.2). The topology of the circuit was derived from the ALICE Pixel Detector (ALPIDE) sensor chip used in the ALICE ITS2 [4]. The analog front-end and the discriminator are continuously active. The current consumption is mainly determined by the bias current (IBIAS) of the first branch , adjustable by one of the local Digital-to-Analog Converter (DAC)s in the

periphery of the pixel array. Targeting the power requirement of 40 mW/cm^2, the value of IBIAS is reduced compared to the one in the TaichuPix design. The choice of the IBIAS value is a trade-off between the power consumption and the speed. By design, the nominal power consumption values of the new front-end in TPSCo 65 nm process are 68.4 nW. The nominal value corresponds to analogue power densities of 26.7 mW/cm^2 for the pixel pitch of 16 µm and 10.9 mW/cm^2 for the pixel pitch of 25 µm.

III. In-pixel digital logic The in-pixel digital electronics inherit the TaichuPix design. Figure 4.12b presents the diagram of the in-pixel logic. It features a hit latch set by a negative pulse from the output of the front-end. The pixel readout follows a double-column drain arrangement. The region for in-pixel digital readout logic is shared by two columns to minimize the crosstalk between analog signals and digital buses. Additionally, it saves space for the routing of the address encoder. The priority logic arbitrates the pixel readout, with the topmost pixel having the highest readout priority. The in-pixel logic also integrates configuration registers for calibrating the pixel front-end, for testing in-pixel readout logic, and for masking the faulty pixel. The configuration function is programmable through the setting of control bits, including MASK_EN, PULSE_EN, DPULSE and APULSE (as shown in Figure 4.12b).



(a) Schematic of the in-pixel front-end.

(b) Diagram of the in-pixel digital logic.

Figure 4.12: Schematic and block diagram of the in-pixel circuits.

IV. Peripheral readout circuits on sensor The main function of the on-chip peripheral readout circuits includes: sending the control signals required by the pixel array and receiving the data from the pixel array; buffering the data to smooth the output data rate; providing a slow control interface for chip configurations and tests.

The data from the pixel array are organized in Double Columns (Dcols). In order to achieve a detection efficiency above 99 %, all double columns of pixel array are read out in parallel. A timestamp is recorded at the end of the double column for the future data

processing. Without a trigger signal, all the readout data are buffered and output. A data compression mode is optional, which, in our estimation, will reduce the output data rate by half.

The peripheral readout circuit's core function is to send control signals to the pixel array and receive data from it. A data-driven schema is preferred. The read signal is only sent when the pixel is triggered. To read the signals sequentially, a priority mechanism must be implemented. The most popular method is address priority. A hit signal is generated when the collected signal exceeds a threshold and is reset after the pixel address is read out.

Based on this approach, the pixel array's clock is inactive in the absence of a hit. This approach effectively minimizes power consumption. To optimize control timing, a hierarchical priority control chain can be implemented.

To accommodate higher data rates, a real-time data compression strategy can be implemented before sending data to First In First Out (FIFO)s.

The address of the first pixel in a package is recorded, while the next three pixels are encoded using a three-bit code, where '0' represents no hit and '1' represents a hit. Operating at a system clock of 40 MHz, the data compression circuits incur no additional timing overhead. By enabling the data compression function, the data volume is reduced, and the readout speed is increased.

The fast chip-level readout is closely related to FIFO accesses. We propose a shareable architecture [10]. The shared FIFO features flexible capacities to handle random hit bursts. As a result, higher hit flux can be accommodated even with a reduced total memory volume.

The power consumption is evaluated based on TaichuPix, which is implemented using a 180 nm process for average hit rates of 1 MPixels/s·cm^2, 15 MPixels/s·cm^2, and 40 MPixels/s·cm^2. The future design of the RSU will use a 65 nm process. The power supply will be reduced from 1.8 V to 1.2 V. The area of the peripheral readout circuits is estimated to be reduced by 50 %. The dynamic power consumption due to clock and data upsets is estimated with a reduction of 4.5 times. However, the static leakage currents will increase significantly. To meet the power density of 40 mW/cm^2, the power consumption of peripheral circuits in RSU is estimated to be 40 mW, the leakage current should be controlled in 5 times of TaichuPix. Power switches will be implemented to meet these requirements. Finally, the power consumption of the future design is estimated as 29 mW and 37.5 mW for 8 MPixels/s·cm^2 (Higgs mode) and 44 MPixels/s·cm^2 (Z mode), respectively.

Considering the application and tests, the sensor chip will provide proper register control and on-chip test mode.

The sensor chip includes control and status registers, which can be categorized into several types:

a. Read-only registers store internal status and can be read via the Inter-Integrated

Circuit (I2C) interface or output from IO through a multiplexer.

b. Internal control and configuration registers enable the selection of work modes, clock frequencies, DAC settings, and more.

c. Special configuration registers manage the pixel array, including mask and calibration registers.

d. Additional registers are dedicated to on-chip test configuration.

The On-Chip Test (OCT) module is planned to generate input signals for peripheral readout circuits, enabling chip debug and data alignment. Waveforms can be customized based on register settings. In chip debug mode, a test output port supports data transmission via the I^2C interface.

The OCT and test output port operate independently.

4.2.2.3 Design of the left-end block

All data from the RSUs per module (see Figure 4.14) are collected and processed by the LEB on the left side of a module. The block diagram in Figure 4.13 illustrates the main functions of the LEB. The data of the RSUs are transmitted to the LEB through a large array of differential point-to-point on-chip serial data links operating at 86.66 Mbps. As mentioned in Section 4.1.2, the individual module of different layers in the detector contains a varying number of RSUs. Among them, the single module in Layer 4 has the highest number of RSUs, which is 10. Since each RSU has 12 data links, the LEB needs to receive a maximum of 120 data links. A group of 128 receivers primarily compensates for phase differences in the incoming data streams from the RSUs and resamples them using the local fast clock. The data encoding blocks gather and encode the data with redundancy to correct errors during off-chip transmission. After encoding, the data is serialized at a speed of 1.39 Gbps and transmitted off-chip using 8 serializers. The Clock Block provides the required clocks for the LEB and RSUs. The functionalities of LEB also include providing slow control and power switches control signals for RSUs.

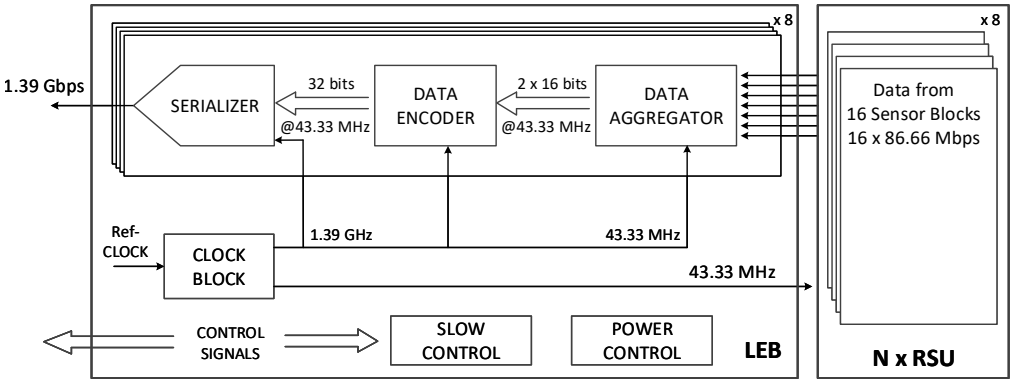


Figure 4.13: Proposed diagram of the LEB. All data from RSUs of one module has to be transmitted to the LEB. 'N × RSU' labeled in the right part of the diagram represents that different layers in the detector contain a varying number of RSUs.

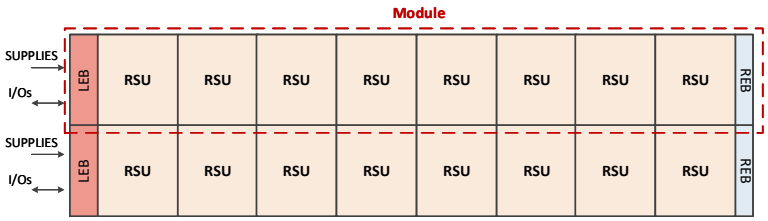


Figure 4.14: Top level floor-plan for a sensor of layer1 (not to scale). It contains two identical modules, with one of them indicated by the dotted red rectangle.

4.2.2.4 Power consumption estimates

As illustrated in Figure 4.9 and 4.10, each RSU consists of pixel matrix, biasing blocks, matrix readouts, and data interface blocks. Table 4.8 provides the expected power consumption of the main functional blocks of the RSU and the total power consumption of a single RSU. In Table 4.8, the entries for the pixel matrix include the power of the pixel analogue circuit and the pixel digital logic. In the current calculations, it is assumed that the pixel size is 25×25 μm^2, which is consistent with the intrinsic position resolution value used in Section 4.1.2. The power of the pixel analogue is calculated by the power density of the pixel front-end (shown in Section 4.2.2.2) and the total area of 12 pixel matrices (dimension of the pixel matrix is shown in Table 4.7). The power consumption of the pixel digital in the table includes the dynamic power of the in-pixel digital logic and the double-column address encoding logic (described in Section 4.2.2.2), as well as power consumption due to the leakage current. The dynamic power consumption of the pixel digital circuit mainly depends on the pixel hit rate. Based on estimations of the hit rate in the vertex detector and testing experience with the TaichuPix prototype, the dynamic power consumption of the pixel digital circuit is relatively small. In contrast, considering the planned use of 65 nm CMOS process, the contribution of leakage current from transistor gate leakage to power consumption is much greater than the dynamic power of the digital circuit. The contribution of the Biasing Blocks is estimated based on the experience of the design in the TaichuPix. The entry for the Matrix readout blocks is described in Section 4.2.2.2. The value for the data interface blocks is obtained from the very preliminary considerations on the transmitting power of the control signals and the readout data of RSUs. Table 4.9 lists the power consumption estimates for the main functional blocks of the LEB (see Figure 4.13).

Table 4.8: Estimates of power consumption of one repeated sensor unit (RSU). All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	Pixelanalogue	Pixeldigital	Biasingblock	Matrixreadout	Datainterface	RSUTotal
Power [mW]	36	30	8	40	17	131

Table 4.9: Estimates of power consumption of the LEB. All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	ClockBlock	DataAggregator	DataEncoder	Serializer	Slow & Powercontrol	LEBTotal
Power [mW]	36	120	80	32	80	348

Combining the power estimates of Table 4.8 and 4.9 with the surface areas of the major blocks found in Table 4.7, one obtains the estimates for the power dissipation densities. The results are given in Table 4.10.

Table 4.10: Estimates of average power dissipation per unit area over the main blocks composing the stitched chip

Components	Power density [mW/cm^2]
Repeated Sensor Unit	38
Left-End Block	485

4.2.3 Backend electronics and cables

In the vertex detector design, flexible printed circuit boards (flex Printed Circuit Board (PCB)s) are integral to the backend electronics system. These flex PCBs serve as conduits for transmitting signals, clocks, control commands, power, and ground connections between the control boards and the detector modules. By providing a lightweight and adaptable interconnection, flex PCBs facilitate efficient data communication and power distribution while minimizing material usage, which is crucial for maintaining the detector's performance and reducing multiple scattering effects.

4.3 Mechanics, cooling and services

This section describes the mechanical design of the VTX, including the support structure and related finite element analysis, detector air cooling and the general scheme of services.

4.3.1 Mechanics

4.3.1.1 General support structure

The baseline design of the vertex detector consists of, from outer radius to inner radius, a single-layer double-sided ladder-based barrel followed by four concentric cylinders constructed with stitching technology-based bent MAPS (Monolithic Active Pixel Sensor).

The innermost cylinder has a radius of 11 mm, and maintains a 0.3 mm gap from the beam pipe. As shown in Figure 4.1, the side view along the beam direction, this figure demonstrates the general structure of the detector and its integrated mechanical support. To be consistent with the physics requirements and goals, the general mechanical support design for the Vertex detector aims to use ultra-light materials to create a rigid enough structure, realizing a low material budget without weakening the spatial resolution.

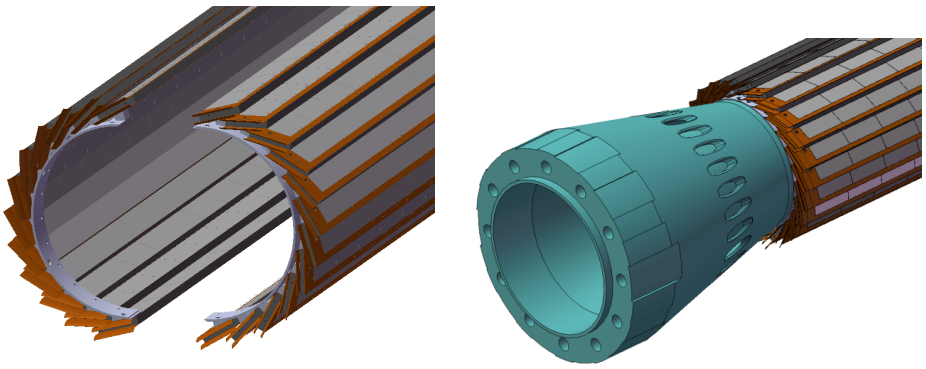
4.3.1.2 Ladder and support

The double-sided ladder is the structural unit of the layer 5 and 6 . It features pixel sensors on both sides of the ladder support, while sensors are glued onto the FPC, which is also glued onto the ladder support. The CFRP is used to make the ladder support due to its low density and high specific modulus and strength. The main body of the ladder support [11] is a hollow shell structure [11] with an overall size of $682 \times 3.2 \times 17.5$ mm^3 . With the assistance of the finite element static analysis, the laminated shell of the ladder support is made of ultra-thin CFRP plies, using the high modulus CFRP at a level equivalent to M40, the CFRP laminate of the shell is made with a thickness of 0.15 mm, to get a conservative estimation by just putting the mass of the sensors and FPC to the bare ladder support (without taking into account their contribution to the rigidity of the complete ladder), it is anticipated that the ladder support deforms very slightly and at a negligible level. According to previous evaluations, about 20 % smaller deformation will be induced for the complete ladder [11].

4.3.1.3 Ladder-based barrel and fixation to the beam pipe (assembly)

The vertex detector is the first detector outside the beam pipe, and structurally it will be integrated into the beam pipe assembly. The outer most layer of the vertex detector, the ladder-based barrel, does not directly mount on the beam pipe; it rests and is secured to the intermediate conical parts that are mounted to the beam pipe, providing support for the vertex structure. The four layers of bent MAPS cylinders are mainly fixed to the extended section of the beam pipe.

The barrel-shaped outer layer detector formed by the double-sided ladders which overlap with each other in the circumferential direction to form a continuous sensitive layer. To facilitate barrel assembling and its installation on the beam pipe integration, the barrel structure is designed as Figure 4.15 shows , it is assembled by two half-barrels, each half-barrel consisting of two half side-rings located at both ends along with several ladders. The ladders are positioned and secured to the side-rings by the surfaces of the tooth-shaped structure of the side-rings. After the two independent half-barrels are pre-assembled on dedicated tooling, they are installed and fixed onto the intermediate conical part of the beam pipe assembly , as illustrated by Figure 4.15 .



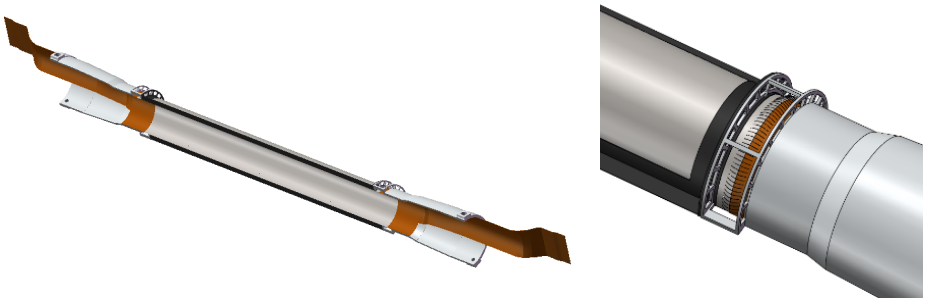
(a) (b)

Figure 4.15: (a) The barrel assembly. (b) The barrel on beam pipe assembly (the outer tube of the beam pipe assembly is not shown)

Structurally, the ladder-based barrel design is consistent with our previous prototyped vertex design. Furthermore, much R&D work involving structural validation tests were conducted during the previous prototype development phase, these experiences can be helpful to optimize the TDR design.

4.3.1.4 Bent MAPS cylinders and fixation to beam pipe

There are four layers of bent MAPS cylinders with different radii and lengths consistent with the physical layout of the vertex detector. Each of the four bent MAPS cylinders is a single detector layer that consists of two half cylinders, as shown in Figure 4.16. To maintain the bent MAPS in the shape of the cylinders, ultra-light local supports made of CFRP have been designed for each layer. Integrated with the electronic readout, the FPC is connected to the curved edge of the bent MAPS on its lateral side by wire bonding . To keep the connecting joint safe and also for protecting the wire bonds, extended support has been designed for each cylinder, as shown in Figure 4.16, it prevents the FPC from deforming very close to the joint area, thereby avoiding damage to the connection. The bent MAPSs, the local support and the extended support form the cylinder assembly. Each cylinder assembly is independent and has no contact with the adjacent layers of cylinder assemblies, also will be mounted onto the beam pipe assembly separately . This kind of design focuses primarily on realizing and facilitating a feasible process for both assembly and wire bonding, as well as installation onto the beam pipe. The results of the finite element simulation analysis indicate that, under constrained conditions at both ends, this structure has very minimal deformation, and the stress on the bent chips is also very low, both of which are negligible, taking the innermost layer bent MAPS cylinder assembly as an example. In addition, some R&D studies of making the bent MAPS have been done; so far, the dummy wafer with a thickness of 40 µm and a radius of 12 mm has been tested and proven to be feasible, refer to Section 4.5.2.3.



(a) (b)

Figure 4.16: The half cylinder assembly (bent MAPS with FPC and the extended support) of the innermost layer. (a) An overview of the half cylinder of bent MAPS detector layer, and the yellow part is FPC. (b) An extended support to prevent the FPC from deforming too close to the joint area.

4.3.2 Cooling

The heat generation of the Vertex detector for both the ladder-based barrel and the bent MAPS cylinders is estimated to be at the same level of 40 mW/cm^2. The operational temperature for the detector is required to be no higher than 30 °C. Thus, cooling is essential for maintaining optimal sensor performance. Generally, electronic equipment with heat generation up to 0.3 W/cm^2 can be cooled using forced air convection. Given the stringent material budget requirements for the vertex detector, compressed air cooling has been selected as the cooling method.

To evaluate the cooling performance of the current structural design of the vertex detector , air cooling simulation analysis was conducted. The simulation results indicated that at an average flow rate of 3.5 m/s, the maximum temperature of the outer ladder is within the required range, as shown in Table 4.11. For the bent MAPS cylinders, the innermost layer is very close to the beam pipe and has no airflow, making it the most challenging layer to cool within the entire detector. The simulation results indicate that at an airflow rate of 3.5 m/s (which satisfies the ladder cooling), with the central beam pipe surface temperature considered, the innermost layer of the bent MAPS cylinder can be cooled to a sufficiently low temperature, as shown in Figure 4.17, thereby meeting the experimental requirements. Additionally, simulations were performed to compare the maximum temperature of the innermost layer at different wind speeds. Based on these simulation results, it can be anticipated that air cooling will meet the current cooling needs of the detector.

Table 4.11: Simulation results of the barrel-maximum temperature on the ladder. Inlet air temperature of 5 °C; air speed of 3.5 m/s.

Power dissipation	Total heat generation of the barrel	Max temperature on ladder
40 mW/cm^2	190 W	29.4 °C

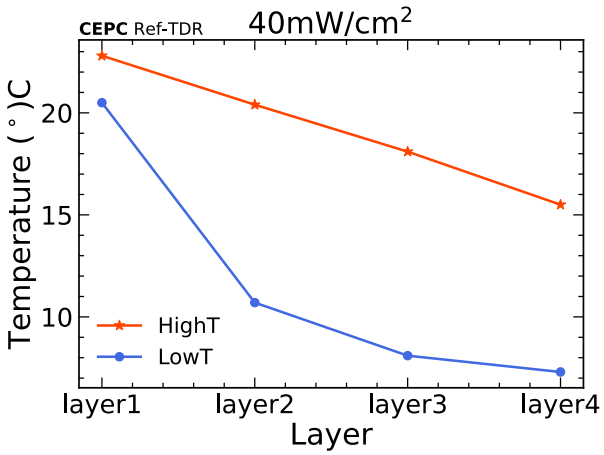


Figure 4.17: Simulation results for the cooling of bent MAPS cylinders, with an airflow rate of 3.5 m/s. The beam pipe surface temperature, as shown in Chapter 3, is taken into account.

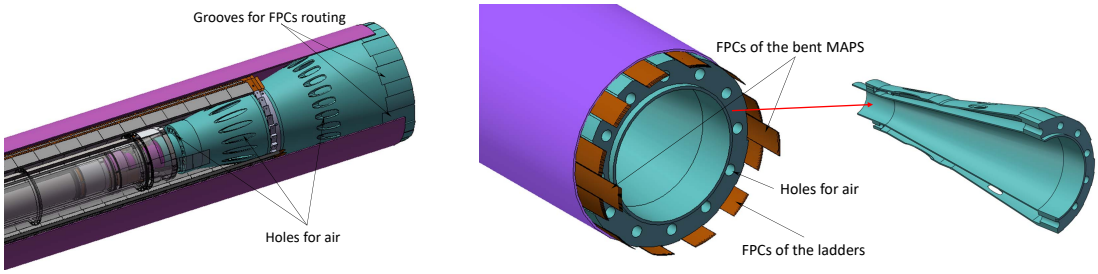
4.3.3 Services

This section introduces the needs and considerations of the general services for the Vertex detector. The vertex uses air cooling; the main service requirement is to ensure proper airflow and good ventilation for the entire detector zone. The vertex detector will be mounted onto and integrated into the beam pipe assembly; the other service requirement is to route all the cables of the VTX out of the very space-limited beam pipe assembly.

Since the VTX consists of a single barrel layer and four concentric cylinder layers, ventilation for each gap between the adjacent layers must be ensured for effective cooling. The mechanical design for the vertex detector fully considered this requirement and also tried to minimize the effect caused by FPCs blocking, which is obviously reflected in the hollow support structures designed for the detector, especially the support of the bent MAPS cylinders. The conical part that is integrated into the beam pipe assembly to support the barrel layer mentioned before also works as the general air distributor for the entire vertex detector. It is a hollow structure; air will be blown into the inside hollow space from the side of the part then distributed to the detector zone through those ventilation holes facing different zones of the detector on the outer surface, as shown in Figure 4.18.

The space for the entire VTX outside the beam pipe is very compact. Together with the beam pipe assembly, for the vertex detector, on both ends of the barrel and the bent

MAPS cylinders, the FPCs of the ladders and the bent MAPS are the only cables that need to be routed out . The FPCs of the bent MAPS cylinders will be routed along their extended support and converged after the end of the outermost layer, and then they are stacked and go through the intermediate conical part via the grooves. The FPCs of the ladders of layer 5 and 6 will be streamlined by converging the FPCs of two adjacent ladders into one conduit, similar to the FPCs of the bent MAPS, then go through the conical part via their specified grooves, as illustrated in Figure 4.18, which effectively halves the spatial occupancy and preventing the circumferential accumulation of FPCs from fully cover the outer surface of the conical part. After all the FPCs are routed outside the beam pipe assembly, they will be transferred to optical fibers via connectors, as described in Section 4.2. Additionally, a half-dummy model of the vertex structure, incorporating the bent MAPS cylinders and two short ladders, was constructed to test the FPC routing . The trial results demonstrated that the routing scheme is fundamentally feasible.



(a) **(b)**

Figure 4.18: Air ventilation and cable routing of the VTX. (a)Air channel design with holes on global support structure for air distribution. Grooves on support structure is designed for FPCs routing. (b) the FPCs of the vertex detector routed out of the side of the beam pipe assembly, along with a cut view of the conical part.

4.4 Alignment and calibration

The vertex detector is designed to precisely measure the trajectory parameters of charged particles close to the interaction point, enabling accurate reconstruction of decay vertices from short-lived particles. Effective alignment is crucial for achieving optimal resolution in the vertex detector.

The alignment strategy for the vertex detector faces significant challenges due to the implementation of bent wafer-scale monolithic pixel sensors. The primary goals of this strategy include achieving high spatial resolution, reducing uncertainties in impact parameters, and ensuring stable alignment through efficient and automated processes.

4.4.1 Initial mechanical alignment and reference alignment system

Initial mechanical alignment will be conducted during detector assembly, utilizing precision optical survey instruments. Sensors will be aligned within a few micrometers of design specifications, and optical method will confirm sensor curvature and cylindrical positioning. Fiducial markers placed strategically on sensor modules and supporting structures will facilitate optical tracking and ensure precise referencing. A stable external alignment system, regularly monitored through X-ray or laser-based and optical survey methods [12], will serve as the reference for continuous alignment.

4.4.2 Track-based alignment

Mechanical alignment procedures during installation provide an initial level of precision in the vertex detector position. This precision is typically significantly worse than the desired design hit resolution. Additional alignment (tracker-based alignment) is needed to account for the position, orientation, and surface deformations of the MAPS sensors. Charged particle tracks obtained from collision data will facilitate iterative alignment corrections during both the commissioning and operational phases. Global and local χ^2 minimization algorithms will refine sensor positioning, enhancing accuracy and ensuring optimal detector performance.

In the current detector design, simulations have demonstrated the ideal performance of the detector; however, in practical applications, it is necessary to consider the typical deformation mode as shown in Figure 4.19. The deformation includes elliptical deformation; irregular, wavy distortion; circular distortion with uniform radial expansion.

These deformation modes can affect the detector's ability to determine the relative positions of collision products as they pass through the vertex detector, ultimately impacting the accuracy of the reconstructed collision parameters d_0 and z_0. The effect of each of these deformations was studied in the simulation by modifying the position of the hits according to the three types of deformation. In particular, for each simulated charged-particle trajectory, the intersection with the deformed geometry was computed to determine the corresponding position of the hit in the local detector coordinates. The track-reconstruction algorithm was then executed assuming an ideal geometry to quantify the effect of the detector deformations in the absence of a detector alignment procedure.

4.4.3 Real-time monitoring

A laser-based online alignment monitoring system will perform real-time checks, verifying alignment accuracy continuously.

Due to the air cooling design in the vertex detector, it is important to monitor the movement of the MAPS sensors. Inspired by the laser alignment system of CMS

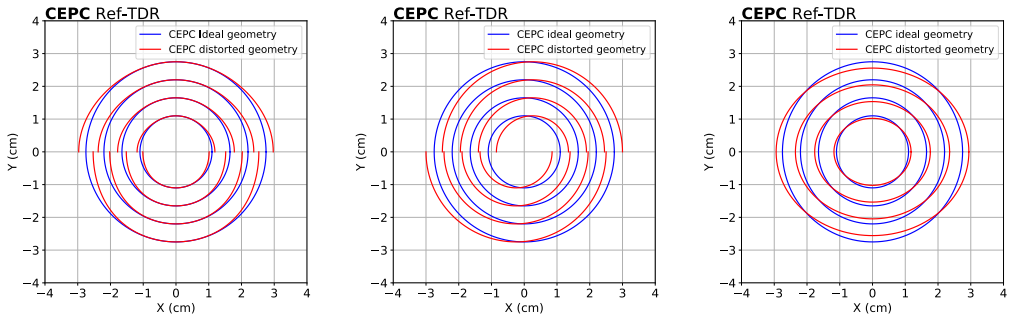


Figure 4.19: Illustration of the hit positions in the transverse plane with ideal vertex geometry and three deformed geometry. The amount of deformation is amplified with respect to the expected one for visualisation. Left Figure: elliptical deformation. The red distorted geometry is elongated horizontally, demonstrating a deformation primarily along the x-axis. Middle Figure: Illustration of the hit positions in the transverse plane for vertex geometry exhibiting irregular, wavy distortion. The distorted geometry has noticeable undulations, indicating non-uniform deformation affecting both the x and y directions unevenly. Right Figure: Illustration of the hit positions in the transverse plane for vertex geometry showing a circular distortion with uniform radial expansion. The distorted geometry presents a uniformly increased radius, representing an isotropic deformation compared to the ideal geometry.

experiment [12], it is proposed to install laser alignment system to keep track of these movement. In Figure 4.20, a laser source placed on the right side of the 4th layer of chips is used to monitor the movement of the first layer of MAPS; laser sources are placed on the service portions on both sides to monitor the movement of the 3rd, 2nd and 1st layer of MAPS. This system utilizes near-infrared laser beams (1050 nm) directed through the vertex detector to detect potential movements or deformations of the mechanical structure. Laser sources located in service areas are triggered to send pulsed infrared light to MAPS sensors of the vertex detector. By detecting their interaction with the silicon sensors, the system can infer movements of the MAPS sensors, ensuring that any deformations due to environmental factors like temperature, air flow, or magnetic fields are promptly identified.

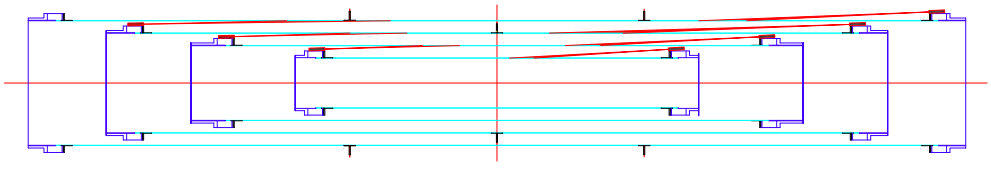


Figure 4.20: A laser-based online alignment monitoring system. Red lines diagonally connect with the aqua blue line (MAPS chip) are the lasers, and the laser sources are placed at both sides of the inner three layers and right side of the 4th layer to monitor the movement of each layer.

To validate the laser calibration system, signals generated by the laser were simulated using Geant4 [13] within the CEPCSW framework. The laser was emitted as a point

source from the position (13 mm, 0, -85 mm), directed at an angle of $\theta = 10^\circ$ and $\phi = 0$. In the absence of a focusing system, a divergence of $\tan\alpha = 0.1$ was established.

The resulting laser beam spot on the second layer of the vertex detector is presented in Figure 4.21.

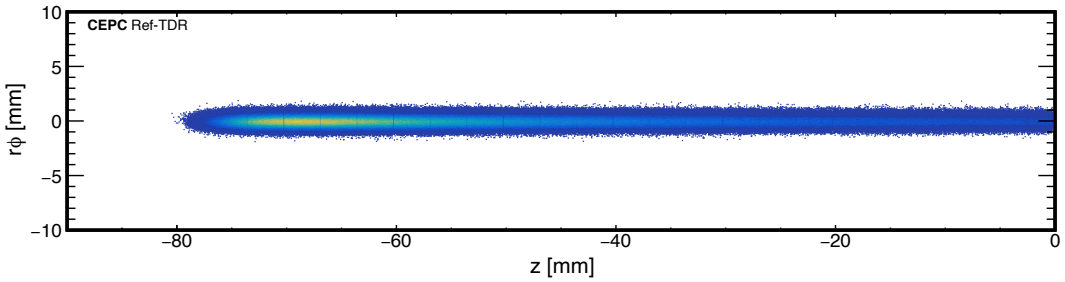


Figure 4.21: The laser beam spot on the second layer from (13 mm, 0, -85 mm) in cylindrical coordinate system, where the horizontal axis is the z-coordinate, and the vertical axis is the $r\phi$ coordinate. And each region is divided by a blank or lower rate than its neighbor means one sensor.

When simulating deformation by radially displacing the second layer outward by $d = 10\mu$m, the resulting distribution of signal IDs, The observed difference of 2 corresponds to a distance of 50μm, which is consistent with relationship $d/\tan\theta \approx 57\mu$m. If an accurate fitting function can be employed to characterize this distribution and precisely determine the most probable position, it would enable more accurate detection of displacement. These findings indicate that the laser calibration system can infer positional changes through the distribution of pixel IDs.

4.5 R&D efforts and results

To meet the stringent requirements of high spatial resolution, low material budget, rapid readout speeds, and low power consumption, significant efforts have been directed toward advancing MAPS technologies, notably through the TaichuPix and JadePix projects.

The JadePix project focuses on investigating CMOS pixel sensors for the CEPC vertex detector, exploring low-power readout schemes. Concurrently, the TaichuPix series is dedicated to developing MAPS featuring advanced in-pixel electronics optimized for rapid readout. These sensors utilize a data-driven, column-drain architecture specifically designed to meet the fast response requirements imposed by the high collision rates at CEPC.

4.5.1 CMOS pixel sensor JadePix series

The CEPC vertex detector imposes stringent requirements on spatial resolution. To achieve a spatial resolution of 3 μm, the pixel size needs to be reduced to less than 20

μm, which is limited by the feature size of integrated circuit technology. JadePix utilizes a specialized 180 nm CMOS integrated circuit process optimized for ionizing radiation detection, which is a modification and development based on the commercial CMOS Imaging Sensor process. The pixel pitch in this process typically ranges from 25 to 30 μm. Therefore, the key focus of JadePix's development is on how to reduce the pixel size while also meeting the requirements for low power consumption and fast time stamping.

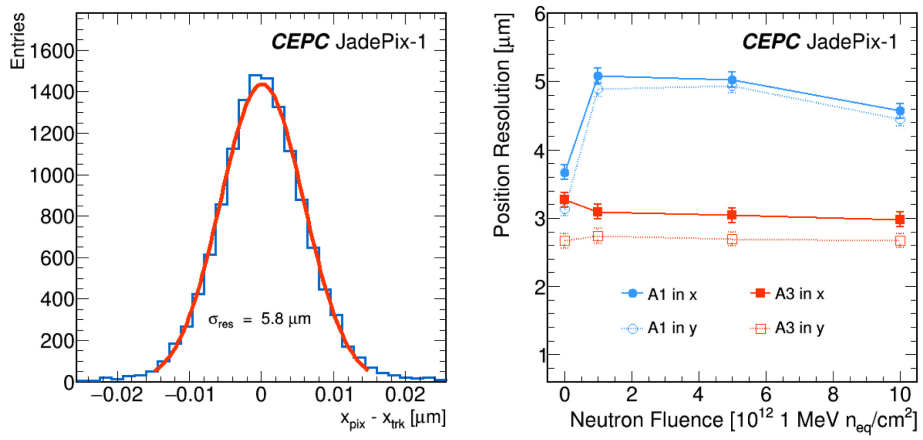
4.5.1.1 Overview of JadePix development

The JadePix series of chips are primarily designed and optimized for high spatial resolution, low power consumption, and fast time stamping. Since 2015, a total of 5 chips have undergone continuous improvements which are shown as Table 4.12.

Table 4.12: Overview of JadePix development

Chip Name	**Pixel Array**	**Pixel Pitch**(μm^2)	**Analog Front-end**	**Matrix Readout**	**Design Team**
JadePix-1	128×192, 160×96	16×16, 33×33	Source follower	Rolling Shutter	IHEP
JadePix-2	96×112	22×22	Diff. Amp., CS Amp.	Rolling Shutter	IHEP
JadePix-3	512×192	16×23, 16×26	ALPIDE	Rolling Shutter	IHEP, CCNU, SDU, DLNU
JadePix-4	356×489	20×29	ALPIDE	AERD	CCNU, IHEP
JadePix-5	896×480	20×30	ALPIDE	AERD	IHEP, CCNU

JadePix-1[14] primarily focused on sensor optimization, comparing different geometric dimensions [15] and providing experimental evidence for the design of small charge collection electrodes [16]. As Figure 4.22 shows, the optimal spatial resolution obtained through beam tests on a $33 \times 33 \mu m^2$ pixel array was 2.7μm [17].



(a) (b)

Figure 4.22: (a) Residual distribution of JadePix-1 sensor in the x direction; (b) position resolution for sensors with a small electrode (A1) and a large electrode (A3) before and after the neutron irradiation.

JadePix-2 investigated AC coupling and different analog front-end amplifiers [18], attempting to optimize resolution, power consumption, and time stamping design using a 180 nm process based on the Minimum Ionising MOS Active pixel sensor (MIMOSA) architecture.

JadePix-3 utilized the low-power front-end amplifier of ALPIDE[4], combined with a Rolling Shutter readout architecture, achieving the smallest pixel design among similar chips at $16\times23\mu m^2$. Infrared laser tests showed spatial resolutions of 3.4 μm (X-direction) and 2.7 μm (Y-direction) [19]. A 5-layer beam telescope system was constructed based on this chip, measuring spatial resolutions on a 5.8 GeV electron beam of 5.2 μm (X-direction) and 4.6 μm (Y-direction) [20] . The cluster size from beam tests was significantly larger than that from laser tests, adversely affecting the spatial resolution. The highest efficiency reached 99 % at the optimum threshold of 160 e^-.

JadePix-4 and JadePix-5 employed ALPIDE analog front-ends and AERD readout architectures. The latter is an efficient sparse readout logic that can quickly read out the addresses of hit pixels at very low power consumption and apply time stamps around the periphery of the pixel array. The AERD readout architecture has been adopted not only by various CMOS pixel chips on the 180 nm process but also by the next-generation 65 nm Stitching process.

4.5.2 MAPS TaichuPix series

To meet the CEPC requirements for operating at the Higgs, Z, and W modes with bunch-crossing intervals of 554 ns, 23 ns, and 185 ns, a maximum hit rate of $36\times10^6 cm^{-2}\cdot s^{-1}$ is required.

In order to address the high hit density of the CEPC, a MAPS, named TaichuPix, has

been developed with the goal of high readout speed and high spatial resolution. TaichuPix-1[7] and TaichuPix-2[8], are multi-project wafers, and TaichuPix-3 is a full-scale prototype with an engineering run. The pixel matrix of TaichuPix-3 is 1024×512 with a pixel pitch of 25 μm, and a thickness of 150 μm. The proposed baseline vertex detector consists of three layers of ladders, with double-sided mounted TaichuPix-3 sensors.

Each pixel of the TaichuPix-3 chip integrates a sensing diode, an analog front-end, and a digital logical readout in each pixel. The analog front-end is designed based on the ALPIDE[4] chip, which is developed for the upgrade of the ALICE ITS[3]. In order to address the high hit rate of CEPC, the analog front-end of TaichuPix-3 has been specifically optimized to ensure a quicker response. In addition, the digital logical readout includes a hit storage register, logic for pixel mask, and test pulse configuration. The digital logical readout follows the FE-I3[21] designed for the ATLAS pixel detector, but it has been modified to adjust the pixel address generator and relocate the timestamp storage from within the pixel to the end of the column. This modification was necessary due to pixel size constraints. Furthermore, the double-column drain peripheral readout architecture of the TaichuPix-3 chip employs an address encoder with a pull-up and pull-down network matrix.

4.5.2.1 TaichuPix specification and performance

Specification Table 4.13 summarizes the design specifications of the TaichuPix-3 chip. The performance of the pixel sensor chip has been verified with a 4 GeV electron beam at Deutsches Elektronen-Synchrotron (DESY) II. The intrinsic spatial resolution was found to be 4.8μm and 4.5μm, and the detection efficiency reached 99 %, which meet the requirements.

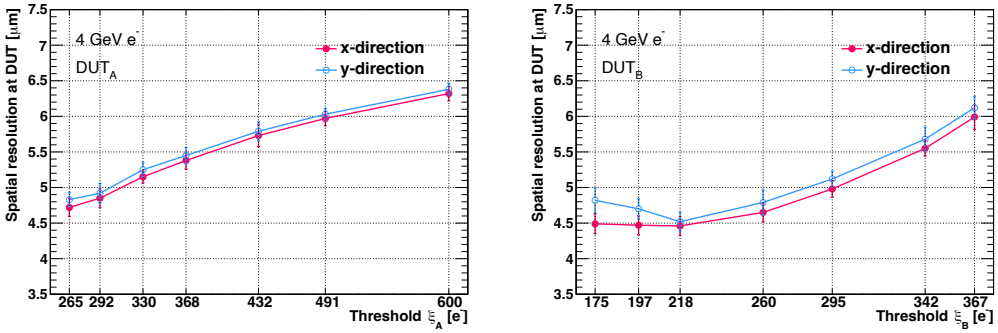
Table 4.13: Design specifications of the TaichuPix-3 chip.

Specification	Index
Pixel size	$25 \times 25 \mu m^2$
Dimension	$15.9 \times 25.7 mm^2$
Techonology	CIS 180nm
Dead time	$< 500ns$
Power density	$< 200mW \cdot cm^{-2}$
Max. Hit rate	$36 \times 10^6 cm^{-2} \cdot s^{-1}$

In order to verify the performance of TaichuPix, we conducted multiple beam tests at DESY II[9].

Spatial resolution The spatial resolution of TaichuPix-3 chips are verified by electron beam provided by DESY II. The intrinsic spatial resolution is derived from an unbiased distribution of tracking residual, which excludes the Device Under Test (DUT). The scattering angle is predicted using Highland formula.

After considering the contribution from track resolution, the intrinsic spatial resolution for TaichuPix-3 chip is about 5μm. Figure 4.23 show the spatial resolution as a function of threshold. In general, a higher threshold leads to a smaller cluster size, which introduces a bias in estimating the actual hitting position and ultimately worsens the intrinsic resolution. As depicted in Figure 4.23, for the two DUTs, increasing the threshold results in a deterioration of the intrinsic resolution. However, for DUT_B, a worse resolution is also observed when the threshold is lower than $\xi_B = 218\ e^-$, which can be attributed to the increased noise at the lower thresholds. The best resolution for DUT_A is 4.72 ± 0.13 (syst.) μm in the x-direciton, 4.83 ± 0.10 (syst.) μm in the y-direciton when $\xi_B = 265\ e^-$. For DUT_B, the best resolution is 4.46 ± 0.13 (syst.) μm int the x-direciton, 4.52 ± 0.13 (syst.)μm int the y-direciton when $\xi_B = 218\ e^-$.



(a) **(b)**

Figure 4.23: Spatial resolution as a function of threshold for DUT_A(a) and DUT_B(b) in the x-direction and y-direction. The error bars represent the total systematic uncertainty.

Detection efficiency The maximum detection efficiency is 99.68 % for DUT_A and 99.76 % for DUT_B. However, the efficiency of DUT_B drops significantly at high thresholds compared to DUT_A. This can be explained by the difference in the process of the two DUTs. An additional low-dose N-layer is added to DUT_A based on DUT_B. This modification enables a larger depletion of the epitaxial layer and results in a larger charge collection area.

4.5.2.2 Prototype of a planar CMOS vertex detector

In striving to fulfill requirements in Table 4.13, a planar CMOS vertex detector prototype (shown as Figure 4.24) has been developed and evaluated[22] using an electron beam from DESY II.

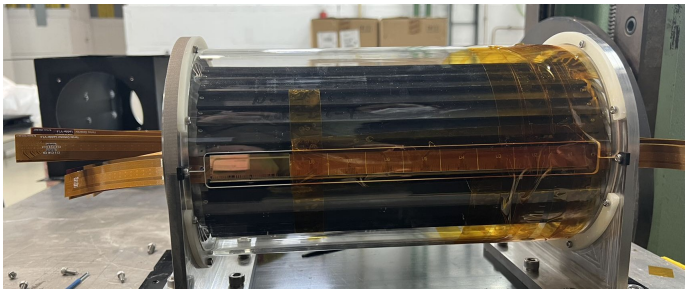


Figure 4.24: Planar vertex detector prototype with six ladders mounted for beam test.

Spatial resolution and detection efficiency The spatial resolution is derived from an unbiased distribution of tracking residual obtained using the GBL track-fitting algorithm, which excludes the DUT. The scattering angle is predicted using the Highland formula. After alignment, the standard deviation for DUT_A and DUT_B at minimum threshold is approximately 5.4 μm and 5.0 μm, respectively. Additionally, the spatial resolution of both DUTs deteriorates as the threshold increases, and due to reduced charge-sharing effects on DUT_A, it exhibits poorer resolution compared to DUT_B. At the lowest threshold setting, the best spatial resolution achieved is 5.38 ± 0.12 (syst.)μm in the u-direction and 5.52 ± 0.10 (syst.)μm in the v-direction for DUT_A, and 4.97 ± 0.08 (syst.)μm in the u-direction and 5.21 ± 0.08 (syst.)μm in the v-direction for DUT_B. To demonstrate the overall performance of the prototype, the measured spatial resolution in this article involves the resolution of the reference tracks.

The efficiencies of DUT_A and DUT_B exhibit a decreasing trend as the threshold increases. The best detection efficiency is 99.3 % and 99.6 % for DUT_A and DUT_B, respectively.

Air cooling The vertex detector is designed for very high spatial resolution. For air cooling, in addition, to cool the detector to a certain temperature, one needs to consider the vibration amplitude caused by the forced airflow, which should not affect the expected high spatial resolution. This issue was noted and studied during the prototype R&D phase. The test results, indicate that even under a higher airflow rate of 4 m/s, the maximum amplitude of vibration of the ladder support is less than 1.9 μm. In addition, during the beam test of the VTX prototype, air cooling with a fan was employed, which decrease the chip temperature from 41°C to 25°C at a power dissipation of approximately $60\mathrm{mW/cm^2}$, and no impact on the spatial resolution was observed. The strategy for addressing vibration in the baseline design of the vertex detector is similar to that of previous studies; prototyping the key structural elements and conducting related tests later on is the preferred method.

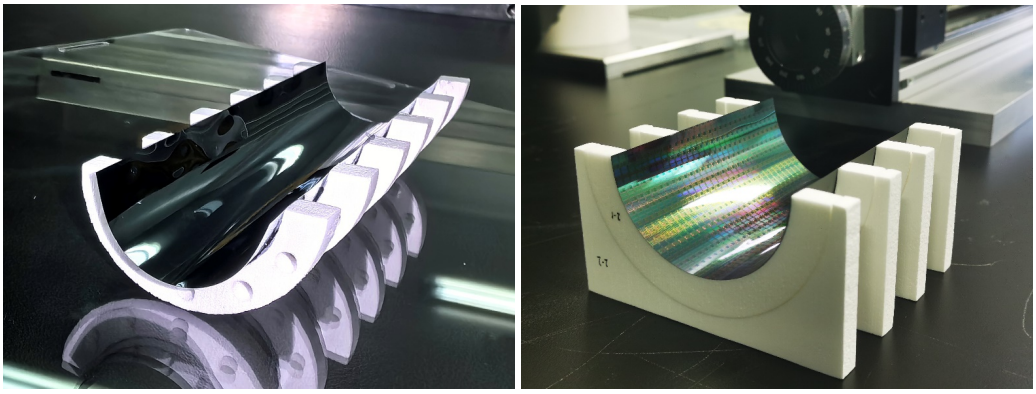
4.5.2.3 Prototype of a stitching CMOS detector

A stitched CMOS pixel sensor has been developed. It was designed and fabricated in a 0.35 μm technology, which provides a thickness of 14 μm epitaxial layer and four metal layers for routing. Since there are triple wells in this process, only NMOS could be used in the pixel. The total pixel array is 644 rows and 3600 columns stitched by a basic pixel array of 92 rows and 600 columns. It works in a rolling shutter readout mode. As a full functional prototype, it integrated column-level discriminator, on-chip zero suppression, interface circuits such as bias DAC, analog buffers, I2C control, Phase-Locked Loop (PLL), Low-Voltage Differential Signaling (LVDS), Low Dropout Regulator (LDO), etc. The total area is up to $11 \times 11\text{cm}^2$. In order to study charge collection efficiency and charge sharing, each basic pixel array has six submatrices with different pixel sizes and diode arrangements. The prototype chip is being tested and its development could provide experience in developing stitched sensor with advanced technology.

The CEPC vertex detector is designed in a structure comprising six layers of coaxial cylindrical silicon pixel detectors . To achieve better positional resolution, the first four layers utilize large-area chips based on a single-layer stitching process, with the innermost detector radius reaching 11 mm. The last two layers will adopt a double-layer ladder structure. The goal is to enhance the single-point spatial resolution of the detector to 3-5 μm, while reducing the average amount of material per layer to 0.15 % X_0. Additionally, the target power consumption for the chips is aimed to be below 40 mW/cm^2.

The radius bending test We have conducted studies on vertex detector with stitching technology. Dummy wafers have been used for bending tests, prototype manufacturing, and, meanwhile, small-area MAPS chips were used to study the impacts of bending on the chip performance.

Silicon is a brittle material. It undergoes an irreversible brittle fracture when the stress exceeds its compressive strength. We thinned the wafers to thicknesses of 30 μm, 40 μm, and 50 μm, and successfully completed bending tests with and without a film, as well as fatigue tests for different radii in various sequences, . Currently, the bending limit test has successfully achieved a minimum bending radius of 12 mm , as shown in Figure 4.25a. Additionally, we performed over 20 times of bending-recovery-bending tests on the same wafer. The prototype in Figure 4.25b has been placed for over 2 years without damage.



(a) **(b)**

Figure 4.25: Prototype for bending test. (a) Testing of bending limit, the minimum bending radius of 12 mm has achieved. (b) Determining the damage-free duration of the bending wafer, this prototype placed for over 2 years without damage.

4.6 Performance

4.6.1 Hit number and efficiency

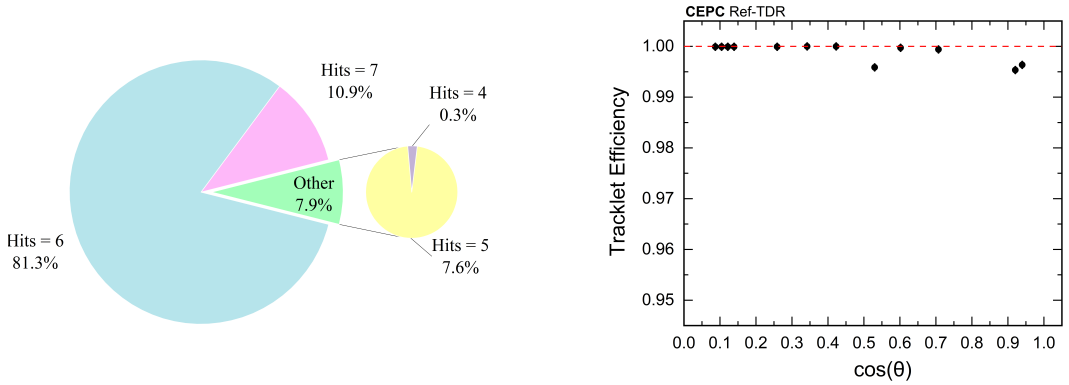
Due to the assembly of modules using sensors, which in turn form ladders or semi-circles, there inevitably exist some dead zones that cannot be used for detection, such as data interface block, switches, periphery, bias as shown in Figure 4.9 and Figure 4.4. When charged particles pass through these regions, no signal output will be obtained, meaning that part of the hits along this trajectory will be lost. During layout optimization, different deflections in the phi direction have been applied to different layers with the aim of avoiding these dead zones, thereby preventing the loss of multiple hits from a single trajectory. Ideally, for all trajectories, losing at most one hit would be the best outcome. Furthermore, for planar Taichu technology, the width of the ladders has been increased to avoid empty sensor regions in the phi direction. However, when the width becomes too large, it could lead to a situation where both adjacent ladders at the same layer have signals, which increases the material volume of the overlapping area. To assess the reasonableness of the dead zones and overlaps, simulations using chargedgeantino were performed to obtain the number of hits in the vertex detector.

The Tracklet Efficiency is defined as the sum of hits left by all chargedgeantinos' simulated trajectories passing through the vertex detector with a hit count greater than or equal to 4, divided by the total number of expected layers (6) that the vertex detector is expected to be traversed by all simulated events. This can be expressed mathematically as:

$$\text{Tracklet Efficiency} = \frac{\sum_i^N \text{Hits}i^{(\geq 4)}}{N \times L} \tag{4.1}$$

where Hits$i^{(\geq 4)}$ represents the number of hits left by the i-th chargedgeantino's simulated trajectory passing through the vertex detector with a hit count greater than or equal to 4, N is the total number of simulated events, and L is the expected number of layers that the vertex detector is expected to be traversed (in this case, 6). As shown in Figure 4.26a, for a chargedgeantino with a momentum of 20 GeV, the particle's tracklet efficiency is 99.635% at $\theta = 60°$. When each track is required to pass through the first layer of the vertex detector, the tracklet efficiency is 96.75%.

Figure 4.26b illustrates the tracklet efficiency and its errors for 20 GeV chargedgeantino particles passing through the baseline vertex detector at different polar angles. The tracklet efficiency is consistently greater than 99% in all cases.



(a) **(b)**

Figure 4.26: Performance on tracking. (a) Tracklet efficiency and its errors for 10000 chargedgeantino particles at 20 GeV. Each track contains exactly 4, 5, 6, or 7 hits, for 10,000 chargedgeantino particles simulated by the baseline vertex detector at $\theta = 20°$ and 20 GeV. (b) Tracklet efficiency and its errors for 10000 chargedgeantino particles at 20 GeV, originating from (0, 0, 0) and passing through the baseline vertex detector at different polar angles.

4.6.2 Resolution

For the two schemes mentioned in Section 4.1.2, namely the baseline and backup schemes, simulations were performed using CEPCSW in conjunction with the remaining sub-detectors of the Track system. Through simulation results, as shown in Figure 4.27, the baseline scheme demonstrates its superior d_0 resolution performance among the two schemes.

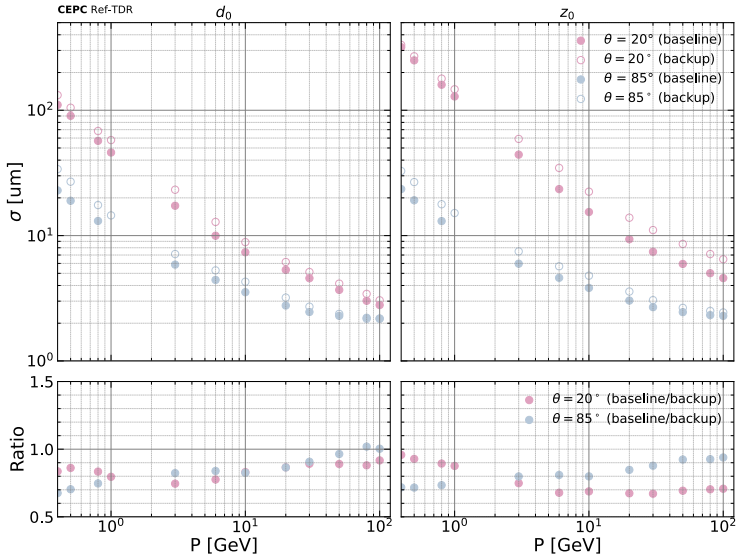


Figure 4.27: The resolution of the impact parameter d_0 and z_0 in the two schemes varies with the change in the momentum of the outgoing particles.

As previously demonstrated during the optimization, the adoption of the low-mass stitching technique allows the baseline scheme of the vertex detector to achieve good resolution of the impact parameter d_0 of tracks even at high momentum, as well as improved d_0 resolution at low momentum. In fact, not only the d_0 resolution, but the baseline scheme also exhibits excellent performance for the resolution of impact parameter z_0, as shown in Figure 4.27. The simulation results demonstrate that the trend of the z_0 resolution as a function of momentum is analogous to that of d_0, with only minor discrepancies observed. This observation aligns with the utilization of pixel detectors in the vertex detector, where the precision of z position measurements is equivalent to that of $r\phi$ measurements. Such findings indicate that when comparing different configurations, focusing exclusively on d_0 resolution is a valid approach that also minimizes the workload. The results indicate that an increase in momentum correlates with an enhancement in resolution. This improvement can be attributed to the pronounced effects of multiple scattering in material at low momentum. Similarly, as the polar angle θ diminishes, the amount of material traversed by charged tracks increases proportionally to $\sim 1/\sin\theta$, which further amplifies the multiple scattering effects and leads to a degradation in resolution.

Similarly, the z_0 resolution of the backup scheme in Figure 4.27 is also slightly worse than of the baseline scheme.

4.6.3 Performance under sensor failure scenarios

In addition to the previously mentioned impact of dead zones on performance, during actual operation, the background of the beam may suddenly increase in intensity for a short period of time especially at the initial stages of accelerator operation when the state

has not yet been optimized and adjusted, resulting in some vertex detector units failing to operate normally. Furthermore, during operation, it is also possible for certain units to become damaged. When such situations arise, the performance of the vertex detector is bound to decline. However, to ensure the smooth progress of physical analysis, the design of the vertex detector must guarantee that even in the worst-case scenarios, the performance does not experience a dramatic drop.

To this end, in the simulation process, we assume that a certain layer of the vertex detector does not produce signals to estimate performance under this special circumstance. As shown in Figure 4.28, the estimated performance for normal conditions and for damages from the first to the sixth layers is presented. It is evident that the current vertex detector scheme can ensure that, in the case of a single layer loss, the performance decrease does not exceed 30 %, with the loss of the first layer having the most significant impact. For cases of individual unit damage, the overall performance can be viewed as a weighted average of the probabilities of the intact and damaged sections. Considering the very low likelihood of two layers being damaged simultaneously, it can be reasonably anticipated that the overall impact will be minimal.

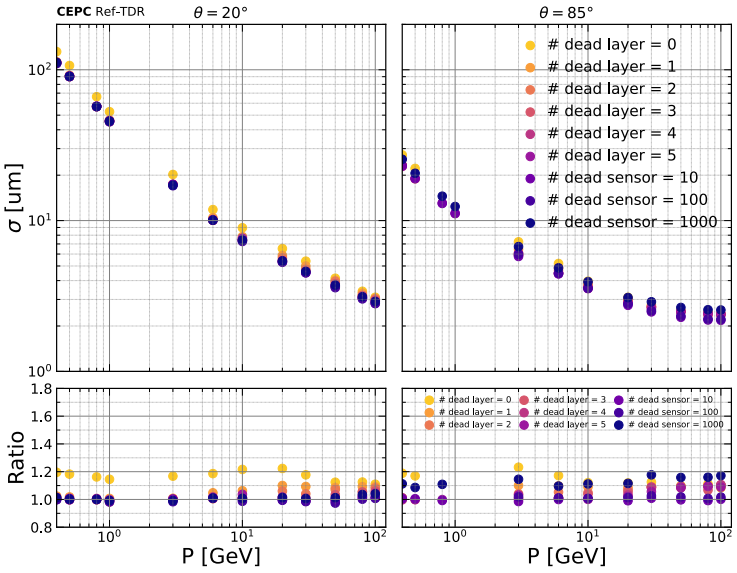


Figure 4.28: Resolution of the impact parameter d_0 of tracks obtained by the baseline vertex detector under different conditions of dead layers/sensors, respectively inactive the first (0), second(1), third(2), fourth(3), fifth(4), sixth(5) whole layer or total 10, 100, 1000 sensors in all layers in simulation.

4.6.4 Performance with beam background

In addition, due to the proximity of the vertex detector to the beam pipe, it is crucial to evaluate the effects of beam background on its performance during the design phase.

This approach incorporates true simulated backgrounds into the signal, as outlined in Section 13.2.4. This method facilitates a comparison of the d_0 resolution before and after

background incorporation, as illustrated in Figure 4.29, where no discernible effects are observed. Thus, it is evident that provided the levels of beam background remain consistent with those determined in current simulation studies, the vertex detector is poised to deliver outstanding performance. Nonetheless, it should be noted that the inclusion of beam background may lead to increased processing time for track reconstruction. Therefore, subsequent efforts should focus on algorithm optimization and enhanced computational efficiency to mitigate this increase.

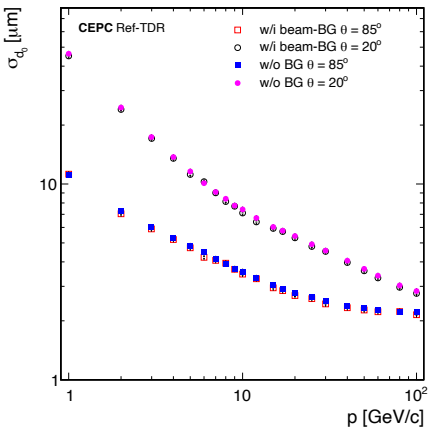


Figure 4.29: Comparison of resolution of the impact parameter d_0 of tracks between clean single muon signal (w/o BG) and mixing beam background (w/i beam-BG) at polar angle of 85° and 20°.

4.7 Summary and future plan

The MAPS-based detector layout consists of 6 cylindrical layers of pixel sensors with pixel sizes in the order of 25 μm × 25 μm, enabling hit resolutions better than 5 μm. The inner four layers are bent MAPS cylinders. The outer two layers are based on double-side ladder technology.

Initial vertex detector prototypes using double-side ladder technology have demonstrated a spatial resolution better than 5 μm with air cooling in DESY testbeam. Geant4-based simulations, demonstrate that the baseline design of vertex detector can achieve the target impact parameter resolution.

Future R&D priorities include:

1. Development of wafer-scale stitching MAPS sensors.
    - Initially, the stitching chip will leverage mature 180 nm technology (e.g., TowerJazz) to keep R&D risks and costs within reasonable bounds. The pixel cell and matrix design will build on the proven architecture of previous prototype chips, with focused efforts on stitching-related challenges and ensuring basic cell designs draw from verified experience.

- The second-generation stitching chip will transition to 65 nm/55 nm technology, with potential candidates including TPSCO's 65 nm technology and domestic HLMC's 55 nm technology. Synergy with sensor development for future LHC upgrades is anticipated.

2. Ultra-thin mechanical supports and low-mass integration techniques.
   - The plan begins with exploring the construction of a mock-up featuring dummy heaters for thermal performance testing. Results will also validate thermal simulation models.
3. Construction of a full-scale vertex detector prototype to address challenges in mechanical precision, cooling performance, and system-level integration.

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