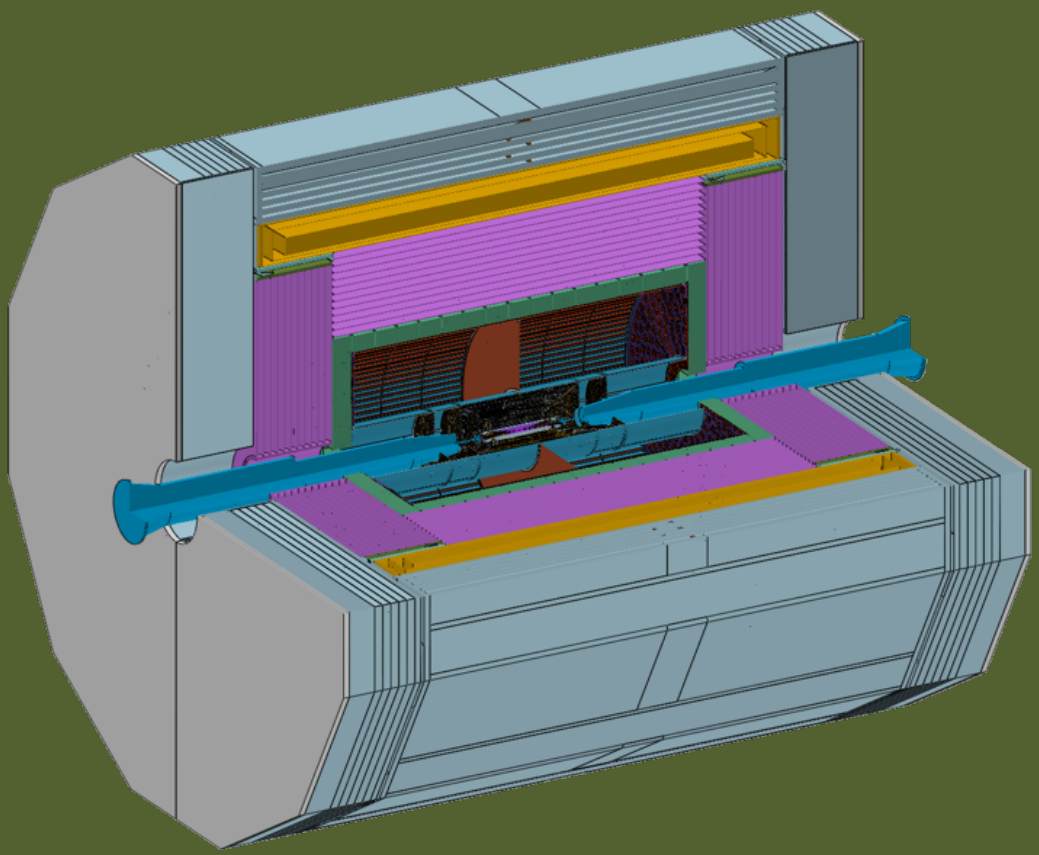
Draft v0.3.1

CEPC Reference Detector

Technical Design Report

Version: 0.3.1 build: 2025-06-12 19:37:26+08:00



Chapter 4 Vertex Detector

The CEPC vertex detector is a crucial component of the tracking system, designed to provide excellent spatial resolution and ultra-low material budget for precision vertexing and flavor tagging.

A high-granularity low-mass design based on Monolithic Active Pixel Sensor (MAPS) has been proposed and selected as the CEPC vertex detector baseline, in order to achieve an excellent impact parameter resolution while maintaining low power consumption and air cooling compatibility. The MAPS technology allows for sub-5 μm spatial resolution and minimal dead zones, with a target material budget of less than 0.15% radiation length (X_0) per layer, ensuring high tracking performance without compromising the calorimeter and timing detector coverage.

The CEPC vertex detector consists of several concentric cylindrical layers surrounding the interaction point and is finely segmented in both the longitudinal and transverse directions. This layout is optimized to provide full solid angle coverage and to ensure efficient reconstruction of secondary and tertiary vertices.

This chapter is organised in the following structure: the overall design considerations are outlined in Sec. 4.1, followed by the design on detector layout along with estimates of the background rate and radiation dose in this layout. Detailed sensor and readout technologies are presented in Sec. 4.2, Mechanics and cooling design as well as service design are presented in Sec. 4.3. R&D of key technology are presented in Sec. 4.5 to support the baseline design of the CEPC vertex detector. The detailed simulation of expected detector performance and detector alignment strategy are presented in Sec. 4.6. Finally, The summary and future plan are presented in Sec. 4.7.

4.1 Detector overall design

4.1.1 Vertex detector design specification

The CEPC is designed to operate at higher collision frequencies, accommodating multiple collision modes. In its initial 10 years, the plan includes running at 240 GeV in the Higgs boson factory mode and at 90 GeV in the Z boson factory mode. Specifically, the collision frequency for the Higgs factory is approximately 1.7 MHz, while the Z boson factory mode operates at about 14.5 MHz during the initial low-luminosity phase and increases to 43 MHz in the later high-luminosity phase. These frequencies significantly exceed the 100 kHz collision frequency of the A Large Ion Collider Experiment (ALICE) experiment, posing challenges in maintaining low power consumption at higher operational frequencies - a critical aspect of the vertex detector chip development for this project. To

balance power efficiency and timing performance, the CEPC vertex detector is designed with a power consumption limit of below 40 mW · cm^{-2} while maintaining a time stamp precision within 100 ns for recorded hits.

Additionally, the CEPC requires the vertex detector to achieve higher spatial resolution, targeting levels between 3 to 5 µm, and to maintain a low material budget of less than 0.15% X_0 per layer. This capability is essential for studying the properties of the Higgs particle, particularly its decay channels involving bottom and charm quarks, and for exploring potential new physics phenomena. The performance of the vertex detector directly impacts the physics objectives of the CEPC.

To meet the requirements mentioned above, the vertex detector has selected 65 nm technology as the baseline for chip development. Preliminary simulations and tests based on the first CEPC vertex detector prototype indicate that the power consumption at low-luminosity Zmode operation for the 180 nm technology is larger than 60 mW/cm^2. This level of power dissipation exceeds the air cooling capacity of the vertex detector, resulting in sensor temperatures surpassing the operational upper limit of 30 °C. To address this critical issue, the vertex detector has adopted 65 nm technology as the baseline technology. This choice significantly reduces power consumption and also offers the potential for smaller pixel sizes, thereby enhancing spatial resolution.

During extended runs at the Z-pole, the vertex detector will be subjected to significant radiation exposure and intense beam-related backgrounds, requiring sensor technologies with high radiation tolerance, low noise, fast timing, and reliable long-term stability. Additionally, the readout electronics must handle high occupancy and deliver data at rates sufficient to cope with the demanding trigger and data acquisition requirements, all while operating under stringent power and cooling constraints to maintain mechanical stability and minimize distortions. In summary, the key requirements are listed in Table 4.1:

Table 4.1: Baseline Requirements and Overall Vertex Detector Design Parameters

Parameter	**Baseline Requirement / Design**
Operation Period	First 10 years (Higgs factory + low-luminosity Zrun)
Number of Barrel Layers	6 layers
Layer Radii	∼11–40 mm
Material Budget per Layer	$\leq 0.15\%\ X_0$
Fluence	$\sim 2 \times 10^{14}$Neq/cm^2 (for first 10 years)
Operation Temperature	~ 5°C to 30°C
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures to minimize mass
Replacement Strategy	Replacement/upgrade after ∼10 years
Spatial Resolution	∼3–5 µm
Power Consumption	< 40mW/cm^2 (air cooling requirement)
Time stamp precision	$\pm$ 100 ns

4.1.2 Detector layout

In the baseline layout, shown as Figure 4.1, the first four layers utilize stitching technology, with each layer composed of two semicircular structures spliced together. This technology employs wafer stitching techniques to fabricate large-area sensors that can be integrated directly into a curved geometry. By reducing or eliminating the need for multiple planar tiles and mechanical support frames, curved sensors significantly lower the overall material budget. There is a mechanical gap between the two semicircular structures ranging from 0.2 to 0.5 mm, as shown in Table 4.2. The semicircular structure achieved through stitching technology requires the entire chip to be bent along the phi direction as a half arc corresponding to each radius. The position of different layers determines the arc length of the semicircle, which defines the width of the whole chip. Additionally, to satisfy the covering pole angle of 8.1°, the length of the whole chip is also determined. Due to wafer size limitations, stitching technology cannot be effectively applied to the large-area outer layers. Therefore, we employ conventional double-layer planar CMOS sensors with a ladder design for the 5th and 6th layers as Figure 4.2 shows. With the outter radius of the beam pipe in the CEPC-TDR set at 10.7 mm, the radius of the innermost layer in the vertex detector baseline is designed to be 11.06 mm based on the chip design of the stitching scheme.

A backup detector layout using 3 layer of double-sided ladders with planar CMOS sensors are also considered. The backup layout represents a well-established, more conventional option. It serves as alternative fallback solution if the baseline layout with curved technology encounters unforeseen challenges. However, it introduces additional material and complexity due to the need for mechanical support, overlaps between ladders, and potentially thicker support elements.

Detailed parameters for baseline vertex detector layout and backup detector layerout are provided in Table 4.2. The intrinsic single-point resolution of the chip is derived from the TaichuPix-3 beam current experiments, with a conservative resolution of 5 μm.

Stitching plan in baseline layout On a 300 mm wafer, the stitching plan is designed to meet the layout requirements of the four stitching layers in the baseline scheme. To enhance the design reticle utilization and streamline the process flow, the same chip is used to fulfill the baseline scheme requirements, and the same mask plate is employed. Due to the required arc length and the integer number of instances needed per layer, an instance with a dimensions of 17.277 $\times$ 20.000 mm^2 is used as the Repeated Sensor Unit (RSU)s (see Section 4.2.2). Three layouts are designed on a wafer, with the A/B/C regions of different lengths designed based on the required z-axis length. The preliminary stitching plan of the silicon wafer and the dimensions of each half layer are depicted in Figure 4.3. Each region is composed of repeated sensor units with different rows and columns, and