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CEPC Reference Detector

Technical Design Report

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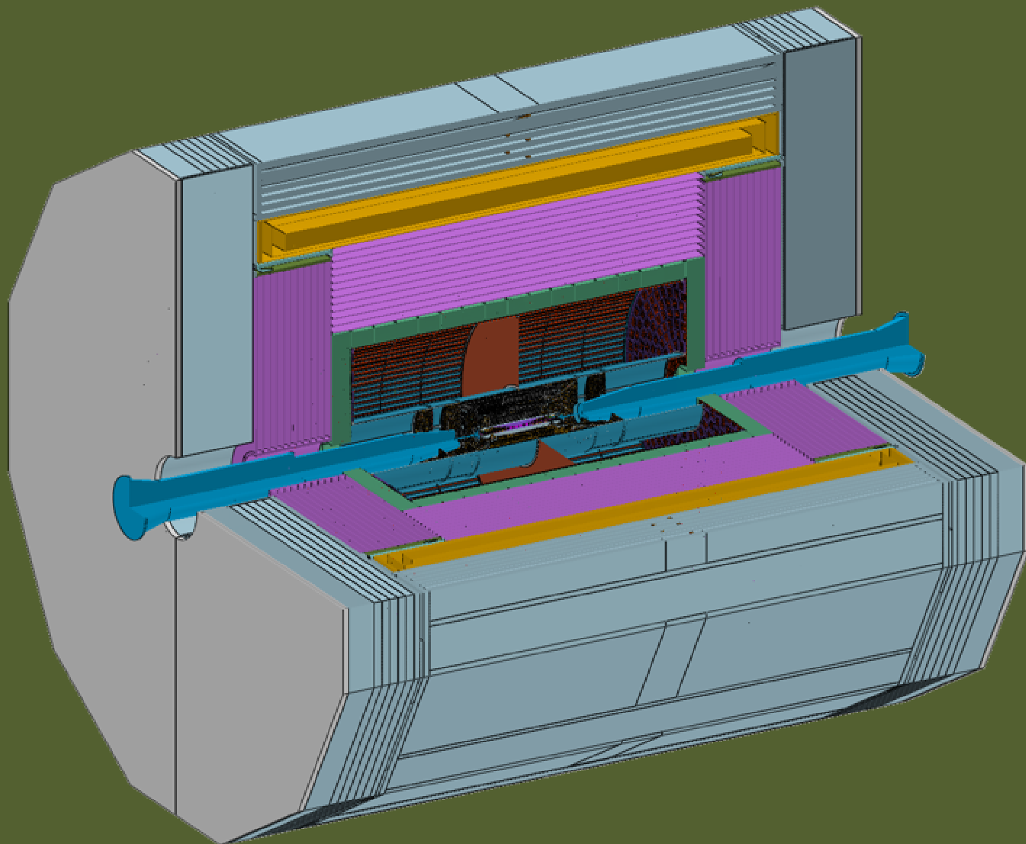

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Chapter 4 Vertex Detector

The Circular Electron Positron Collider (CEPC) Vertex Detector (VTX) is a crucial component of the tracking system, designed to deliver exceptional spatial resolution for precise vertexing and flavor tagging.

This chapter is organised as: the overall design considerations are outlined in Section 4.1, followed by the design on detector layout along with estimates of the background rate and radiation dose in this layout. Detailed sensor and readout technologies are presented in Section 4.2, Mechanics and cooling design as well as service design are presented in Section 4.3. R&D of key technology are presented in Section 4.5 to support the baseline design of the CEPC VTX. The detailed simulation of expected detector performance and detector alignment strategy are presented in Section 4.6. Section 4.7 introduces an alternative layout, and Section 4.8 summarizes the design and outlines future plans.

4.1 Detector overall design

4.1.1 Vertex detector design specification

The CEPC physics program relies on precise identification of heavy-flavor ($b-$ and $c-$) quarks and τ leptons, necessitating accurate track parameter measurements near the Interaction Point (IP) to reconstruct displaced decay vertices of short-lived particles. This requires a VTX with a material budget of $\leq 0.15\%\ X_0$ per layer and a spatial resolution of $< 5\ \mu$m. The key requirements are listed in Table 4.1.

Table 4.1: Physics Requirements

Parameter	**Baseline Requirement**
Spatial Resolution	$< 5\ \mu$m
Material Budget per Layer	$\leq 0.15\%\ X_0$
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

The CEPC VTX is built as six concentric cylindrical pixel layers stretching from a radius of 11 mm to 40 mm around the beam pipe. In the inner four layers, ultra-thin stitched CPSs are thinned to 40 µm and gently bent to the required curvature, so that each layer forms a seamless half-cylinder. Conventional ladder designs with CPSs mounted on both sides are used for layers 5 and 6. The pixel pitches are determined according to the requirement of 5 µm single-point resolution. All layers share a common 65 nm CPS front-end that integrates amplification, discrimination and zero suppression in-pixel, achieving less than 5 µm single-point resolution with a time stamp precision of 100 ns. The 100 ns readout window for the CEPC VTX is chosen to balance high timing precision

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for resolving collision events at high frequencies (especially in Z mode) with low power consumption and efficient data processing. A stitched Repeated Sensor Unit (RSU) is the building block of the curved chips, maximising wafer utilisation. Average power density is required to be under the 40mW/cm^2 cm, the limit of air-cooling .

The CEPC is designed to operate at high collision frequencies, accommodating multiple collision modes. In its initial 10 years, the plan includes running at 240 GeV in the Higgs boson factory mode and at 90 GeV in the Z boson factory mode. Specifically, the collision frequency for the Higgs factory is approximately 1.7 MHz, while the Z boson factory mode operates at about 14.5 MHz during the initial low-luminosity phase and increases to 43 MHz in the later high-luminosity phase. These frequencies posing challenges in maintaining low power consumption at higher operational frequencies - a critical aspect of the VTX chip development for this project. The CEPC VTX is designed with a power consumption limit of below 40 mW/cm^2 while maintaining a time stamp precision within ±100 ns for recorded hits. The ±100 ns readout window for the CEPC VTX is chosen to balance high timing precision for resolving collision events at high frequencies (up to 43 MHz in Z mode) with low power consumption and efficient data processing.

To meet the requirements of low power consumption, low material budget, and high spatial resolution listed in Table 4.1, the CMOS Pixel Sensors (CPS) is adopted as the sensor type for the VTX. Preliminary simulations and tests based on the first CEPC VTX prototype indicate that the power consumption of sensor at low-luminosity Z mode operation for the 180 nm technology running is larger than 60mW/cm^2. This level of power dissipation exceeds the air cooling capacity of the VTX, resulting in sensor temperatures surpassing the operational upper limit of 30°C, which may introduce higher noise levels and accelerate the aging of sensors, mechanical components, and other associated systems. To tackle this critical issue, the VTX has established Tower Partners Semiconductor Co. (TPSCo)'s 65 nm CPS technology as its baseline. Additionally, HLMC's 55 nm CPS technology is being explored as a potential alternative. This choice significantly reduces power consumption and also offers the potential for smaller pixel sizes, thereby enhancing spatial resolution. In summary, the design parameters are listed in Table 4.2:

4.1.2 Detector layout

Based on the requirements of the VTX, the VTX consists of six layers, covering the pole angle of 8.1°, and is located within the range of 11~40 mm. Leveraging the existing chip design schemes for the VTX, stitching CPS technology, and planar CPS technology, the design of the first four layers and the last two layers of the VTX is completed. Using traditional planar CPS technology, each chip is fixed on both sides of the support along the beam direction (z-direction) to form a ladder structure. At a determined radial position,

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Table 4.2: Vertex Detector Design Parameters

Parameter	Design
Spatial Resolution	$\sim 5\ \mu$m
Material Budget per Layer	$\leq 0.15\%\ X_0$
Power Consumption	< 40mW/cm^2 (air cooling requirement)
Time stamp precision	$\pm$ 100 ns
Fluence	$\sim 2 \times 10^{14}$Neq/cm^2 (for first 10 years)
Operation Temperature	$\sim$ 5°C to 30°C
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

103 identical ladder structures are arranged sequentially around the z-direction to form the last
104 two layers of the VTX, named Planar Vertex Layer (PVTX). The application of stitching
105 technology significantly reduces the total material budget of the VTX, with only the first
106 four layers utilizing this technology. The corresponding layers are named the Curved
107 Vertex Layer (CVTX). Two identical sensors of a specific size designed for this layer are
108 bent in the ϕ-direction and then stitched along the z-direction to form a cylindrical surface.
109 The size and number of sensors used in each layer are determined by the radial position
110 of that layer in the VTX.

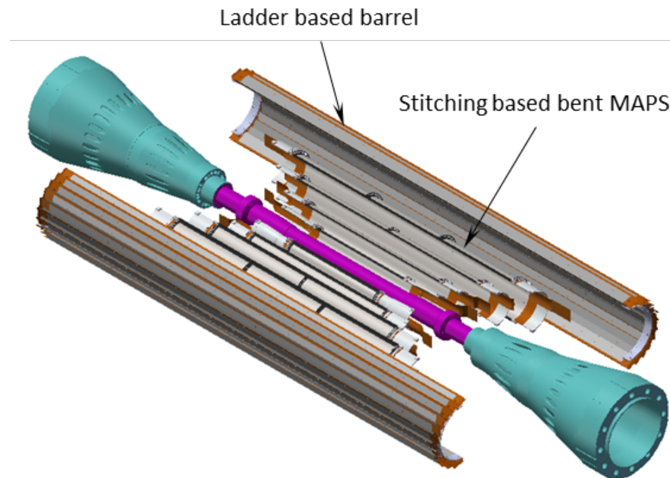

Figure 4.1: Diagram of the VTX. The first four layers are designed as single-layer structures (full-model cylindrical structure) using bent stitched sensors, while the last two layers are designed as double-layer structures (ladder structure) utilizing planar CPS.

111 **Stitching design** For the sensors constituting the curved layer of the VTX, the width of
112 the bent sensor along the ϕ-direction corresponds to the arc length of a semicircle with a
113 specific radius determined by the CVTX. To achieve the required polar angle coverage of
114 8.1°, the length of the sensor's sensitive region along the beam direction (z-direction) is also

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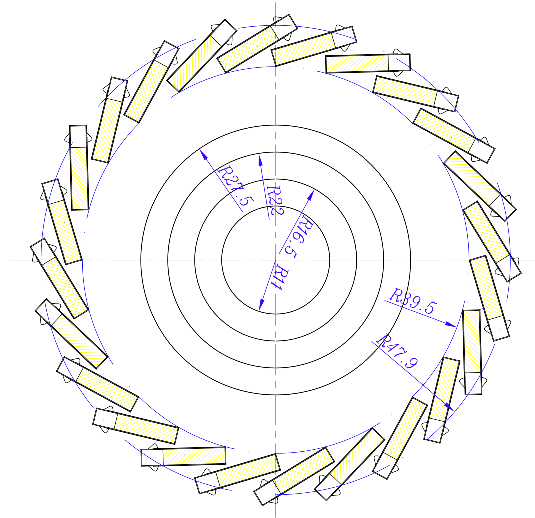

Figure 4.2: Sectional view of the VTX layout whose units are millimeters. The inner four layers are bent CPS with semi-cylindrical structure and for the fifth and sixth layers are double-layer planar CPSs with ladder desgin.

Table 4.3: Geometric configuration parameters. Radius and length, and material budget of the support structure for each layer of the VTX, as well as the arc length corresponding to Curved Vertex Layer (CVTX) and the height of ladder corresponding to Planar Vertex Layer (PVTX).

CVTX/ PVTX X	**radius mm**	**length mm**	**arc length mm**	**height mm**	**support thickness μm**
CVTX 1	11.1	161.4	69.1	-	45
CVTX 2	16.6	242.2	103.7	-	32
CVTX 3	22.1	323.0	138.2	-	31
CVTX 4	27.6	403.8	172.8	-	29
PVTX 5-6	39.5	682.0	-	3.3	300

precisely defined. Due to limitations in current semiconductor manufacturing technology and processes, the sensors are arranged on 300 mm wafers, and the dimensions of a complete sensor is constrained by the wafer size. As a result, the number of sensors used in the z-direction varies for different CVTXs. Based on the radius and length requirements of the CVTX, a 17.277×20.000 mm^2 RSU is defined as the basic unit (see Section 4.2.2.1). Three stitched sensors of different sizes are designed on a wafer, as shown in the type A/B/C in Figure 4.3. Each type of sensor comprises modules arranged in multiple rows, where a module integrates several RSUs along with I/O pads and power supply positioned at both the left and right edges.

CVTX 1 and CVTX 3 share the type C sensor, with CVTX 1 containing the two type C sensors of the two modules, as depicted in Figure 4.4. CVTX 2 utilizes the type A sensor, consisting of two type A sensors (each with three modules) arranged along the z-direction and two arranged along ϕ-direction. CVTX 3 employs the type C sensor,

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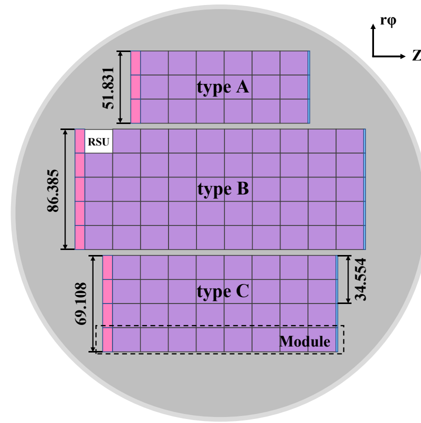

Figure 4.3: The arrangement of stitching frames on a 300 mm wafer. The units of the dimension marked in the figure are millimeters. The purple part represents the RSUs, the pink represents the Left-end Readout Block (LRB), and the blue represents the Right-end Power Block (RPB). The short-dashed line area represents a module consisting of several RSUs, one LRB, and one RPB. To meet the requirements of each layer of the VTX, the type A/B/C sensors are designed with different lengths and widths. The type A and B sensors are used to make one of the sensors for CVTX 2 and CVTX 4, respectively. The full type C sensor can be used for one of the sensors for CVTX 3. The type C sensor can be divided into four modules along the vertical direction. Using two modules of the type C sensor can make a sensor for CVTX 1.

consisting of two type C sensors (each with four modules) arranged along the z-direction and two arranged along the ϕ-direction. CVTX 4 adopts the type B sensor, consisting of two type B sensors (each with five modules) arranged along the z-direction and two arranged along the ϕ-direction. CVTXs 2, 3, and 4 are spliced in the z-direction, resulting in a 0.5 mm splicing seam at $z = 0$.

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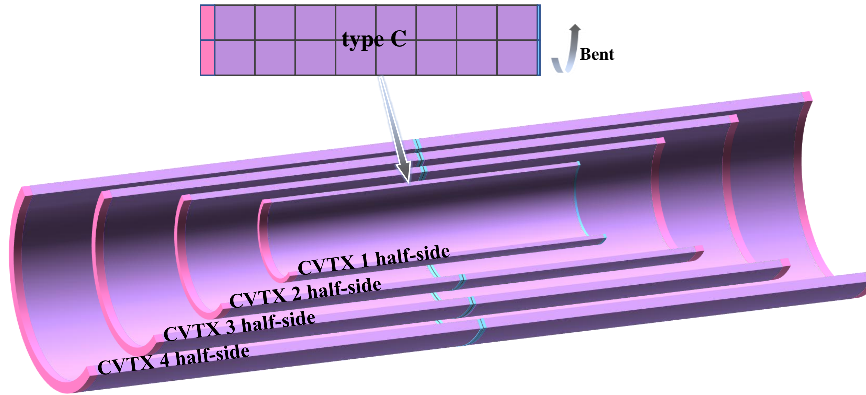

Figure 4.4: The type C sensor is diced into a sensor containing two modules, which are bent along the ϕ-direction to form a semi-cylindrical structure for the CVTX 1. Two type A sensors (each with three modules), bent along the ϕ-direction and arranged along the z-direction, create the semi-cylindrical structure for CVTX 2, with LRBs at both ends and a maximum 0.5 mm seam between RPBs (shown in gray). CVTX 3 and CVTX 4 are constructed similarly to CVTX 2.

133 Considering the mechanical dead zones in the ϕ direction and the dead zones in the
134 width of the whole sensor, the CVTX 1, CVTX 2, CVTX 3, and CVTX 4 of the VTX are
135 rotated by an angle when mounted. This angular adjustment minimizes the occurrence of
136 multiple dead zones at the same angle in the $r\phi$ plane. Each semi-cylindrical structure is
137 supported by a material with a specific thickness (see Section 4.3.1.4).

138 **Double-sided Ladders** The outer layers (5 and 6) of the CEPC VTX do not use stitching
139 technology due to wafer size limitations, as these layers require larger sensors that exceed
140 the practical stitching capabilities on standard 300 mm wafers, leading to the adoption of
141 conventional double-layer planar CPS ladders for simpler integration at larger radii.
142 The fifth and sixth layers are constructed using planar CPSs, each sized 15.9×25.7
143 mm^2 with a thickness of 40 µm. The back of the chip is glued to the Flexible Printed
144 Circuit (FPC) that conducts power and transmits the signal. The chip is treated as a unit,
145 and the dead zones of the adhesive are arranged from the $-z/2$ region to the $z/2$ region at
146 intervals of 0.1 mm. The FPC is glued to both sides of the support structure Carbon Fiber
147 Reinforced Polymer (CFRP) to create a complete ladder cell as shown in Figure 4.5 and
148 Figure 4.6, where the effective thickness of the support structure CFRP hollow pipe is 300
149 µm, as described in the Section 4.3.1.3. The geometric center of the ladder unit rotates
150 around the origin at a specific radius position from the $\phi = 0$ position, while maintaining
151 the height of the wire, forming a barrel structure known as PVTX 5-6 to ensure that no
152 particles leak out in the ϕ-direction. A total of 24 ladder structures are utilized in the fifth
153 and sixth layers.

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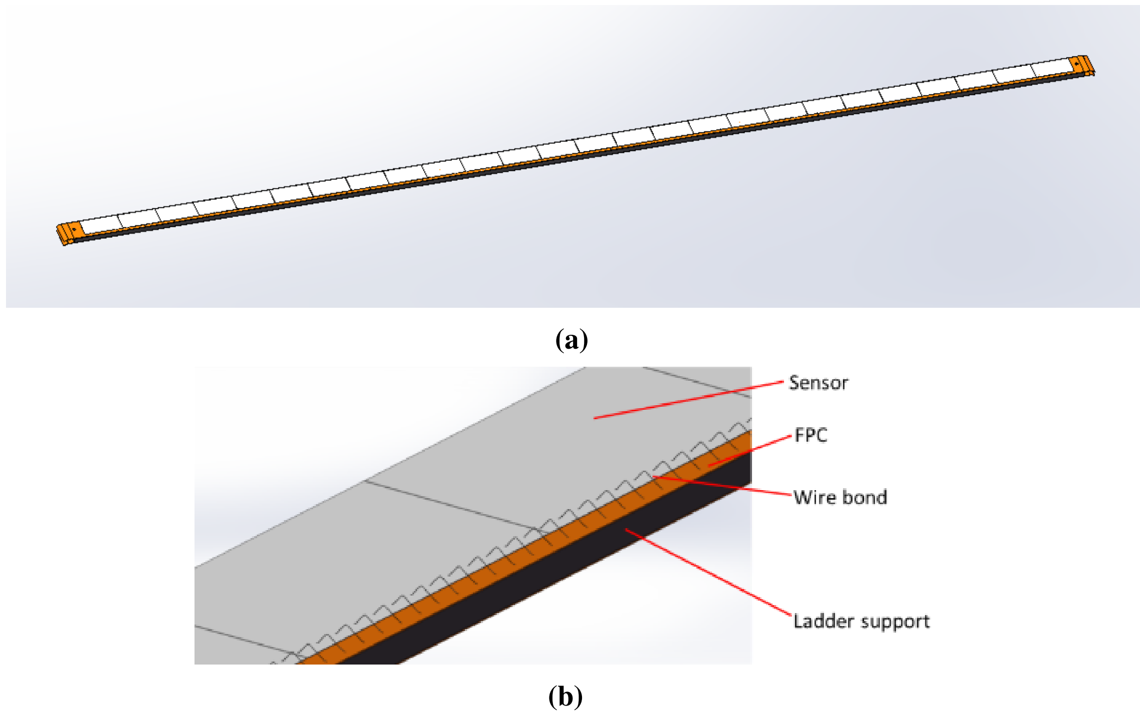

(a)

(b)

Figure 4.5: A ladder is composed of 26 chips glued to an FPC mounted on a carbon fiber support: (a) the full ladder assembly; (b) ladder detail showing sensors wire bonded to FPC.

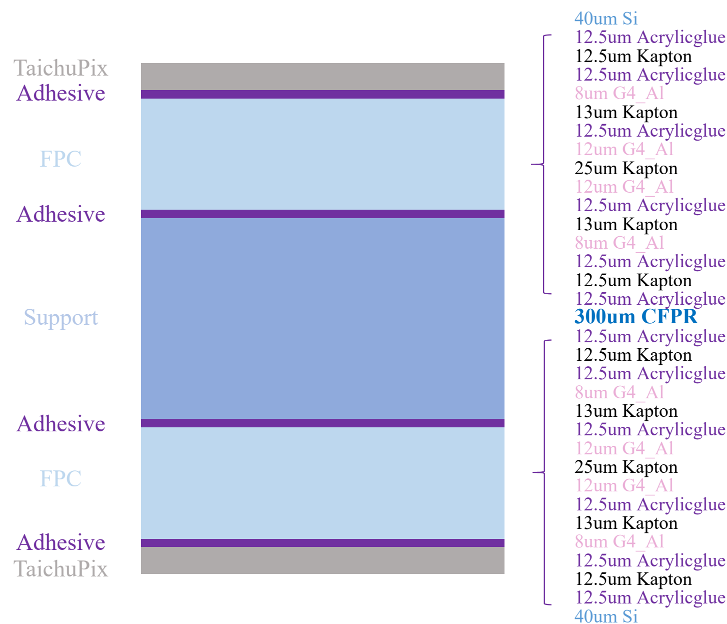

Figure 4.6: Simplified transversal cross-section of a ladder, composed of two layers of chips on the outside and other materials, such as glue, carbon fiber, and aluminum, in the bulk. Each ladder of layer 5 and 6 in the VTX utilizes this structure.

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Material budget Figure 4.7 shows the variation of the average material budget X_0 with θ in the ϕ-direction. Table 4.4 lists the material budget of each layer for the VTX at θ = 90°.

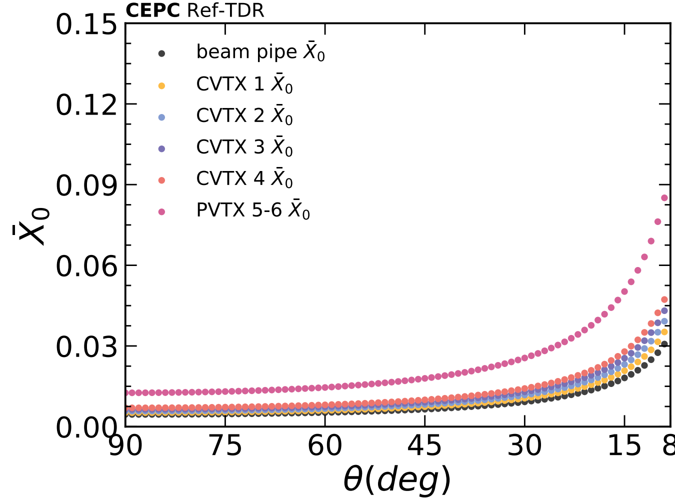

Figure 4.7: The average radiation length $\bar{X}_0$ (averaged over the full azimuthal range ϕ) of the VTX as a function of the polar angle θ (in degrees). As the polar angle θ decreases, the path length through each detector layer increases, resulting in a higher accumulated material budget.

Table 4.4: The material budget parameters of each layer for the VTX.

Unit	Beampipe	layer 1	layer 2	layer 3	layer 4	layer 5	layer 6
$\bar{X}_0$ (% X_0)	0.454	0.067	0.059	0.058	0.061	0.280	0.280

4.1.3 Background estimation

Hit rate significantly affects the design specifications of the sensor. Details of each component's contribution to the VTX will be discussed in the Chapter **??**. Here we will only present the total hit rate, data rate, occupancy, and other relevant information for each mode. With hit rate being defined as the number of particles hitting the RSU per unit time and unit area, data rate equals to hit rate times cluster size, which indicates the number of pixels fired by a single particle, and occupancy is calculated within a specified time window at pixel level.

In order to calculate the data rate, information about the cluster size is essential. To compute the data rate more accurately, we did not set the cluster size as a fixed value; instead, we referenced the results from the TaichuPix-3 beam test and calculated the cluster size based on the particle's incidence angle. The background hit rate and data rate are shown as Table 4.5, data rate is estimated here as DataRate = HitRate ×32 bit / pixel ×

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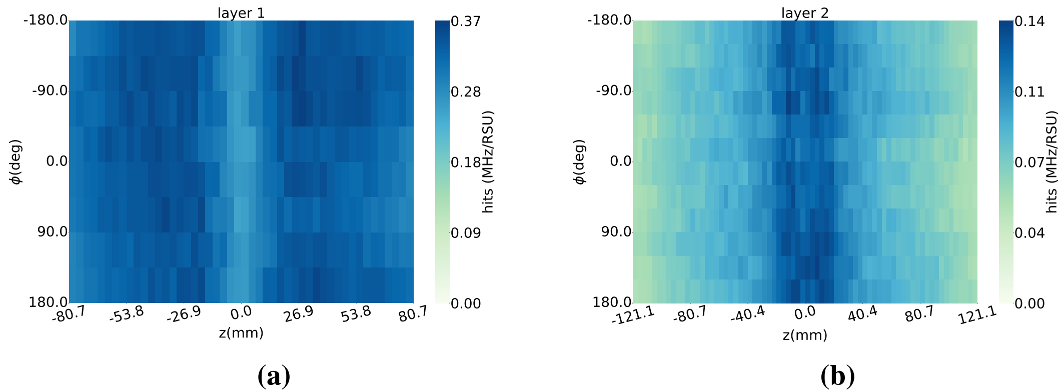
ClusterSize. Hit rate distributions of Higgs as well as Z mode are shown in Figure 4.8 and Figure 4.9.



(a) **(b)**

Figure 4.8: Hit rate distribution of beam induced background in VTX during Higgs mode runs. The shape of VTX is approximately cylindrical, where the horizontal axis can be equivalently regarded as the z-axis (along with beam pipe) of the global coordinate, and the vertical axis can be equivalently regarded as the polar angle ϕ of the global coordinate. (a) Layer one distribution: The hit rate across the entire layer is approximately uniformly distributed, with a slight decrease at $z = 0$. (b) Layer two distribution: The hit rate distribution in this layer is predominantly concentrated within $z = \pm 40$mm. This spatial concentration stems from the barrel-shaped geometry of the VTX, which inherently produces elevated hit rates near the polar angle $\theta = 90°(z = 0)$ region. The rest of the layers are not shown for their low hit rate.

One bunch spacing was used as time window to calculate the occupancy of different modes at various levels, and the results are as Table 4.6.

4.2 Sensors and electronics design

4.2.1 Sensor technology overview

The current design and development of the CEPC VTX are centered on utilizing CPS technology for chip design and manufacturing. This technology integrates the sensor and readout electronics onto a single chip, significantly reducing both pixel size and power consumption while delivering high-performance detection capabilities. Such features meet the stringent requirements for high spatial resolution, low material budget, and rapid readout speeds.

The Solenoidal Tracker at RHIC (STAR) experiment at Relativistic Heavy Ion Collider (RHIC) successfully employs Monolithic Active Pixel Sensor (MAPS) technology in its VTX [1], and the STAR MAPS VTX features excellent spatial resolution [1, 2]. The Inner Tracker System (ITS)2 of European Organization for Nuclear Research (CERN)'s

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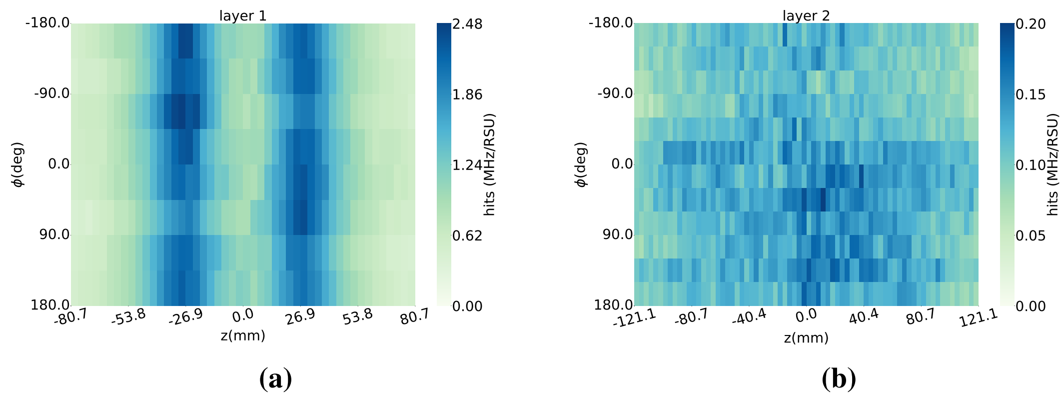

(a) **(b)**

Figure 4.9: Hit rate distribution of beam induced background in VTX during Z mode runs. The shape of VTX is approximately cylindrical, where the horizontal axis can be equivalently regarded as the z-axis (along with beam pipe) of the global coordinate, and the vertical axis can be equivalently regarded as the polar angle ϕ of the global coordinate. (a) Layer one distribution: The comparatively lower beam energy of the CEPC in Z mode ($\sim$ 90 GeV) relative to the Higgs mode ($\sim$ 240 GeV) induces cyclotron motion in most charged background particles within the first layer under magnetic confinement. This phenomenon leads to localized enhancements in hit rate at specific azimuthal positions of the first layer. (b) Layer two distribution: The hit rate distribution displays marked irregularity, attributable to the majority of particles undergoing cyclotron motion within the first layer due to magnetic field confinement. For the major difference between high-lumi Z with Z is luminosity, which means their hit rate distribution is similar, the hit rate distribution of high-lumi Z would not be shown here.

186 A Large Ion Collider Experiment (ALICE) experiment is the largest scale MAPS system
187 among high energy physics experiments [3]. ITS2 is a full-pixel silicon detector based
188 on TowerJazz 180 nm technology. It boasts exceptional technical parameters, including
189 approximately 5 µm high resolution, an extremely low material budget of less than 0.3%
190 X_0 per layer, stable readout support for collision frequencies up to 100 kHz, and power
191 consumption as low as 40 mW·cm^{-2} [3, 4]. The upcoming ITS3 upgrade for the ALICE
192 experiment introduces the concept of ”curved wafer-level chips”, aiming to achieve a self-
193 supporting wafer structure [5, 6]. This development is based on TowerJazz TPSCo 65 nm
194 technology. This innovation could potentially reduce the material budget of the VTX by
195 a factor of 3 to 5. The ITS3 project is currently in the research and development phase.
196 The comparison of key parameters between different VTXs mentioned above is shown as
197 Teble 4.7.

198 ### 4.2.2 Stitched sensor prototype design

199 The Complementary Metal Oxide Semiconductor (CMOS) stitching technology en-
200 ables the production of chips significantly larger than the dimensions of the design reticle.

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Table 4.5: Summary of background estimation. For Higgs and Z mode, the highest hit rate as well as data rate appeared at the first layer. Comparing with Higgs mode (240GeV), the difference between layer one and layer two in Z mode (90GeV) is much larger due to more low energy charged background particles performing cyclotron motion within the first layer. For high-lumi Z mode, read-out system will be optimized (detailed discussion was shown in Section **??**). Based on accelerator parameters, a rough estimation can be made for reference by simply multiplying the existing Z mode results by a factor of three. Synchrotron radiation is included, and detailed information about synchrotron radiation was shown in Chapter **??**.

Layer	**Ave. Hit Rate MHz/cm^2**	**Max. Hit Rate MHz/cm^2**	**Ave. Data Rate Mbps/cm^2**	**Max. Data Rate Mbps/cm^2**
Higgs mode: Bunch Spacing: 277ns, 63%Gap, 25× 25 μm^2/ pixel				
1	2.5	2.8	260	340
2	0.67	1.15	70	110
3	0.17	0.35	20	38
4	0.078	0.18	10	31
5	0.026	0.15	3.4	24
6	0.018	0.085	2.4	13
Z mode: Bunch Spacing: 69ns, 9%Gap, 25× 25 μm^2/ pixel				
1	9.4	19	1400	2800
2	0.89	1.5	120	240
3	0.31	0.75	46	190
4	0.19	0.47	30	160
5	0.045	0.095	6.4	14
6	0.035	0.072	4.8	12

Table 4.6: Occupancy estimation. Considering that the only difference between the two modes in the current simulation lies in the bunch settings, the occupancy in both modes should be similar. Therefore, they are combined and presented as Z mode. Synchrotron radiation is not included.

Layer	**Mode**	**Ave. Occupancy@Pixel (×10^{-5} / BX)**	**Max. Occupancy@Pixel (×10^{-5} / BX)**
1	Higgs	1.818	2.331
2		0.484	0.778
3		0.137	0.265
4		0.071	0.219
5		0.024	0.170
6		0.017	0.095
1	Z Mode	0.972	2.026
2		0.085	0.168
3		0.033	0.124
4		0.022	0.108
5		0.005	0.011
6		0.004	0.009

201 The design reticle is divided into sub-frames that align with the sub-frames of the pho-
202 tomasks. By selectively exposing these reticle sub-frames onto adjacent locations follow-
203 ing the designed pattern, manufacturers can create large chips with dimensions nearing the
204 wafer's diameter. This innovative approach expands the possibilities for chip design and

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Table 4.7: Comparison of sensor technology in VTXs of different experiments: ALICE Pixel Detector (ALPIDE)(ALICE ITS2), MOSAIX(ALICE ITS3), Taichu-3 (the first CEPC VTX prototype), and Taichu-Stitching(CEPC VTX).

Sensors	Technology Node	Power Consumption	Readout Speed	Spatial Resolution
ALPIDE [3, 4]	180 nm	$40 \mathrm{mW/cm}^2$	Up to 100 kHz	5 µm
MOSAIX [5]	65 nm	$40 \mathrm{mW/cm}^2$	164 kHz	5 µm
Taichu-3 [7–9]	180 nm	$80 \sim 100 \mathrm{mW/cm}^2$	40 MHz	5 µm
Taichu-Stitching	65 nm	$\leq 40 \mathrm{mW/cm}^2$	Up to 43 MHz	3-5 µm

205 production, allowing for more efficient utilization of wafer space. Taking into account the
206 difficulty and the yield of stitching technology, the baseline design of the stitched sensor
207 prototype involves using 1D stitching to achieve stitched-chip along the beam pipe direc-
208 tion. The feasibility of 2D stitching will also be continuously explored during research
209 and development.

210 4.2.2.1 Sensor architecture and functional blocks

211 The idea of using a stitched sensor chip to construct half of the detector layer is
212 inspired by the design of the ALICE ITS3[5][6] sensor. Thanks to the promising results
213 obtained in the MOnolithic Stitched Sensor (MOSS) and MOnolithic Stitched sensor with
214 Timing (MOST) prototypes for the ALICE ITS3 project [5], this consideration benefits
215 from the scheme of the MOSS and MOST prototype. Detailed R&D on the stitching floor-
216 plan for the VTX is under assessment at the time of writing. The preliminary stitching
217 plan of the silicon wafer and the dimensions of each half layer are introduced in Figure 4.3.
218 Figure 4.10 presents a schematic floor-plan of the sensor for Layer 1, implemented
219 by dicing out two adjacent modules. Each module operates independently. The sensitive
220 area of a module consists of eight RSUs, each representing an instance of the same
221 design. On the left side of the module, the Left-end Readout Block (LRB) facilitates
222 signal interconnections to the external systems and the power supplies to the module.
223 The Right-end Power Block (RPB), located on the right side, consists solely of power
224 transmission buses for the power distribution.

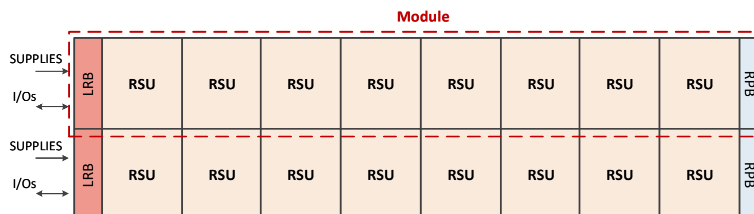

Figure 4.10: Top level floor-plan for a sensor of layer1 (not to scale). It comprises two identical modules, with one of them indicated by the dotted red rectangle.

225 Figure 4.11 illustrates the preliminary floor-plan of an RSU. The RSU is divided

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into several identical Sensor Blocks. Each sensor block is fully independent from the others with its own biasing generator, slow control and periphery readout circuit, as shown in Figure 4.12. The sensor block has local power switches located at the right side of the sensor block that can be selectively switched on by the user control. This powering granularity reduces the sensitivity of the stitched sensor to possible manufacturing faults. In the case of a supply short in one of the sensor blocks, it allows to switch off the faulty sensor blocks and maintain the others functioning normally. Considering the sensitive area of a sensor block will introduce an extra dead area in the event of switching off, the dimension of the pixel matrix in a sensor block should be choose carefully. The scale of a sensor block will be optimized in the future design for a trade-off between the power granularity and the data transmission performance. In the preliminary design at the time of writing, one RSU contains 12 identical sensor blocks and 4 stitched interface blocks arranged in two rows. Data of each sensor block has to be transmitted to the LRB through the one-to-one direct connection between the sensor block and the LRB. As the longest transmission distance reaches more than 20 cm for the rightmost sensor block of the module, the regeneration of the signal periodically over the link is necessary. This function is proposed to be implemented in the stitched data interface blocks. The stitched data interface block transmits control signals and data from sensor blocks to the LRB. The RSU is divided into multiple sections internally, different functional blocks are repeated multiple times. An RSU contains 12 Pixel Matrices, Biasing Blocks, Power Switch Blocks, and Matrix Readout Blocks, and 4 Stitched Data interface Blocks.

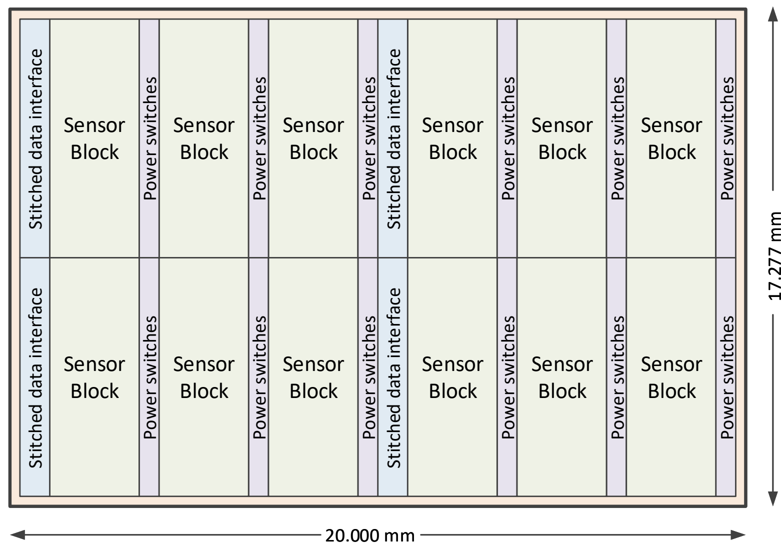

Figure 4.11: Proposed floor-plan for a RSU (not to scale). It contains several identical sensor blocks. Each of them has a pixel matrix with its own biasing generator, slow control and periphery readout circuit. Each sensor block can be selectively switched on/off. The stitched data interface blocks are used to transmit control signals and data to the edge of the stitching sensor.

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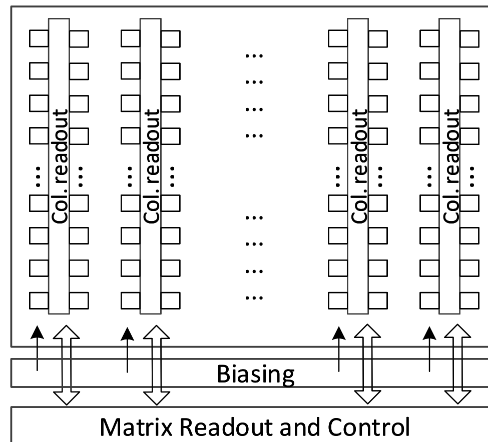

Figure 4.12: Architecture of the sensor block. It consists of a pixel matrix, a biasing generator and a periphery readout and control.

247 **4.2.2.2 Design of the repeated sensor unit**

248 Each pixel cell integrates a sensing diode, a front-end amplifier, a discriminator
249 and a digital pixel readout. The in-pixel digital readout benefited from the TaichuPix
250 prototype. Each pixel contains a hit storage register and logic for pixel mask and test pulse
251 configuration. A common threshold level is applied to all the discriminators of the pixels.
252 Every pixel can be tested and calibrated individually, combining charge injection scans
253 and threshold scans.

254 **I. Sensing diode** A sensing diode is formed by an N-implant electrode in a P-type
255 epitaxial layer. The geometry of the sensing diode involves a trade-off among charge
256 collection performance (i.e. efficiency, collection time, and radiation tolerance), area, and
257 sensor capacitance. As discussed in Section 4.5.1, the sensor performance optimization
258 was previously explored with the 180 nm TowerJazz CPS technology. These studies
259 provide foundational insights for enhancing sensor performance in the 65 nm TowerJazz
260 CPS process. A variety of pixel test structures are proposed to be designed in the initial
261 phase of the stitched sensor R&D phase of the stitched sensor to further optimize the
262 sensor geometry for compatibility with the 65 nm CPS process. The structures include
263 different electrode diameters, spacing between the electrode and the surrounding PWELL,
264 PWELL geometries, and methods of applying reverse bias to the sensor diode.

265 **II. Pixel Front-end** The simplified schematic of the analogue front-end is shown in
266 Figure 4.13a, which had been verified with the TaichuPix prototype (see Section 4.5.2).
267 The topology of the circuit was derived from the ALPIDE sensor chip used in the ALICE
268 ITS2 [4]. The analog front-end and the discriminator are continuously active.

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III. In-pixel digital logic The in-pixel digital electronics, as shown in Figure 4.13b presents the diagram of the in-pixel logic. It features a hit latch set by a negative pulse from the output of the front-end. The pixel readout follows a double-column drain arrangement. The region for in-pixel digital readout logic is shared by two columns to minimize the crosstalk between analog signals and digital buses. Additionally, it saves space for the routing of the address encoder. The priority logic arbitrates the pixel readout, with the topmost pixel having the highest readout priority. The in-pixel logic also integrates configuration registers for calibrating the pixel front-end, for testing in-pixel readout logic, and for masking the faulty pixel. The configuration function is programmable through the setting of control bits, including MASK_EN, PULSE_EN, DPULSE and APULSE (as shown in Figure 4.13b).

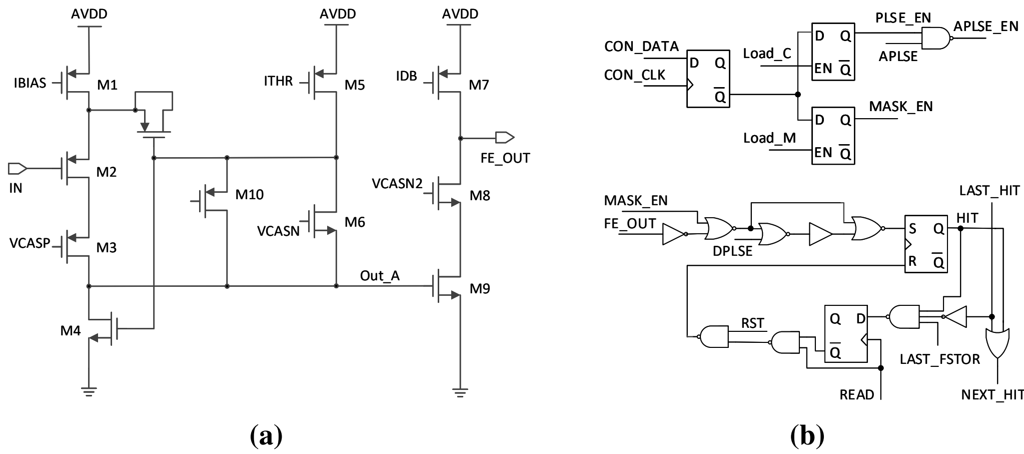

Figure 4.13: Schematic and block diagram of the in-pixel circuits. (a) Analog front-end, including a charge-sensitive amplifier and discriminator. (b) Diagram of the digital logic. It features a hit latch set by a negative pulse from the output of the front-end. The pixel readout follows a double-column drain arrangement. The in-pixel logic also integrates configuration registers for calibrating the pixel front-end, for testing in-pixel readout logic, and for masking the faulty pixel.

IV. Peripheral readout circuits on sensor The main function of the on-chip peripheral readout circuits includes: sending control signals required by the pixel array and receiving data from the pixel array; buffering the data to smooth the output data rate; providing a slow control interface for chip configurations and tests.

The data from the pixel array are organized in Double Columns (Dcols). In order to achieve a detection efficiency close to 100%, all double columns of pixel array are read out in parallel. A timestamp is recorded at the end of the double column for the future data processing. Without a trigger signal, all the readout data are buffered and sent out. A data compression mode is optional, which coulod reduce the output data rate by half.

The peripheral readout circuit's core function is to send control signals to the pixel array and receive data from it. A data-driven schema is preferred. The read signal is only

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sent when the pixel is triggered. To read the signals sequentially, a priority mechanism must be implemented. The most popular method is address priority. A hit signal is generated when the collected signal exceeds a threshold and is reset after the pixel address is read out.

Based on this approach, the pixel array's clock is inactive in the absence of a hit. This approach effectively minimizes power consumption. To optimize control timing, a hierarchical priority control chain can be implemented.

To accommodate higher data rates, a real-time data compression strategy can be implemented before sending data to First In First Out (FIFO)s.

The address of the first pixel in a package is recorded, while the next three pixels are encoded using a three-bit code, where '0' represents no hit and '1' represents a hit. Operating at a system clock of 43.33 MHz, the data compression circuits incur no additional timing overhead. By enabling the data compression function, the data volume is reduced, and the readout speed is increased.

The fast chip-level readout is closely related to FIFO accesses. We propose a shareable architecture [10]. The shared FIFO features flexible capacities to handle random hit bursts. As a result, higher hit flux can be accommodated even with a reduced total memory volume.

The power consumption is evaluated based on TaichuPix, which is implemented using a 180 nm process for average hit rates of 1 MPixels/s·cm^2, 15 MPixels/s·cm^2, and 40 MPixels/s·cm^2. The future design of the RSU will use a 65 nm process. The power supply will be reduced from 1.8 V to 1.2 V. The area of the peripheral readout circuits is estimated to be reduced by 50%. The dynamic power consumption due to clock and data upsets is estimated with a reduction of 4.5 times. However, the static leakage currents will increase significantly. To limit the power density within 40 mW/cm^2, the power consumption of peripheral circuits in RSU is estimated to be 40 mW, and the leakage current should be controlled in 5 times of TaichuPix. Power switches will be implemented to meet these requirements. Finally, the power consumption of the future design is estimated as 29 mW and 37.5 mW for 8 MPixels/(s·cm^2) at Higgs mode and 42 MPixels/(s·cm^2) at Z mode, respectively.

Considering the application and tests, the chip will provide proper register control and on-chip test mode.The On-Chip Test (OCT) module is planned to generate input signals for peripheral readout circuits, enable chip debug and data alignment. The register control provides internal status access and configuration of readout function, bias voltage/current, pixel mask and calibration, and so on.

4.2.2.3 Design of the left-end readout block

All data from a row of RSUs of a module, seeing Figure 4.10, are collected and processed by the LRB located on the left side of the module. Primary functions of the

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LRB are illustrated in the The block diagram of Figure 4.14. The RSU data are transmitted to the LRB via a large array of differential point-to-point on-chip serial data links, which operate at 86.66 Mbps. As modules of different CVTXs containing different numbers of RSUs, the module in CVTX-4 houses the largest quantity, i.e. 10RSUs. Since each RSU is equipped with 12 data links, the LRB must accommodate up to 120 data links. A group of 128 receivers primarily compensates for phase differences in the incoming data streams from the RSUs and resamples them using a local fast clock. The data encoding blocks collect and encode the data with redundancy to correct errors during off-chip transmission. After encoding, the data are serialized at a rate of 1.39 Gbps and transmitted off-chip using 8 serializers. The Clock Block supplies clocks required for the LRB and RSUs. Additionally, the LRB facilitates slow control and manages power switch control signals for the RSUs.

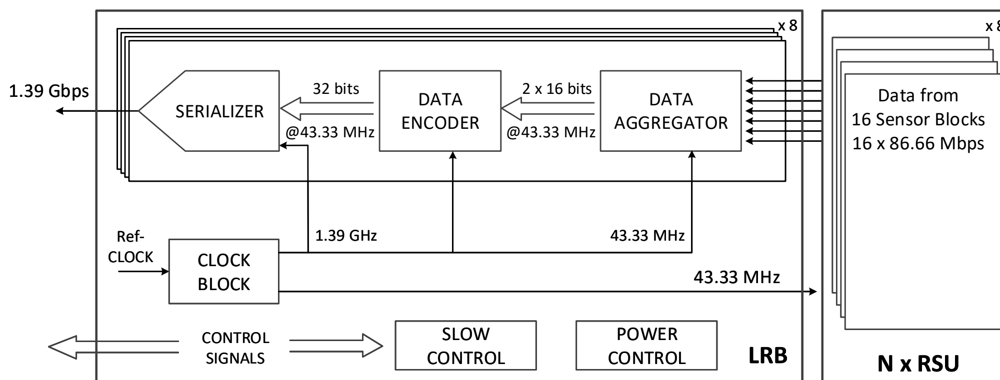

Figure 4.14: Proposed diagram of the Left-end Readout Block (LRB). All data from Repeated Sensor Unit (RSU)s of one module has to be transmitted to the LRB. 'N × RSU' labeled in the right part of the diagram represents that different layers in the detector contain a varying number of RSUs.

4.2.2.4 Power consumption estimates

As illustrated in Figure 4.11 and 4.12, each RSU consists of pixel matrix, biasing blocks, matrix readouts, and data interface blocks. The expected power consumption of the main functional blocks of an RSU as well as the total power consumption of a single RSU are listed in Table 4.8. The current consumption is mainly determined by the bias current (IBIAS) of the first branch, adjustable by one of the local Digital-to-Analog Converter (DAC)s in the periphery of the pixel array. Targeting the requirement of 40 mW/cm^2, the value of IBIAS is reduced compared to the one in the TaichuPix design. The choice of the IBIAS value is a trade-off between the power consumption and the speed. By design, the nominal power consumption values of the new front-end in TPSCo 65 nm process are 68.4 nW. The nominal value corresponds to analogue power densities of 26.7 mW/cm^2 for the pixel pitch of 16 µm and 10.9 mW/cm^2 for the pixel pitch of 25 µm. In Table 4.8, the entries for the pixel matrix include the power of the pixel analogue circuit and the

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353 pixel digital logic. In the current calculations, it is assumed that the pixel size is 25 × 25
354 μm^2, which is consistent with the intrinsic position resolution value used in Section 4.1.2.
355 The power of the pixel analogue is calculated by the power density of the pixel front-end
356 (shown in Section 4.2.2.2) and the total area of 12 pixel matrices. The power consumption
357 of the pixel digital in the table includes the dynamic power of the in-pixel digital logic
358 and the double-column address encoding logic (described in Section 4.2.2.2), as well as
359 power consumption due to the leakage current. The dynamic power consumption of the
360 pixel digital circuit mainly depends on the pixel hit rate. Based on estimations of the hit
361 rate in the VTX and testing experience with the TaichuPix prototype, the dynamic power
362 consumption of the pixel digital circuit is relatively small. In contrast, considering the
363 planned use of 65 nm CPS process, the contribution of leakage current from transistor gate
364 leakage to power consumption is much greater than the dynamic power of the digital circuit.
365 The contribution of the Biasing Blocks is estimated based on the experience of the design
366 in the TaichuPix. The entry for the Matrix readout blocks is described in Section 4.2.2.2.
367 The value for the data interface blocks is obtained from the very preliminary considerations
368 on the transmitting power of the control signals and the readout data of RSUs. Table 4.9
369 lists the power consumption estimates for the main functional blocks of the LRB (see
370 Figure 4.14).

Table 4.8: Estimates of power consumption of one RSU. All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	Pixel analogue	Pixel digital	Biasing block	Matrix readout	Data interface	RSU Total
Power [mW]	36	30	8	40	17	131

Table 4.9: Estimates of power consumption of the LRB. All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	Clock Block	Data Aggregator	Data Encoder	Serializer	Slow & Power control	LRBTotal
Power [mW]	36	120	80	32	80	348

371 Combining the power estimates of Table 4.8 and 4.9 with the surface areas of the
372 major blocks, one obtains the estimates for the power dissipation densities. The results
373 are given in Table 4.10.

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Table 4.10: Estimates of average power dissipation per unit area over the main functional blocks composing the stitched chip

Components	Power density [mW/cm^2]
Repeated Sensor Unit	38
Left-end Readout Block	485

374 ### 4.2.3 Backend electronics and cables

375 The FPCs is integrated to the backend electronics system. These FPCs serve as
376 conduits for transmitting signals, clocks, control commands, power, and ground connec-
377 tions between the control boards and the detector modules. By providing a lightweight and
378 adaptable interconnection, the FPCs facilitate efficient data communication and power dis-
379 tribution while minimizing material usage, which is crucial for maintaining the detector's
380 performance and reducing multiple scattering effects.

381 ## 4.3 Mechanics, cooling and services

382 This section describes the mechanical design of the VTX, including the support
383 structure and related finite element analysis, detector air cooling and the general scheme
384 of services.

385 ### 4.3.1 Mechanics

386 #### 4.3.1.1 General support structure

387 The baseline design of the VTX consists of, from inner radius to outer radius, four
388 concentric cylinders constructed with stitching technology-based bent CPS followed by
389 a single-layer double-sided ladder-based barrel. The innermost cylinder has a radius of
390 11 mm, and maintains a 0.3 mm gap from the beam pipe. The Figure 4.1 demonstrates
391 the general structure of the detector and its integrated mechanical support. The general
392 mechanical support design for the VTX aims to use ultra-light materials to create a rigid
393 enough structure, realizing a low material budget without weakening the spatial resolution.

394 #### 4.3.1.2 Ladder and support

395 The double-sided ladder is the structural unit of the layer 5 and 6 . It features pixel
396 sensors on both sides of the ladder support, while sensors are glued onto the FPC, which
397 is in turn glued onto the ladder support. The CFRP is used to make the ladder support
398 due to its low density and high specific modulus and strength. The main body of the

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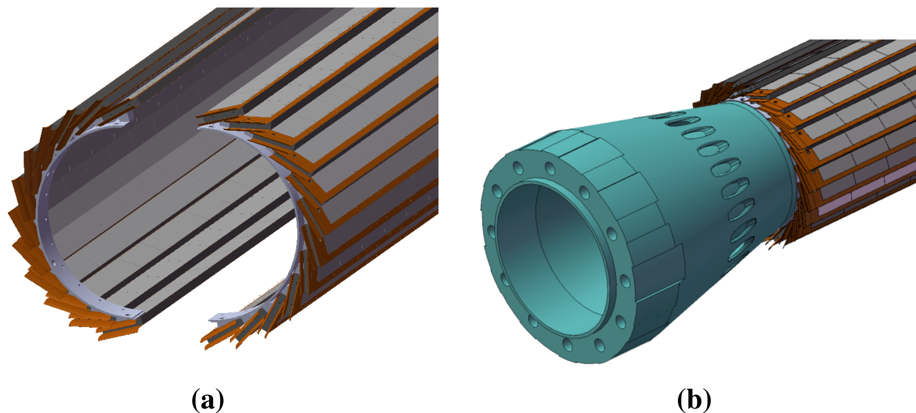
399 ladder support [11] is a hollow shell structure [11] with an overall size of $682 \times 3.2 \times 17.5$
400 mm^3 . With the assistance of the finite element static analysis, the laminated shell of the
401 ladder support is made of ultra-thin CFRP plies, using the high modulus CFRP at a level
402 equivalent to M40, the CFRP laminate of the shell is made with a thickness of 0.15 mm,
403 to get a conservative estimation by just putting the mass of the sensors and FPC to the
404 bare ladder support (without taking into account their contribution to the rigidity of the
405 complete ladder), it is anticipated that the ladder support deforms very slightly and at a
406 negligible level. According to previous evaluations, about 20% smaller deformation will
407 be induced for the complete ladder [11].

408 #### 4.3.1.3 Ladder-based barrel and fixation to the beam pipe (assembly)

409 The VTX is the first detector outside the beam pipe, and structurally it will be
410 integrated into the beam pipe assembly. The outermost layer of the VTX, the ladder-based
411 barrel, does not directly mount on the beam pipe; it rests and is secured to the intermediate
412 conical parts that are mounted to the beam pipe, providing support for the vertex structure.
413 The four layers of the CVTX are mainly fixed to the extended section of the beam pipe.

414 The barrel-shaped outer layer detector formed by the double-sided ladders which
415 overlap with each other in the circumferential direction to form a continuous sensitive
416 layer. To facilitate barrel assembling and its installation on the beam pipe integration, the
417 barrel structure is designed as in Figure 4.15 shows. It is assembled by two half-barrels,
418 with each half-barrel consisting of two half side-rings located at both ends along with
419 several ladders. The ladders are positioned and secured to the side-rings by the surfaces
420 of the tooth-shaped structure of the side-rings. After the two independent half-barrels
421 are pre-assembled on dedicated tooling, they are installed and fixed onto the intermediate
422 conical part of the beam pipe assembly, as illustrated in Figure 4.15.



(a) **(b)**

Figure 4.15: (a) The outer layer of the VTX barrel. (b) The outer layer of VTX assembled on the beam pipe

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423 The ladder-based barrel design is consistent with our previous prototyped vertex
424 design. Furthermore, much R&D work involving structural validation tests were conducted
425 during the previous prototype development phase. These experiences can be helpful to
426 optimize the TDR design.

427 #### 4.3.1.4 Bent CPS cylinders and fixation to beam pipe

428 There are four layers of bent CPS cylinders with different radii and lengths consistent
429 with the physical layout of the VTX. Each of the four bent CPS cylinders is a single
430 detector layer that consists of two half cylinders, as shown in Figure 4.16. To maintain the
431 bent CPS in the shape of the cylinders, ultra-light local supports made of CFRP have been
432 designed for each layer. Integrated with the electronic readout, the FPC is connected to the
433 curved edge of the bent CPS on its lateral side by wire bonding. To keep the connecting
434 joint safe and also for protecting the wire bonds, extended support has been designed for
435 each cylinder, as shown in Figure 4.16, it prevents the FPC from deforming very close
436 to the joint area, thereby avoiding damage to the connection. The bent CPSs, the local
437 support and the extended support form the cylinder assembly. Each cylinder assembly is
438 independent and has no contact with the adjacent layers of cylinder assemblies, also will be
439 mounted onto the beam pipe assembly separately . This kind of design focuses primarily
440 on realizing and facilitating a feasible process for both assembly and wire bonding, as well
441 as installation onto the beam pipe. The results of the finite element simulation analysis
442 indicate that, under constrained conditions at both ends, this structure has very minimal
443 deformation, and the stress on the bent chips is also very low, both of which are negligible.

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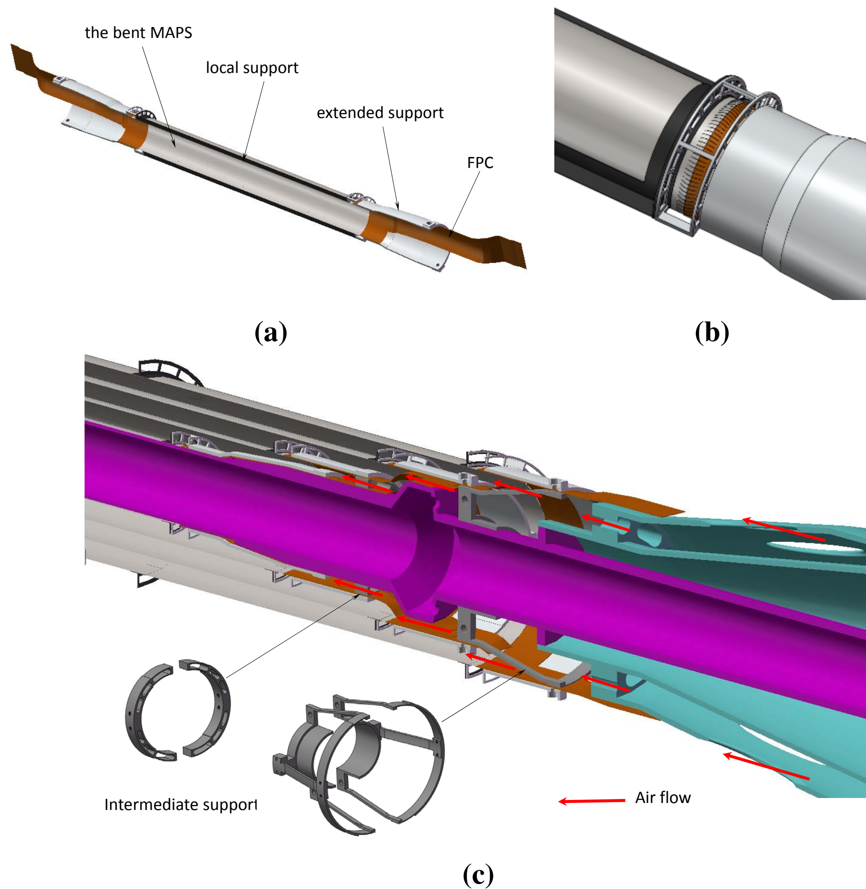

Figure 4.16: The half cylinder assembly (bent CPS with FPC and the extended support) of the innermost layer. (a) An overview of the half cylinder of bent CPS detector layer, and the yellow part is FPC. (b) An extended support to prevent the FPC from deforming too close to the joint area. (c) Cylinders installation and intermediate support.

444 ### 4.3.2 Cooling

445 The heat generation of the VTX for both the ladder-based barrel and the bent CPS
446 cylinders is estimated to be at the same level of 40 mW/cm^2. The operational temperature
447 for the detector is required to be no higher than 30 °C. Thus, cooling is essential for main-
448 taining optimal sensor performance. Generally, electronic equipment with heat generation
449 up to 0.3 W/cm^2 can be cooled using forced air convection. Given the stringent material
450 budget goal for the VTX, forced air cooling has been selected as the cooling method.
451 To evaluate the cooling performance of the current structural design of the VTX ,
452 air cooling simulation analysis was conducted. The simulation results indicated that at an
453 average flow rate of 3.5 m/s, the maximum temperature of the outer ladder is within the
454 required range, as shown in Table 4.11. For the bent CPS cylinders, the innermost layer
455 is very close to the beam pipe and has no airflow, making it the most challenging layer to
456 cool within the entire detector. The simulation results indicate that at an airflow rate of 3.5

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Table 4.11: Simulation results of the barrel-maximum temperature on the ladder. Inlet air temperature of 5 °C; air speed of 3.5 m/s.

Power dissipation	Total heat generation of the barrel	Max temperature on ladder
40 mW/cm^2	190 W	29.4 °C

457 m/s (which satisfies the ladder cooling), with the central beam pipe surface temperature
458 considered, the innermost layer of the bent CPS cylinder can be cooled to a sufficiently low
459 temperature, as shown in Figure 4.17, thereby meeting the requirements. Additionally,
460 simulations were performed to compare the maximum temperature of the innermost layer
461 at different wind speeds. Based on these simulation results, it can be anticipated that air
462 cooling will meet the cooling needs of the detector.

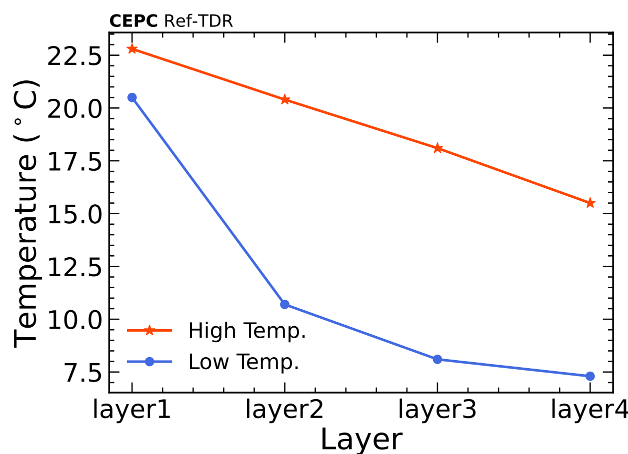

Figure 4.17: Thermal simulation results of highest and lowest temperature on bent CPS cylinders layers of the VTX. "High (Low) Temp." in the legend indicated the highest (lowest) temperature of the bent sensor in that layer. The results are simulated with an airflow rate of 3.5 m/s for air cooling and overall power consumption of 40 mW/cm^2 for sensors. The beam pipe surface temperature, as shown in Chapter **??**, is taken into account.

463 ### 4.3.3 Services

464 This section introduces the needs and considerations of the general services for the
465 VTX. The vertex uses air cooling; the main service requirement is to ensure proper airflow
466 and good ventilation for the entire detector zone. The VTX will be mounted onto and
467 integrated into the beam pipe assembly; the other service requirement is to route all the
468 cables of the VTX out of the very space-limited beam pipe assembly.
469 Since the VTX consists of a single barrel layer and four concentric cylinder layers,
470 ventilation for each gap between the adjacent layers must be ensured for effective cooling.
471 The mechanical design for the VTX fully considered this requirement and also tried

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472 to minimize the effect caused by FPCs blocking, which is obviously reflected in the
473 hollow support structures designed for the detector, especially the support of the bent CPS
474 cylinders. The conical part that is integrated into the beam pipe assembly to support the
475 barrel layer mentioned before also works as the general air distributor for the entire VTX.
476 It is a hollow structure; air will be blown into the inside hollow space from the side of the
477 part then distributed to the detector zone through those ventilation holes facing different
478 zones of the detector on the outer surface, as shown in Figure 4.18.

479 The space for the entire VTX inside the beam pipe is very compact. Together with the
480 beam pipe assembly, for the VTX, on both ends of the barrel and the bent CPS cylinders,
481 the FPCs of the ladders and the bent CPS are the only cables that need to be routed
482 out. The FPCs of the bent CPS cylinders will be routed along their extended support
483 and converged after the end of the outermost layer, and then they are stacked and go
484 through the intermediate conical part via the grooves. The FPCs of the ladders of barrel
485 will be streamlined by converging the FPCs of two adjacent ladders into one conduit,
486 similar to the FPCs of the bent CPS, then go through the conical part via their specified
487 grooves, as illustrated in Figure 4.18, which effectively halves the spatial occupancy and
488 preventing the circumferential accumulation of FPCs from fully cover the outer surface of
489 the conical part. After all the FPCs are routed outside the beam pipe assembly, they will
490 be transferred to optical fibers via connectors, as described in Section 4.2. Additionally, a
491 half-dummy model of the vertex structure, incorporating the bent CPS cylinders and two
492 short ladders, was constructed to test the FPC routing, as shown in Figure 4.19. The trial
493 results demonstrated that the routing scheme is fundamentally feasible.

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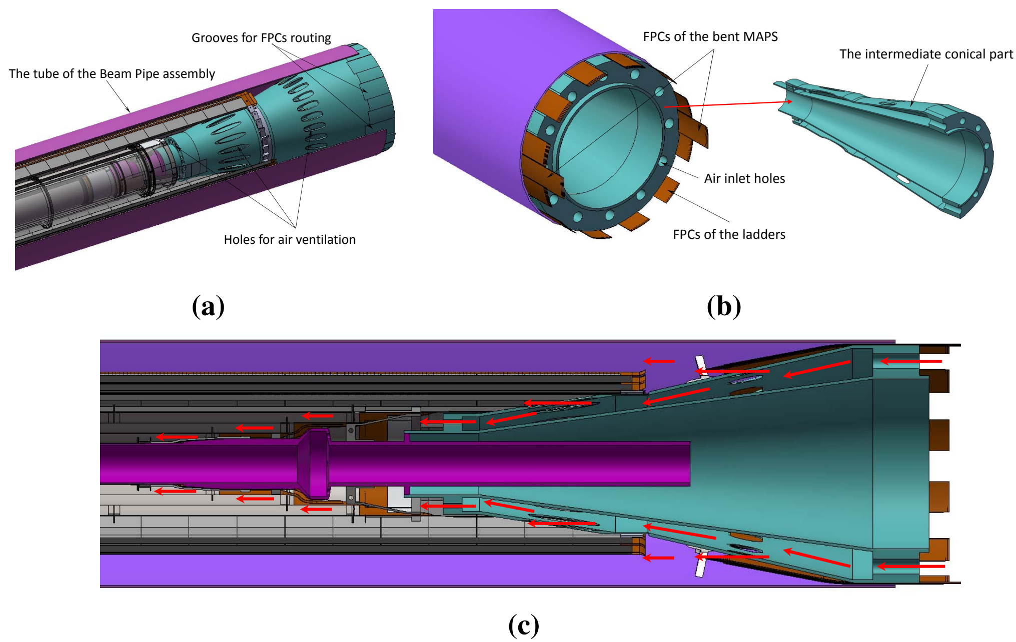

Figure 4.18: Air ventilation and cable routing of the VTX. (a) Air channel design with holes on global support structure for air distribution. Grooves on support structure is designed for FPCs routing. (b) The FPCs of the VTX routed out of the side of the beam pipe assembly, along with a cut view of the conical part. (c) Air channel, red arrows are air flow.

Figure 4.19: Half-dummy model of the vertex structure, featuring bent CPS cylinders, two short ladders, the intermediate conical part, and a transparent half-tube of the beam pipe assembly. FPCs from two adjacent ladders are twisted and converged by a guide frame fixed on the conical part, then routed along the groove and clamped by the outer tube.

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494 ## 4.4 Alignment and calibration

495 The VTX is designed to precisely measure the trajectory parameters of charged
496 particles close to the interaction point, enabling accurate reconstruction of decay vertices
497 from short-lived particles. Effective alignment is crucial for achieving optimal resolution
498 in the VTX.
499 The alignment strategy for the VTX faces significant challenges due to the implemen-
500 tation of the CVTX pixel sensors. The primary goals of this strategy include achieving
501 high spatial resolution, reducing uncertainties in impact parameters, and ensuring stable
502 alignment through efficient and automated processes.

503 ### 4.4.1 Initial mechanical alignment and reference alignment system

504 Initial mechanical alignment will be conducted during detector assembly, utilizing
505 precision optical survey instruments. Sensors will be aligned within a few micrometers
506 of design specifications, and optical method will confirm sensor curvature and cylindrical
507 positioning. Fiducial markers placed strategically on sensor modules and supporting
508 structures will facilitate optical tracking and ensure precise referencing. A stable external
509 alignment system, regularly monitored through X-ray or laser-based and optical survey
510 methods [12], will serve as the reference for continuous alignment.

511 ### 4.4.2 Track-based alignment

512 Mechanical alignment procedures during installation provide an initial level of pre-
513 cision in the VTX position. This precision is typically significantly worse than the desired
514 design hit resolution. Additional alignment (tracker-based alignment) is needed to account
515 for the position, orientation, and surface deformations of the CPSs. Charged particle tracks
516 obtained from collision data will facilitate iterative alignment corrections during both the
517 commissioning and operational phases. Global and local χ^2 minimization algorithms will
518 refine sensor positioning, improving accuracy and ensuring optimal detector performance.
519 In the current detector design, simulations have demonstrated the ideal performance
520 of the detector; however, in practical applications, it is necessary to consider the typical de-
521 formation mode as shown in Figure 4.20. The deformation includes elliptical deformation;
522 irregular, wavy distortion; circular distortion with uniform radial expansion.
523 These deformation modes can affect the detector's ability to determine the relative
524 positions of collision products as they pass through the VTX, ultimately influencing the
525 accuracy of the reconstructed collision parameters d_0 and z_0. The effect of each type of
526 deformations was studied in the simulation by modifying the position of hits according
527 to the three types of the deformation. In particular, for each simulated charged-particle
528 trajectory, the intersection with the deformed geometry was computed to determine the

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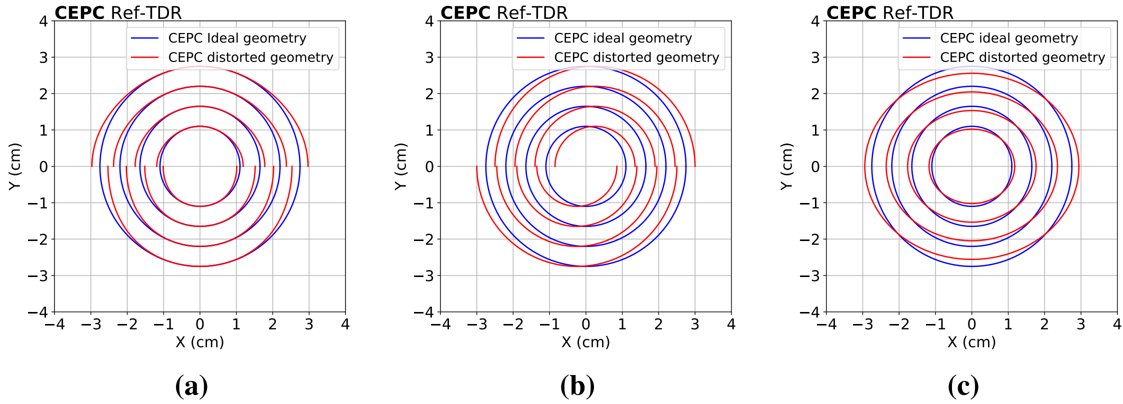

(a) **(b)** **(c)**

Figure 4.20: Illustration of the hit positions in the transverse plane with ideal vertex geometry and three deformed geometry. The amount of deformation is amplified with respect to the expected one for visualisation. (a) Elliptical deformation. The red distorted geometry is elongated horizontally, demonstrating a deformation primarily along the x-axis. (b) Illustration of the hit positions in the transverse plane for vertex geometry exhibiting irregular, wavy distortion. The distorted geometry has noticeable undulations, indicating non-uniform deformation affecting both the x and y directions unevenly. (c) Illustration of the hit positions in the transverse plane for vertex geometry showing a circular distortion with uniform radial expansion. The distorted geometry presents a uniformly increased radius, representing an isotropic deformation compared to the ideal geometry.

corresponding position of the hit in the local detector coordinates. The track-reconstruction algorithm was then executed assuming an ideal geometry to quantify the effect of the detector deformations in the absence of a detector alignment procedure.

4.4.3 Real-time monitoring

A laser-based online alignment monitoring system will perform real-time checks, verifying alignment accuracy continuously.

Due to the air cooling design in the VTX, it is important to monitor the movement of the CPSs. Inspired by the laser alignment system of CMS experiment [12], it is proposed to install laser alignment system to keep track of these movement. As shown in Figure 4.21, laser sources are placed on the service portions of CVTX layers; there are two sources on both sides of inner three layers and one source at the right side of the 4th layer. This system utilizes near-infrared laser beams (1050 nm) directed through the VTX to detect potential movements or deformations of the mechanical structure. Laser sources located in service areas are triggered to send pulsed infrared light to CVTXs of the VTX. By detecting their interaction with the silicon sensors, the system can infer movements of the CVTXs, ensuring that any deformations due to environmental factors like temperature, air flow, or magnetic fields are promptly identified.

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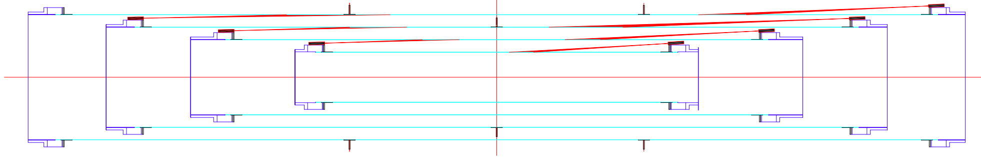

Figure 4.21: A laser-based online alignment monitoring system. Red lines diagonally connect with the aqua blue line (CVTX chip) are the lasers, and the laser sources are placed at both sides of the inner three layers and right side of the 4th layer to monitor the movement of each layer.

546 To validate the laser calibration system, signals generated by the laser were simulated
547 using Geant4 [13] within the CEPC Software (CEPCSW) framework. The laser was
548 emitted as a point source from the position (13 mm, 0, -85 mm), directed at an angle of
549 $\theta = 10°$ and $\phi = 0$. In the absence of a focusing system, a divergence of $\tan\alpha = 0.1$ was
550 established.

551 The resulting laser beam spot on the second layer of the VTX is presented in Fig-
552 ure 4.22.

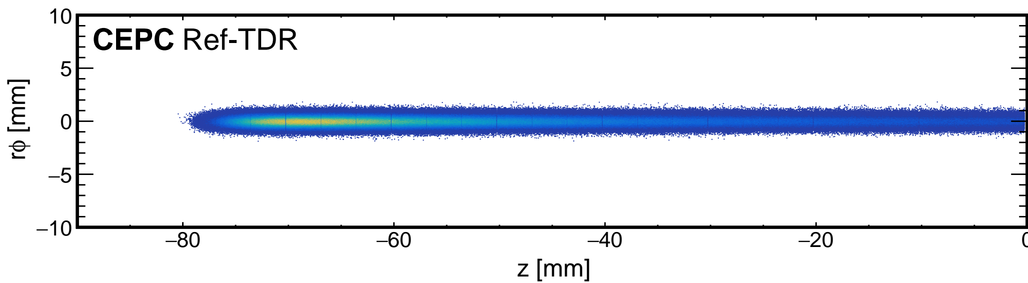

Figure 4.22: Laser beam spot on the second layer from (13 mm, 0, -85 mm) in cylindrical coordinate system, where the horizontal axis is the z-coordinate, and the vertical axis is the $r\phi$ coordinate. Each region is divided by a blank or lower rate than its neighbor means one sensor.

553 When simulating deformation by radially displacing the second layer outward by $d =$
554 $10\mu m$, the resulting distribution of signal IDs, The observed difference of 2 corresponds
555 to a distance of $50\mu m$, which is consistent with relationship $d/\tan\theta \approx 57\mu m$. These
556 findings indicate that the laser calibration system can infer positional changes through the
557 distribution of pixel IDs.

558 4.5 R&D efforts and results

559 To meet the stringent requirements of high spatial resolution, low material budget,
560 rapid readout speeds, and low power consumption, significant efforts have been directed
561 toward advancing CPS technologies, notably through the TaichuPix and JadePix projects.

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562 The JadePix project focuses on investigating CMOS pixel sensors for the CEPC VTX, 563 exploring low-power readout schemes. Concurrently, the TaichuPix project is dedicated 564 to developing CPS featuring advanced in-pixel electronics optimized for rapid readout. 565 These sensors utilize a data-driven, column-drain architecture specifically designed to 566 meet the fast response requirements imposed by the high collision rates at CEPC.

567 4.5.1 CIS JadePix series

568 The CEPC VTX imposes stringent requirements on spatial resolution. To achieve a 569 spatial resolution of 3 μm, the pixel size needs to be reduced to less than 20 μm, which is 570 limited by the feature size of integrated circuit technology. JadePix utilizes a specialized 571 180 nm CPS integrated circuit process optimized for ionizing radiation detection, which 572 is a modification and development based on the commercial CPS process. The pixel pitch 573 in this process typically ranges from 25 to 30 μm. Therefore, the key focus of JadePix's 574 development is on how to reduce the pixel size while also meeting the requirements for 575 low power consumption and fast time stamping.

576 4.5.1.1 Overview of JadePix development

577 The JadePix series of chips are primarily designed and optimized for high spatial 578 resolution, low power consumption, and fast time stamping. Since 2015, a total of 5 chips 579 have undergone continuous improvements which are shown in Table 4.12.

Table 4.12: Overview of JadePix development

Chip Name	Pixel Array	Pixel Pitch(μm^2)	Analog Front-end	Matrix Readout	Design Team
JadePix-1	128×192, 160×96	16×16, 33×33	Source follower	Rolling Shutter	IHEP
JadePix-2	96×112	22×22	Diff. Amp., CS Amp.	Rolling Shutter	IHEP
JadePix-3	512×192	16×23, 16×26	ALPIDE	Rolling Shutter	IHEP, CCNU, SDU, DLNU
JadePix-4	356×489	20×29	ALPIDE	AERD	CCNU, IHEP
JadePix-5	896×480	20×30	ALPIDE	AERD	IHEP, CCNU

580 JadePix-1[14] primarily focused on sensor optimization, comparing different geomet- 581 ric dimensions [15] and providing experimental evidence for the design of small charge 582 collection electrodes [16]. As shown in Figure 4.23 shows, the optimal spatial resolution 583 obtained through beam tests on an array of pixels with pixel pitches of $33 \times 33 \mu m^2$ pixel 584 array was 2.7μm [17].

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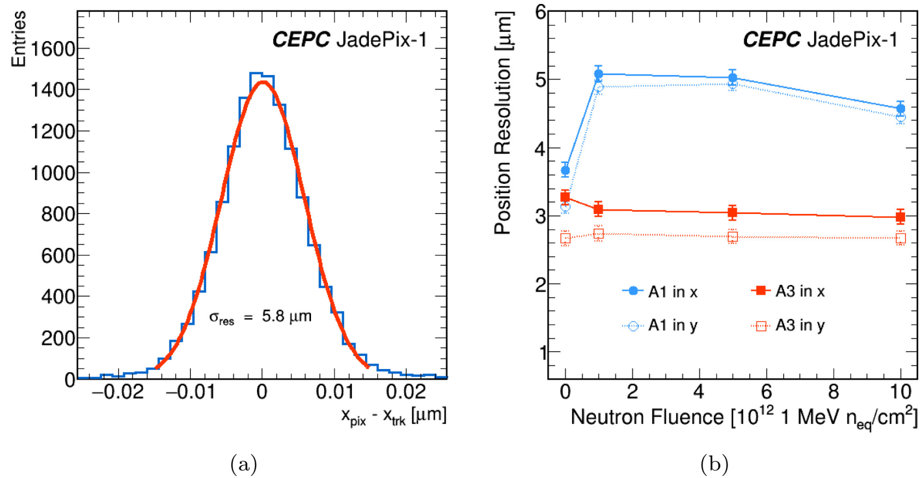

(a) (b)

Figure 4.23: (a) Residual distribution of JadePix-1 sensor in the x direction. (b) Position resolution for sensors with a small electrode (A1) and a large electrode (A3) before and after the neutron irradiation.

585 JadePix-2 investigated AC coupling and different analog front-end amplifiers [18],
586 attempting to optimize resolution, power consumption, and time stamping design using
587 a 180 nm process based on the Minimum Ionising MOS Active pixel sensor (MIMOSA)
588 architecture.
589 JadePix-3 utilized the low-power front-end amplifier of ALICE Pixel Detector (ALPIDE)[4],
590 combined with a Rolling Shutter readout architecture, achieving the smallest pixel design
591 among similar chips at $16 \times 23 \mu m^2$. Infrared laser tests showed spatial resolutions of 3.4
592 μm (X-direction) and 2.7 μm (Y-direction) [19]. A 5-layer beam telescope system was
593 constructed based on this chip, measuring spatial resolutions on a 5.8 GeV electron beam
594 of 5.2 μm (X-direction) and 4.6 μm (Y-direction) [20] . The cluster size from beam tests
595 was significantly larger than that from laser tests, adversely affecting the spatial resolution.
596 The highest efficiency reached 99% at the optimum threshold of 160 e^-.
597 JadePix-4 and JadePix-5 employed ALPIDE analog front-ends and AERD readout
598 architectures. The latter is an efficient sparse readout logic that can quickly read out the
599 addresses of hit pixels at very low power consumption and apply time stamps around the
600 periphery of the pixel array. The AERD readout architecture has been adopted not only
601 by various CPSs on the 180 nm process but also by the next-generation 65 nm Stitching
602 process.

603 4.5.2 CIS TaichuPix series

604 In order to address the high hit density of the CEPC, a CPS, named TaichuPix, has
605 been developed with the goal of high readout speed and high spatial resolution. TaichuPix-
606 1[7] and TaichuPix-2[8], are multi-project wafers, and TaichuPix-3 is a full-scale prototype
607 with an engineering run. The pixel matrix of TaichuPix-3 is 1024×512 with a pixel pitch

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608 of 25 μm, and a thickness of 150 μm. The proposed baseline VTX consists of three layers
609 of ladders, with double-sided mounted TaichuPix-3 sensors.

610 Each pixel of the TaichuPix-3 chip integrates a sensing diode, an analog front-end,
611 and a digital logical readout in each pixel. The analog front-end is designed based on the
612 ALPIDE[4] chip, which is developed for the upgrade of the ALICE ITS[3]. In order to
613 address the high hit rate of CEPC, the analog front-end of TaichuPix-3 has been specifically
614 optimized to ensure a quicker response. In addition, the digital logical readout includes a
615 hit storage register, logic for pixel mask, and test pulse configuration. The digital logical
616 readout follows the FE-I3[21] designed for the ATLAS pixel detector, but it has been
617 modified to adjust the pixel address generator and relocate the timestamp storage from
618 within the pixel to the end of the column. This modification was necessary due to pixel
619 size constraints. Furthermore, the double-column drain peripheral readout architecture of
620 the TaichuPix-3 chip employs an address encoder with a pull-up and pull-down network
621 matrix.

622 #### 4.5.2.1 TaichuPix specification and performance

623 **Specification** The design specifications of the TaichuPix-3 chip are summarized in Ta-
624 ble 4.13. The performance of the pixel sensor chip has been verified with a 4 GeV electron
625 beam at Deutsches Elektronen-Synchrotron (DESY) II. The intrinsic spatial resolution was
626 found to be 4.8μm and 4.5μm, and the detection efficiency reached 99%, which meet the
627 requirements.

Table 4.13: Design specifications of the TaichuPix-3 chip.

Specification	Index
Pixel size	$25 \times 25 \mu m^2$
Dimension	$15.9 \times 25.7 mm^2$
Techonology	CPS 180nm
Dead time	< 500ns
Power density	$< 200 mW \cdot cm^{-2}$
Max. Hit rate	$36 \times 10^6 cm^{-2} \cdot s^{-1}$

628 In order to verify the performance of TaichuPix, we conducted multiple beam tests at
629 DESY II[9].

630 **Spatial resolution** The spatial resolution of TaichuPix-3 chips are verified by electron
631 beam provided by DESY II. The intrinsic spatial resolution is derived from an unbiased
632 distribution of tracking residual, which excludes the Device Under Test (DUT). The
633 scattering angle is predicted using Highland formula.

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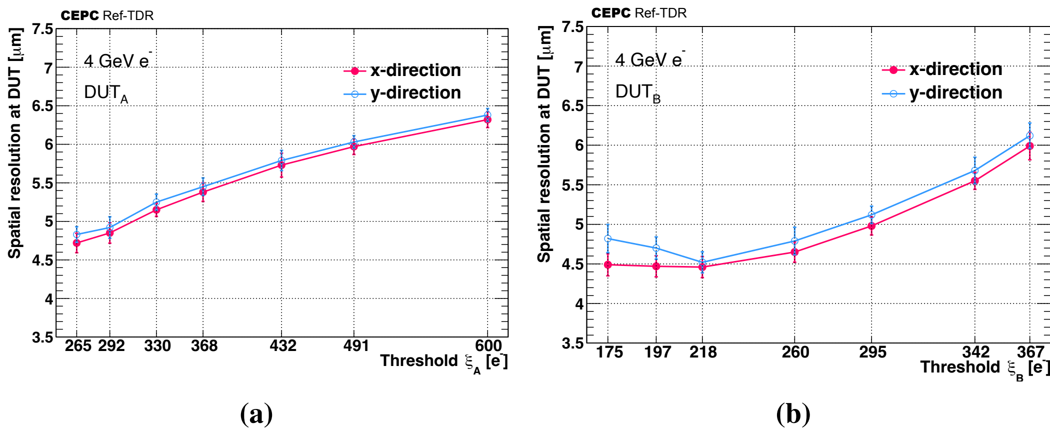
634 After considering the contribution from track resolution, the intrinsic spatial resolu-
635 tion for TaichuPix-3 chip is about 5μm. The spatial resolution as a function of threshold
636 is shown in Figure 4.24. In general, a higher threshold leads to a smaller cluster size,
637 which introduces a bias in estimating the actual hitting position and ultimately worsens
638 the intrinsic resolution. As depicted in Figure 4.24, for the two DUTs, increasing the
639 threshold results in a deterioration of the intrinsic resolution. $\mathrm{DUT_A}$ is fabricated using
640 the standard back-bias diode process, along with an extra deep N-layer mask, $\mathrm{DUT_B}$ is
641 fabricated without the extra deep N-layer, serving as a comparison to $\mathrm{DUT_A}$. However, for
642 $\mathrm{DUT_B}$, a worse resolution is also observed when the threshold is lower than $\xi_B = 218\ e^-$,
643 which can be attributed to the increased noise at the lower thresholds. The best resolution
644 for $\mathrm{DUT_A}$ is 4.72 ± 0.13 μm in the x-direction (shorter side of sensors), 4.83 ± 0.10 μm in
645 the y-direction (longer side of sensors) when $\xi_B = 265\ e^-$. For DUT_B, the best resolution
646 is 4.46 ± 0.13 μm int the x-direction, 4.52 ± 0.13 μm int the y-direction when $\xi_B = 218$
647 e^- .



(a) **(b)**

Figure 4.24: Spatial resolution as a function of threshold for DUT_A(a) and DUT_B(b) in two different directions: x-direction (shorter side of sensors) and y-direction (longer side of sensors). The error bars represent the total systematic uncertainty.

648 **Detection efficiency** The maximum detection efficiency is 99.76% for DUT_B and
649 99.68% for DUT_A. However, the efficiency of DUT_B drops significantly at high thresholds
650 compared to DUT_A. This can be explained by the difference in the process of the two
651 DUTs. Comparing to DUT_B, DUT_A has an additional low-dose N-layer, which enables a
652 larger depletion of the epitaxial layer and results in a larger charge collection area.

653 #### 4.5.2.2 Prototype of a planar CPS VTX

654 In striving to fulfill requirements in Table 4.13, a planar CPS VTX prototype (shown
655 as Figure 4.25) has been developed and evaluated[22] using an electron beam from DESY
656 II. The VTX prototype comprises three layers of concentric barrels positioned at radii

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657 of about 18.1 mm, 36.6 mm, and 59.9 mm . The detector module, also known as the
658 ladder, is a dual-sided structure that can place sensors on both sides. The ladder consists
659 of a pixel sensor chip, with up to ten on each side, a flexible printed circuit (FPC), and a
660 support structure made of carbon fiber. Two sensors are wire-bonded onto the end of the
661 FPC to cover the maximum area allowed by the collimator in DESY II, which measures
662 $2.5 \times 2.5 \mathrm{cm}^2$.

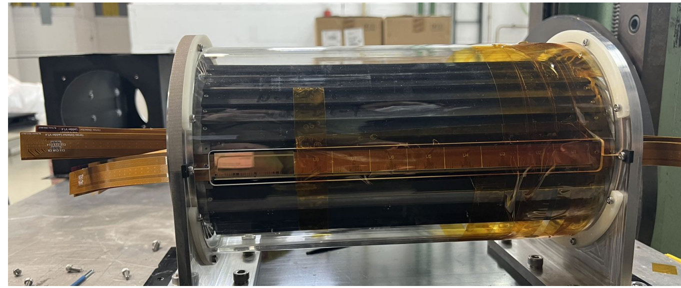

Figure 4.25: Planar VTX prototype with six instrumented double-sided ladders mounted for beam test. This was a full-size prototype with all carbon fiber mechanical ladders installed. Two Taichu chips were mounted on each side of the ladder. The beam was shot through the 6 double-sided ladders providing 12 measurement points.

663 **Spatial resolution and detection efficiency** The spatial resolution is derived from an
664 unbiased distribution of tracking residual obtained using the GBL track-fitting algorithm,
665 which excludes the DUT. The scattering angle is predicted using the Highland formula.
666 After alignment, the standard deviation for $\mathrm{DUT_A}$ and $\mathrm{DUT_B}$ at minimum threshold is
667 approximately 5.4 μm and 5.0 μm, respectively. Additionally, the spatial resolution of both
668 DUTs deteriorates as the threshold increases, and due to reduced charge-sharing effects on
669 $\mathrm{DUT_A}$, it exhibits poorer resolution compared to $\mathrm{DUT_B}$. At the lowest threshold setting,
670 the best spatial resolution achieved is 5.38 ± 0.12 μm in the u-direction and 5.52 ± 0.10
671 μm in the v-direction for $\mathrm{DUT_A}$, and 4.97 ± 0.08 μm in the u-direction and 5.21 ± 0.08 μm
672 in the v-direction for $\mathrm{DUT_B}$. To demonstrate the overall performance of the prototype, the
673 measured spatial resolution in this article involves the resolution of the reference tracks.

674 The efficiencies of $\mathrm{DUT_A}$ and $\mathrm{DUT_B}$ exhibit a decreasing trend as the threshold
675 increases. The best detection efficiency is 99.3% and 99.6% for $\mathrm{DUT_A}$ and $\mathrm{DUT_B}$,
676 respectively.

677 **Air cooling** The VTX is designed for very high spatial resolution. For air cooling, in
678 addition, to cool the detector to a certain temperature, one needs to consider the vibration
679 amplitude caused by the forced airflow, which should not affect the expected high spatial
680 resolution. This issue was noted and studied during the prototype R&D phase. The test
681 results indicate that the maximum amplitude of vibration of the ladder support is less than
682 1.9 μm even under a higher airflow rate of 4 m/s. In addition, during the beam test of the
683 VTX prototype, air cooling with a fan was employed, which decrease the chip temperature

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from 41°C to 25°C at a power dissipation of approximately $60\text{mW}/\text{cm}^2$, and no impact on the spatial resolution was observed. The strategy for addressing vibration in the baseline design of the VTX is similar to that of previous studies; prototyping the key structural elements and conducting related tests later on is the preferred method.

4.5.2.3 Prototype of a stitching CMOS detector

A stitched CPS has been developed. It was designed and fabricated in a 0.35 μm technology, which provides a thickness of 14 μm epitaxial layer and four metal layers for routing. Since there are triple wells in this process, only NMOS could be used in the pixel. The total pixel array is 644 rows and 3600 columns stitched by a basic pixel array of 92 rows and 600 columns. It works in a rolling shutter readout mode. As a full functional prototype, it integrated column-level discriminator, on-chip zero suppression, interface circuits such as bias DAC, analog buffers, Inter-Integrated Circuit (I2C) control, Phase-Locked Loop (PLL), Low-Voltage Differential Signaling (LVDS), Low Dropout Regulator (LDO), etc. The total area is up to $11 \times 11\text{cm}^2$. In order to study charge collection efficiency and charge sharing, each basic pixel array has six submatrices with different pixel sizes and diode arrangements. The prototype chip is being tested and its development could provide experience in developing stitched sensor with advanced technology.

The radius bending test We have conducted studies on VTX with stitching technology. Dummy wafers have been used for bending tests, prototype manufacturing, and, meanwhile, small-area CPS were used to study the impacts of bending on the chip performance.

Silicon is a brittle material. It undergoes an irreversible brittle fracture when the stress exceeds its compressive strength. We thinned the wafers to thicknesses of 30 μm, 40 μm, and 50 μm, and successfully completed bending tests with and without a film, as well as fatigue tests for different radii in various sequences, . Currently, the bending limit test has successfully achieved a minimum bending radius of 12 mm , as shown in Figure 4.26a. Additionally, we performed over 20 times of bending-recovery-bending tests on the same wafer. The prototype in Figure 4.26b has been placed for over 2 years without damage.

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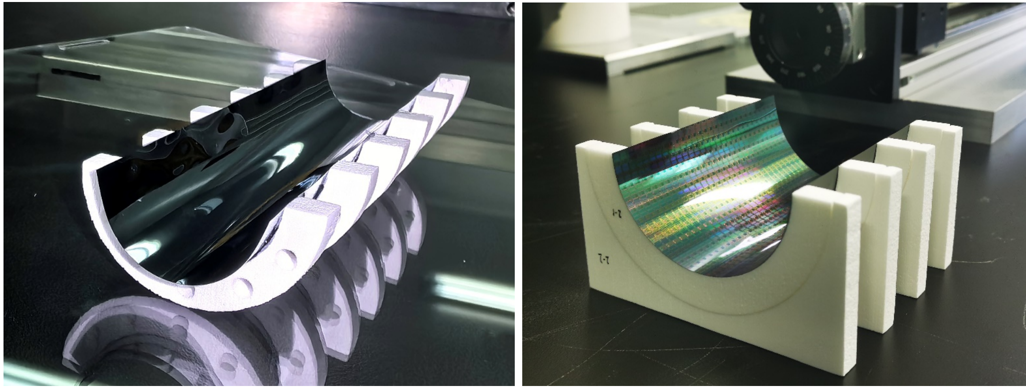

(a) (b)

Figure 4.26: Prototype for bending test. (a) Testing of bending limit, the minimum bending radius of 12 mm has achieved. (b) Determining the damage-free duration of the bending wafer, this prototype placed for over 2 years without damage.

4.6 Performance

4.6.1 Hit number and efficiency

There are two types of dead zones: one is due to assembling pixel sensors to ladders or semi-cylinders, which in turn to form detector barrels; another is due to functional blocks in the sensor design, such as data interfaces, power switches, etc, as shown in Figure 4.11. No hits will be produced when charged particles pass through these regions. During layout optimization, different deflections in the ϕ direction have been applied to different layers to minimize the loss of the number of hits from a single trajectory. Furthermore, the width of the PVTX has been increased to avoid empty sensor regions in the phi direction. However, when the width becomes too large, it could lead to a situation where both adjacent ladders at the same layer have signals, which increases the material volume of the overlapping area. To assess the reasonableness of the dead zones and overlaps, simulations using chargedgeantino were performed to obtain the number of hits in the VTX.

A quantity, called Tracklet Efficiency, is defined as the ratio of the sum of hits left in the VTX by reconstructable trajectories to the total number of expected hits by all simulated tracks. It can be expressed mathematically as:

$$\text{Tracklet Efficiency} = \frac{\sum_i^N \text{Hits}i^{(\geq 4)}}{N \times L} \tag{4.1}$$

where $\text{Hits}i^{(\geq 4)}$ represents the number of hits left by the i-th chargedgeantino trajectory passing through the VTX with a hit count no less than four, N is the total number of simulated events, and L is the expected number of layers that the VTX is expected to be traversed (six in this case). As shown in Figure 4.27a, for a chargedgeantino with a momentum of 20 GeV, the particle's tracklet efficiency is 99.635% at $\theta = 20°$. When

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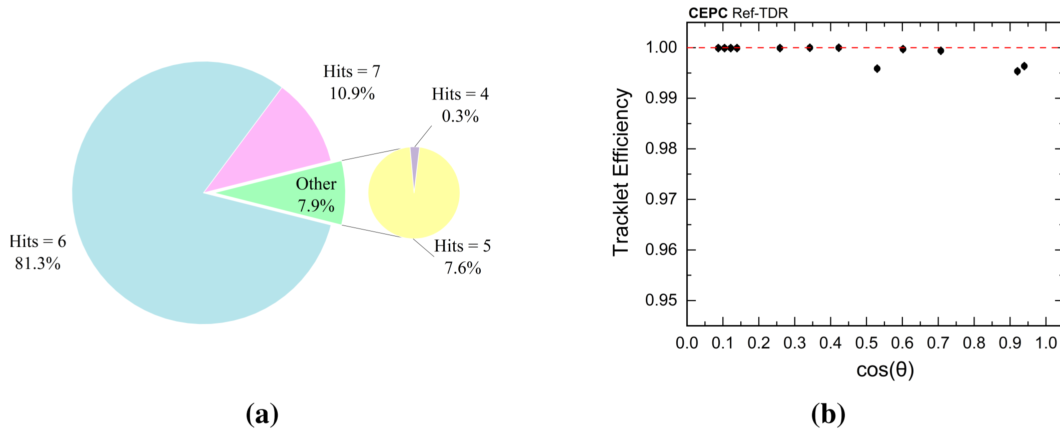
each track is required to pass through the first layer of the VTX, the tracklet efficiency is 96.75%.

Figure 4.27b illustrates the tracklet efficiency and its errors for 20 GeV chargedgeantino particles passing through the VTX at different polar angles. The tracklet efficiency is consistently close to 100% in all cases.



(a) **(b)**

Figure 4.27: Performance on tracking. (a) Each track includes the percentage of hits when the number of hits is 4, 5, 6, and 7, based on the simulation of 10,000 chargedgeantino particles by the VTX at $\theta = 20°$ and 20 GeV. (b) Tracklet efficiency and its errors for 10000 chargedgeantino particles at 20 GeV, originating from collision vertex (0, 0, 0) and passing through the VTX at different polar angles.

4.6.2 Resolution

The VTX design described in Section 4.1.2 will serve as the the baseline schemes in the following sections. Additionally, a backup scheme is proposed whose detailed information is shown in Section 4.7. Simulations were performed using CEPCSW in conjunction with the remaining sub-detectors of the tracking system, with μ^- as the outgoing particles and a conservative single-point resolution of 5µm assumed for the pixel sensor. Through simulation results, as shown in Figure 4.28, the baseline scheme demonstrates its superior d_0 resolution performance among the two schemes.

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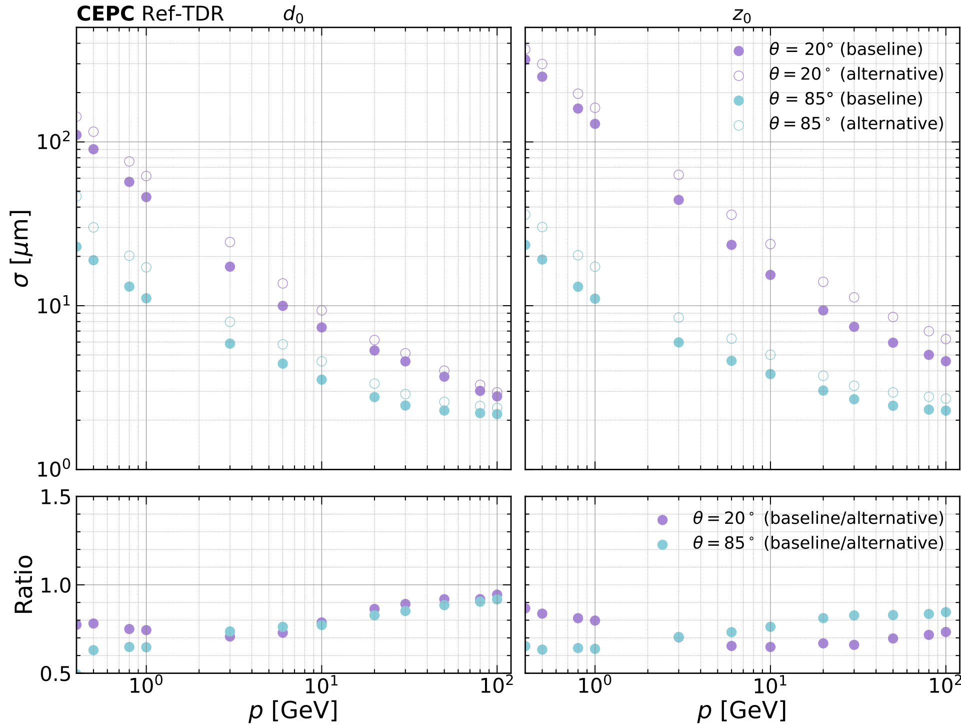

Figure 4.28: According to the full simulation in CEPCSW framework, the resolution of impact parameters d_0 and z_0 for two schemes is simulated using μ^- particles at different momenta and emission angles. Due to its more compact design and lower material budget, the baseline scheme achieves a resolution 10% ∼ 40% higher than the alternative scheme in the range of 0.4 GeV ∼ 100 GeV .

745 As previously demonstrated during the optimization, the adoption of the low-mass
746 stitching technique allows the baseline scheme of the VTX to achieve good resolution
747 of the impact parameter d_0 of tracks even at high momentum, as well as improved d_0
748 resolution at low momentum. In fact, not only the d_0 resolution, but the baseline scheme
749 also exhibits excellent performance for the resolution of impact parameter z_0, as shown
750 in Figure 4.28. The simulation results demonstrate that the trend of the z_0 resolution
751 as a function of momentum is analogous to that of d_0, with only minor discrepancies
752 observed. This observation aligns with the utilization of pixel detectors in the VTX,
753 where the precision of z position measurements is equivalent to that of $r\phi$ measurements.
754 Such findings indicate that when comparing different configurations, focusing exclusively
755 on d_0 resolution is a valid approach that also minimizes the workload. The results
756 indicate that an increase in momentum correlates with an enhancement in resolution. This
757 improvement can be attributed to the pronounced effects of multiple scattering in material
758 at low momentum. Similarly, as the polar angle θ approaches to the beam line, the amount
759 of material traversed by charged tracks increases proportionally to $\sim 1/\sin\theta$, which further
760 amplifies the multiple scattering effects and leads to a degradation in resolution.

761 Similarly, the z_0 resolution of the backup scheme in Figure 4.28 is also slightly worse
762 than that of the baseline scheme.

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763 ### 4.6.3 Performance under sensor failure scenarios

764 Some VTX units may fail to operate normally or even become damaged in the future
765 actual operation for various reasons. When such situations arise, the performance of the
766 VTX is bound to decline. However, to ensure the smooth progress of physical analysis, the
767 design of the VTX must guarantee that even in the worst-case scenarios, the performance
768 does not experience a dramatic drop.

769 To this end, in the simulation process, we assume that a certain layer of the VTX does
770 not produce signals to estimate performance under this special circumstance. As shown in
771 Figure 4.29, the estimated performance for normal conditions and for damages from the
772 first to the sixth layers is presented. It is evident that the current VTX scheme can ensure
773 that, in the case of a single layer loss, the performance decrease does not exceed 25%, with
774 the loss of the first layer having the most significant impact. For cases of individual unit
775 damage, the overall performance can be viewed as a weighted average of the probabilities
776 of the intact and damaged sections. Considering the very low likelihood of two layers
777 being damaged simultaneously, it can be reasonably anticipated that the overall impact
778 will be minimal.

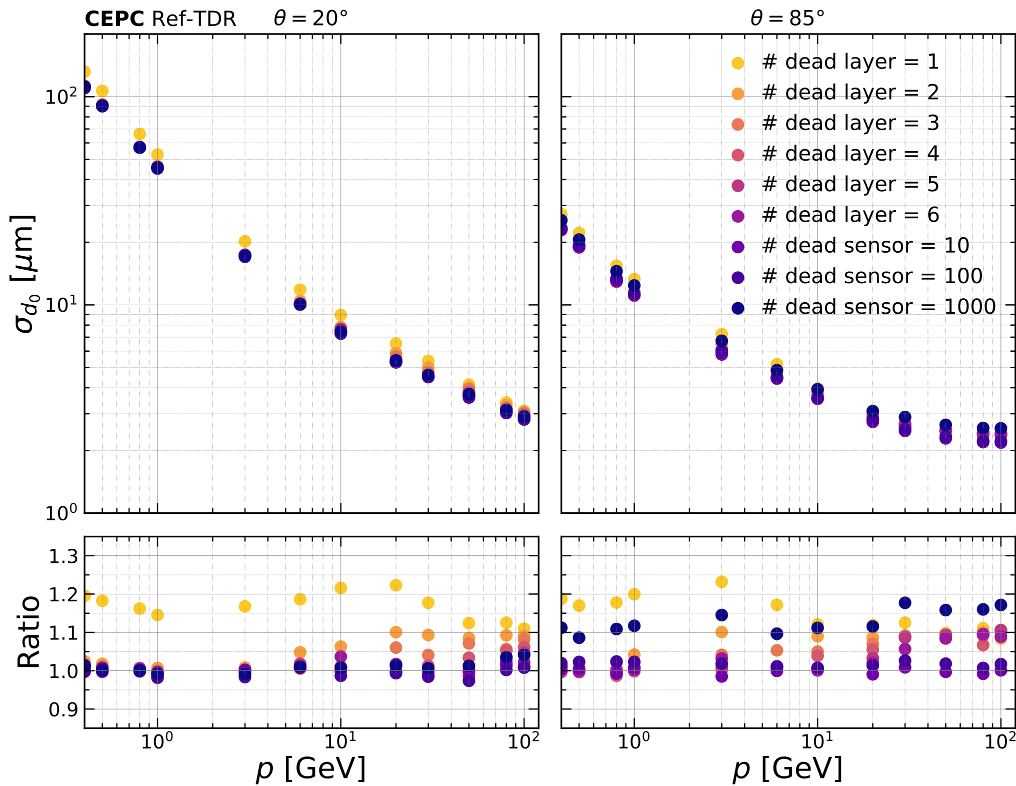

Figure 4.29: Resolution of the impact parameter d_0 for tracks obtained by the baseline VTX under different dead layer/sensor conditions, including complete layer failures and 10, 100, 1000 sensor failures (RSUs in CVTX, Taichu chips in PVTX), with ratios to the baseline scheme.

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779
4.6.4 Performance with beam background

780 In addition, due to the proximity of the VTX to the beam pipe, it is crucial to evaluate
781 the effects of beam background on its performance during the design phase.

782 This approach incorporates true simulated backgrounds into the signal, as outlined
783 in Section ??. This method facilitates a comparison of the d_0 resolution before and after
784 background incorporation, as illustrated in Figure 4.30, where no discernible effects are
785 observed. Thus, it is evident that provided the levels of beam background remain consistent
786 with those obtained in current simulation studies, the VTX is poised to deliver outstanding
787 performance. Nonetheless, it should be noted that the inclusion of beam background may
788 lead to increased processing time for track reconstruction. Therefore, subsequent efforts
789 should focus on algorithm optimization and enhanced computational efficiency to mitigate
790 this increase.

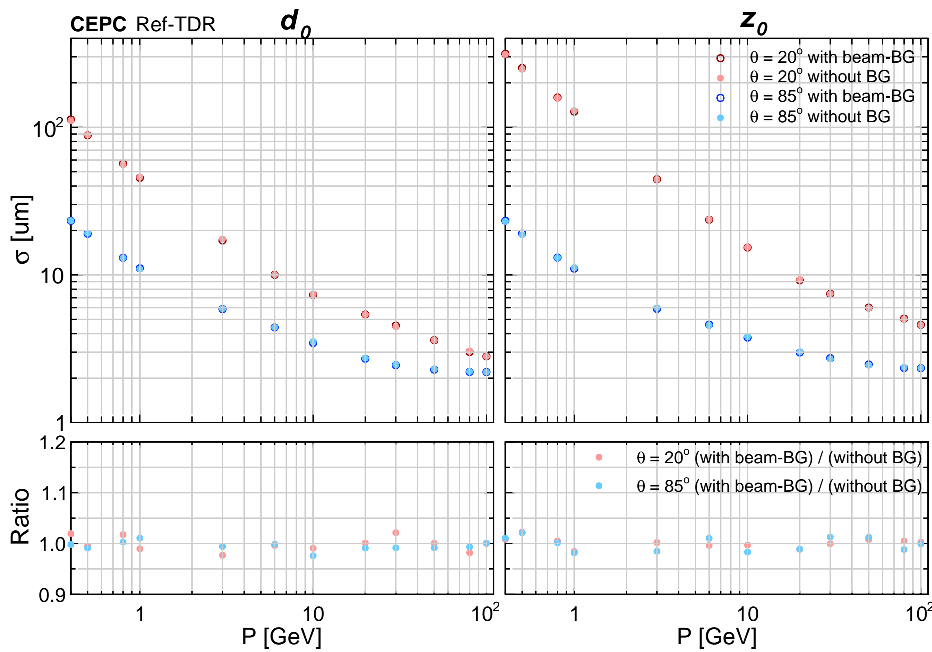

Figure 4.30: Comparison of resolution of the impact parameter d_0 and z_0 of tracks between clean single muon signal (without BG) and mixing beam background (with beam-BG) at polar angle of 85° and 20°.

791
4.7 Alternative Solutions

792 Another VTX design using three layers of double-sided ladders with planar CPSs
793 has also been considered, as shown in Figure 4.31. The design represents a conventional
794 but well-established option. It serves as an alternative fallback solution if the baseline
795 design with curved technology encounters unforeseen challenges. However, it introduces

additional material and complexity due to the need for mechanical support, overlaps between ladders, and potentially thicker support elements.

Detailed parameters for backup VTX layout is provided in Table 4.14. The intrinsic single-point resolution of the chip is derived from the TaichuPix-3 beam tests, with a conservative resolution of 5 µm.

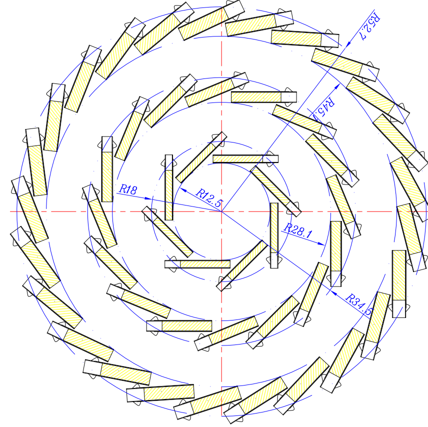

Figure 4.31: Sectional view of the VTX backup layout whose units are millimeters. All the six layers (three layers of double sided ladders) are composed of planar CPSs. PVTX 1-2, PVTX 3-4, and PVTX 5-6 include 8, 16, and 25 ladders, respectively.

Table 4.14: Geometric configuration parameters for the backup scheme. Radius and length, and material budget of the support structure for each layer of the VTX, as well as the height of ladder corresponding to PVTX.

PVTX X	radius [mm]	length [mm]	height [mm]	support thickness [μm]
PVTX 1-2	12.46	260.0	1.8	300
PVTX 3-4	27.89	494.0	2.6	300
PVTX 5-6	43.79	749.0	3.3	300

4.8 Summary and future plan

The CPS-based detector layout consists of six cylindrical layers of pixel sensors with pixel pitches in the order of 25 µm × 25 µm, enabling hit resolutions better than 5 µm. The inner four layers are bent CPS cylinders. The outer two layers are based on double-side ladder technology.

Initial VTX prototypes using double-side ladder technology have demonstrated a spatial resolution better than 5 µm with air cooling in DESY testbeam. Geant4-based simulations, demonstrate that the baseline design of VTX can achieve the target impact parameter resolution.

Future R&D priorities include:

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1. Development of wafer-scale stitching CPSs.
    - Initially, the stitching chip will leverage mature 180 nm technology (e.g., TowerJazz) to keep R&D risks and costs within reasonable bounds. The pixel cell and matrix design will build on the proven architecture of previous prototype chips, with focused efforts on stitching-related challenges and ensuring basic cell designs draw from verified experience.
    - The second-generation stitching chip will transition to 65 nm/55 nm technology, with potential candidates including TPSCo's 65 nm technology and domestic HLMC's 55 nm technology. Synergy with sensor development for future LHC upgrades is anticipated.
2. Ultra-thin mechanical supports and low-mass integration techniques.
    - The plan begins with exploring the construction of a mock-up featuring dummy heaters for thermal performance testing. Results will also validate thermal simulation models.
3. Construction of a full-scale VTX prototype to address challenges in mechanical precision, cooling performance, and system-level integration.

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894 # Glossary

895 **AERD** Address-Encoder and Reset-Decoder 29, 30
896 **ALICE** A Large Ion Collider Experiment 10, 12, 14, 31
897 **ALPIDE** ALICE Pixel Detector 12, 14, 29–31

898 **BX** Bunch Crossing 11

899 **CEPC** Circular Electron Positron Collider 1, 2, 6, 9, 12, 29–31
900 **CEPCSW** CEPC Software 28, 36
901 **CERN** European Organization for Nuclear Research 9
902 **CFRP** Carbon Fiber Reinforced Polymer 6, 19–21
903 **CMOS** Complementary Metal Oxide Semiconductor 10, 29
904 **CPS** CMOS Pixel Sensors 2
905 **CVTX** Curved Vertex Layer 3–6, 17, 20, 26–28, 38

906 **DAC** Digital-to-Analog Converter 17, 34
907 **Dcols** Double Columns 15
908 **DESY** Deutsches Elektronen-Synchrotron 31–33
909 **DUT** Device Under Test 31–33

910 **FIFO** First In First Out 16
911 **FPC** Flexible Printed Circuit 6, 7, 19–22, 24, 25, 33

912 **I2C** Inter-Integrated Circuit 34
913 **IBIAS** bias current 17
914 **IP** Interaction Point 1
915 **ITS** Inner Tracker System 9, 10, 12, 14, 31

916 **LDO** Low Dropout Regulator 34
917 **LRB** Left-end Readout Block 5, 6, 12, 13, 16–18
918 **LVDS** Low-Voltage Differential Signaling 34

919 **MAPS** Monolithic Active Pixel Sensor 9, 10
920 **MIMOSA** Minimum Ionising MOS Active pixel sensor 30
921 **MOSS** MOnolithic Stitched Sensor 12
922 **MOST** MOnolithic Stitched sensor with Timing 12

923 **OCT** On-Chip Test 16

924 **PLL** Phase-Locked Loop 34
925 **PVTX** Planar Vertex Layer 3, 4, 6, 35, 38, 40

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926 **RHIC** Relativistic Heavy Ion Collider 9

927 **RPB** Right-end Power Block 5, 6, 12

928 **RSU** Repeated Sensor Unit 2, 4, 5, 8, 12, 13, 16–18, 38

929 **STAR** Solenoidal Tracker at RHIC 9

930 **TPSCo** Tower Partners Semiconductor Co. 2, 10, 17, 41

931 **VTX** Vertex Detector 1–10, 12, 18–29, 31–41