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CEPC Reference Detector

Technical Design Report

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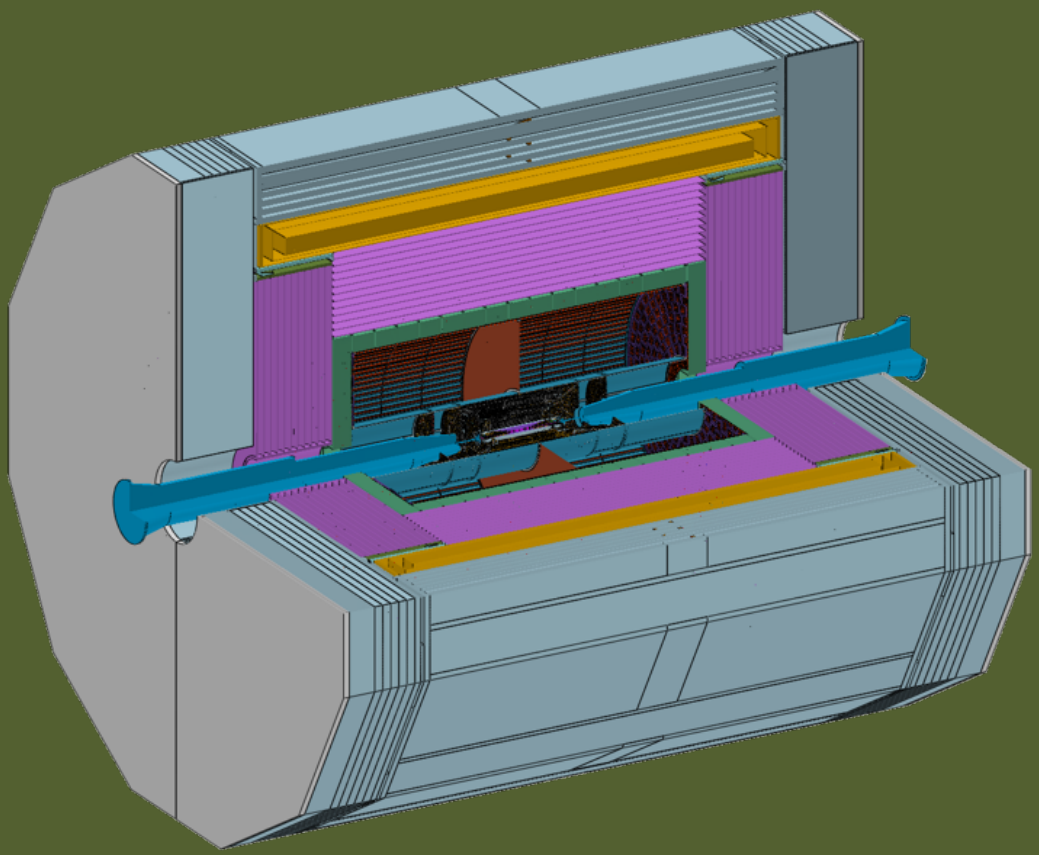

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Contents

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Chapter 4 Vertex Detector

The Circular Electron Positron Collider (CEPC) vertex detector (VTX) is a crucial component of the tracking system, designed to deliver exceptional spatial resolution for precise vertexing and flavor tagging.

[wm: Add a paragraph to introduce previous R&D briefly, introducing TaichuPix etc.]

This chapter is organised as: the overall design considerations are outlined in Section 4.1, followed by the design on detector layout along with estimates of the background rate and radiation dose in this layout. Detailed sensor and readout technologies are presented in Section 4.2, Mechanics and cooling design as well as service design are presented in Section 4.3. R&D of key technology are presented in Section 4.5 to support the baseline design of the CEPC vertex detector. The detailed simulation of expected detector performance and detector alignment strategy are presented in Section 4.6. Section 4.7 introduces an alternative backup layout, and Section 4.8 summarizes the design and outlines future plans.

4.1 Detector overall design

4.1.1 Vertex detector design specification

The CEPC physics program relies on precise identification of heavy-flavor (b and c) quarks and τ leptons, necessitating accurate track parameter measurements near the interaction point (IP) to reconstruct displaced decay vertices of short-lived particles. *[wm: Quantified physics requirements needed here. It may be a few sentences or refer to somewhere.]* This requires a vertex detector with a material budget of $\leq 0.15\%\, X_0$ per layer and a spatial resolution of < 5 μm. *[wm: The two numbers dependent on number of layers. Clarify it.] The polar angle coverage is with* $|\cos\theta| < 0.99$ *by ...* The requirements are summarized in Table 4.1.

Table 4.1: Physics Requirements

Parameter	Baseline Requirement
Spatial Resolution	< 5 μm
Material Budget per Layer	$\leq 0.15\%\, X_0$
Angular Coverage	$\|\cos\theta\| < 0.99$

The CEPC vertex detector is built as six concentric cylindrical pixel layers stretching from a radius of 11 mm to 40 mm around the beam pipe. In the inner four layers, ultra-thin stitched *CMOS pixel sensors (CPS)* are thinned to 40 μm and gently bent to the required

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curvature, so that each layer forms a seamless half-cylinder. Conventional ladder designs with CPSs mounted on both sides are used for layers 5 and 6. *The pixel pitches are determined according to the requirement of 5 μm single-point resolution* All layers share a common 65 nm Complementary Metal Oxide Semiconductor (CMOS) front-end that integrates amplification, discrimination and zero suppression in-pixel, achieving a time stamp precision of 100 ns. The 100 ns readout window for the CEPC vertex detector is chosen to balance high timing precision for resolving collision events at high frequencies (especially in Z mode) with low power consumption and efficient data processing. A stitched Repeated Sensor Unit (RSU) is the building block of the curved chips, maximising wafer utilisation. Average power density is required to be under 40 $\mathrm{mW/cm^2}$*, the limitation of air-cooling.*

The CEPC is designed to operate at high collision frequencies, accommodating multiple collision modes. In its initial 10 years, the plan includes running at 240 GeV in the Higgs boson factory mode and at 90 GeV in the Z boson factory mode. Specifically, the collision frequency for the Higgs factory is approximately 1.7 MHz, while the Z boson factory mode operates at about 14.5 MHz during the initial low-luminosity phase and increases to 43 MHz *[wm: also in 10 years?]* in the later high-luminosity phase. These frequencies pose challenges in maintaining low power consumption at higher operational frequencies - a critical aspect of the vertex detector chip development for this project.

To meet the requirements of low power consumption, low material budget, and high spatial resolution as listed in Table 4.1, the *CMOS based pixel sensor*, a kind of Monolithic Active Pixel Sensor (MAPS), is adopted as the sensor type for the vertex detector. Preliminary simulations and tests based on the first CEPC vertex detector prototype indicate that the power consumption *of sensors with* 180 nm *technology running* at low-luminosity Z mode is larger than 60 $\mathrm{mW/cm^2}$. This level of power dissipation exceeds the air cooling capacity of the vertex detector, resulting in sensor temperatures surpassing the operational upper limit of 30 °C, which may introduce higher noise levels and accelerate the aging of sensors, mechanical components, and other associated systems. To tackle this critical issue, the vertex detector has chosen TPSco's 65 nm Cmos Image Sensor (CIS) technology as its baseline. Additionally, HLMC's 55 nm CIS technology is being explored as a potential alternative. *[wm: full names of TPSco and HLMC?]* The choice significantly reduces power consumption and also offers the potential for smaller pixel sizes, thereby improving spatial resolution. The design parameters are summarized in Table 4.2.

4.1.2 Detector layout

The layout of the VTX is shown in Figure 4.1 and Figure 4.2. It consists of six layers, spreading in radius from 11 mm to about 40 mm, and the polar angle coverage is with

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Table 4.2: Vertex Detector Design Parameters

Parameter	Design
Spatial Resolution	~ 5 μm
Material Budget per Layer	$\leq 0.15\%\ X_0$
Power Consumption	$< 40\text{mW/cm}^2$ (air cooling requirement)
Time stamp precision	$\pm$ 100 ns
Fluence	$\sim 2 \times 10^{14}\text{Neq/cm}^2$ (for first 10 years)
Operation Temperature	$\sim 5°\text{C}$ to $30°\text{C}$
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

$|\cos\theta| < 0.99$.

The inner four layers are made of CMOS stitching sensors and named curved vertex layers (CVTXs). The sensors are thinned to a certain thickness so that each of them can be bent to form a half-cylinder and a pair of them form a whole cylinder. Each CVTX is composed of one or two pairs of sensors, of which the dimensions and the number of pairs are determined by the radial position.

The outer two layers make use of traditional CMOS sensors and are named planar vertex layers (PVTXs). The sensors are fixed on both sides of a support structure to form a ladder. The ladders are arranged circularly to form a rough barrel, seeing Figure 4.2.

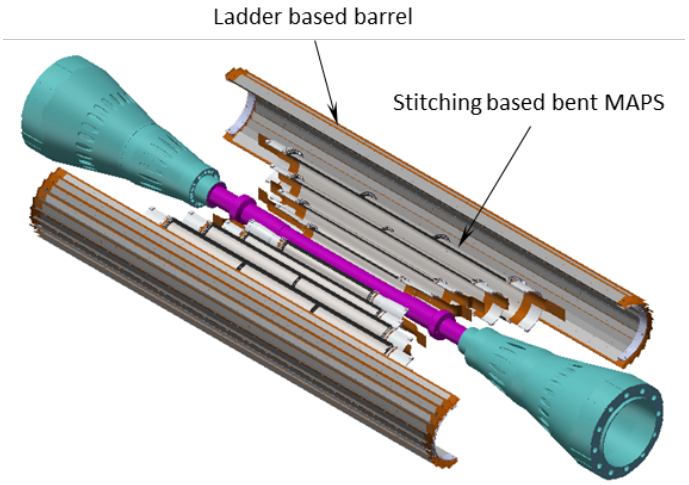

Figure 4.1: Diagram of the vertex detector. The first four layers are designed as single-layer structures (full-model cylindrical structure) using bent stitched sensors, while the last two layers are designed as double-layer structures (ladder structure) utilizing planar CIS.

Stitching design For sensors constituting the curved layer of the vertex detector, the *width* of a bent sensor along the ϕ-direction corresponds to the arc length of a semicircle

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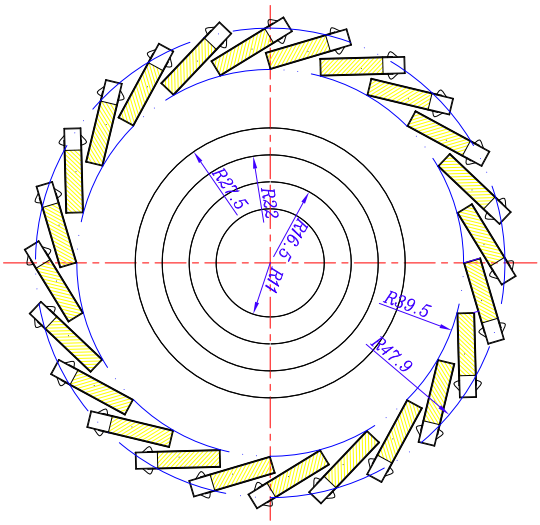

Figure 4.2: Sectional view of the Vertex Detector (VTX) layout. The inner four layers are bent CIS with semi-cylindrical structure and for the 5th and 6th layers are double-layer planar CISs with ladder desgin.

Table 4.3: Geometric configuration parameters. Radius and length, and material budget of the support structure for each layer of the VTX, as well as the arc length corresponding to Curved Vertex Layer (CVTX) and the height of ladder corresponding to Planar Vertex Layer (PVTX).

CVTX/ PVTX X	radius mm	length mm	arc length mm	height mm	support thickness μm
CVTX 1	11.1	161.4	69.1	-	45
CVTX 2	16.6	242.2	103.7	-	32
CVTX 3	22.1	323.0	138.2	-	31
CVTX 4	27.6	403.8	172.8	-	29
PVTX 5-6	39.5	682.0	-	3.3	300

with a specific radius determined by the CVTX. To achieve the required polar angle coverage , the length of the sensor's sensitive region along the beam direction (z-direction) is also precisely defined. Due to limitations in current semiconductor manufacturing technology and processes, the sensors are arranged on 300 mm wafers, and *the dimensions* of a complete sensor is constrained by the wafer size. As a result, the number of sensors used in the z-direction varies for different CVTXs. Based on the radius and length requirements of the CVTX, a 17.277 $\times$ 20.000 mm^2 RSU is defined as the basic unit (see Section 4.2.2.1). Three stitched sensors of different sizes are designed on a wafer, as shown in the type A/B/C in Figure 4.3. Each type of sensor comprises modules arranged in multiple rows, where a module integrates several RSUs along with I/O pads and power supply positioned at both the left and right edges.

CVTX 1 and CVTX 3 share the type C sensor, with CVTX 1 containing the two type C sensors of the two modules, as depicted in Figure 4.4. CVTX 2 utilizes the type

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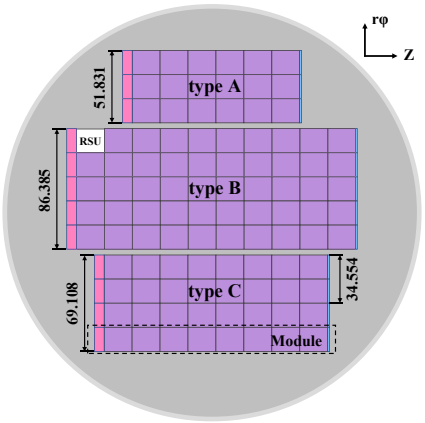

Figure 4.3: The arrangement of stitching frames on a 300 mm wafer. The purple part represents the RSUs, the pink represents the Left-end Readout Block (LRB), and the blue represents the Right-end Power Block (RPB). The short-dashed line area represents a module consisting of several RSUs, one LRB, and one RPB. To meet the requirements of each layer of the vertex detector, the type A/B/C sensors are designed with different lengths and widths. The type A and B sensors are used to make one of the sensors for CVTX 2 and CVTX 4, respectively. The full type C sensor can be used for one of the sensors for CVTX 3. The type C sensor can be divided into four modules along the vertical direction. Using two modules of the type C sensor can make a sensor for CVTX 1.

A sensor, consisting of two type A sensors (each with three modules) arranged along the z-direction and two arranged along ϕ-direction. CVTX 3 employs the type C sensor, consisting of two type C sensors (each with four modules) arranged along the z-direction and two arranged along the ϕ-direction. CVTX 4 adopts the type B sensor, consisting of two type B sensors (each with five modules) arranged along the z-direction and two arranged along the ϕ-direction. CVTXs 2, 3, and 4 are spliced in the z-direction, resulting in a 0.5 mm splicing seam at $z = 0$.

Considering the mechanical dead zones in the ϕ direction and the dead zones in the width of the whole sensor, the CVTX 1, CVTX 2, CVTX 3, and CVTX 4 of the vertex detector are rotated by an angle when mounted. This angular adjustment minimizes the occurrence of multiple dead zones at the same angle in the $r\phi$ plane. Each semi-cylindrical structure is supported by a material with a specific thickness (see Section 4.3.1.4).

Double-sided Ladders The outer layers (5 and 6) of the CEPC vertex detector do not use stitching technology due to wafer size limitations, as these layers require larger sensors that exceed the practical stitching capabilities on standard 300 mm wafers, leading to the adoption of conventional double-layer planar CIS ladders for simpler integration at larger radii.

The fifth and sixth layers are constructed using planar CISs, each sized 15.9 × 25.7 mm^2 with a thickness of 40 μm. The back of the chip is *glued* to the Flexible Printed Circuit (FPC) that conducts power and transmits the signal. The chip is treated as a unit,

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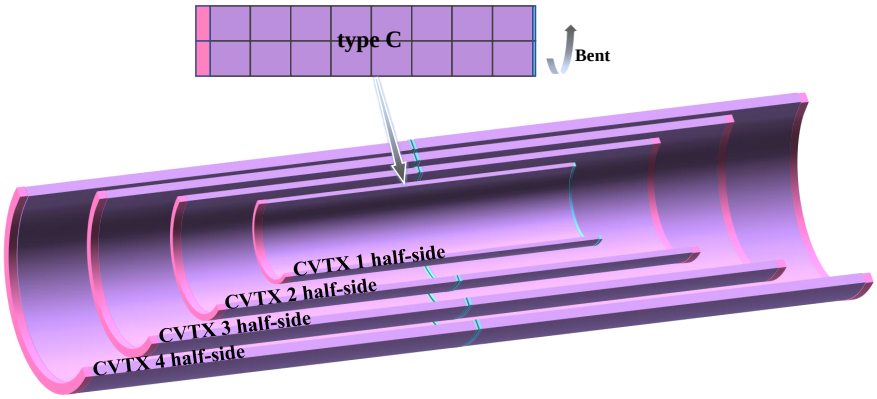

Figure 4.4: The type C sensor is diced into a sensor containing two modules, which are bent along the ϕ-direction to form a semi-cylindrical structure for the CVTX 1. Two type A sensors (each with three modules), bent along the ϕ-direction and arranged along the z-direction, create the semi-cylindrical structure for CVTX 2, with LRBs at both ends and a maximum 0.5 mm seam between RPBs (shown in gray). CVTX 3 and CVTX 4 are constructed similarly to CVTX 2.

and the dead zones of the adhesive are arranged from the $-z/2$ region to the $z/2$ region at intervals of 0.1 mm. The FPC is glued to both sides of the support structure Carbon Fiber Reinforced Polymer (CFRP) to create a complete ladder cell as shown in Figure 4.5 and Figure 4.6, where the effective thickness of the support structure CFRP hollow pipe is 300 µm, as described in the Section 4.3.1.3. The geometric center of the ladder unit rotates around the origin at a specific radius position from the $\phi = 0$ position, while maintaining the height of the wire, forming a barrel structure known as PVTX 5-6 to ensure that no particles leak out in the ϕ-direction. A total of 24 ladder structures are utilized in the fifth and sixth layers.

Material budget Figure 4.7 shows the variation of the average material budget X_0 with θ in the ϕ-direction. Table 4.4 lists the material budget of each layer for the VTX at $\theta = 90°$.

Table 4.4: The material budget parameters of each layer for the vertex detector.

Unit	Beampipe	layer 1	layer 2	layer 3	layer 4	layer 5	layer 6
$\bar{X_0}$ (% X_0)	0.454	0.067	0.059	0.058	0.061	0.280	0.280

4.1.3 Background estimation

Hit rate significantly affects the design specifications of the sensor. *Details* of each component's contribution to the VTX will be discussed in the Chapter **??**. *Here* we only

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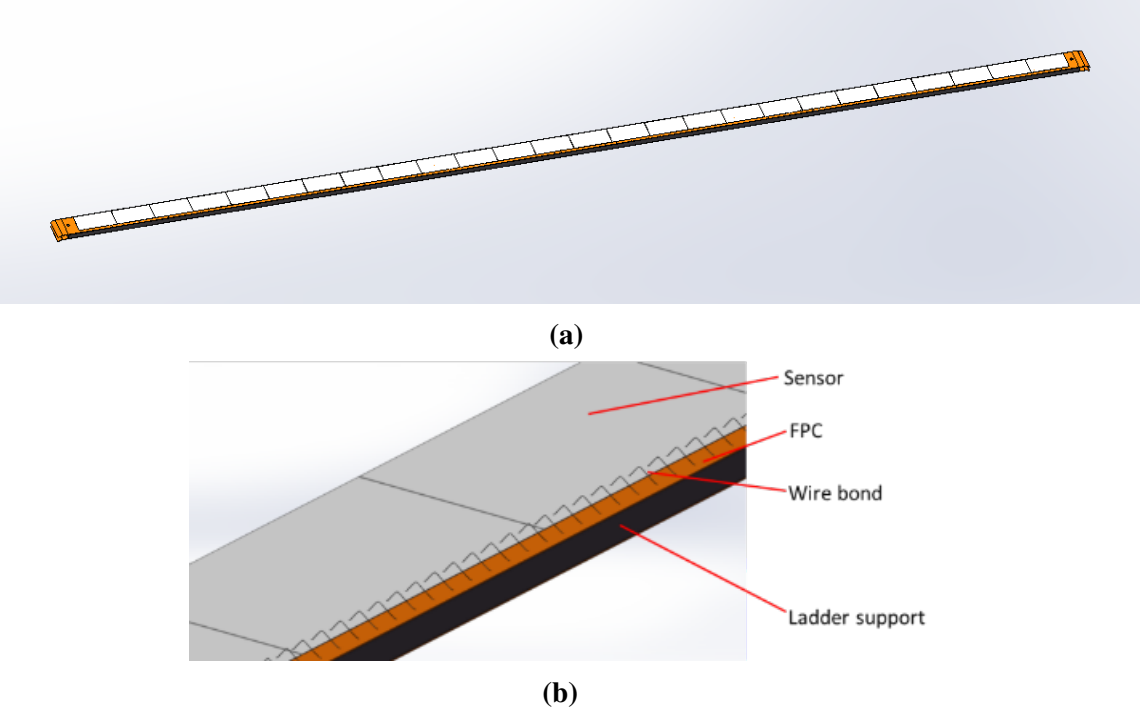

Figure 4.5: ladder structure. (a) The ladder assembly. (b) Local details of the ladder.

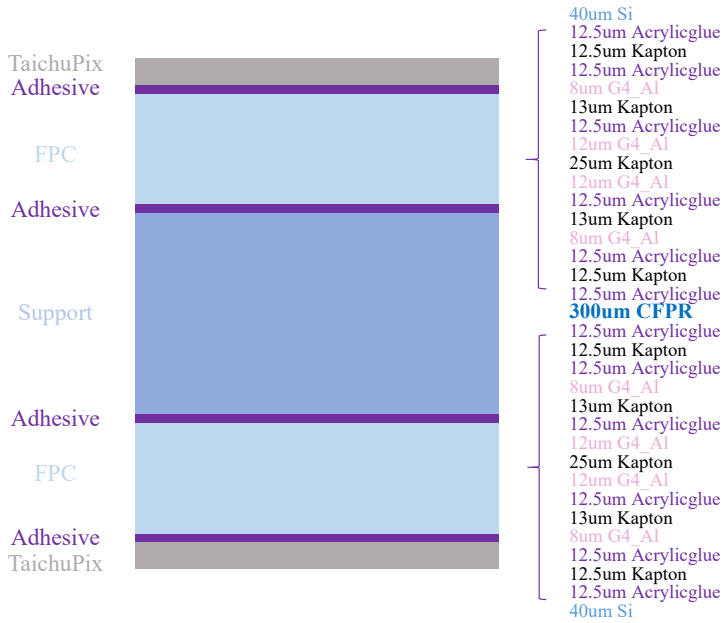

Figure 4.6: Longitudinal cross-section of a ladder, composed of two layers of chips and other materials, such as glue, carbon fiber, and aluminum. Each ladder of PVTX 5-6 in the vertex layout utilizes this structure.

present the total hit rate, data rate, occupancy, and other relevant information for each mode. With hit rate being defined as the *number* of particles hitting the RSU *per unit time and unit area*, data rate equals to hit rate times cluster size, which indicates the number

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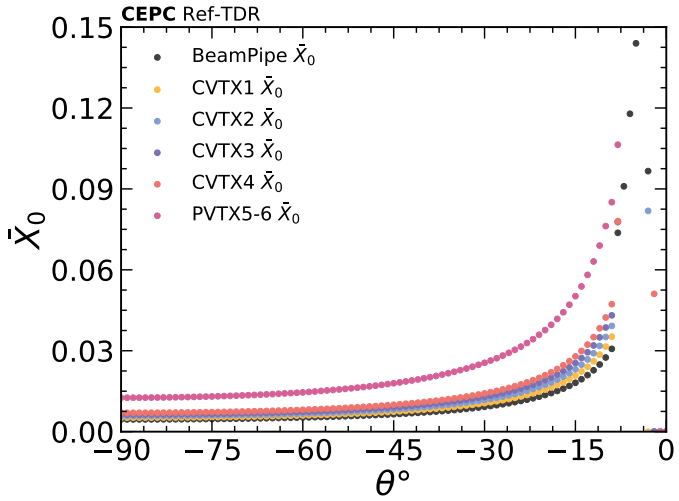

Figure 4.7: The average value $\bar{X}_0$ within the range of $\phi \in (0, 360)°$ of vertex detector varies with θ.

of pixels fired by a single particle, and occupancy is calculated within a specified time window at pixel level.

In order to calculate the data rate, information about the cluster size is essential. To compute the data rate more accurately, we did not set the cluster size as a fixed value; instead, we referenced the results from the TaichuPix-3 beam test and calculated the cluster size based on the particle's incidence angle. The background hit rate and data rate are shown as Table 4.5, data rate is estimated here as DataRate = HitRate ×32 bit / pixel × ClusterSize. Hit rate distributions of Higgs as well as Z mode are shown *in* Figure 4.8 and Figure 4.9.

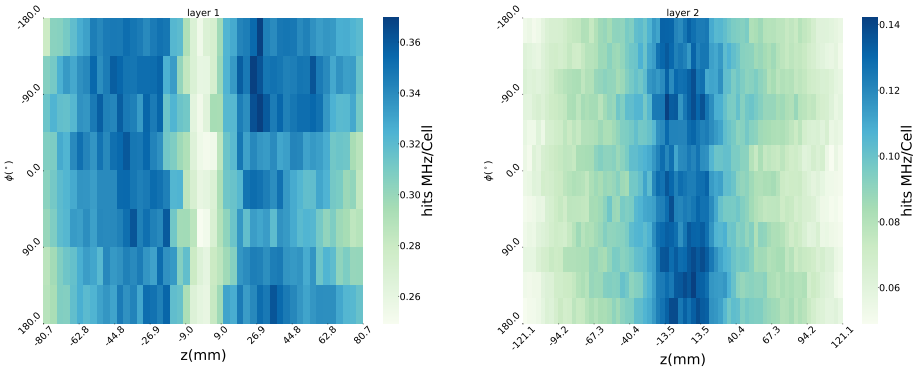

Figure 4.8: Hit rate distribution of Higgs mode. The shape of VTX is approximately cylindrical, where the x-axis can be equivalently regarded as the z-axis of the global coordinate, and the y-axis can be equivalently regarded as the polar angle ϕ of the global coordinate. Synchrotron radiation is not included.

For the VTX, the primary sources of beam background are synchrotron radiation and pair production. However, due to the excessive computational resources required

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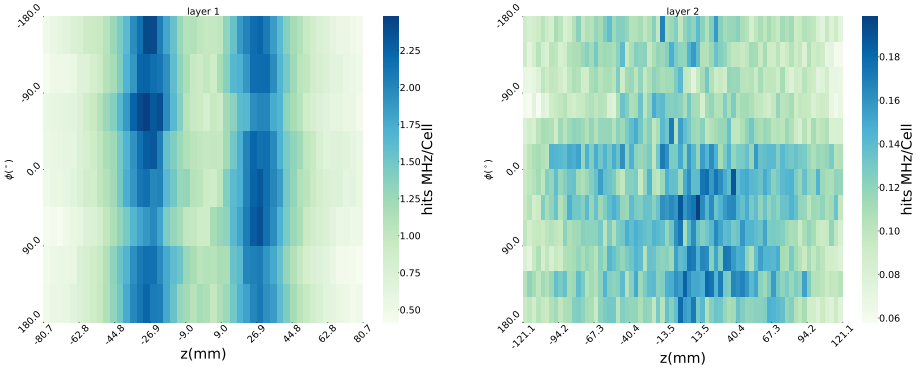

Figure 4.9: Hit rate distribution of Z mode. For we could not completely handle high-lumi Z mode now, as well as the major difference between high-lumi Z with Z mode is luminosity which means their hit rate distribution is similar, the hit rate distribution of high-lumi Z would not be shown here. Synchrotron radiation is not included.

Table 4.5: Summary of background estimation. Current detector scheme cannot completely handle high-lumi Z mode, so the result of high-lumi Z will not be shown here. For the results of high-lumi Z, based on accelerator parameters, a rough estimation can be made by simply multiplying the existing Z mode results by a factor of 3. Synchrotron radiation is included.

Layer	**Ave. Hit Rate MHz/cm^2**	**Max. Hit Rate MHz/cm^2**	**Ave. Data Rate Mbps/cm^2**	**Max. Data Rate Mbps/cm^2**
Higgs mode: Bunch Spacing: 277ns, 63 %Gap, 25× 25 μm^2/ pixel				
1	2.5	2.8	260	340
2	0.67	1.15	70	110
3	0.17	0.35	20	38
4	0.078	0.18	10	31
5	0.026	0.15	3.4	24
6	0.018	0.085	2.4	13
Z mode: Bunch Spacing: 69ns, 9 %Gap, 25× 25 μm^2/ pixel				
1	9.4	19	1400	2800
2	0.89	1.5	120	240
3	0.31	0.75	46	190
4	0.19	0.47	30	160
5	0.045	0.095	6.4	14
6	0.035	0.072	4.8	12

for simulating and analyzing synchrotron radiation, we did not perform simulations and analyses with the same event statistics and granularity as those for other beam backgrounds. Based on simulation results of approximately 1×10^9 synchrotron photons, we estimate that the beam background contribution from synchrotron radiation is comparable to that from pair production. Therefore, when presenting Table 4.5, to incorporate the synchrotron radiation results, we multiplied the pair production contribution by a factor of 2. However, it should be noted that the actual maximum value will be lower than simply doubling the pair production results.

We *use the* bunch spacing as a time window to calculate the occupancy of different

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modes at various levels, and the results are as Table **??**.

Table 4.6: Occupancy estimation. Considering that the only difference between the two modes in the current simulation lies in the bunch settings, the occupancy in both modes should be similar. Therefore, they are combined and presented as Z mode. Synchrotron radiation is not included.

Layer	Mode	Ave. Occupancy@Pixel ($\times 10^{-5}$ / BX)	Max. Occupancy@Pixel ($\times 10^{-5}$ / BX)
1	Higgs	1.818	2.331
2		0.484	0.778
3		0.137	0.265
4		0.071	0.219
5		0.024	0.170
6		0.017	0.095
1	Z Mode	0.972	2.026
2		0.085	0.168
3		0.033	0.124
4		0.022	0.108
5		0.005	0.011
6		0.004	0.009

4.2 Sensors and electronics design

4.2.1 Sensor technology overview

The current design and development of the CEPC vertex detector are centered on utilizing CIS technology for chip design and manufacturing. This technology integrates the sensor and readout electronics onto a single chip, significantly reducing both pixel size and power consumption while delivering high-performance detection capabilities. Such features meet the stringent requirements for high *spatial* resolution, low material budget, and rapid readout speeds.

[wm: This paragraph is over detailed...] The Solenoidal Tracker at RHIC (STAR) experiment at Relativistic Heavy Ion Collider (RHIC) successfully employs MAPS technology in its vertex detector [1], and the STAR MAPS vertex detector features excellent spatial resolution [1, 2]. The Inner Tracker System (ITS)2 of European Organization for Nuclear Research (CERN)'s A Large Ion Collider Experiment (ALICE) experiment is the largest scale MAPS system among high energy physics experiments [3]. ITS2 is a full-pixel silicon detector based on TowerJazz 180 nm technology. It boasts exceptional technical parameters, including approximately 5 μm high resolution, an extremely low material budget of less than 0.3 % X_0 per layer, stable readout support for collision frequencies up to 100 kHz, and power consumption as low as 40 mW·cm^{-2} [3, 4]. The upcoming ITS3 upgrade for the ALICE experiment introduces the concept of "curved wafer-level chips", aiming to achieve a self-supporting wafer structure [5, 6]. This de-

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velopment is based on TowerJazz Tower Partners Semiconductor Co. (TPSCo) 65 nm technology. This innovation could potentially reduce the material budget of the vertex detector by a factor of 3 to 5. The ITS3 project is currently in the research and development phase. The comparison of key parameters between different vertex detectors mentioned above is shown as Teble 4.7.

Table 4.7: Comparison of sensor technology in vertex detectors of different experiments: ALICE Pixel Detector (ALPIDE)(ALICE ITS2), MOSAIX(ALICE ITS3), Taichu-3 (the first CEPC vertex detector prototype), and Taichu-Stitching(CEPC vertex detector).

Sensors	Technology Node	Power Consumption	Readout Speed	Spatial Resolution
ALPIDE [3, 4]	180 nm	40mW/cm^2	Up to 100 kHz	5 μm
MOSAIX [5]	65 nm	40mW/cm^2	164 kHz	5 μm
Taichu-3 [7–9]	180 nm	80 ~ 100mW/cm^2	40 MHz	5 μm
Taichu-Stitching	65 nm	≤ 40mW/cm^2	Up to 43 MHz	3-5 μm

4.2.2 Stitched sensor prototype design

The *CMOS* stitching technology enables the production of chips significantly larger than the dimensions of the design reticle. The design reticle is divided into sub-frames that align with the sub-frames of the photomasks. By selectively exposing these reticle sub-frames onto adjacent locations following the designed pattern, manufacturers can create large chips with dimensions nearing the wafer's diameter. This innovative approach expands the possibilities for chip design and production. *[wm: The statements on advantages are either not ture, or arguable, and nevertheless unnessary, thereby removed.]* Taking into account the difficulty and the yield of stitching technology, the baseline design of the stitched sensor prototype involves using 1D stitching to achieve stitched-chip along the beam pipe direction. The feasibility of 2D stitching will also be continuously explored during research and development.

4.2.2.1 Sensor architecture and functional blocks

The idea of using a stitched sensor chip to construct half of the detector layer is inspired by the design of the ALICE ITS3[5][6] sensor. Thanks to the promising results obtained in the MOnolithic Stitched Sensor (MOSS) and MOnolithic Stitched sensor with Timing (MOST) prototypes for the ALICE ITS3 project [5], this consideration benefits from the scheme of the MOSS and MOST prototype. Detailed R&D on the stitching floor-plan for the vertex detector is under assessment at the time of writing. The preliminary stitching plan of the silicon wafer and the dimensions of each half layer are introduced in Figure 4.3.

Figure 4.10 presents a schematic floor-plan of the sensor for Layer 1, implemented by dicing out two adjacent modules. Each module operates independently. The sensitive

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area of a module consists of eight RSUs, each representing an instance of the same design. On the left side of the module, the Left-end Readout Block (LRB) facilitates signal interconnections to the external systems and the power supplies to the module. The Right-end Power Block (RPB), located on the right side, consists solely of power transmission buses for the power distribution.

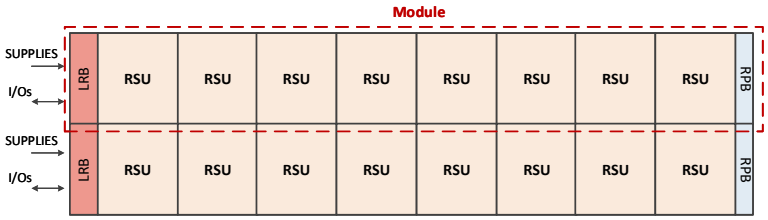

Figure 4.10: Top level floor-plan for a sensor of layer1 (not to scale). It comprises two identical modules, with one of them indicated by the dotted red rectangle.

Figure 4.11 illustrates the preliminary floor-plan of *an* RSU. *The* RSU is divided into several identical Sensor Blocks. Each sensor block is fully independent from the others with its own biasing generator, slow control and periphery readout circuit, *as* shown in Figure 4.12. The sensor block has local power switches located at the right side of the sensor block that can be selectively switched on by the user control. This powering granularity reduces the sensitivity of the stitched sensor to possible manufacturing faults. In the case of a supply short in one of the sensor blocks, it allows to switch off the faulty sensor blocks and maintain the others functioning normally. Considering the sensitive area of a sensor block will introduce an extra dead area in the event of switching off, the dimension of the pixel matrix in a sensor block should be choose carefully. The scale of a sensor block will be optimized in the future design for a trade-off between the power granularity and the data transmission performance. In the preliminary design at the time of writing, one RSU contains 12 identical sensor blocks and 4 stitched interface blocks arranged in two rows. Data of each sensor block has to be transmitted to the LRB through the one-to-one direct connection between the sensor block and the LRB. As the longest transmission distance reaches more than 20 cm for the rightmost sensor block of the module, the regeneration of the signal periodically over the link is necessary. This function is proposed to be implemented in the stitched data interface blocks. The stitched data interface block transmits control signals and data from sensor blocks to the LRB. The RSU is divided into multiple sections internally, different functional blocks are repeated multiple times. An RSU contains *Pixel Matrices*, Biasing Blocks, Power *Switch* Blocks, and Matrix Readout Blocks, and 4 Stitched Data interface Blocks.

4.2.2.2 Design of the repeated sensor unit

Each pixel cell integrates a sensing diode, a front-end amplifier, a discriminator and a digital pixel readout. The in-pixel digital readout benefited from the TaichuPix

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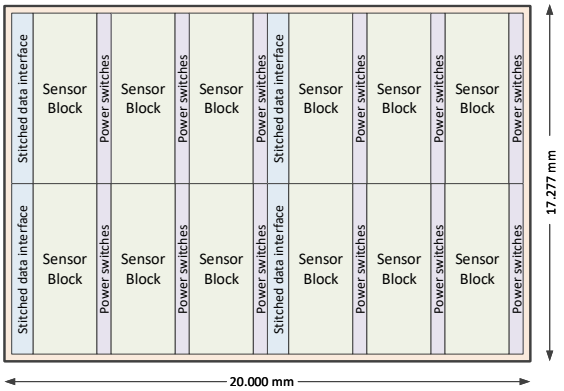

Figure 4.11: Proposed floor-plan for a RSU (not to scale). It contains several identical sensor blocks. Each of them has a pixel matrix with its own biasing generator, slow control and periphery readout circuit. Each sensor block can be selectively switched on/off. The stitched data interface blocks are used to transmit control signals and data to the edge of the stitching sensor.

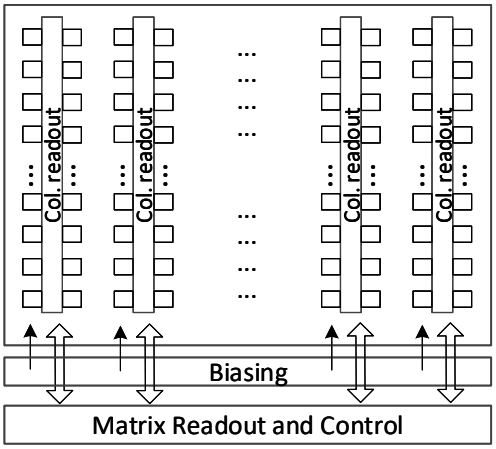

Figure 4.12: Architecture of the sensor block. It consists of a pixel matrix, a biasing generator and a periphery readout and control.

prototype. Each pixel contains a hit storage register and logic for pixel mask and test pulse configuration. A common threshold level is applied to all the discriminators of the pixels. Every pixel can be tested and calibrated individually, combining charge injection scans and threshold scans.

I. Sensing diode A sensing diode is formed by an N-implant electrode in a P-type epitaxial layer. The geometry of the sensing diode involves a trade-off among charge collection performance (i.e. efficiency, collection time, and radiation tolerance), area, and sensor capacitance. As discussed in Section 4.5.1, the sensor performance optimization was previously explored *with* the 180 nm TowerJazz CIS technology. These studies provide foundational insights for enhancing sensor performance in the 65 nm TowerJazz CIS process. *A variet of* pixel test structures are proposed in the initial R&D phase of

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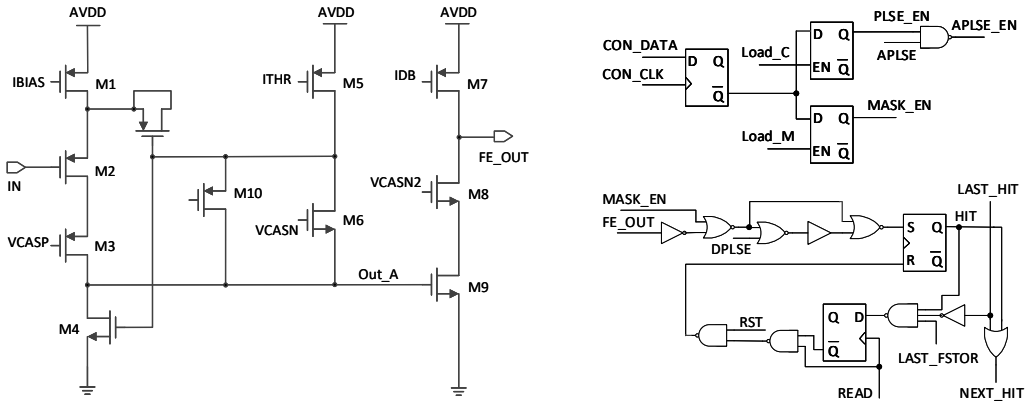
the stitched sensor to further optimize the sensor geometry for compatibility with the 65 nm CIS process. *The* structures *include* different electrode diameters, spacing between the electrode and the surrounding PWELL, PWELL geometries, and methods of applying reverse bias to the sensor diode.

II. Pixel Front-end The simplified schematic of the analogue front-end is shown in Figure 4.13a, which had been verified *with* the TaichuPix prototype (see Section 4.5.2). The topology of the circuit was derived from the ALPIDE *sensor* used in the ALICE ITS2 [4]. The analog front-end and the discriminator are continuously active.

III. In-pixel digital logic The in-pixel digital electronics*, as shown in Figure 4.13b,* inherit the TaichuPix design. It features a hit latch set by a negative pulse from the output of the front-end. The pixel readout follows a double-column drain arrangement. The region for in-pixel digital readout logic is shared by two columns to minimize the crosstalk between analog signals and digital buses. Additionally, it saves space for the routing of the address encoder. The priority logic arbitrates the pixel readout, with the topmost pixel having the highest readout priority. The in-pixel logic also integrates configuration registers for calibrating the pixel front-end, for testing in-pixel readout logic, and for masking the faulty pixel. The configuration function is programmable through the setting of control bits, including MASK_EN, PULSE_EN, DPULSE and APULSE.



(a) **(b)**

Figure 4.13: Schematic and block diagram of the in-pixel circuits. (a) Schematic of the analog front-end. (b) Diagram of the digital logic.

IV. Peripheral readout circuits on sensor The main function of the on-chip peripheral readout circuits includes: sending *control signals* required by the pixel array and receiving *data* from the pixel array; buffering the data to smooth the output data rate; providing a slow control interface for chip configurations and tests.

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The data from the pixel array are organized in Double Columns (Dcols). In order to achieve a detection efficiency close to 100 %, all double columns of pixel array are read out in parallel. A timestamp is recorded at the end of the double column for the future data processing. Without a trigger signal, all the readout data are buffered and *sent out*. A data compression mode is optional, which *could* reduce the output data rate by half.

The peripheral readout circuit's core function is to send control signals to the pixel array and receive data from it. A data-driven schema is preferred. The read signal is only sent when the pixel is triggered. To read the signals sequentially, a priority mechanism must be implemented. The most popular method is address priority. A hit signal is generated when the collected signal exceeds a threshold and is reset after the pixel address is read out.

Based on this approach, the pixel array's clock is inactive in the absence of a hit. This approach effectively minimizes power consumption. To optimize control timing, a hierarchical priority control chain can be implemented.

To accommodate higher data rates, a real-time data compression strategy can be implemented before sending data to First In First Out (FIFO)s.

The address of the first pixel in a package is recorded, while the next three pixels are encoded using a three-bit code, where '0' represents no hit and '1' represents a hit. Operating at a system clock of 43.33 MHz, the data compression circuits incur no additional timing overhead. By enabling the data compression function, the data volume is reduced, and the readout speed is increased.

The fast chip-level readout is closely related to FIFO accesses. We propose a shareable architecture [10]. The shared FIFO features flexible capacities to handle random hit bursts. As a result, higher hit flux can be accommodated even with a reduced total memory volume.

The power consumption is evaluated based on TaichuPix, which is implemented using a 180 nm process for average hit rates of 1 MPixel/s/cm^2, 15 MPixel/s/cm^2 and 40 MPixel/s/cm^2. The future design of the RSU will use a 65 nm process. The power supply will be reduced from 1.8 V to 1.2 V. The area of the peripheral readout circuits is estimated to be reduced by *50%*. The dynamic power consumption due to clock and data upsets is estimated with a reduction of 4.5 times. However, the static leakage currents will increase significantly. To *limit* the power density *within* 40 mW/cm^2, the power consumption of peripheral circuits in RSU is estimated to be 40 mW, *and* the leakage current should be controlled in 5 times of TaichuPix. Power switches will be implemented to meet these requirements. Finally, the power consumption of the future design is estimated as 29 mW and 37.5 mW for 8 MPixel/s/cm^2 at Higgs mode and 42 MPixel/s/cm^2 at *Z mode*, respectively.

Considering the application and tests, the chip will provide proper register control and on-chip test mode.The On-Chip Test (OCT) module is planned to generate input signals for peripheral readout circuits, enable chip debug and data alignment. The register control

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provides internal status access and configuration of readout function, bias voltage/current, pixel mask and calibration, and so on.

4.2.2.3 Design of the left-end readout block

All data from a row of RSUs of a module, seeing Figure 4.10, are collected and processed by a LRB located on the left side of the module. Primary functions of the LRB are illustrated in the block diagram of Figure 4.14. The RSU data are transmitted to the LRB via a large array of differential point-to-point on-chip serial data links, which operate at 86.66 Mbps. As modules of different CVTXs containing different numbers of RSUs, the module in CVTX-4 houses the largest quantity, i.e. 10 RSUs. Since each RSU is equipped with 12 data links, the LRB must accommodate up to 120 data links. A group of 128 receivers primarily compensates for phase differences in the incoming data streams from the RSUs and resamples them using a local fast clock. The data encoding blocks collect and encode the data with redundancy to correct errors during off-chip transmission. After encoding, the data are serialized at a rate of 1.39 Gbps and transmitted off-chip using 8 serializers. The Clock Block supplies *clocks* required for the LRB and RSUs. Additionally, the LRB facilitates slow control and manages power switch control signals for the RSUs.

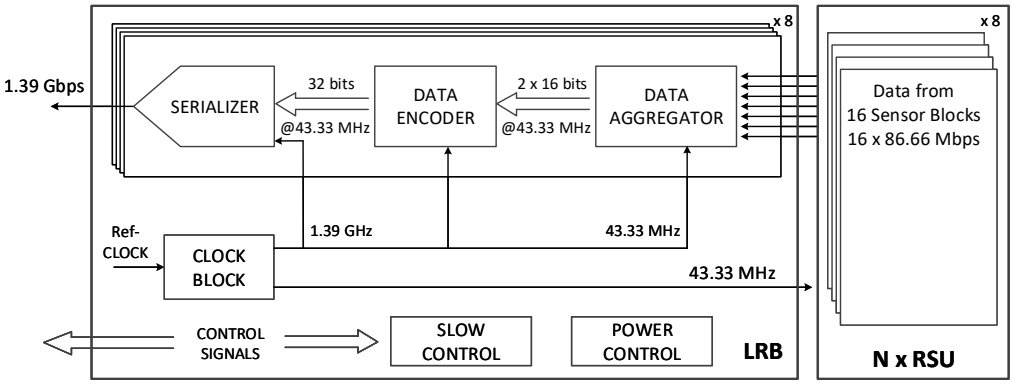

Figure 4.14: Proposed diagram of the LRB. All data from RSUs of one module has to be transmitted to the LRB. 'N × RSU' labeled in the right part of the diagram represents that different layers in the detector contain a varying number of RSUs.

4.2.2.4 Power consumption estimates

As illustrated in Figure 4.11 and 4.12, each RSU consists of a pixel matrix, biasing blocks, matrix readouts, and data interface blocks. *The expected power consumption of the main functional blocks of an RSU as well as the total power consumption of a single RSU are listed in Table 4.8.* The current consumption is mainly determined by the bias current (IBIAS) of the first branch, adjustable by one of the local Digital-to-Analog Converter (DAC)s in the periphery of the pixel array. Targeting *the requirement* of 40 mW/cm^2, the value of IBIAS is reduced compared to the one in the TaichuPix design. The choice of

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the IBIAS value is a trade-off between the power consumption and the speed. By design, the nominal power consumption values of the new front-end in TPSCo 65 nm process are 68.4 nW. The nominal value corresponds to analogue power densities of 26.7 mW/cm^2 for the pixel pitch of 16 μm and 10.9 mW/cm^2 for the pixel pitch of 25 μm. In Table 4.8, the entries for the pixel matrix include the power of the pixel analogue circuit and the pixel digital logic. In the current calculations, it is assumed that the pixel size is 25 × 25 μm^2, which is consistent with the intrinsic position resolution value used in Section 4.1.2. The power of the pixel analogue is calculated by the power density of the pixel front-end (shown in Section 4.2.2.2) and the total area of 12 pixel matrices. The power consumption of the pixel digital in the table includes the dynamic power of the in-pixel digital logic and the double-column address encoding logic (described in Section 4.2.2.2), as well as power consumption due to the leakage current. The dynamic power consumption of the pixel digital circuit mainly depends on the pixel hit rate. Based on estimations of the hit rate in the vertex detector and testing experience with the TaichuPix prototype, the dynamic power consumption of the pixel digital circuit is relatively small. In contrast, considering the planned use of 65 nm CIS process, the contribution of leakage current from transistor gate leakage to power consumption is much greater than the dynamic power of the digital circuit. The contribution of the Biasing Blocks is estimated based on the experience of the design in the TaichuPix. The entry for the Matrix readout blocks is described in Section 4.2.2.2. The value for the data interface blocks is obtained from the very preliminary considerations on the transmitting power of the control signals and the readout data of RSUs. Table 4.9 lists the power consumption estimates for the main functional blocks of the LRB (see Figure 4.14).

Table 4.8: Estimates of power consumption of one RSU. All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	Pixel analogue	Pixel digital	Biasing block	Matrix readout	Data interface	RSU Total
Power [mW]	36	30	8	40	17	131

Table 4.9: Estimates of power consumption of the LRB. All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	Clock Block	Data Aggregator	Data Encoder	Serializer	Slow & Power control	LRBTotal
Power [mW]	36	120	80	32	80	348

Combining the power estimates of Table 4.8 and 4.9 with the surface areas of the major blocks, one obtains the estimates for the power dissipation densities. The results are given in Table 4.10.

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Table 4.10: Estimates of average power dissipation per unit area over the main functional blocks composing the stitched chip

Components	Power density [mW/cm^2]
Repeated Sensor Unit	38
Left-end Readout Block	485

4.2.3 Backend electronics and cables

The flex Printed Circuit Board (PCB) is *integrated* to the backend electronics system in the VTX design. These flex PCBs serve as conduits for transmitting signals, clocks, control commands, power, and ground connections between the control boards and the detector modules. By providing a lightweight and adaptable interconnection, *the* flex PCBs facilitate efficient data communication and power distribution while minimizing material usage, which is crucial for maintaining the detector's performance and reducing multiple scattering effects.

4.3 Mechanics, cooling and services

This section describes the mechanical design of the VTX, including the support structure and related finite element analysis, detector air cooling and the general scheme of services.

4.3.1 Mechanics

4.3.1.1 General support structure

The baseline design of the vertex detector consists of, from inner radius to outer radius, four concentric cylinders constructed with stitching technology-based bent CIS followed by a single-layer double-sided ladder-based barrel. The innermost cylinder has a radius of 11 mm, and maintains a 0.3 mm gap from the beam pipe. *The* Figure 4.1 demonstrates the general structure of the detector and its integrated mechanical support. *The general* mechanical support design for the vertex detector aims to use ultra-light materials to create a rigid enough structure, realizing a low material budget without weakening the spatial resolution.

4.3.1.2 Ladder and support

The double-sided ladder is the structural unit of the layer 5 and 6 . It features pixel sensors on both sides of the ladder support, while sensors are glued onto the FPC *[wm: not flex PCB as in 4.2.3?]*, which is *in turn* glued onto the ladder support. The CFRP

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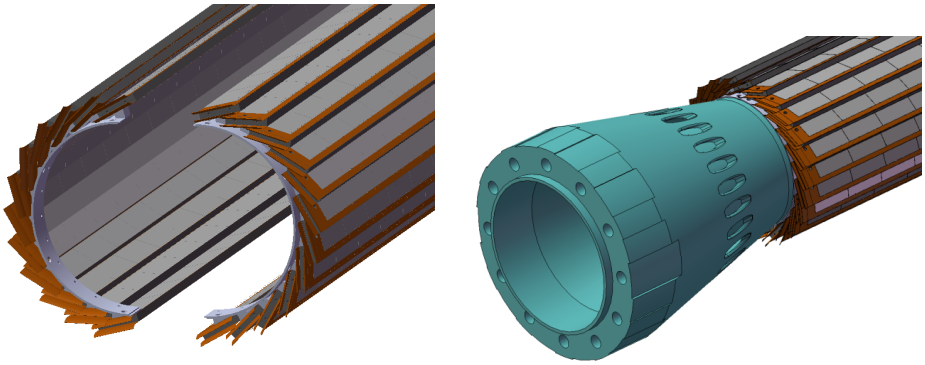
is used to make the ladder support due to its low density and high specific modulus and strength. The main body of the ladder support is a hollow shell structure [11] with an overall size of $682 \times 3.2 \times 17.5$ mm^3 . With the assistance of the finite element static analysis, the laminated shell of the ladder support is made of ultra-thin CFRP plies, using the high modulus CFRP at a level equivalent to M40, the CFRP laminate of the shell is made with a thickness of 0.15 mm, to get a conservative estimation by just putting the mass of the sensors and FPC to the bare ladder support (without taking into account their contribution to the rigidity of the complete ladder), it is anticipated that the ladder support deforms very slightly and at a negligible level. According to previous evaluations, about *20%* smaller deformation will be induced for the complete ladder [11].

4.3.1.3 Ladder-based barrel and fixation to the beam pipe (assembly)

The *VTX* is the first detector outside the beam pipe, and structurally it will be integrated into the beam pipe assembly. The outermost layer of the *VTX*, the ladder-based barrel, does not directly mount on the beam pipe; it rests and is secured to the intermediate conical parts that are mounted to the beam pipe, providing support for the vertex structure. The four layers of *the CVTX* are mainly fixed to the extended section of the beam pipe.

The barrel-shaped outer layer detector formed by the double-sided ladders which overlap with each other in the circumferential direction to form a continuous sensitive layer. To facilitate barrel assembling and its installation on the beam pipe integration, the barrel structure is designed as *in* Figure 4.15. *It* is assembled by two half-barrels, *with* each half-barrel consisting of two half side-rings located at both ends along with several ladders. The ladders are positioned and secured to the side-rings by the surfaces of the tooth-shaped structure of the side-rings. After the two independent half-barrels are pre-assembled on dedicated tooling, they are installed and fixed onto the intermediate conical part of the beam pipe assembly, as illustrated *in* Figure 4.15b.



(a) **(b)**

Figure 4.15: (a) The barrel assembly. (b) The barrel on beam pipe assembly (the outer tube of the beam pipe assembly is not shown)

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The ladder-based barrel design is consistent structurally with our previous prototyped vertex design. Furthermore, much R&D work involving structural validation tests were conducted during the previous prototype development phase. *These* experiences can be helpful to optimize the TDR design.

4.3.1.4 Bent CIS cylinders and fixation to beam pipe

There are four layers of CVTX with different radii and lengths consistent with the physical layout of the vertex detector. Each CVTX is a single detector layer that consists of two half cylinders, as shown in Figure 4.16. To maintain the bent CMOS sensors in the cylindrical shape, ultra-light local supports made of CFRP have been used in design. Integrated with the electronic readout, the FPC is connected to the CVTX edge via wire bonding. To keep the connecting joint safe and also for protecting the wire bonds, extended support has been designed for each cylinder, as shown in Figure 4.16. It prevents the FPC from deforming very close to the joint area, thereby avoiding damage to the connection. The CVTX, the local support and the extended support form a cylinder assembly. Each cylinder assembly is independent and has no contact with the adjacent layers of cylinder assemblies. They will be mounted onto the beam pipe assembly separately. This kind of design focuses primarily on realizing and facilitating a feasible process for both assembly and wire bonding, as well as installation onto the beam pipe. The results of the finite element simulation analysis indicate that, under constrained conditions at both ends, this structure has very minimal deformation, and the stress on the bent chips is also very low, both of which are negligible.

4.3.2 Cooling

The heat generation of the VTX for both the ladder-based barrel and the CVTX cylinders is estimated to be at the level of 40 $\mathrm{mW/cm^2}$. The operational temperature for the detector is required to be no higher than 30 °C. Thus, cooling is essential for maintaining optimal sensor performance. Generally, electronic equipment with heat generation up to 300 $\mathrm{mW/cm^2}$ can be cooled using forced air convection. Given the stringent material budget goal for the VTX, forced air cooling has been selected as the cooling method.

Air cooling simulation analysis has been conducted to evaluate the cooling performance of the current structural design of the VTX. The simulation results indicate that at an average flow rate of 3.5 m/s the maximum temperature of the outer ladder is within the required range, as shown in Table 4.11. For the CVTX cylinders, the innermost layer is very close to the beam pipe and has no airflow, making it the most challenging layer to cool within the entire detector. The simulation results indicate that at an airflow rate of 3.5 m/s with the central beam pipe surface temperature considered, the innermost layer of the CVTX cylinder can be cooled to a sufficiently low temperature, as shown in Fig-

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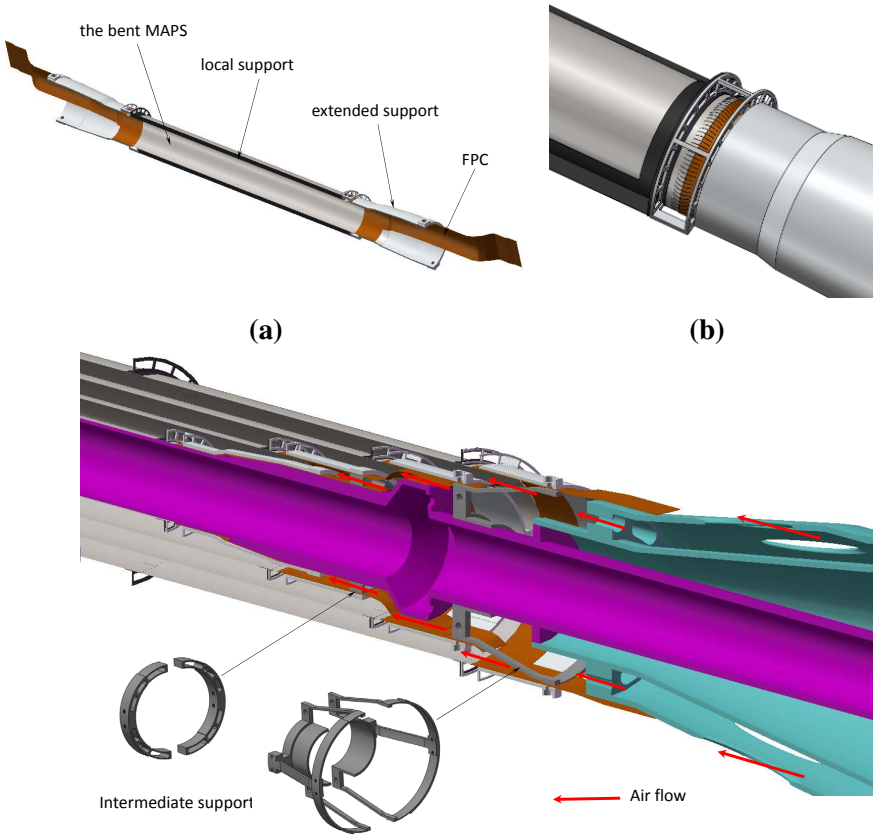

Figure 4.16: The half cylinder assembly (bent CIS with FPC and the extended support) of the innermost layer. (a) An overview of the half cylinder of bent CIS detector layer, and the yellow part is FPC. (b) An extended support to prevent the FPC from deforming too close to the joint area. (c) Cylinders installation and intermediate support.

ure 4.17, thereby meeting the requirements. Additional simulations were also performed to compare the maximum temperature of the innermost layer at different wind speeds. Based on these simulation results, it is anticipated that air cooling would meet the cooling needs of the detector.

Table 4.11: Simulation results of the barrel-maximum temperature on the ladder. Inlet air temperature of 5 °C; air speed of 3.5 m/s.

Power dissipation	Total heat generation of the barrel	Max temperature on ladder
40 mW/cm^2	190 W	29.4 °C

4.3.3 Services

This section introduces the needs and considerations of the general services for the VTX, which uses air cooling. The main service requirement is to ensure proper airflow

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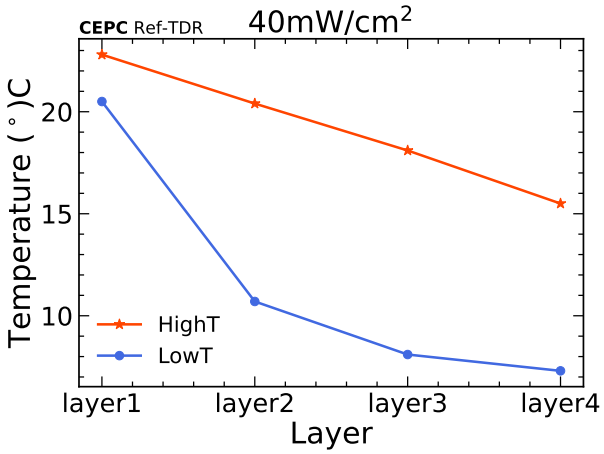

Figure 4.17: Simulation results for the cooling of bent CIS cylinders, with an airflow rate of 3.5 m/s. The beam pipe surface temperature, as shown in Chapter **??**, is taken into account.

and good ventilation for the entire detector zone. The vertex detector will be mounted onto and integrated into the beam pipe assembly; the other service requirement is to route all the cables of the VTX out of the very space-limited beam pipe assembly.

Since the VTX consists of a single barrel layer and four concentric cylinder layers, ventilation for each gap between the adjacent layers must be ensured for effective cooling. The mechanical design for the vertex detector fully considered this requirement and also tried to minimize the effect caused by FPCs blocking, which is obviously reflected in the hollow support structures designed for the detector, especially the support of the CVTX cylinders. The conical part that is integrated into the beam pipe assembly to support the barrel layer mentioned before also works as the general air distributor for the entire vertex detector. It is a hollow structure; air will be blown into the inside hollow space from the side of the part then distributed to the detector zone through those ventilation holes facing different zones of the detector on the outer surface, as shown in Figure 4.18.

The space for the entire VTX inside the beam pipe is very compact. Together with the beam pipe assembly, for the vertex detector, on both ends of the barrel and the CVTX cylinders, the FPCs of the ladders and the CVTX are the only cables that need to be routed out. The FPCs of the CVTX cylinders will be routed along their extended support and converged after the end of the outermost layer, and then they are stacked and go through the intermediate conical part via the grooves. The FPCs of the ladders of PVTX will be streamlined by converging the FPCs of two adjacent ladders into one conduit, similar to the FPCs of the CVTX, then go through the conical part via their specified grooves, as illustrated in Figure 4.18, which effectively halves the spatial occupancy and preventing the circumferential accumulation of FPCs from fully cover the outer surface of the conical part. After all the FPCs are routed outside the beam pipe assembly, they will

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be transferred to optical fibers via connectors, as described in Section 4.2. A half-dummy model of the vertex structure, incorporating the CVTX cylinders and two short ladders, has been constructed to test the FPC routing. The trial results demonstrate that the routing scheme is basically feasible.

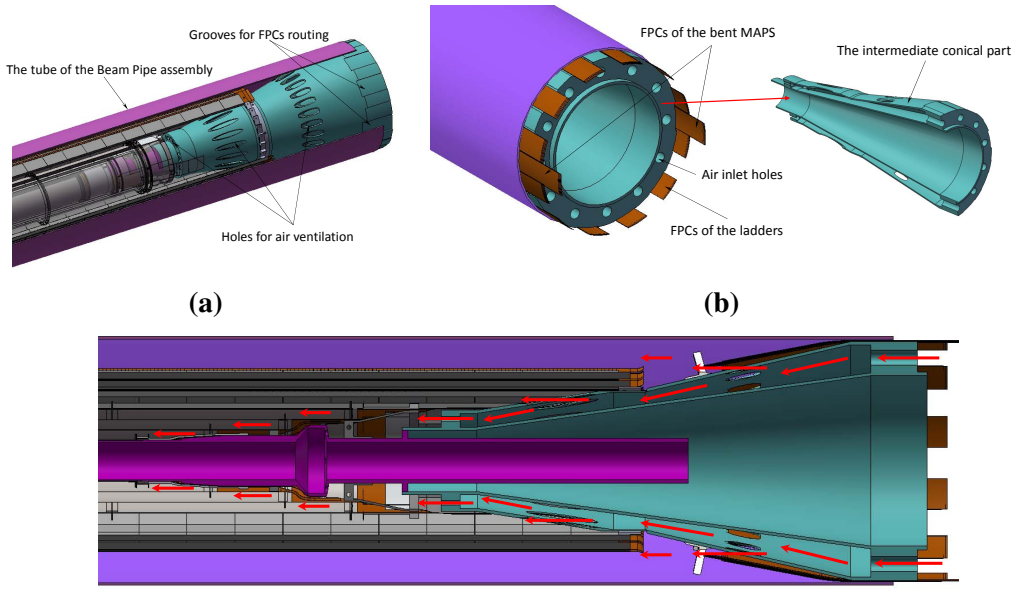

Figure 4.18: Air ventilation and cable routing of the VTX. (a)Air channel design with holes on global support structure for air distribution. Grooves on support structure is designed for FPCs routing. (b) The FPCs of the vertex detector routed out of the side of the beam pipe assembly, along with a cut view of the conical part. (c) Air channel, red arrows are air flow.

4.4 Alignment and calibration

The VTX is designed to precisely measure the trajectory parameters of charged particles close to the interaction point, enabling accurate reconstruction of decay vertices from short-lived particles. Effective alignment is crucial for achieving optimal resolution in the VTX.

The alignment strategy for the VTX faces significant challenges due to the implementation of *the CVTX* pixel sensors. The primary goals of this strategy include achieving high spatial resolution, reducing uncertainties in impact parameters, and ensuring stable alignment through efficient and automated processes.

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4.4.1 Initial mechanical alignment and reference alignment system

Initial mechanical alignment will be conducted during detector assembly, utilizing precision optical survey instruments. Sensors will be aligned within a few micrometers of design specifications, and optical method will confirm sensor curvature and cylindrical positioning. Fiducial markers placed strategically on sensor modules and supporting structures will facilitate optical tracking and ensure precise referencing. A stable external alignment system, regularly monitored through X-ray or laser-based and optical survey methods [12], will serve as the reference for continuous alignment.

4.4.2 Track-based alignment

Mechanical alignment procedures during installation provide an initial level of precision in the VTX position. This precision is typically significantly worse than the desired design hit resolution. Additional alignment (tracker-based alignment) is needed to account for the position, orientation, and surface deformations of the CVTXs. Charged particle tracks obtained from collision data will facilitate iterative alignment corrections during both the commissioning and operational phases. Global and local χ^2 minimization algorithms will refine sensor positioning, *improving* accuracy and ensuring optimal detector performance.

In the current detector design, simulations have demonstrated the ideal performance of the detector; however, in practical applications, it is necessary to consider the typical deformation mode as shown in Figure 4.19. The deformation includes elliptical deformation; irregular, wavy distortion; circular distortion with uniform radial expansion.

These deformation modes can affect the detector's ability to determine the relative positions of collision products as they pass through the VTX, ultimately *influencing* the accuracy of the reconstructed collision parameters d_0 and z_0. The effect of each *type of* deformations was studied in the simulation by modifying the position of *hits* according to *the deformation*. In particular, for each simulated charged-particle trajectory, the intersection with the deformed geometry was computed to determine the corresponding position of the hit in the local detector coordinates. The track-reconstruction algorithm was then executed assuming an ideal geometry to quantify the effect of the detector deformations in the absence of a detector alignment procedure. *[wm: And...?]*

4.4.3 Real-time monitoring

A laser-based online alignment monitoring system will perform real-time checks, verifying alignment accuracy continuously.

Due to the air cooling design in the VTX, it is important to monitor the movement of the CVTXs. Inspired by the laser alignment system of CMS experiment [12], it is

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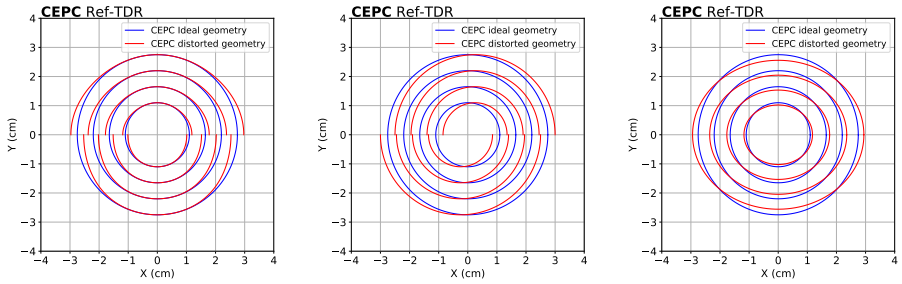

(a) **(b)** **(c)**

Figure 4.19: Illustration of the hit positions in the transverse plane with ideal vertex geometry and three deformed geometry. The amount of deformation is amplified with respect to the expected one for visualisation. (a) Elliptical deformation. The red distorted geometry is elongated horizontally, demonstrating a deformation primarily along the x-axis. (b) Illustration of the hit positions in the transverse plane for vertex geometry exhibiting irregular, wavy distortion. The distorted geometry has noticeable undulations, indicating non-uniform deformation affecting both the x and y directions unevenly. (c) Illustration of the hit positions in the transverse plane for vertex geometry showing a circular distortion with uniform radial expansion. The distorted geometry presents a uniformly increased radius, representing an isotropic deformation compared to the ideal geometry.

proposed to install laser alignment system to keep track of these movement. *As shown in Figure 4.20, laser sources are placed on the service portions of CVTX layers; there are two sources on both sides of inner three layers and one source at the right side of the 4th layer.* This system utilizes near-infrared laser beams (1050 nm) directed through the VTX to detect potential movements or deformations of the mechanical structure. Laser sources located in service areas are triggered to send pulsed infrared light to CVTXs of the VTX. By detecting their interaction with the silicon sensors, the system can infer movements of the CVTXs, ensuring that any deformations due to environmental factors like temperature, air flow, or magnetic fields are promptly identified.

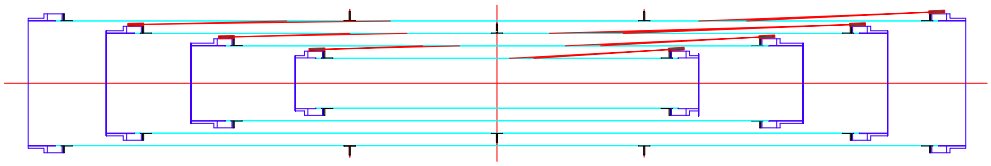

Figure 4.20: A laser-based online alignment monitoring system. Red lines diagonally connect with the aqua blue line (CVTX chip) are the lasers, and the laser sources are placed at both sides of the inner three layers and right side of the 4th layer to monitor the movement of each layer.

To validate the laser calibration system, signals generated by the laser were simulated using Geant4 [13] within the CEPC Software (CEPCSW) framework. The laser was emitted as a point source from the position (13 mm, 0, -85 mm), directed at an angle of

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$\theta = 10^\circ$ and $\phi = 0$. In the absence of a focusing system, a divergence of $\tan\alpha = 0.1$ was established. The resulting laser beam spot on the second layer of the VTX is presented in Figure 4.21.

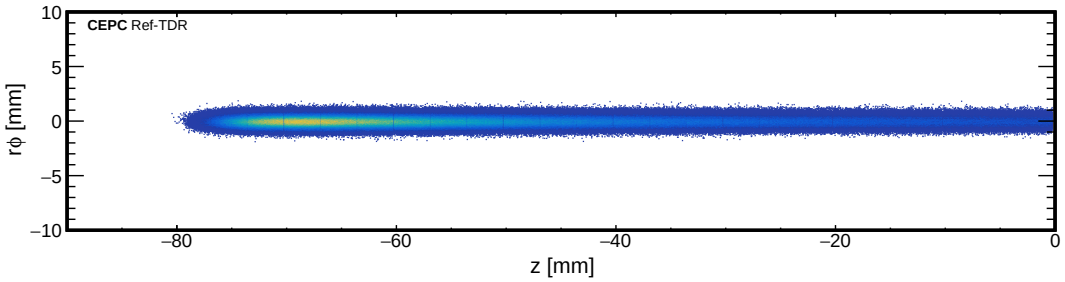

Figure 4.21: The laser beam spot on the second layer from (13 mm, 0, -85 mm) in cylindrical coordinate system, where the horizontal axis is the z-coordinate, and the vertical axis is the $r\phi$ coordinate. And each region is divided by a blank or lower rate than its neighbor means one sensor.

When simulating deformation by radially displacing the second layer outward by $d = 10\,\mu\text{m}$, the resulting distribution of signal IDs, The observed difference of 2 corresponds to a distance of 50µm, which is consistent with relationship $d/\tan\theta \approx 57\mu\text{m}$. If an accurate fitting function can *[wm: why didn't do?]* be employed to characterize this distribution and precisely determine the most probable position, it would enable more accurate detection of displacement. These findings indicate that the laser calibration system can infer positional changes through the distribution of pixel IDs.

4.5 R&D efforts and results

To meet the stringent requirements of high spatial resolution, low material budget, rapid readout speeds, and low power consumption, significant efforts have been directed toward advancing CIS technologies, notably through the TaichuPix and JadePix projects.

The JadePix project focuses on investigating CMOS pixel sensors for the CEPC vertex detector, exploring low-power readout schemes. Concurrently, the TaichuPix *project* is dedicated to developing CIS featuring advanced in-pixel electronics optimized for rapid readout. These sensors utilize a data-driven, column-drain architecture specifically designed to meet the fast response requirements imposed by the high collision rates at CEPC.

4.5.1 CIS JadePix series

The CEPC VTX imposes stringent requirements on spatial resolution. To achieve a spatial resolution of 3 µm, the pixel size needs to be reduced to less than 20 µm, which is limited by the feature size of integrated circuit technology. JadePix utilizes a specialized

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180 nm CIS integrated circuit process optimized for ionizing radiation detection, which is a modification and development based on the commercial CIS process. The pixel pitch in this process typically ranges from 25 to 30 μm. Therefore, the key focus of JadePix's development is on how to reduce the pixel size while also meeting the requirements for low power consumption and fast time stamping.

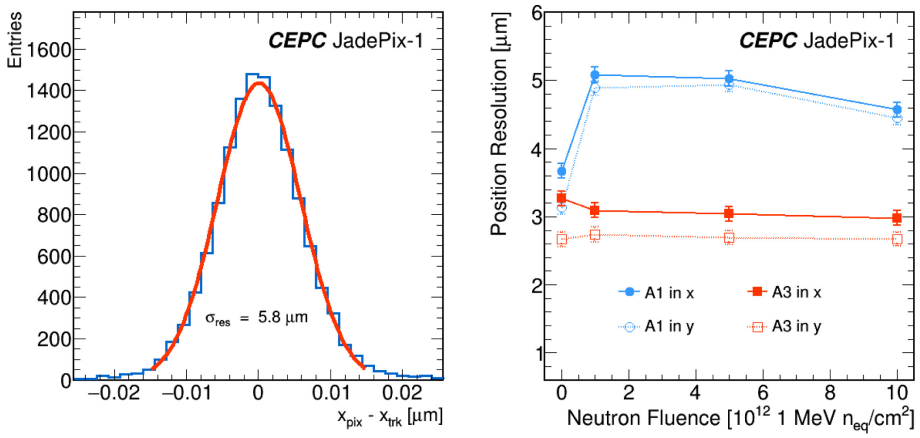
4.5.1.1 Overview of JadePix development

The JadePix series of chips are primarily designed and optimized for high spatial resolution, low power consumption, and fast time stamping. Since 2015, a total of 5 chips have undergone continuous improvements which are shown *in* Table 4.12.

Table 4.12: Overview of JadePix development

Chip Name	Pixel Array	Pixel Pitch(μm^2)	Analog Front-end	Matrix Readout	Design Team
JadePix-1	128×192, 160×96	16×16, 33×33	Source follower	Rolling Shutter	IHEP
JadePix-2	96×112	22×22	Diff. Amp., CS Amp.	Rolling Shutter	IHEP
JadePix-3	512×192	16×23, 16×26	ALPIDE	Rolling Shutter	IHEP, CCNU, SDU, DLNU
JadePix-4	356×489	20×29	ALPIDE	AERD	CCNU, IHEP
JadePix-5	896×480	20×30	ALPIDE	AERD	IHEP, CCNU

JadePix-1[14] primarily focused on sensor optimization, comparing different geometric dimensions [15] and providing experimental evidence for the design of small charge collection electrodes [16]. As *shown in* Figure 4.22, the optimal spatial resolution obtained through beam tests on *an array of pixels with pixel pitches of* 33×33 μm^2 was 2.7 μm[17].



(a) (b)

Figure 4.22: (a) Residual distribution of JadePix-1 sensor in the x direction. (b) Position resolution for sensors with a small electrode (A1) and a large electrode (A3) before and after the neutron irradiation.

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JadePix-2 investigated AC coupling and different analog front-end amplifiers [18], attempting to optimize resolution, power consumption, and time stamping design using a 180 nm process based on the Minimum Ionising MOS Active pixel sensor (MIMOSA) architecture.

JadePix-3 utilized the low-power front-end amplifier of ALPIDE[4], combined with a Rolling Shutter readout architecture, achieving the smallest pixel design among similar chips at 16×23 μm^2. Infrared laser tests showed spatial resolutions of 3.4 µm (X-direction) and 2.7 µm (Y-direction) [19]. A 5-layer beam telescope system was constructed based on this chip, measuring spatial resolutions on a 5.8 GeV electron beam of 5.2 µm (X-direction) and 4.6 µm (Y-direction) [20] . *[wm: The pixel size is less than that of JadePix-1, but the resolutions are worse. Why?]* The cluster size from beam tests was significantly larger than that from laser tests, adversely affecting the spatial resolution. *[wm: In general the bigger the cluster, the more the resolution can be improved. Why it's reversed here?]* The highest efficiency reached 99 % at the optimum threshold of 160 e^-.

JadePix-4 and JadePix-5 employed ALPIDE analog front-ends and AERD readout architectures. The latter is an efficient sparse readout logic that can quickly read out the addresses of hit pixels at very low power consumption and apply time stamps around the periphery of the pixel array. The AERD readout architecture has been adopted not only by *various* CISs on the 180 nm process but also by the next-generation 65 nm Stitching process.

4.5.2 CIS TaichuPix series

In order to address the high hit density of the CEPC, a CIS, named TaichuPix, has been developed with the goal of high readout speed and high spatial resolution. TaichuPix-1[7] and TaichuPix-2[8], are multi-project wafers, and TaichuPix-3 is a full-scale prototype with an engineering run. The pixel matrix of TaichuPix-3 is 1024×512 with a pixel pitch of 25 µm, and a thickness of 150 µm.

Each pixel of the TaichuPix-3 chip integrates a sensing diode, an analog front-end, and a digital logical readout in each pixel. The analog front-end is designed based on the ALPIDE [4] *chip*. In order to address the high hit rate of CEPC, the analog front-end of TaichuPix-3 has been specifically optimized to ensure a quicker response. In addition, the digital logical readout includes a hit storage register, logic for pixel mask, and test pulse configuration. The digital logical readout follows the FE-I3[21] designed for the ATLAS pixel detector, but it has been modified to adjust the pixel address generator and relocate the timestamp storage from within the pixel to the end of the column. This modification was necessary due to pixel size constraints. Furthermore, the double-column drain peripheral readout architecture of the TaichuPix-3 chip employs an address encoder with a pull-up and pull-down network matrix.

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4.5.2.1 TaichuPix specification and performance

Specification *The design specifications of the TaichuPix-3 chip are summarized in Table 4.13.* The performance of the pixel sensor chip has been verified with a 4 GeV electron beam at Deutsches Elektronen-Synchrotron (DESY) II. The intrinsic spatial resolution was found to be 4.8 μm and 4.5 μm, and the detection efficiency reached 99 %, which meet the requirements.

Table 4.13: Design specifications of the TaichuPix-3 chip.

Specification	Index
Pixel size	$25 \times 25 \mu m^2$
Dimension	$15.9 \times 25.7 mm^2$
Techonology	CIS 180nm
Dead time	$< 500ns$
Power density	$< 200mW \cdot cm^{-2}$
Max. Hit rate	$36 \times 10^6 cm^{-2} \cdot s^{-1}$

In order to verify the performance of TaichuPix, we conducted multiple beam tests at DESY II[9].

Spatial resolution The spatial resolution of TaichuPix-3 chips are verified by electron beam provided by DESY II. The intrinsic spatial resolution is derived from an unbiased distribution of tracking residual, which excludes the Device Under Test (DUT). The scattering angle is predicted using Highland formula.

After considering the contribution from track resolution, the intrinsic spatial resolution for TaichuPix-3 chip is about 5μm. *The spatial resolution as a function of threshold is shown in Figure 4.23.* In general, a higher threshold leads to a smaller cluster size, which introduces a bias in estimating the actual hitting position and ultimately worsens the intrinsic resolution. As depicted in Figure 4.23, for the two DUTs, *[wm: difference of DUTa and DUTb should be described here, as they are referred in the following discussions.]* increasing the threshold results in a deterioration of the intrinsic resolution. However, for DUT_B, a worse resolution is also observed when the threshold is lower than $\xi_B = 218\ e^-$, which can be attributed to the increased noise at the lower thresholds. The best resolution for DUT_A is 4.72 ± 0.13 (syst.) μm in the x-direciton, 4.83 ± 0.10 (syst.) μm in the y-direciton when $\xi_B = 265\ e^-$. For DUT_B, the best resolution is 4.46 ± 0.13 (syst.) μm int the x-direciton, 4.52 ± 0.13 (syst.)μm int the y-direciton when $\xi_B = 218\ e^-$. *[wm: When uncertainties are listed, the stat. error can't be omitted, whereas the syst. can.]*

Detection efficiency The maximum detection efficiency is 99.76% for DUT_B and 99.68% for DUT_A. However, the efficiency of DUT_B drops significantly at high thresholds com-

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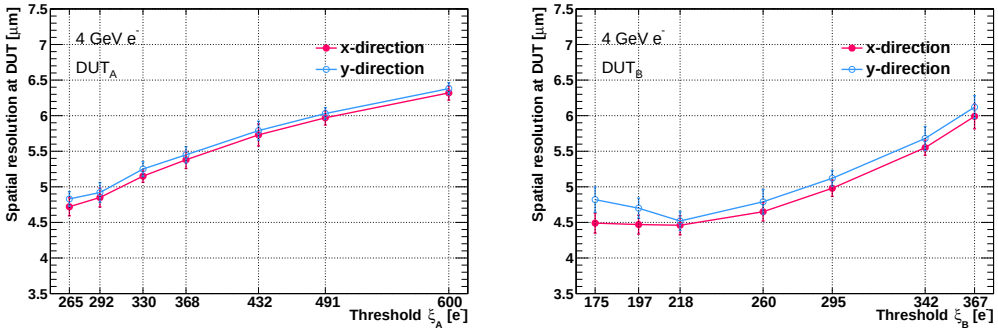

(a) **(b)**

Figure 4.23: Spatial resolution as a function of threshold for DUT_A(a) and DUT_B(b) in the x-direction and y-direction. The error bars represent the total systematic uncertainty.

pared to DUT_A. This can be explained by the difference in the process of the two DUTs. Comparing to DUT_B, DUT_A has an additional low-dose N-layer, which enables a larger depletion of the epitaxial layer and results in a larger charge collection area.

4.5.2.2 Prototype of a planar CIS vertex detector

In striving to fulfill requirements in Table 4.13, a planar CIS vertex detector prototype (shown *in* Figure 4.24) has been developed and evaluated[22] using an electron beam from DESY II.

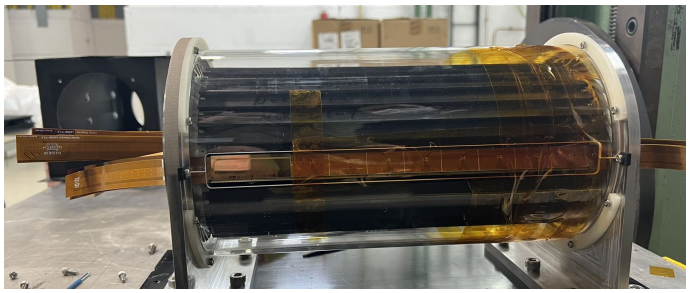

Figure 4.24: Planar vertex detector prototype with six ladders mounted for beam test.

[wm: Contents in the following two paragraphs are very similar as those in the previous section. Better to improve.]

Spatial resolution and detection efficiency The spatial resolution is derived from an unbiased distribution of tracking residual obtained using the GBL track-fitting algorithm, which excludes the DUT. The scattering angle is predicted using the Highland formula. After alignment, the standard deviation for $\mathrm{DUT_A}$ and $\mathrm{DUT_B}$ at minimum threshold is approximately 5.4 µm and 5.0 µm, respectively. Additionally, the spatial resolution of both DUTs deteriorates as the threshold increases, and due to reduced charge-sharing

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effects on DUT_A, it exhibits poorer resolution compared to DUT_B. At the lowest threshold setting, the best spatial resolution achieved is 5.38 ± 0.12 (syst.)μm in the u-direction and 5.52 ± 0.10 (syst.)μm in the v-direction for DUT_A, and 4.97 ± 0.08 (syst.)μm in the u-direction and 5.21 ± 0.08 (syst.)μm in the v-direction for DUT_B. To demonstrate the overall performance of the prototype, the measured spatial resolution in this article involves the resolution of the reference tracks.

The efficiencies of DUT_A and DUT_B exhibit a decreasing trend as the threshold increases. The best detection efficiency is 99.3 % and 99.6 % for DUT_A and DUT_B, respectively.

Air cooling The VTX is designed for very high spatial resolution. For air cooling, in addition, to cool the detector to a certain temperature, one needs to consider the vibration amplitude caused by the forced airflow, which should not affect the expected high spatial resolution. This issue was noted and studied during the prototype R&D phase. *The test results indicate that the maximum amplitude of vibration of the ladder support is less than 1.9* μm *even under a higher airflow rate of 4 m/s.* In addition, during the beam test of the VTX prototype, air cooling with a fan was employed, which decrease the chip temperature from 41°C to 25°C at a power dissipation of approximately 60 mW/cm^2 , and no impact on the spatial resolution was observed. The strategy for addressing vibration in the baseline design of the VTX is similar to that of previous studies; prototyping the key structural elements and conducting related tests later on is the preferred method.

4.5.2.3 Prototype of a stitching CMOS detector

A stitched CIS has been developed. It was designed and fabricated in a 0.35 μm technology, which provides a thickness of 14 μm epitaxial layer and four metal layers for routing. Since there are triple wells in this process, only NMOS could be used in the pixel. The total pixel array is 644 rows and 3600 columns stitched by a basic pixel array of 92 rows and 600 columns. It works in a rolling shutter readout mode. As a full functional prototype, it integrated column-level discriminator, on-chip zero suppression, interface circuits such as bias DAC, analog buffers, Inter-Integrated Circuit (I2C) control, Phase-Locked Loop (PLL), Low-Voltage Differential Signaling (LVDS), Low Dropout Regulator (LDO), etc. The total area is up to $11 \times 11\,cm^2$. In order to study charge collection efficiency and charge sharing, each basic pixel array has six submatrices with different pixel sizes and diode arrangements. The prototype chip is being tested and its development could provide experience in developing stitched sensor with advanced technology.

The radius bending test We have conducted studies on vertex detector with stitching technology. Dummy wafers have been used for bending tests, prototype manufacturing,

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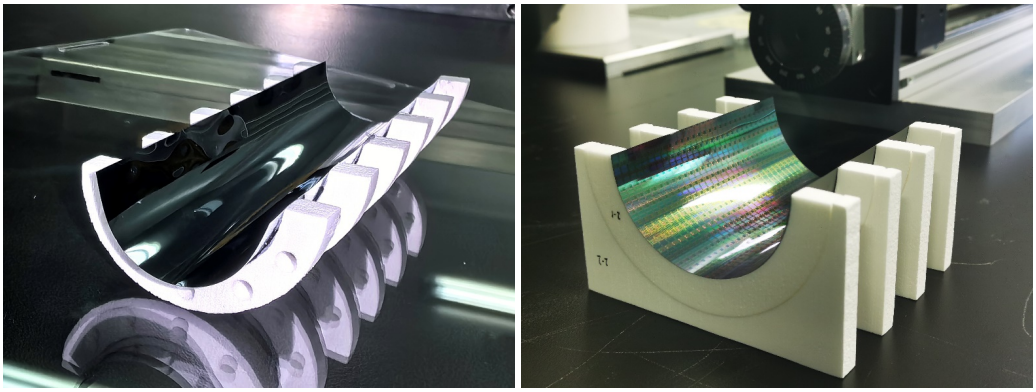
and, meanwhile, small-area CIS were used to study the impacts of bending on the chip performance.

Silicon is a brittle material. It undergoes an irreversible brittle fracture when the stress exceeds its compressive strength. We thinned the wafers to thicknesses of 30 μm, 40 μm, and 50 μm, and successfully completed bending tests with and without a film, as well as fatigue tests for different radii in various sequences, . Currently, the bending limit test has successfully achieved a minimum bending radius of 12 mm , as shown in Figure 4.25a. Additionally, we performed over 20 times of bending-recovery-bending tests on the same wafer. The prototype in Figure 4.25b has been placed for over 2 years without damage.



(a) **(b)**

Figure 4.25: Prototype for bending test. (a) Testing of bending limit, the minimum bending radius of 12 mm has achieved. (b) Determining the damage-free duration of the bending wafer, this prototype placed for over 2 years without damage.

4.6 Performance

4.6.1 Dead zones and tracking efficiency

There are two types of dead zones: one is due to assembling pixel sensors to ladders or semi-cylinders, which in turn to form detector barrels; another is due to functional blocks in the sensor design, such as data interfaces, power switches, etc, as shown in Figure 4.11. No hits will be produced when charged particles pass through these regions. During layout optimization, different deflections in the ϕ direction have been applied to different layers *to minimize* the loss of *the number of* hits from a single trajectory. Furthermore, the width of *the PVTX* ladders has been increased to avoid empty sensor regions in the phi direction. However, when the width becomes too large, it could lead to a situation where both adjacent ladders at the same layer have signals, which increases the material volume of the overlapping area. To assess the reasonableness of the dead zones

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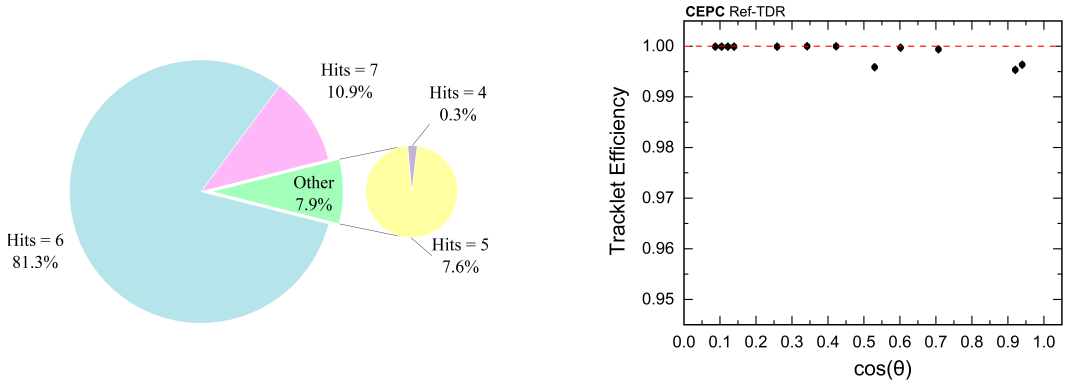
and overlaps, simulations using chargedgeantino were performed to obtain the number of hits in the VTX.

A quantity, called Tracklet Efficiency, is defined as the ratio of the sum of hits left in the VTX by reconstructable trajectories to the total number of expected hits by all simulated tracks. It can be expressed mathematically as,

$$\text{Tracklet Efficiency} = \frac{\sum_i^N \text{Hits}i^{(\geq 4)}}{N \times L} \tag{4.1}$$

where $\text{Hits}i^{(\geq 4)}$ represents the number of hits left by the i-th *chargedgeantino trajectory* passing through the VTX with a hit count *no less than four*, N is the total number of simulated events, and L is the expected number of layers *(hits)* that the VTX is expected to be traversed (*six* in this case). As shown in Figure 4.26a, for a chargedgeantino with a momentum of 20 GeV, the particle's tracklet efficiency is 99.635% *[wm: uncertainty?]* at $\theta = 20°$. When each track is required to pass through the first layer of the VTX, the tracklet efficiency is 96.75%.

Figure 4.26b illustrates the tracklet efficiency and its errors for 20 GeV chargedgeantino particles passing through the VTX at different polar angles. The tracklet efficiency is consistently close to 100% in all cases.



(a) **(b)**

Figure 4.26: Performance on tracking. (a) Each track includes the percentage of hits when the number of hits is 4, 5, 6, and 7, based on the simulation of 10,000 chargedgeantino particles by the VTX at $\theta = 20°$ and 20 GeV. (b) Tracklet efficiency and its errors for 10000 chargedgeantino particles at 20 GeV, originating from collision vertex (0, 0, 0) and passing through the VTX at different polar angles.

4.6.2 Resolution

The VTX design described in Section 4.1.2 will serve as the the baseline schemes in the following sections. Additionally, a backup scheme is proposed whose detailed information is shown in Section 4.7. Simulations were performed using CEPCSW in conjunction with the remaining sub-detectors of the *tracking system*, with μ^- as the

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outgoing particles and a conservative single-point resolution of *5 μm* assumed for *the pixel sensor*. Through simulation results, as shown in Figure 4.27, the baseline scheme demonstrates its superior d_0 resolution performance among the two schemes.

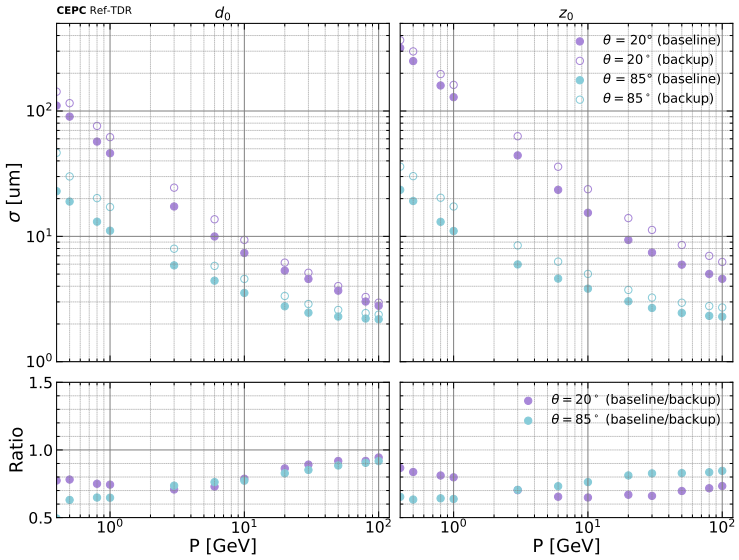

Figure 4.27: The resolution of the impact parameter d_0 and z_0 in the two schemes varies with the change in the momentum of the outgoing μ^- particles.

As previously demonstrated during the optimization, the adoption of the low-mass stitching technique allows the baseline scheme of the VTX to achieve good resolution of the impact parameter d_0 of tracks even at high momentum, as well as improved d_0 resolution at low momentum. In fact, not only the d_0 resolution, but the baseline scheme also exhibits excellent performance for the resolution of impact parameter z_0, as shown in Figure 4.27. The simulation results demonstrate that the trend of the z_0 resolution as a function of momentum is analogous to that of d_0, with only minor discrepancies observed. This observation aligns with the utilization of pixel detectors in the VTX, where the precision of z position measurements is equivalent to that of $r\phi$ measurements. Such findings indicate that when comparing different configurations, focusing exclusively on d_0 resolution is a valid approach that also minimizes the workload. The results indicate that an increase in momentum correlates with an enhancement in resolution. This improvement can be attributed to the pronounced effects of multiple scattering in material at low momentum. Similarly, as the polar angle θ *approaches to the beam line*, the amount of material traversed by charged tracks increases proportionally to $\sim 1/\sin\theta$, which further amplifies the multiple scattering effects and leads to a degradation in resolution.

Similarly, the z_0 resolution of the backup scheme in Figure 4.27 is also slightly worse than *that* of the baseline scheme.

4.6.3 Performance under sensor failure scenarios

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Some VTX units may fail to operate normally or even become damaged in the future actual operation for various reasons. When such situations arise, the performance of the VTX is bound to decline. However, to ensure the smooth progress of physical analysis, the design of the VTX must guarantee that even in the worst-case scenarios, the performance does not experience a dramatic drop.

To this end, in the simulation process, we assume that a certain layer of the VTX does not produce signals to estimate performance under this special circumstance. As shown in Figure 4.28, the estimated performance for normal conditions and for damages from the first to the sixth layers is presented. It is evident that the current vertex detector scheme can ensure that, in the case of a single layer loss, the performance decrease does not exceed 25 %, with the loss of the first layer having the most significant impact. For cases of individual unit damage, the overall performance can be viewed as a weighted average of the probabilities of the intact and damaged sections. Considering the very low likelihood of two layers being damaged simultaneously, it can be reasonably anticipated that the overall impact will be minimal.

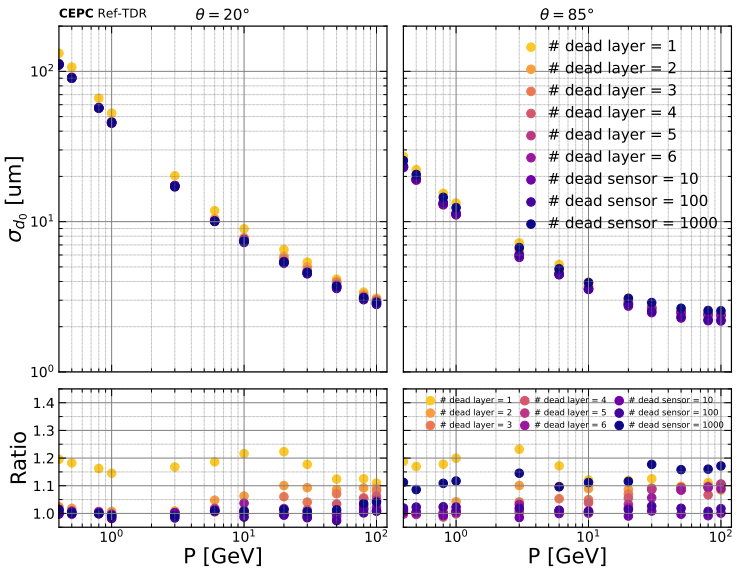

Figure 4.28: Resolution of the impact parameter d_0 for tracks obtained by the baseline vertex detector under different dead layer/sensor conditions, including complete layer failures and 10, 100, 1000 sensor failures (RSUs in CVTX, Taichu chips in PVTX), with ratios to the baseline scheme.

4.6.4 Performance with beam background

In addition, due to the proximity of the VTX to the beam pipe, it is crucial to evaluate the effects of beam background on its performance during the design phase.

This approach incorporates true simulated backgrounds into the signal, as outlined in Section **??**. This method facilitates a comparison of the d_0 resolution before and after

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background incorporation, as illustrated in Figure 4.29, where no discernible effects are observed. Thus, it is evident that provided the levels of beam background remain consistent with those *obtained* in current simulation studies, the VTX is poised to deliver outstanding performance. Nonetheless, it should be noted that the inclusion of beam background may lead to increased processing time for track reconstruction. Therefore, subsequent efforts should focus on algorithm optimization and enhanced computational efficiency to mitigate this increase.

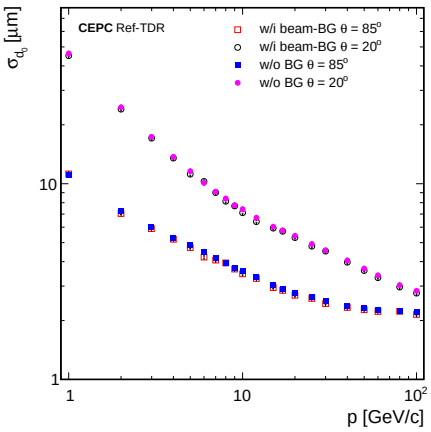

Figure 4.29: Comparison of resolution of the impact parameter d_0 of tracks between clean single muon signal (w/o BG) and mixing beam background (w/i beam-BG) at polar angle of 85° and 20°.

4.7 A fallback solution

Another VTX design using *three* layers of double-sided ladders with planar CISs *has* also been considered, *as shown in Figure 4.30.* The *design* represents a *conventional but well-established* option. It serves as *an* alternative fallback solution if the baseline *design* with curved technology encounters unforeseen challenges. However, it introduces additional material and complexity due to the need for mechanical support, overlaps between ladders, and potentially thicker support elements.

Detailed parameters for backup vertex detector layout is provided in Table 4.14. The intrinsic single-point resolution of the chip is derived from the TaichuPix-3 beam tests, with a conservative resolution of 5 μm.

4.8 Summary and future plan

The CIS-based detector layout consists of *six* cylindrical layers of pixel sensors with pixel *pitches* in the order of 25 μm ×25 μm, enabling hit resolutions better than 5 μm. The

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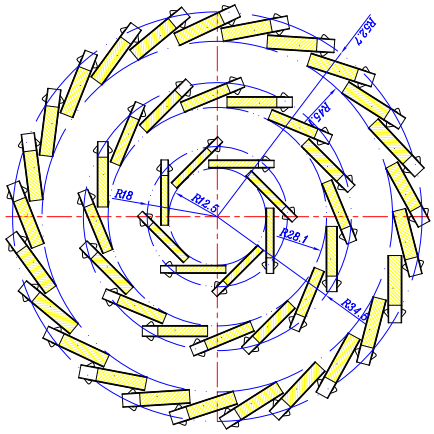

Figure 4.30: Sectional view of the VTX backup layout. All the 6 layers (3 layers of double sided ladders) are composed of planar CISs. PVTX 1-2, PVTX 3-4, and PVTX 5-6 include 8, 16, and 25 ladders, respectively.

Table 4.14: Geometric configuration parameters for the backup scheme. Radius and length, and material budget of the support structure for each layer of the VTX, as well as the height of ladder corresponding to PVTX.

PVTX X	radius [mm]	length [mm]	height [mm]	support thickness [μm]
PVTX 1-2	12.46	260.0	1.8	300
PVTX 3-4	27.89	494.0	2.6	300
PVTX 5-6	43.79	749.0	3.3	300

inner four layers are bent CIS cylinders. The outer two layers are based on double-side ladder technology.

Initial vertex detector prototypes using double-side ladder technology have demonstrated a spatial resolution better than 5 µm with air cooling in DESY testbeam. Geant4-based simulations, demonstrate that the baseline design of vertex detector can achieve the target impact parameter resolution.

Future R&D priorities include:

1. Development of wafer-scale stitching CISs.
    - Initially, the stitching chip will leverage mature 180 nm technology (e.g., TowerJazz) to keep R&D risks and costs within reasonable bounds. The pixel cell and matrix design will build on the proven architecture of previous prototype chips, with focused efforts on stitching-related challenges and ensuring basic cell designs draw from verified experience.
    - The second-generation stitching chip will transition to 65 nm/55 nm technology, with potential candidates including TPSCO's 65 nm technology and domestic HLMC's 55 nm technology. Synergy with sensor development for future LHC upgrades is anticipated.
2. Ultra-thin mechanical supports and low-mass integration techniques.

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- The plan begins with exploring the construction of a mock-up featuring dummy heaters for thermal performance testing. Results will also validate thermal simulation models.

3. Construction of a full-scale vertex detector prototype to address challenges in mechanical precision, cooling performance, and system-level integration.

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Glossary

AERD Address-Encoder and Reset-Decoder 27, 28
ALICE A Large Ion Collider Experiment 10, 11, 14
ALPIDE ALICE Pixel Detector 11, 14, 27, 28

BX Bunch Crossing 10

CEPC Circular Electron Positron Collider 1, 2, 5, 10, 11, 26, 28
CEPCSW CEPC Software 25, 33
CERN European Organization for Nuclear Research 10
CFRP Carbon Fiber Reinforced Polymer 6, 18–20
CIS Cmos Image Sensor 2–5, 10, 13, 14, 17, 18, 20–22, 26–32, 36, 37
CMOS Complementary Metal Oxide Semiconductor 2, 26
CVTX Curved Vertex Layer 4–6, 24, 25, 35

DAC Digital-to-Analog Converter 16, 31
Dcols Double Columns 15
DESY Deutsches Elektronen-Synchrotron 29, 30
DUT Device Under Test 29–31

FIFO First In First Out 15
FPC Flexible Printed Circuit 5, 6, 18–23

I2C Inter-Integrated Circuit 31
IBIAS bias current 16, 17
ITS Inner Tracker System 10, 11, 14

LDO Low Dropout Regulator 31
LRB Left-end Readout Block 5, 6, 12, 16, 17
LVDS Low-Voltage Differential Signaling 31

MAPS Monolithic Active Pixel Sensor 2, 10
MIMOSA Minimum Ionising MOS Active pixel sensor 28
MOSS MOnolithic Stitched Sensor 11
MOST MOnolithic Stitched sensor with Timing 11

OCT On-Chip Test 15

PCB Printed Circuit Board 18
PLL Phase-Locked Loop 31
PVTX Planar Vertex Layer 4, 6, 7, 35, 37

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940 **RHIC** Relativistic Heavy Ion Collider 10

941 **RPB** Right-end Power Block 5, 6, 12

942 **RSU** Repeated Sensor Unit 2, 4, 5, 7, 12, 13, 15–17, 35

943 **STAR** Solenoidal Tracker at RHIC 10

944 **TPSCo** Tower Partners Semiconductor Co. 11, 17

945 **VTX** Vertex Detector 4, 6, 8, 18, 22, 23, 31, 37