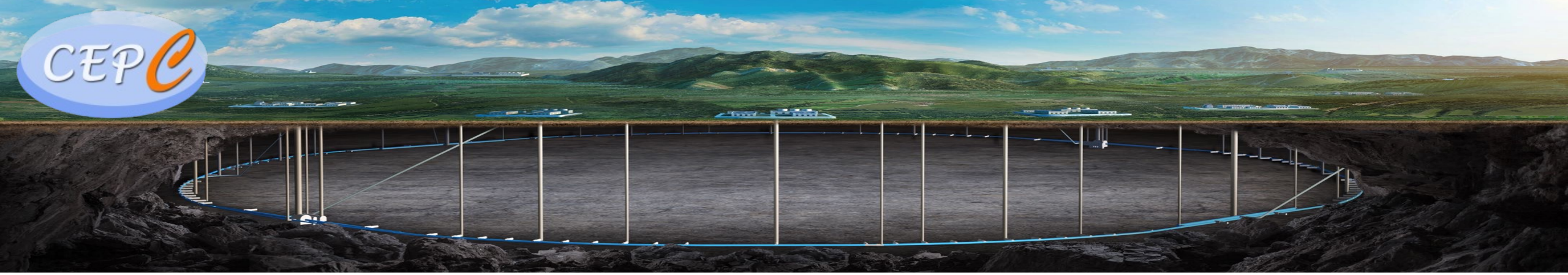


CEPC Silicon Tracker Detector

Qi Yan

On behalf of the CEPC Silicon Tracker Group

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Content

- Overview of IDRC feedback and main changes
- Detailed description of the changes
- Requirement and overall design
- Detailed design including electronics, cooling and mechanics
- Performance from simulation or beam test
- Research team and working plan
- Summary
- (in Backup) ALL the answers to Review comments

Overview of IDRC Feedback and Main Changes

- Main points from IDRC feedback:

  1) Simplification of the overview section and LGAD readout ASIC section.
  2) Emphasis on HV-CMOS pixel (ITK) and AC-LGAD (OTK) baseline design, with a lower R&D priority assigned to alternative design (e.g., CMOS strips).
  3) Carefully organization and acceleration of R&D activities for HV-CMOS pixels, AC-LGAD, and LATRIC (LGAD readout ASIC).

- Main changes implemented in response to IDRC feedback:

  1) The overview section and LGAD readout ASIC section have been simplified and reorganized.

  (e.g. most descriptions of the overall tracker system have been moved to Chapter 2).

  2) Alternative ITK and OTK design, including CMOS strips for the endcap, have been removed and assigned lower R&D priority.
  3) R&D activities are effectively addressed in the future plan sections and summarized in our “answers” to IDRC recommendations.

Detailed Description of the Changes

- Following the IDRC suggestions, the major changes to the chapter layout include:
  - Most descriptions of the overall tracker system have been moved to Chapter 2.
  - Alternative ITK and OTK designs have been removed.
  - Beam background estimation has been simplified and moved to the overview section.

- IDRC's latest feedback after this revision:
  - Concerning the chapter organization, this is significantly improved, facilitating the reading. The ITK and OTK dedicated sections … also cover the important aspects of ... removal of the alternative sensor technologies for ITK and OTK has greatly improved the draft's readability.

Version in April

Simplification

Removal of ITK endcap alternative design

Removal of OTK alternative design

Move to the overview section

Latest version

Chapter 5 Silicon Tracker

simplified

New Overview Section

5.1 Overview

To support precise measurements of Higgs boson properties and other key physics objectives, the tracking system must deliver permille-level momentum resolution for charged particles with momenta below 100 GeV/c. In addition, ToF measurements are essential for particle identification in flavor physics studies and jet substructure analyses, particularly for hadron and jet (b or c) tagging.

To meet these requirements, the baseline design of the STK includes three barrel layers and four endcap layers in the ITK, and one barrel layer and one endcap layer in the OTK, as shown in Figure 5.1. This layout enables precise determination of particle trajectories, with a bending lever arm of $\sim 1.6\,\mathrm{m}$ in the barrel region, spanning from the innermost ITK layer to the OTK. Additionally, the OTK provides precise timing measurement as a ToF detector for particle identification. The total surface area of the STK is $\sim 100\,\mathrm{m}^2$.

Each detector layer is required to achieve a spatial resolution of $10\,\mu\mathrm{m}$ or better in the bending direction. At the same time, the detector material budget must be minimized to reduce multiple scattering, which is critical for maintaining good resolution at low momenta. The material thickness per ITK layer is constrained to be $< 1\%$ of a radiation length (X_0), while the OTK allows slightly more material, as it is the outermost tracking layer.

To meet these constraints, the ITK adopts $150\,\mu\mathrm{m}$ thick monolithic CMOS sensor, which integrates both the sensor and readout circuitry on a single chip. Under the high-luminosity Z-pole operation with 23 ns bunch spacing, a timing resolution of a few nanoseconds or better is required for bunch tagging. Accordingly, monolithic High Voltage Complementary Metal-Oxide-Semiconductor (HV-CMOS) pixel sensor technology is

…

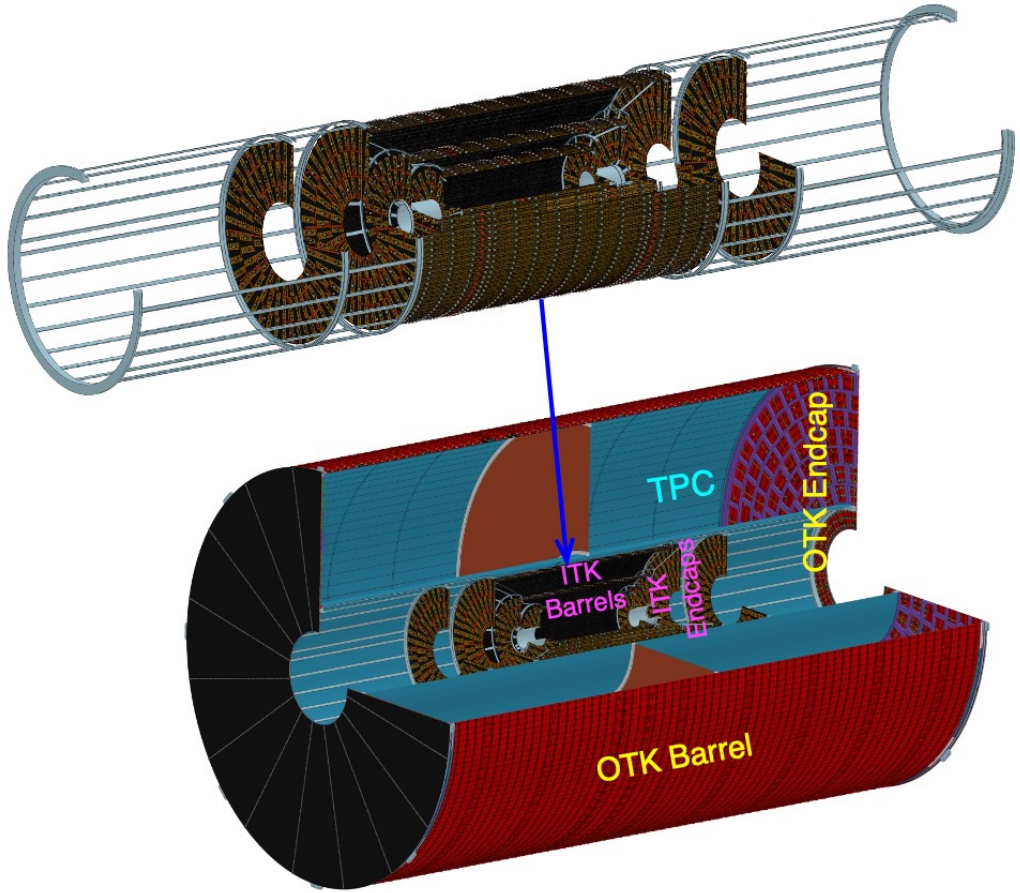
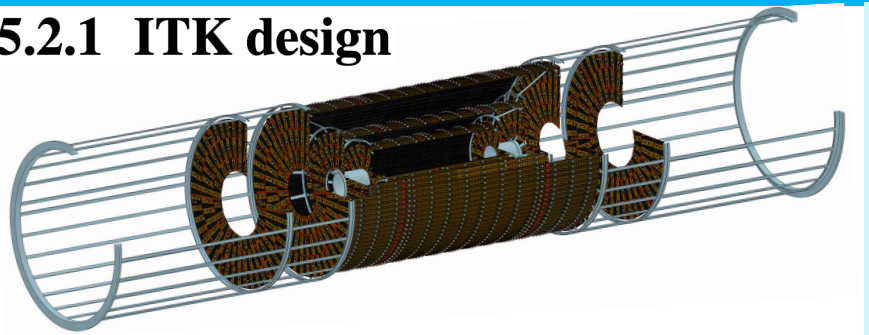


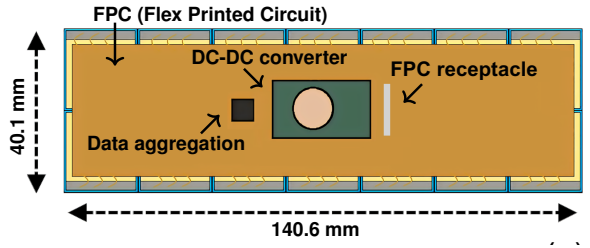
Figure 5.1: Layout of the Silicon Tracker (ITK and OTK). The ITK consists of three barrel layers and four endcap layers, together with two extended connection rings, forming the complete ITK assembly that is inserted into the inner barrel of the TPC. The OTK, as the outermost component of the tracker system, includes one barrel layer and one endcap layer, mounted outside of the TPC. It provides both high-precision spatial and timing measurements.

Summary of ITK Design Based on HV-CMOS Pixel Sensor

5.2.1 ITK design



- Three barrel and four endcap layers (~20 m^2).
- HV-CMOS sensor COFFEE2 has verified the sensor process and in-pixel analog front-end.
- The latest COFFEE3 sensor, submitted for tape-out in Jan and received in May 2025, is currently undergoing testing.



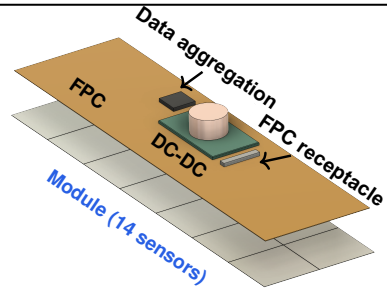
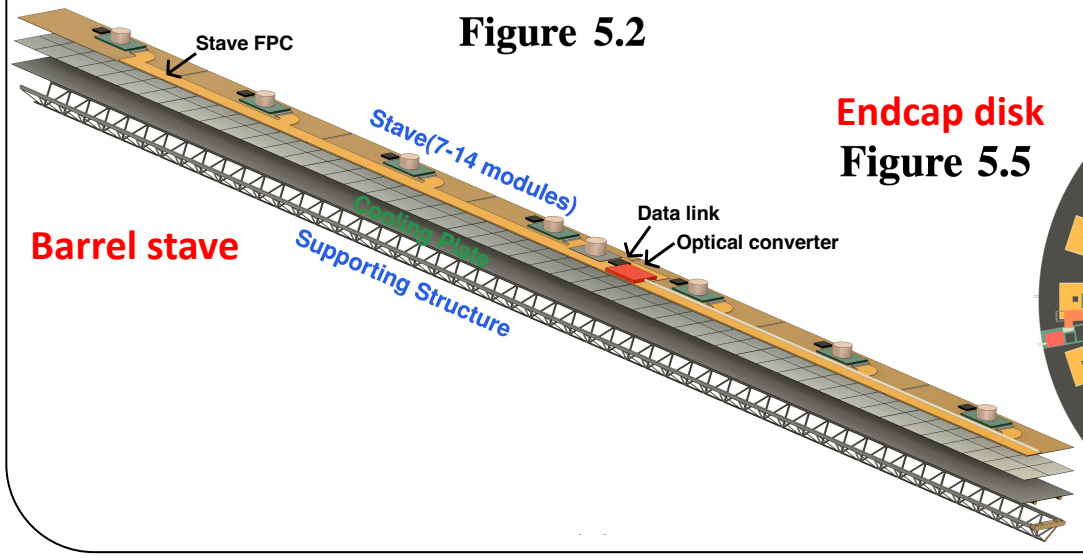
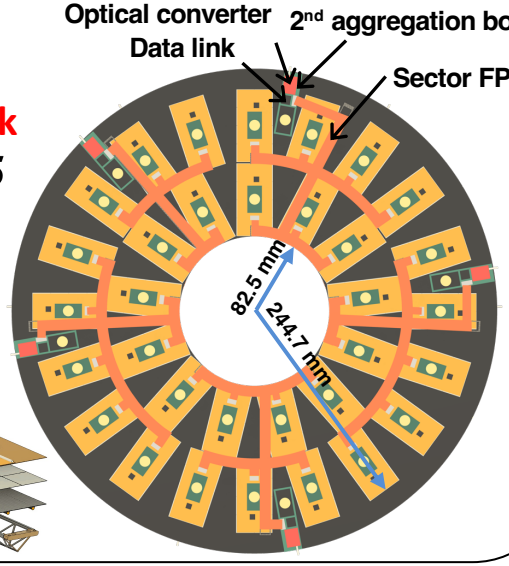


Figure 5.2



Endcap disk

Figure 5.5



HV-CMOS sensor prototype (COFFEE3)

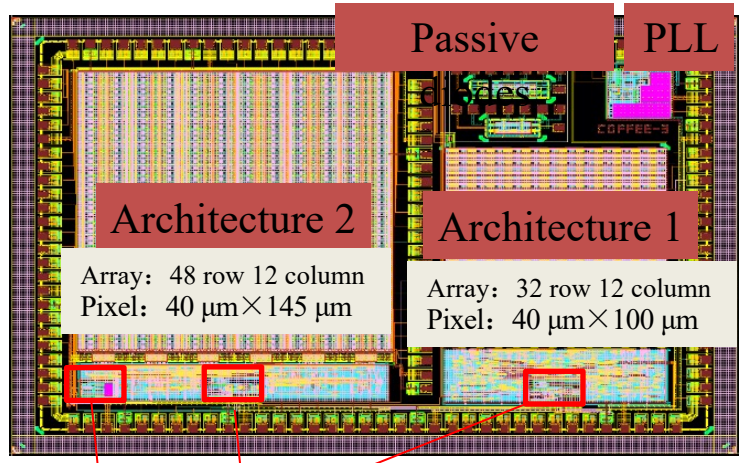


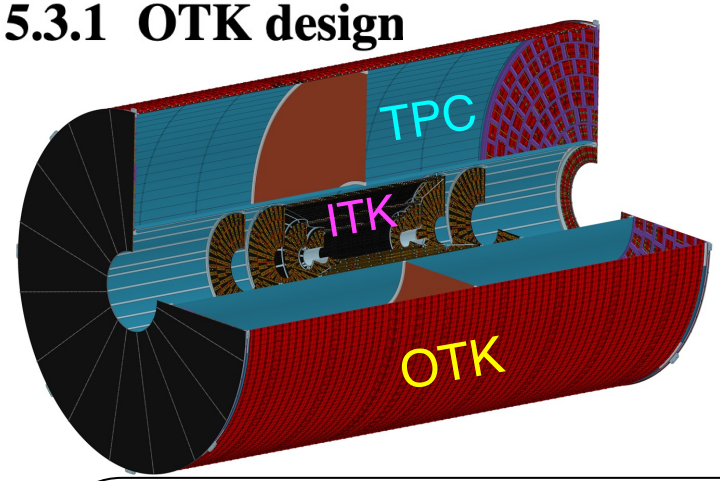
Figure 5.21

HV-CMOS sensor specification for ITK	
Sensor size	2 cm × 2 cm
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Timing resolution	3-5 ns
Power	200 mW/cm²
Process node	55 nm

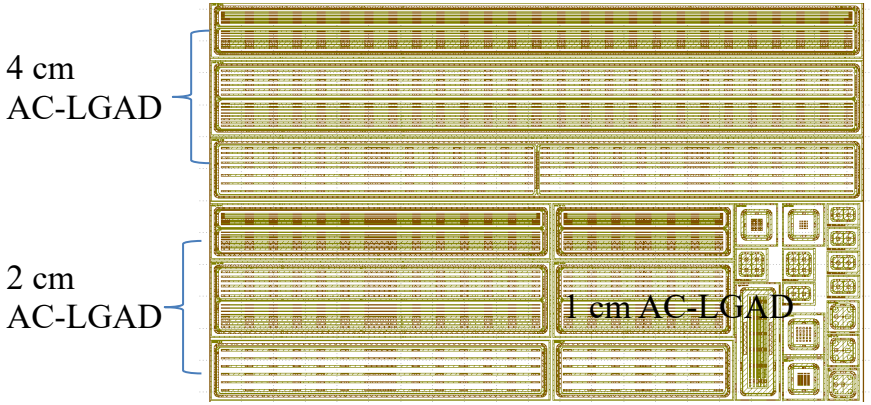
Table 5.3

Summary of OTK Design Based on LGAD Strip Sensor

5.3.1 OTK design



AC-LGAD prototype (latest submitted)



- One barrel layer and one endcap layer (~85 m^2).
- The latest LGAD sensor was submitted for tape-out in March and waiting for the return.

LGAD sensor specification for OTK	
Sensor size	(3-4.5) cm × (3-5) cm
Strip pitch	~100 μm
Spatial resolution	10 μm
Timing resolution	50 ps
Power	300 mW/cm^2

Barrel

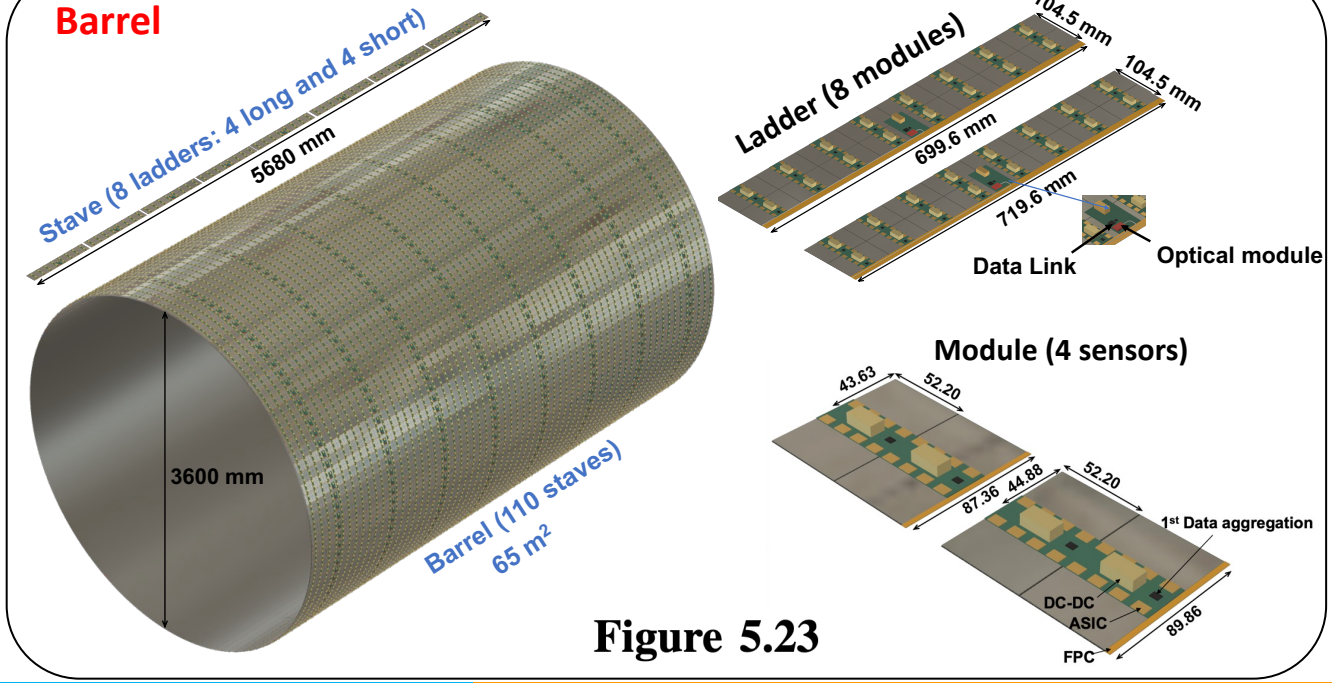


Figure 5.23

Endcap

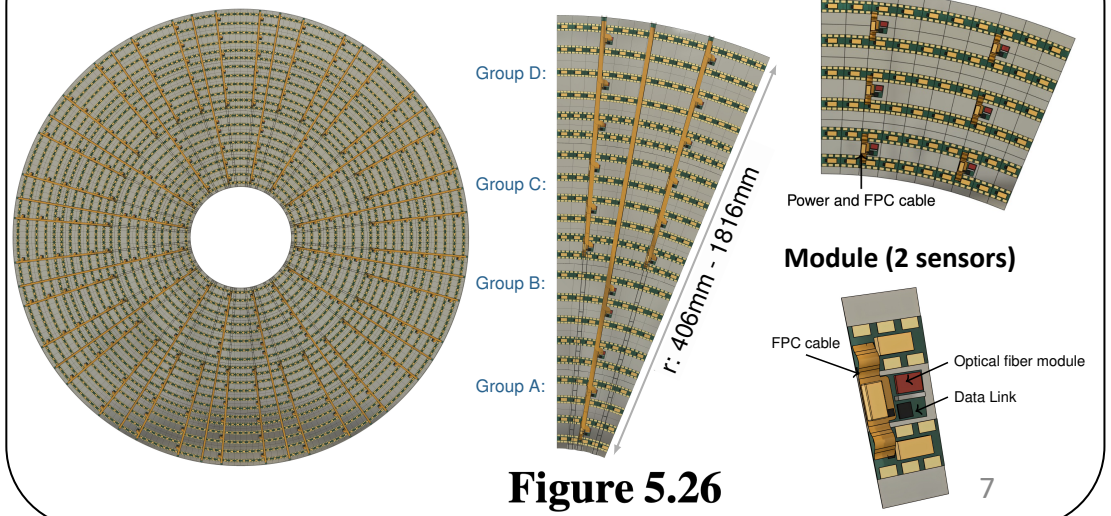
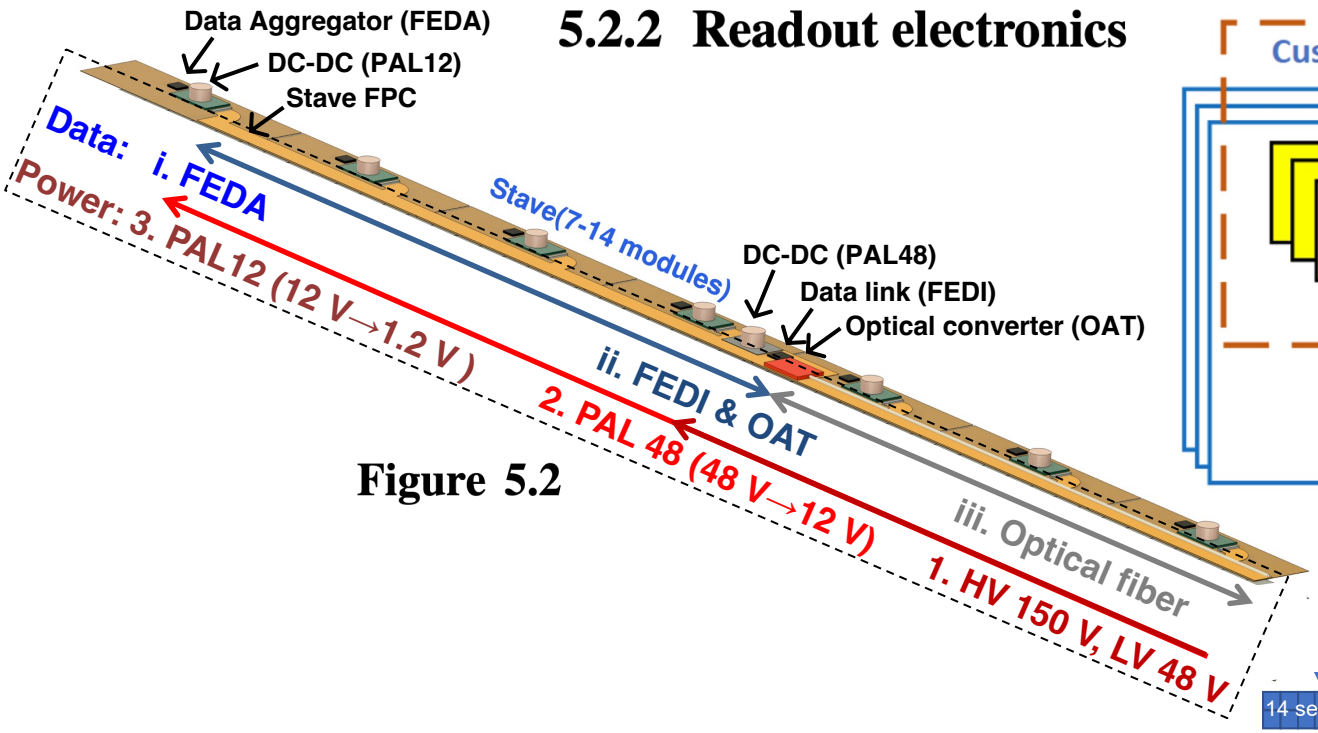


Figure 5.26

Design Including Power and Readout Electronics



5.2.2 Readout electronics

Figure 5.2

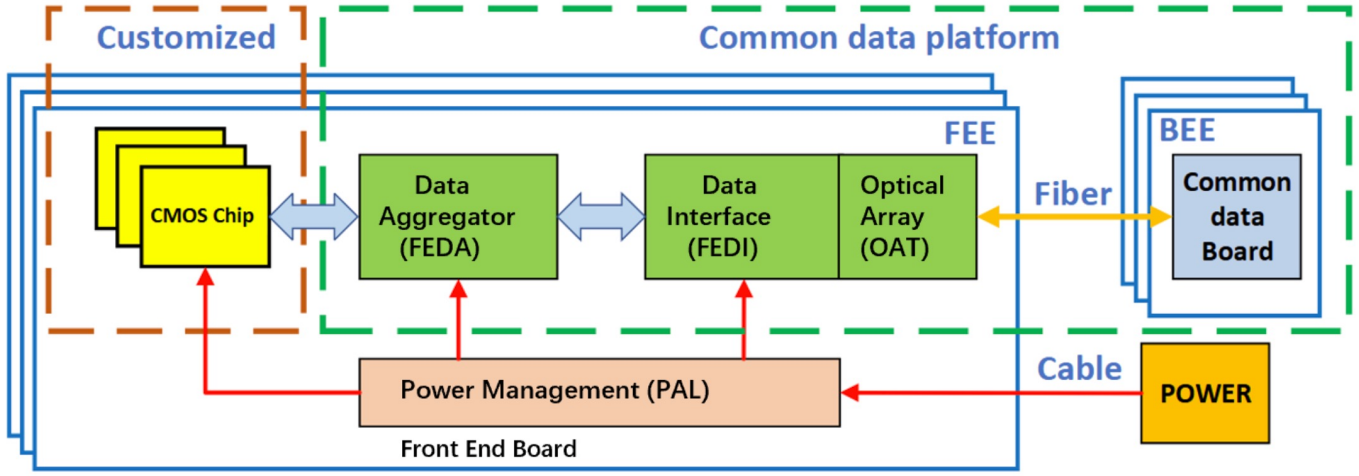


Figure 5.6

- In the readout design, each sensor can tolerate up to 86.67 Mbps, corresponding to a maximum hit rate of 4.1×10^5 Hz/cm^2 – about 42 times higher than the estimated peak background hit rates (9.9×10^3 Hz/cm^2) under the most challenging high-luminosity Z-pole operation mode.

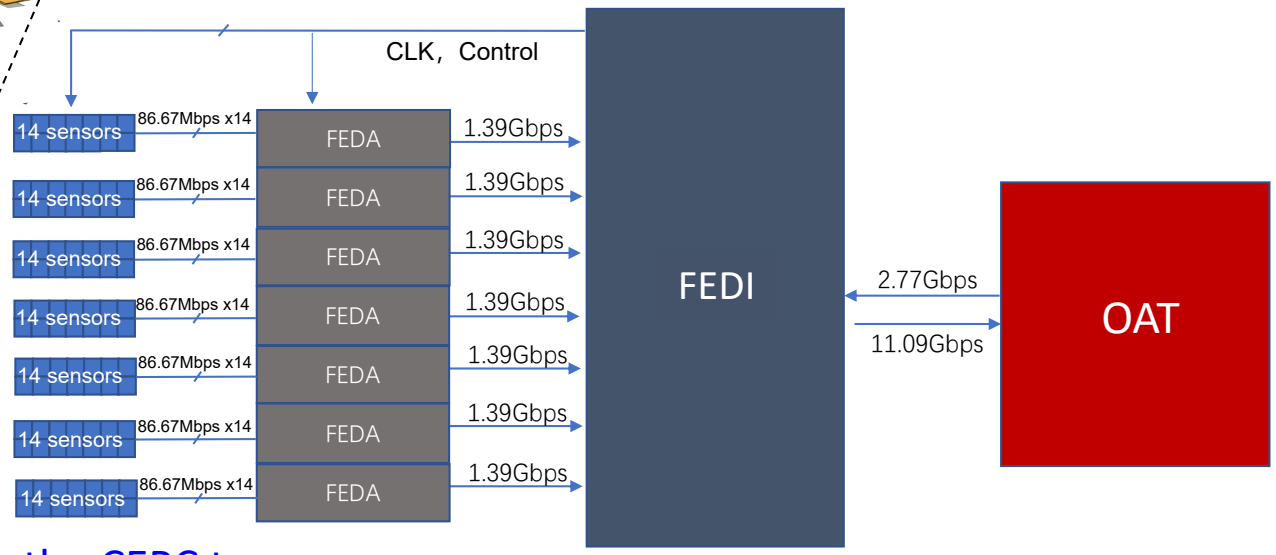


Figure 5.7

The FEDA, FEDI, OAT, and PAL chips are under development by the CEPC team.

Design Including Cooling and Mechanics

5.2.3 Mechanical and cooling design

ITK Barrel stave

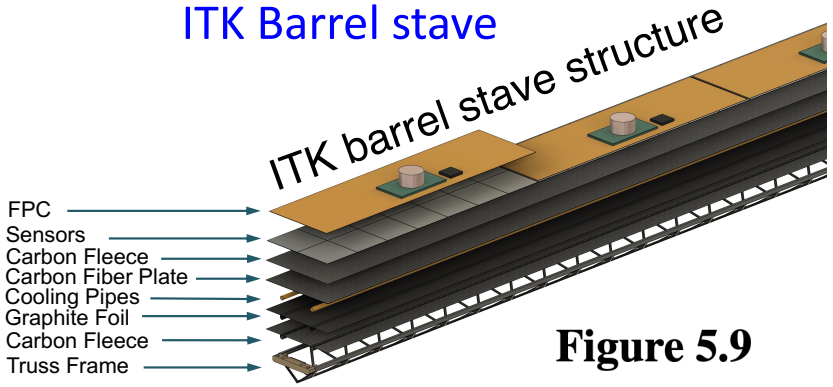


Figure 5.9

5.3.3 Mechanical and cooling design

OTK endcap 1/16 sector

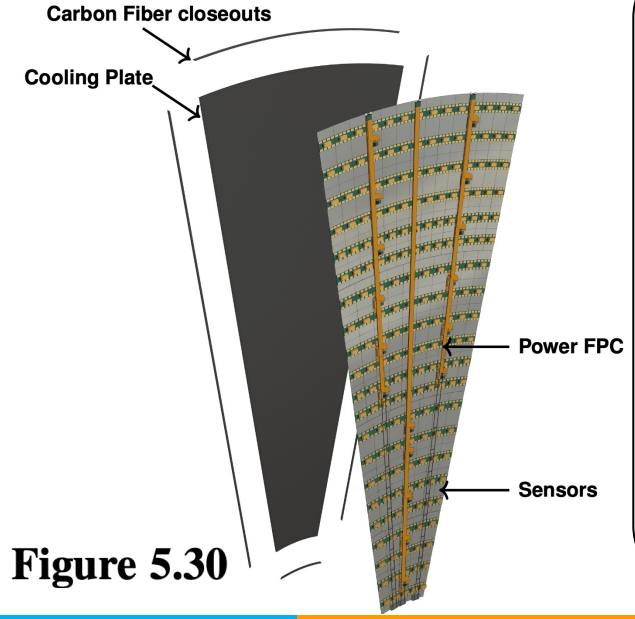


Figure 5.30

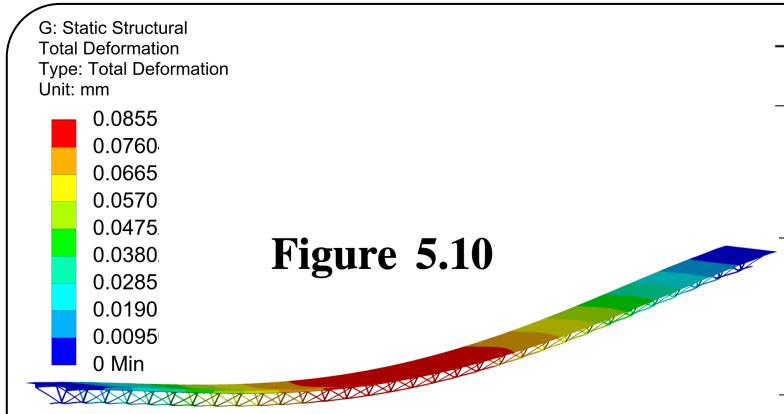


Figure 5.10

Maximum sag of first ITK barrel stave is 85 µm.

Table 5.6

Functional unit	Component	Material	Thickness [µm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	150	28.41	0.053
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64†	28.41	0.006
	Cooling fluid	Water		35.76	0.028
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Truss Frame	Carbon rowing				0.080
Power Bus FPC					0.070
Total					0.677

40 coil layer cooling loops

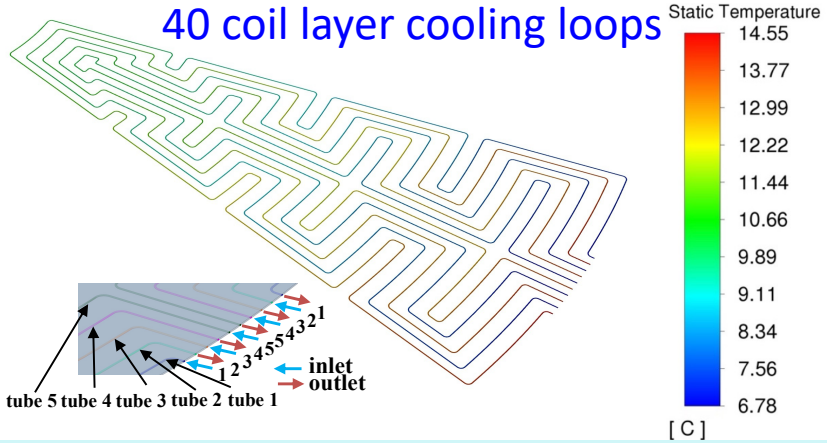
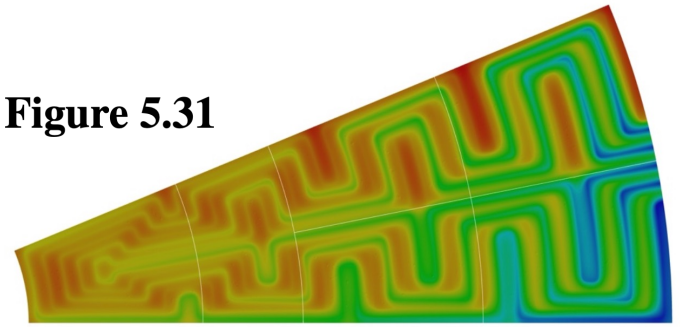


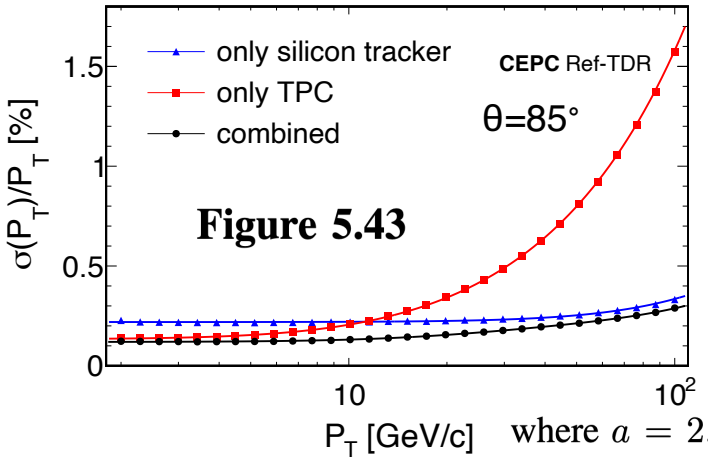
Figure 5.31



- The OTK endcap 1/16 sector uses 5-loop water cooling pipes with a pipe inner diameter of 2.3 mm, a flow velocity of 2 m/s, and an inlet temperature of 5°C. The sensor temperature is <15°C and senor temperature gradient is <4°C.

Performance

Momentum resolution in the barrel region:



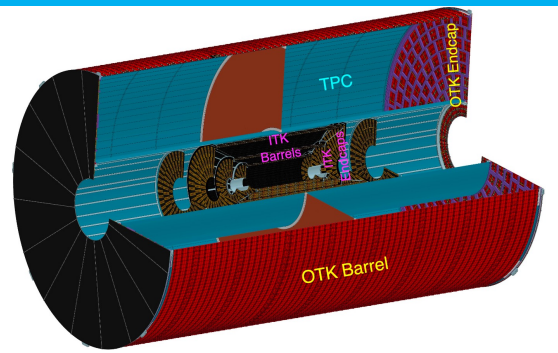
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Si}} = ap_t \oplus \frac{b}{\beta\sqrt{\sin\theta}}$$

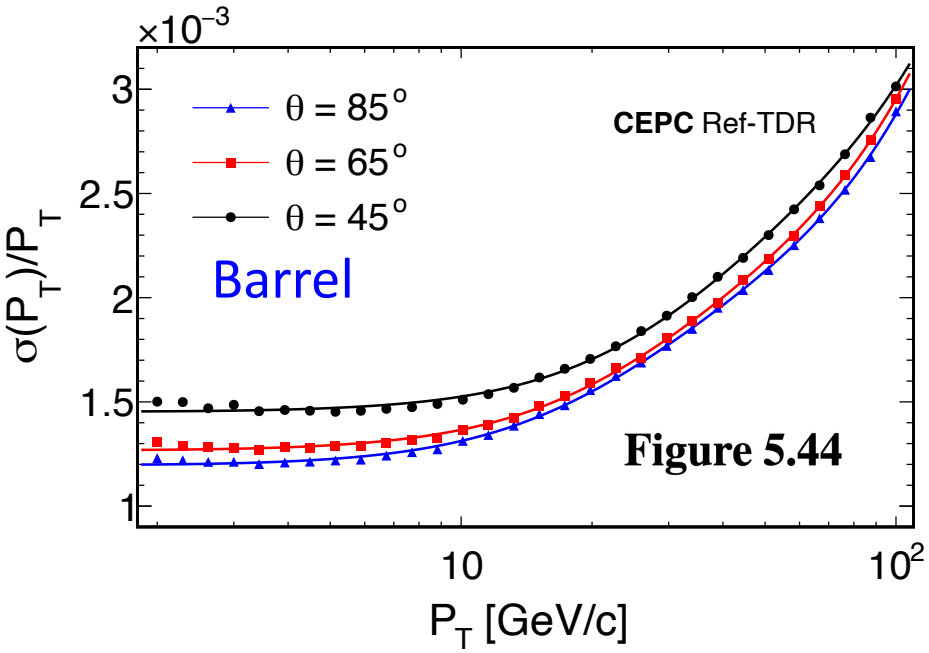
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{TPC}} = as_1 p_t \oplus \frac{bs_2}{\beta\sqrt{\sin\theta}}$$

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Combined}} = \frac{1}{\sqrt{\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Si}}^{-2} + \left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{TPC}}^{-2}}}$$

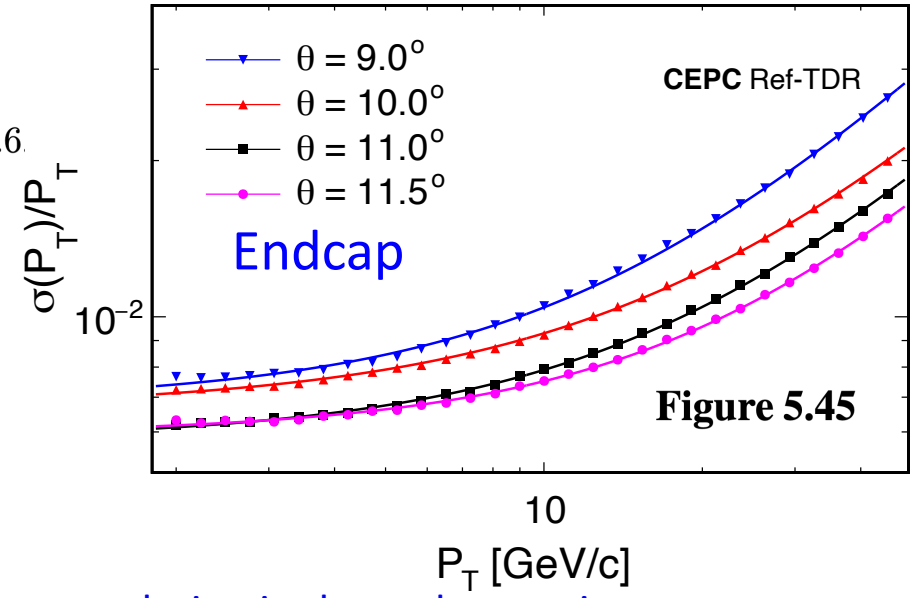
where $a = 2.1 \times 10^{-5}$, $b = 2.2 \times 10^{-3}$, $s_1 \approx 4$, and $s_2 \approx 0.6$

- Full simulation: systematic study of the tracker design and its performance





5.5 Performance



Momentum resolution in the endcap region:

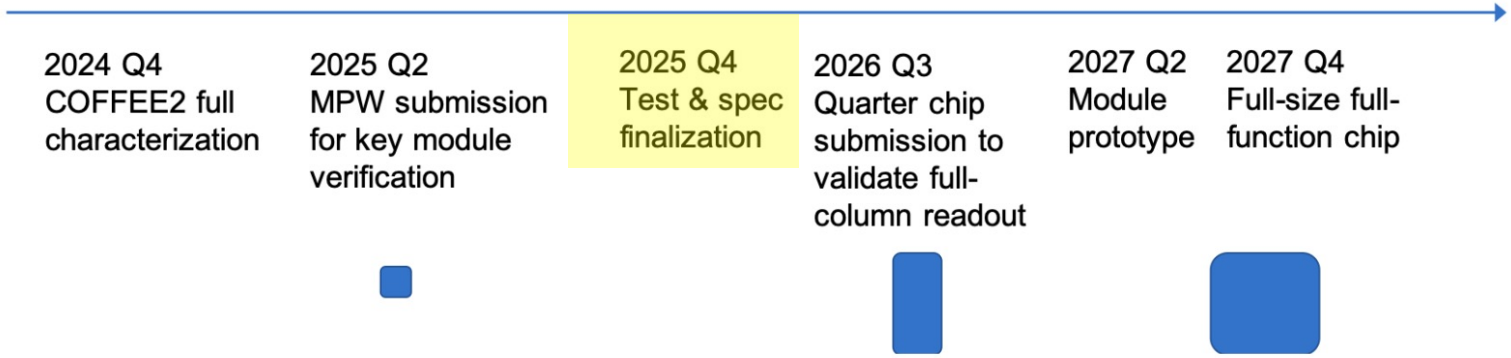
$$\frac{\sigma_{p_t}}{p_t} = \frac{a' p_t}{(tan\theta)^2} \oplus \frac{b'}{\beta tan\theta\sqrt{\cos\theta}} \oplus \frac{c'\sqrt{p_t}}{\sqrt{\beta}(\tan\theta)^{\frac{3}{2}}(\cos\theta)^{\frac{1}{4}}}$$

where $a' \approx 1.1 \times 10^{-5}$, $b' \approx 1.1 \times 10^{-3}$, and $c' = 1.2 \times 10^{-4}$

R&D Plan Following the Ref-TDR

5.2.5 Future plan

- HV-CMOS pixels:



5.3.6 Future plan

- AC-LGAD strips+ASIC:

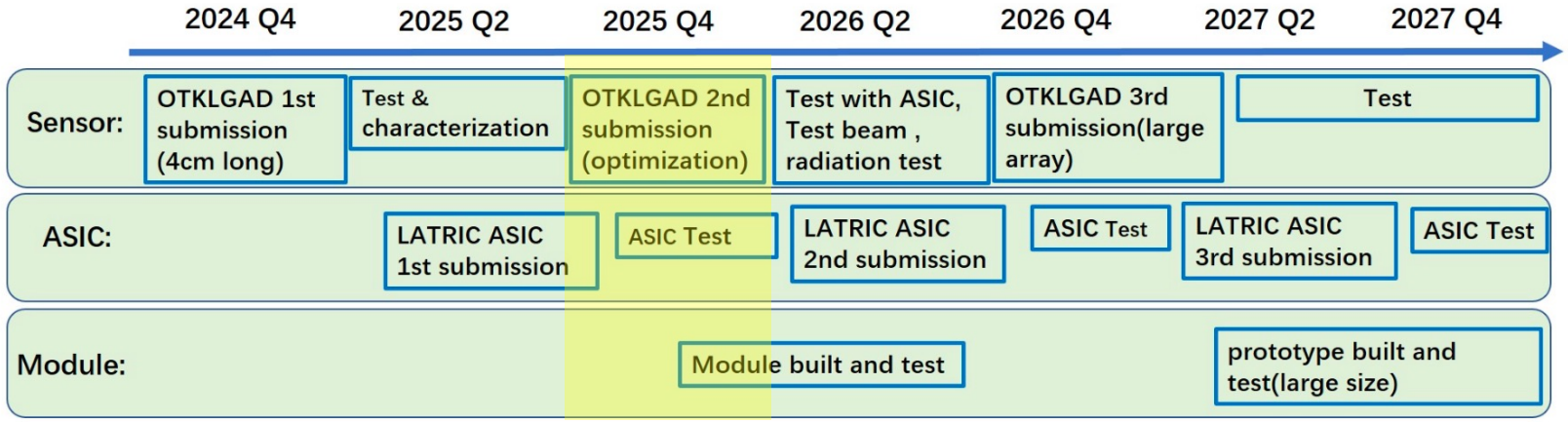
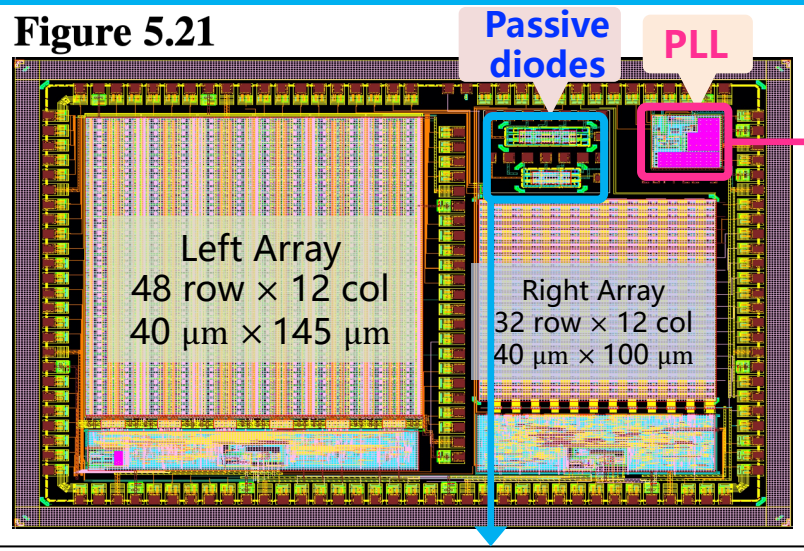


Figure 5.42

Development of the mechanical and cooling systems is progressing in parallel, with the goal of delivering a prototype detector by the end of 2027.

Update R&D Progress on HV-CMOS Pixel Sensor (1)

Figure 5.21

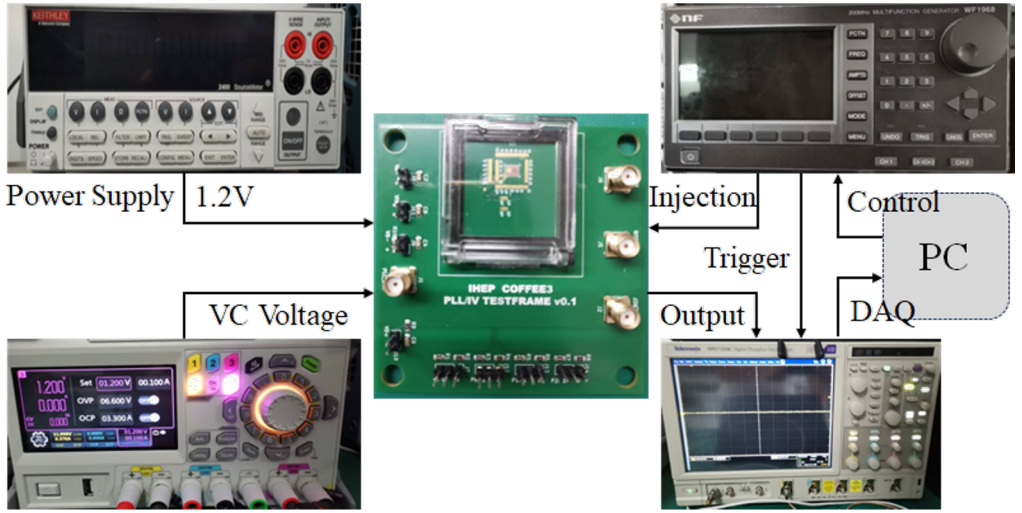


COFFEE3 sensor received at the end of May

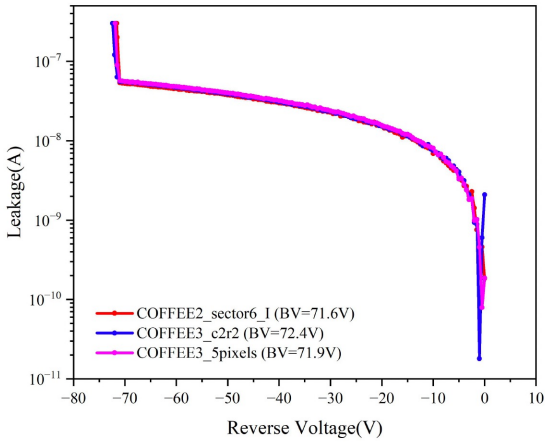
Task list:

- [✓] IV
- [✓] CV
- [✓] Radioactive source
- [✓] VCO (Voltage Controlled Oscillator)
- [✓] Divider

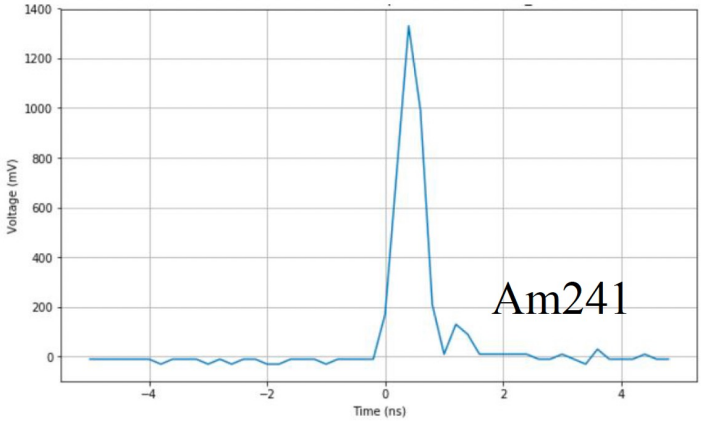
PLL: A new module for clock synchronization, providing up to 320 MHz output from a 40 MHz input (higher output limited by the test setup).



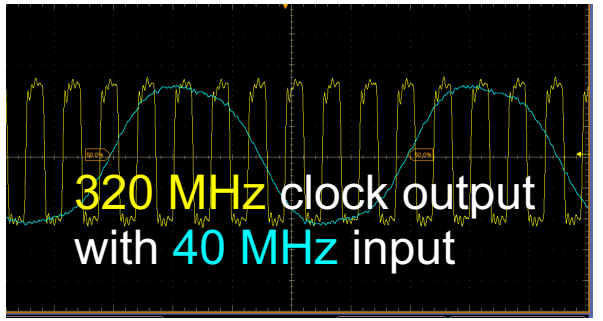
Passive diode array: validation of sensor performance; test result consistent with COFFEE2.

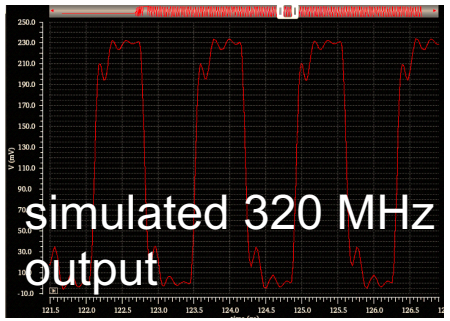


Breakdown voltage: -71V

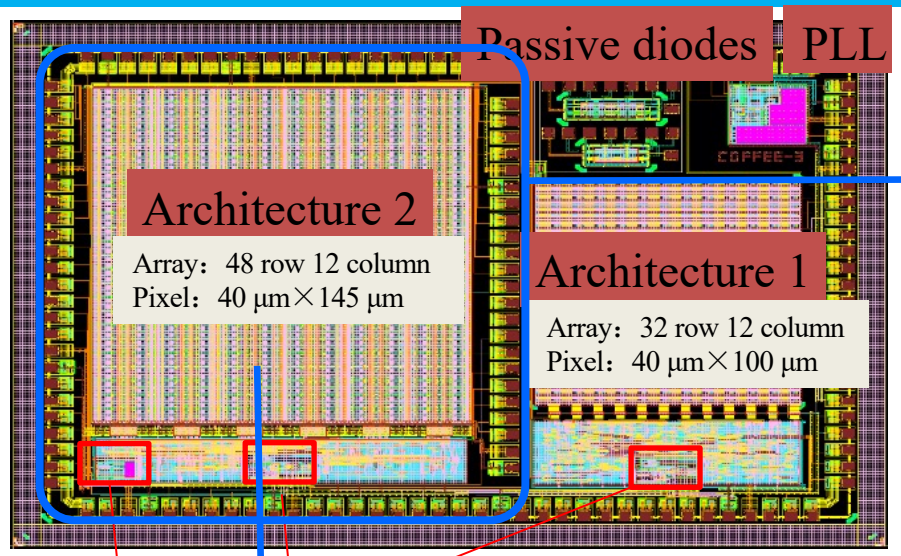


Responsive to α radioactive source



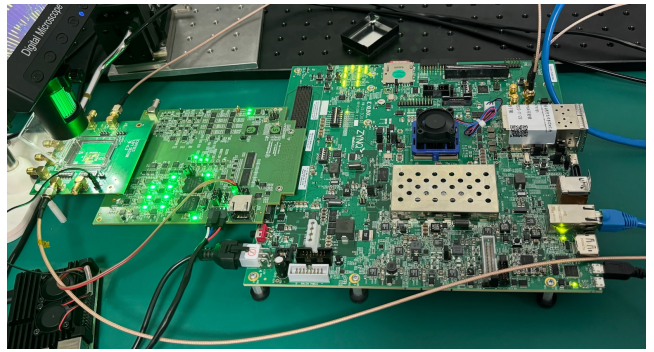


Update R&D Progress on HV-CMOS Pixel Sensor (2)



Left pixel array: the readout architecture fully exploits the 55nm process potential, including in-pixel TDC.

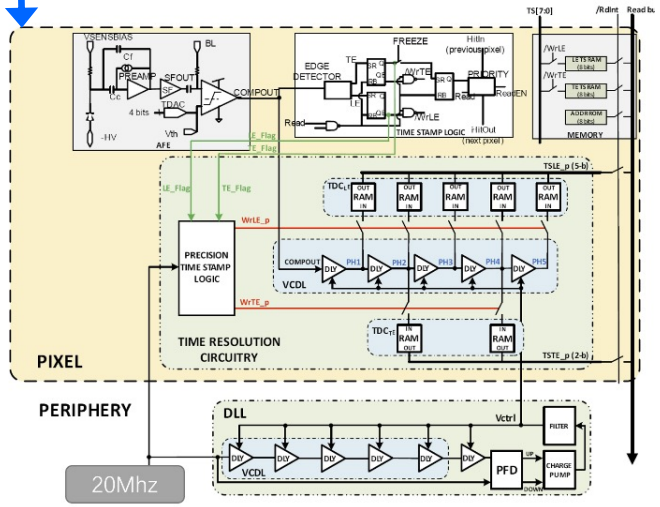
Testing units:
- In-pixel TDC
- Column readout
- LVDS driver
- …



Dedicated test PCB + Caribou readout board

Active contributor in Caribou user community → Improving & debugging with latest FPGA and software versions

In-pixel Coarse-Fine TDC

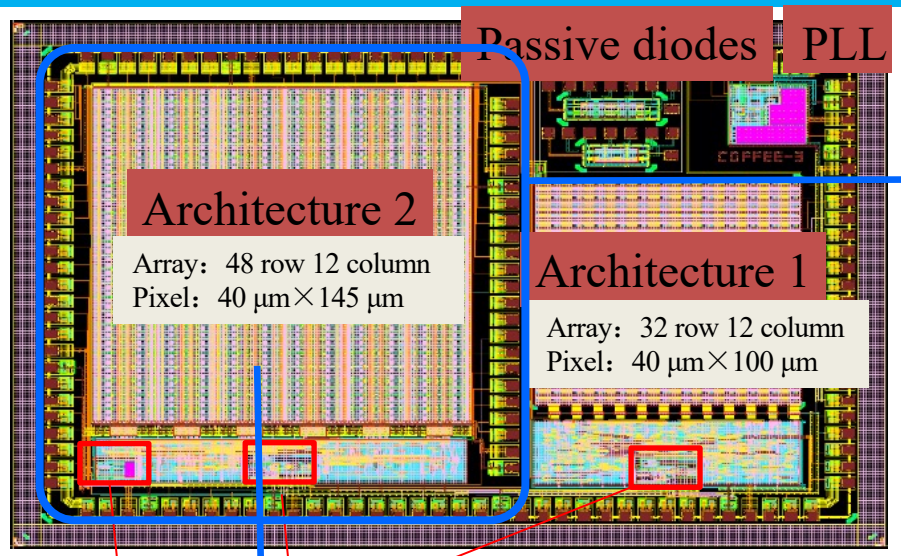


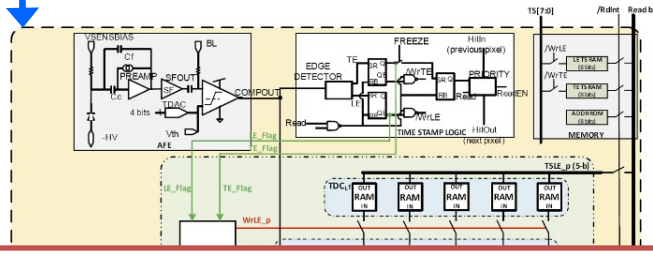
The pixel array has been configured, and the working point is being tuned to achieve optimal response for subsequent tests.

Task list:

[✓] SPI configuration
[…] In-pixel circuit validation
[…] Digital periphery validation
[…] Performance studies (timing, power, etc.)

Update R&D Progress on HV-CMOS Pixel Sensor (2)

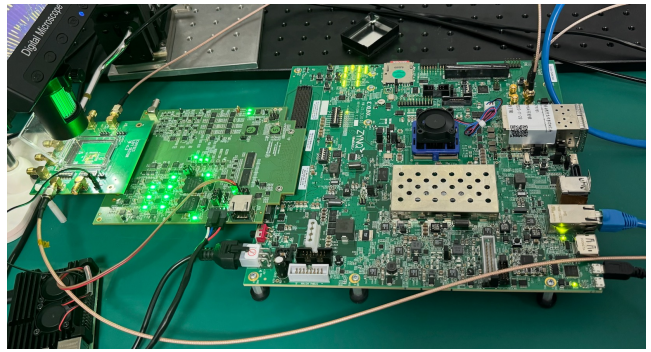




In-pixel Coarse-Fine TDC

Left pixel array: the readout architecture fully exploits the 55nm process potential, including in-pixel TDC.

Testing units:
- In-pixel TDC
- Column readout
- LVDS driver
- …



Dedicated test PCB + Caribou readout board

Active contributor in Caribou user community → Improving & debugging with latest FPGA and software versions

The pixel array has been configured, and the working point is being tuned to achieve optimal response for subsequent tests.

Task list:

- This study is to address the IDRC recommendation:
  - R-A-5-2: We strongly encourage prioritizing the COFFEE3 validation campaign… successful testing of COFFEE3 would constitute a critical milestone for the CEPC silicon tracking system, helping to de-risk the ITK concept …

Update R&D Progress on LGAD ASIC

The first LATRIC prototype, LATRIC-V0, submitted for tape-out in April, was wire bonded and delivered to IHEP on Aug 25:

- The ASIC integrates a pre-amplifer, a discriminator, a TDC, and a serializer for data output.
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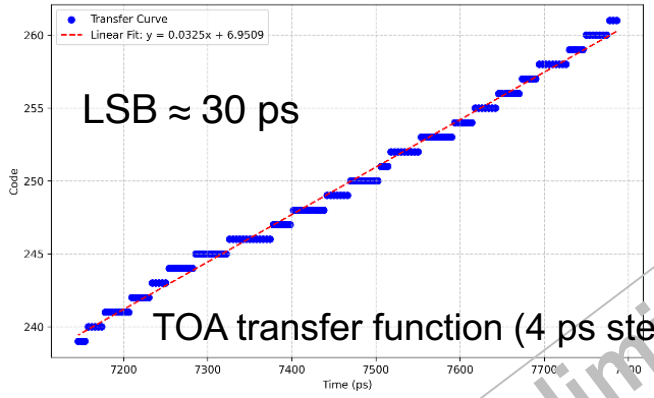
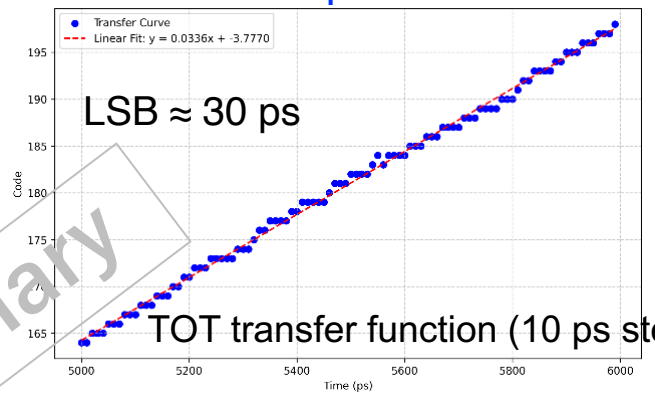
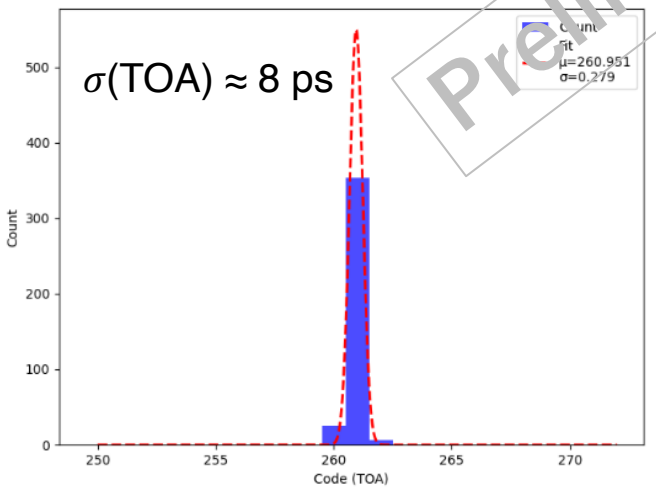
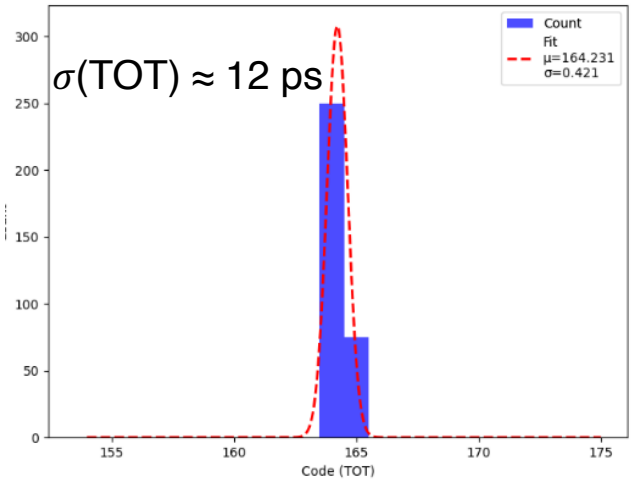
- More in-depth tests are on-going.

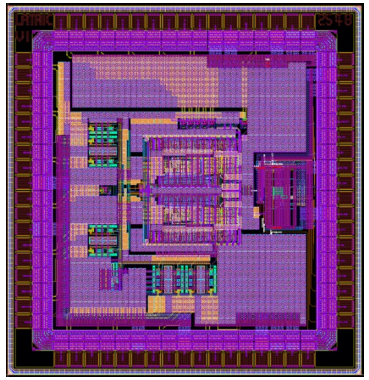
The next 8-channel LATRIC-V1 is scheduled for tape-out in October.



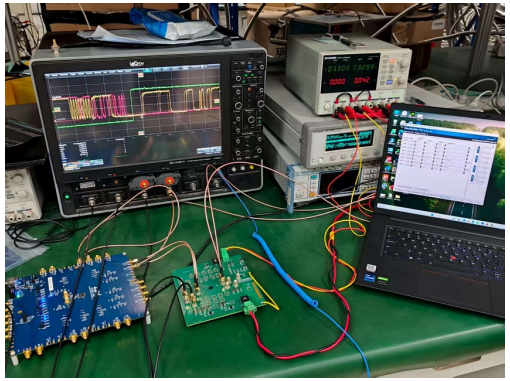


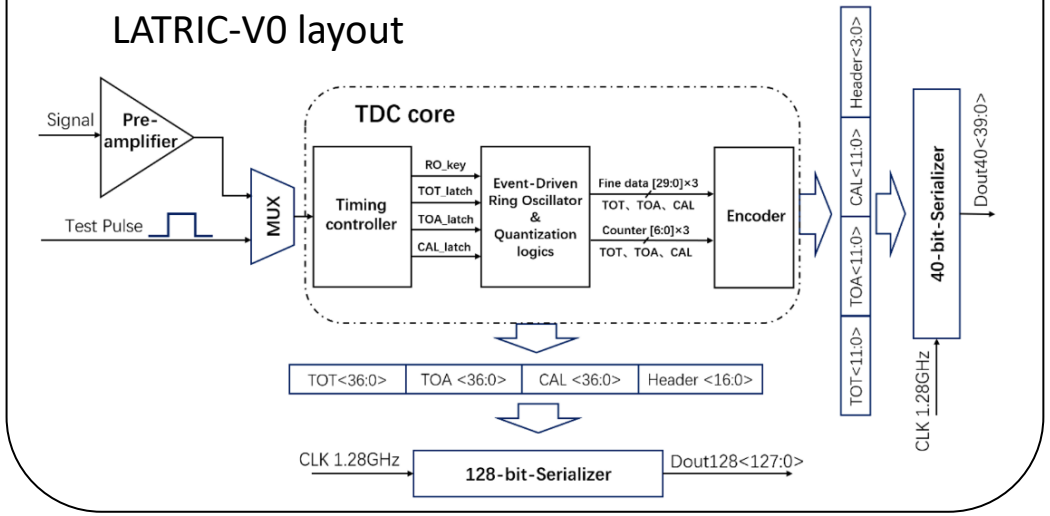






LATRIC-V0 layout



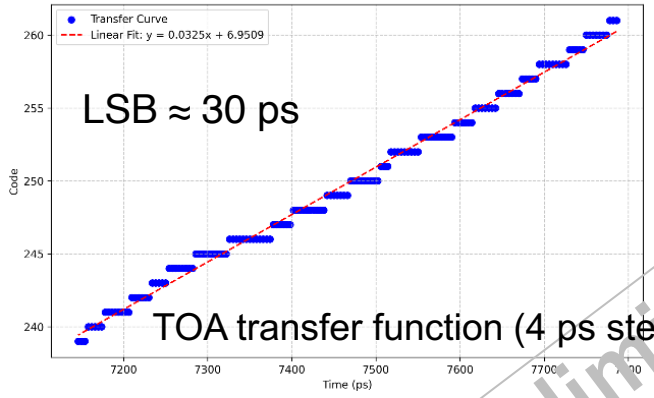


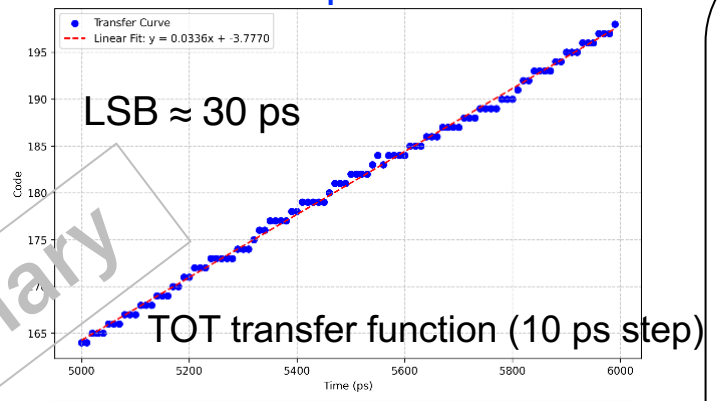
Update R&D Progress on LGAD ASIC

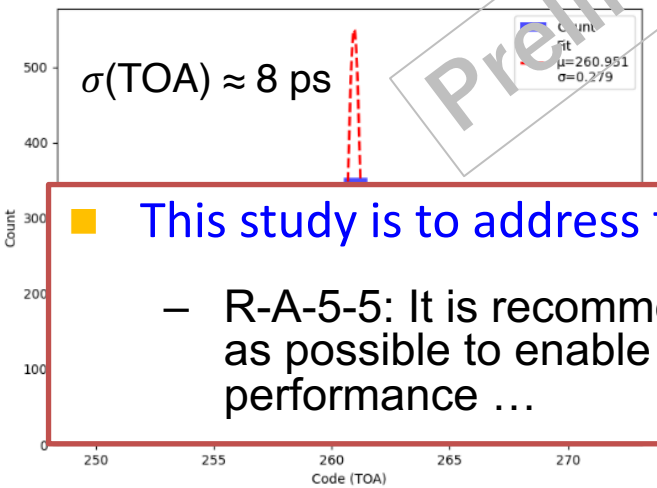
The first LATRIC prototype, LATRIC-V0, submitted for tape-out in April, was wire bonded and delivered to IHEP on Aug 25:

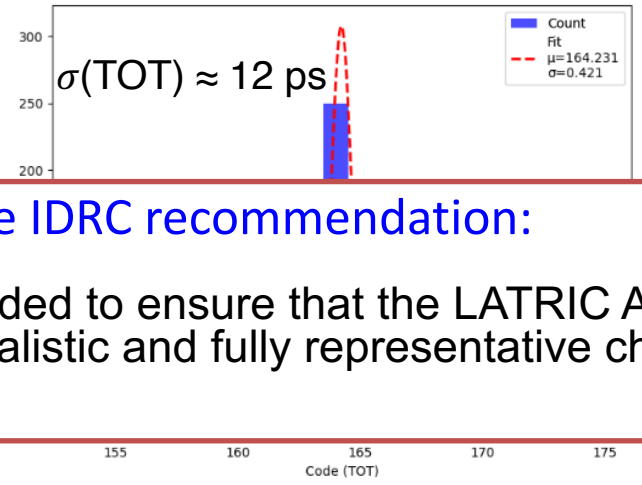
- The ASIC integrates a pre-amplifer, a discriminator, a TDC, and a serializer for data output.
- Preliminary tests find that the LSB is 29.8 ps, meeting the 30 ps design goal. The measured TDC power consumption is 0.1 mA (1.2 V) @ 0.5 MTPS (Mega-Trigger Per Second), 0.3 mA @ 1 MTPS, and 0.5 mA @ 2 MTPS, agreeing with the design.
- More in-depth tests are on-going.

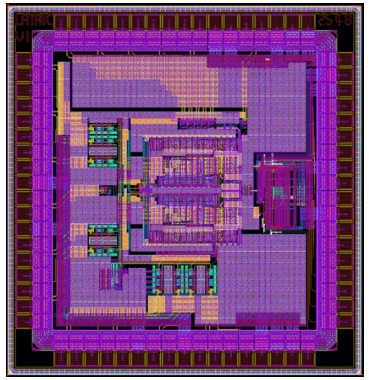
The next 8-channel LATRIC-V1 is scheduled for tape-out in October.



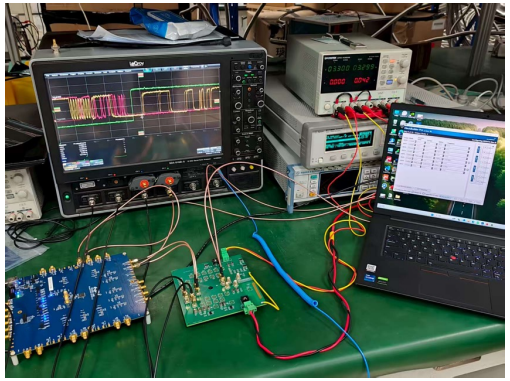


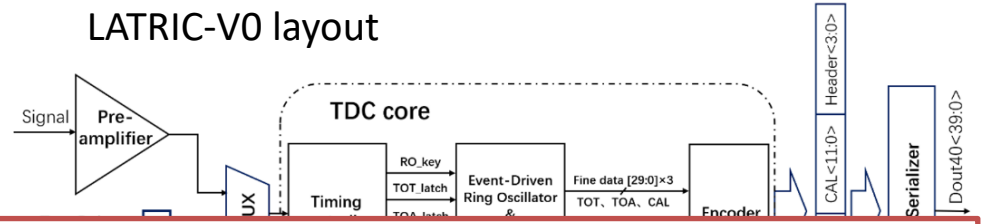






LATRIC-V0 layout

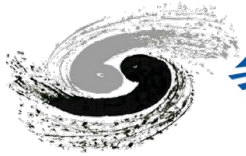


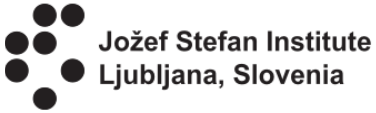


- This study is to address the IDRC recommendation:
  - R-A-5-5: It is recommended to ensure that the LATRIC ASIC is made available for sensor bonding as early as possible to enable realistic and fully representative characterization of the AC-LGAD sensor performance …

Our Research Team

- Currently active: 29 institutes, 50 staff, and 50+ postdocs & students





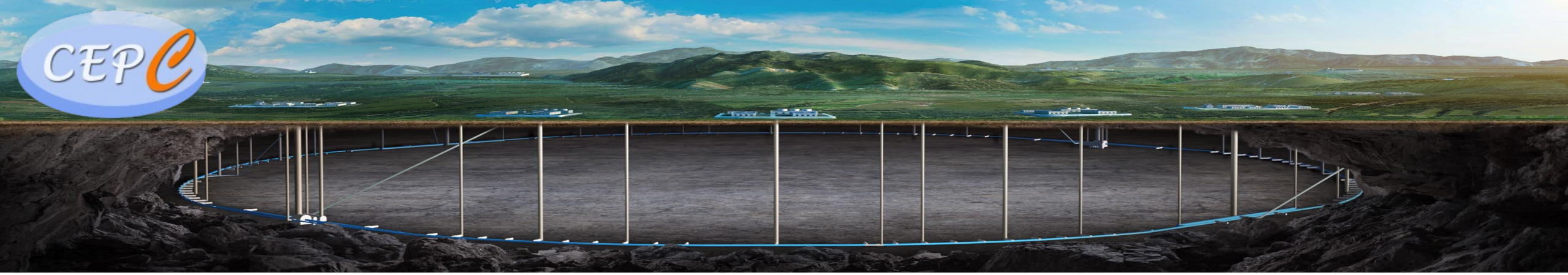
We welcome collaborations with more domestic research institutions and partners worldwide!

Summary

- The complete design of the Silicon Tracker and the latest R&D progress, along with the main revisions in response to IDRC comments on the Ref-TDR, have been presented.

- Our next major focus will be on R&D, aiming key technology achievements and prototype detector development. Ongoing efforts in sensor technology, readout electronics, mechanical prototypes, and cooling systems are steadily advancing toward this goal.

- These advancements are crucial to meet the stringent performance requirements of the CEPC Silicon Tracker and ensuring the overall success of the CEPC project.



Answers to IDRC Feedback

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Inner Tracker (ITK)

Recommendations

- R-A-5-1: Given the limited resources available for R&D and the increased complexity associated with the CMOS strip-based solution for the ITK endcap, we recommend a careful evaluation of the merit and timing of continuing this development. The CMOS strip approach remains a promising technological direction; however, it may be appropriate to continue work at a lower priority to preserve long-term potential, while focusing current resources on advancing the baseline HV-CMOS pixel system.

The CMOS strip approach has merit, for example in the simplicity of its readout architecture and the availability of high-resistivity silicon wafers in the 180 nm process. However, its maturity is currently much lower compared to the HV-CMOS pixel technology.

As indicated in our previous Ref-TDR draft, the CMOS strip was presented only as a backup or alternative option. In line with the Referee's suggestion, we have assigned a lower priority to CMOS strip R&D and will primarily focus our resources on advancing the HV-CMOS pixel baseline. Accordingly, all content related to CMOS strips has been removed from the current Ref-TDR to ensure a clear focus on the HV-CMOS baseline.

Recommendations

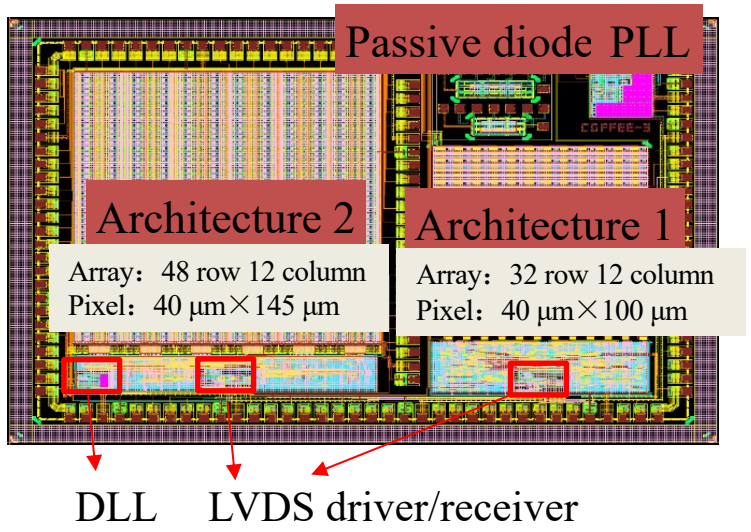
- R-A-5-2: We strongly encourage prioritizing the COFFEE3 validation campaign. As a comprehensive integration of position sensing and timing capabilities within a monolithic HV-CMOS technology, successful testing of COFFEE3 would constitute a critical milestone for the CEPC silicon tracking system, helping to de-risk the ITK concept and validate the soundness of the baseline detector design.

We are fully aware of the importance of the COFFEE3 validation. The latest COFFEE3 sensor was received at the end of May, and the test campaign was launched immediately upon receipt.

Several aspects of COFFEE3 have already been validated, and the remaining tests are currently in progress. The initial results are encouraging, and to date, no critical design issues with the sensor have been identified.

COFFEE3 Test Setup

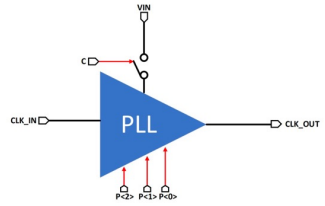
COFFEE3 incorporates two readout architectures, both featuring nearly a complete ASIC readout framework. This solution can be extended to final chip.

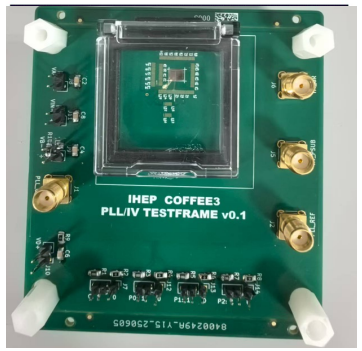


- **Architecture 1:** An optimized design framework based on the current process conditions (Triple-well process)；
- **Architecture 2:** An improved solution that requires process modification (Deep P-well required) to fully utilize the advantages of the 55 nm process node.

PLL (and IV) Test Board

- Mostly for PLL block only





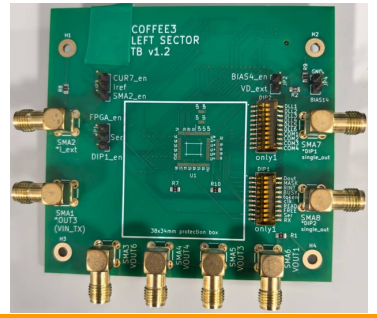
- SPI config between the FPGA and the CMOS matrix EOC
- power supply from Caribou DAQ
- reference voltage/current from Caribout to CMOS matrix
- 4 pixel CSA output from CMOS matrix => SMA cable => osc. scope
- ~10 Digitial signal output from EOC
- 6 DLL output
- LVDS Transceiver test between EOC and DAQ
  - Tx and Rx driver study
  - digital circuits for data serializer

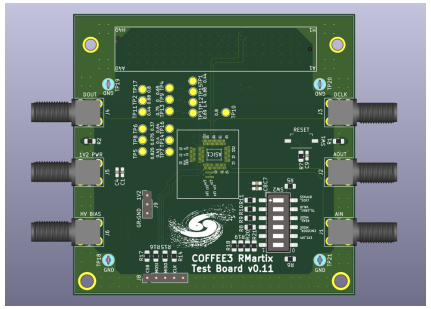
Caribou DAQ at IHEP

- both ZC706 and ZCU102 running fine with CaR boards

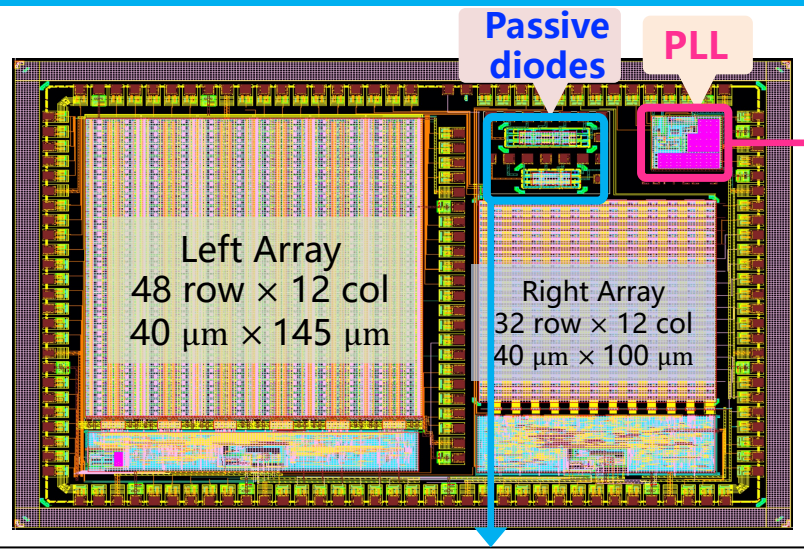
Left and Right Matrix Test Board

- Test Board (TB) designs for left and right matrix separately
- COFFEE3 left matrix is under test: laser, responce scan, SPI communication...





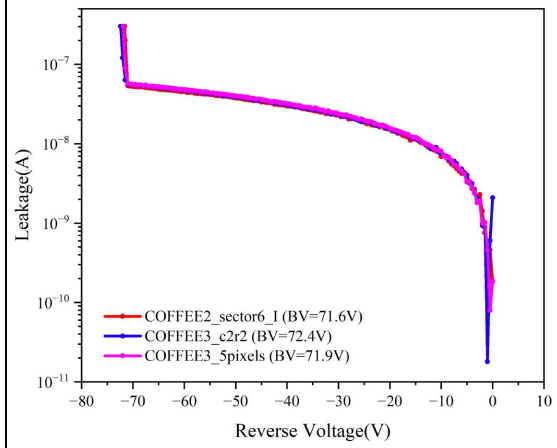
Tests of Passive Diode Array and PLL (COFFEE3)



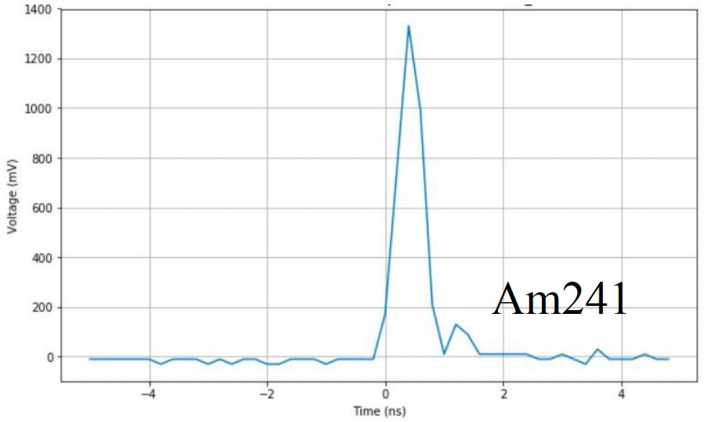
Task list:

- [✓] IV
- [✓] CV
- [✓] Radioactive source
- [✓] VCO (Voltage Controlled Oscillator)
- [✓] Divider

Passive diode array: validation of sensor performance; test result consistent with COFFEE2.

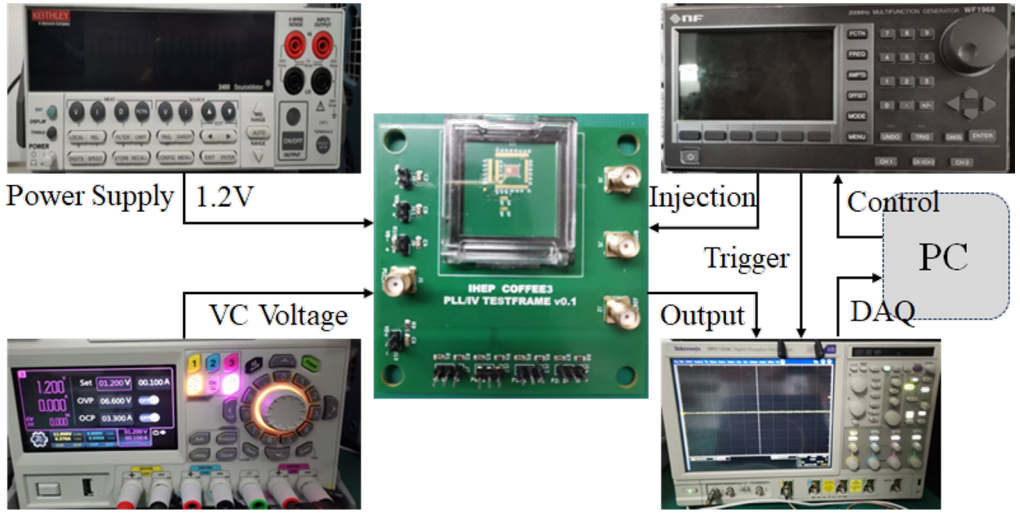


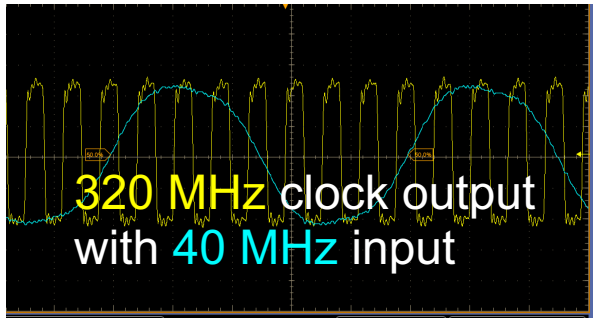
Breakdown voltage: -71V

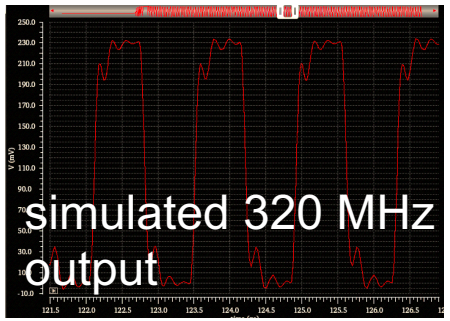


Responsive to α radioactive source

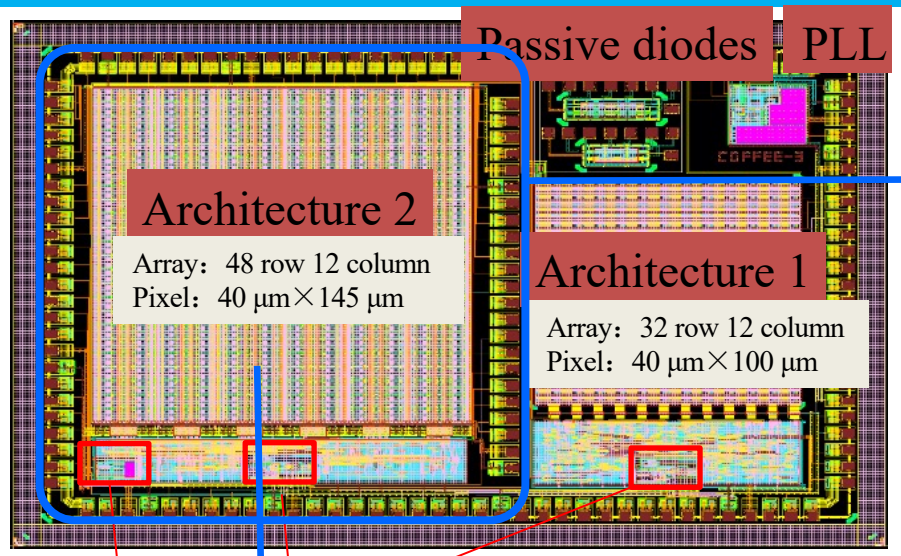
PLL: A new module for clock synchronization, providing up to 320 MHz output from a 40 MHz input (higher output limited by the test setup).





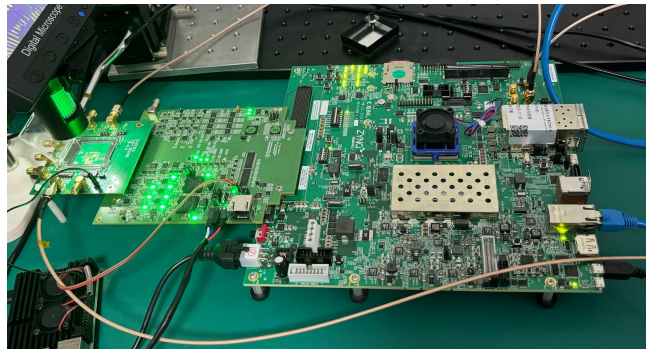


Tests of Pixel Array (COFFEE3)



Left pixel array: the readout architecture fully exploits the 55nm process potential, including in-pixel TDC.

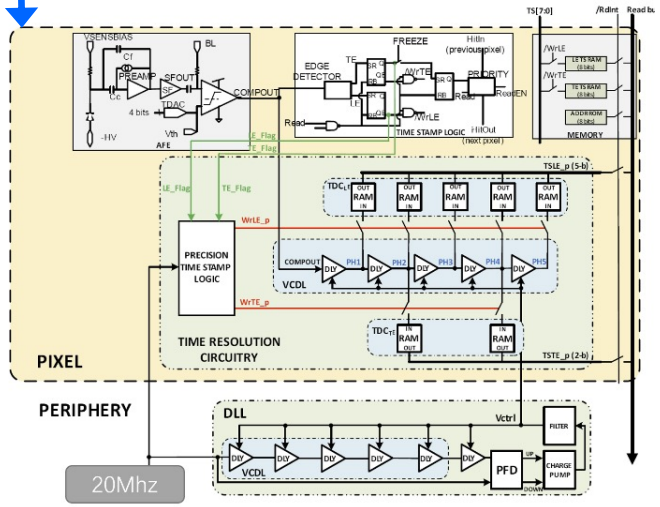
Testing units:
- In-pixel TDC
- Column readout
- LVDS driver
- …



Dedicated test PCB + Caribou readout board

Active contributor in Caribou user community → Improving & debugging with latest FPGA and software versions

In-pixel Coarse-Fine TDC



The pixel array has been configured, and the working point is being tuned to achieve optimal response for subsequent tests.

Task list:

[✓] SPI configuration
[…] In-pixel circuit validation
[…] Digital periphery validation
[…] Performance studies (timing, power, etc.)

Findings

- F-A-5-1: The Inner Tracker (ITK) of the CEPC silicon tracking system adopts a baseline technology based on HV-CMOS monolithic active pixel sensors (SMIC 55), offering excellent spatial resolution (pixel size: 34 μm × 150 μm), moderate time resolution (3–5 ns), and low material per layer (<1% X_0). As an alternative for the endcap, a HV-CMOS strip sensor technology is also under development.
- F-A-5-2: Since the last review in October 2024, the project has made notable progress in ASIC development. The COFFEE3 chip (SMIC 55 nm)—the second-generation HV-CMOS prototype— was successfully submitted for fabrication in January 2025 and is expected to be delivered for testing in May 2025. COFFEE3 integrates two readout architectures, supports in-pixel time stamping, and includes significant improvements in power optimization and data-driven readout. In parallel, the CSC1 chip, which integrates a passive CMOS strip sensor and an analog front- end placed in the periphery (CMSC 180 nm process), is scheduled for tape-out in April 2025. Together, these developments demonstrate strong and steady progress in the ITK technology program.
- F-A-5-3: Significant system-level advancements have also been achieved, particularly in mechanical design, cooling, and thermal management. The ITK now incorporates a well-defined multi-loop water-cooling system capable of maintaining stable operation at a power density of ~200 mW/cm², with thermal gradients controlled below 4° C. Updated mechanical simulations confirm the structural integrity of staves and validate the mechanical design for integration and prototyping.

Comments

- C-A-5-1: The alternative ITK endcap technology based on CMOS strips, while offering slightly better intrinsic spatial resolution (~4 μm), presents greater challenges compared to the HVCMOS pixel baseline. Achieving 3D tracking requires stereo configurations, increasing the material budget and mechanical complexity. Furthermore, the integration of a CMOS readout circuit in the strip sensor periphery, although innovative, may introduce additional design and integration risks.

- C-A-5-2: The COFFEE3 chip successfully consolidates the sensor, analog front-end, coarse-fine TDC for time-of-arrival and time-over-threshold measurements, and data-driven digital readout into a single device. Achieving these capabilities within a power density of ~200 mW/cm² is an impressive technical goal. A successful validation of COFFEE3 would represent a major milestone, demonstrating the technological feasibility of the CEPC ITK concept

Outer Tracker (OTK)

Recommendations

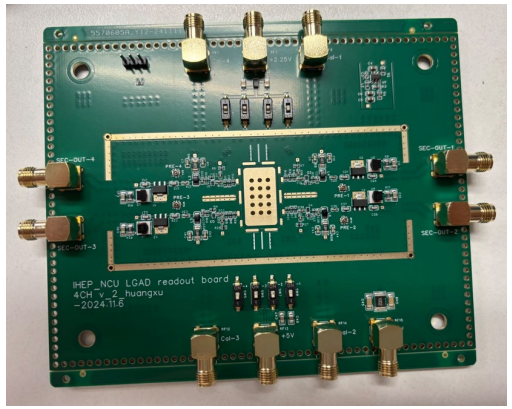
OTK

- R-A-5-3: To fully exploit the potential of this design iteration, it is strongly recommended to conduct exhaustive performance characterization of the newly submitted AC-LGAD sensors in test beams. These studies are critical to experimentally validate the effects of strip length, pitch, electrode width, n^+-well doping, and isolation structures on timing and position resolution, power dissipation, and occupancy. Given the importance of timely feedback 9 and the current unavailability of the LATRIC ASIC, it is advised to perform these measurements using fast discrete amplifiers until the LATRIC ASIC becomes available.

We will conduct exhaustive performance characterization of the newly summitted AC-LGAD prototype in test beams. Once the sensors are received from the tape-out, comprehensive measurements will be carried out using radioactive sources, laser systems, and subsequent test beam studies to thoroughly assess their performance.

Following the submission of the new AC-LGAD prototype in March 2025, we have been actively preparing the testing setup. Fast discrete amplifiers have already been integrated into our test readout board and will be employed for the forthcoming sensor characterization. Specifically:

- 4-channels readout boards have been fabricated for AC-LGAD testing;
- a two-stage amplifiers with an overall gain of ~70 has been implemented;
- the signal shape has been significantly improved, showing no obvious oscillations observed.



Recommendations

OTK

- R-A-5-4: The collaboration should continue evaluating other LGAD sensor options and should closely follow novel developments, particularly the trench-isolated DC-LGADs currently under investigation by the team.

We are open to exploring various LGAD sensor options to achieve high performance through the optimization of spatial resolution, timing resolution, and power efficiency.

Trench-isolated LGADs are particularly important, as the isolation structure reduces sensor capacitance and thus lowers power consumption. In addition to the LGAD prototype submitted in March, as previously reported, we are currently preparing another tape-out that includes trench-isolated designs with both DC- and AC-coupled variants. We will continue to closely follow ongoing developments and conduct detailed evaluations to identify the most suitable sensor technology for our application.

Recommendations

OTK

- R-A-5-5: It is recommended to ensure that the LATRIC ASIC is made available for sensor bonding as early as possible to enable realistic and fully representative characterization of the AC-LGAD sensor performance. Integrating the final readout ASIC with the sensor is crucial to obtaining accurate estimates of timing, position resolution, and power consumption. Given the critical role of the OTK in correcting space charge distortions in the TPC, it is essential that the OTK be robustly designed with service granularity in mind, exploring all known failure modes and developing strategies to mitigate them.

The prototype LATRIC ASIC was submitted for tape out in April and received in mid-August. We are pleased to report that the testing results are very encouraging, with the measured Least Significant Bit (LSB) of the TDC meeting the design goal of 30 ps, and the power consumption agrees with the design ….

The subsequent development phases, targeting a multi-channel design with full component integration, are carefully planned to accelerate the development and verification cycles. We are confident to deliver this on schedule, enabling timely sensor bonding and realistic performance characterization.

Prototype LATRIC Layout and Testing Results OTK

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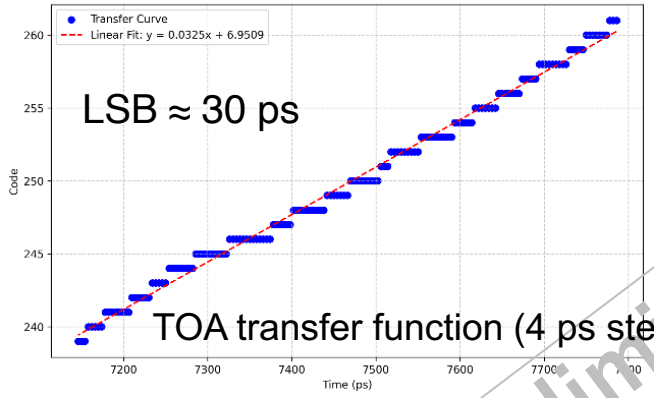
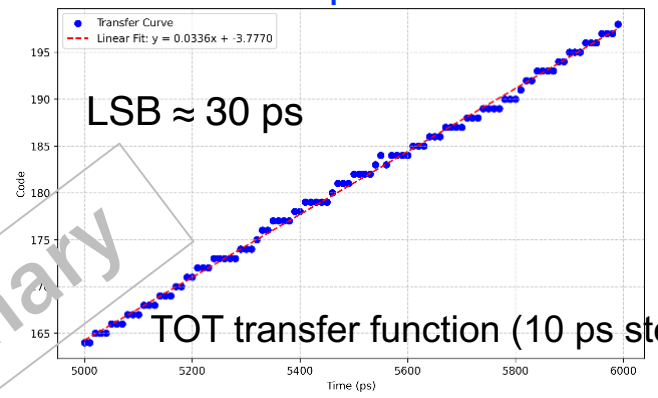
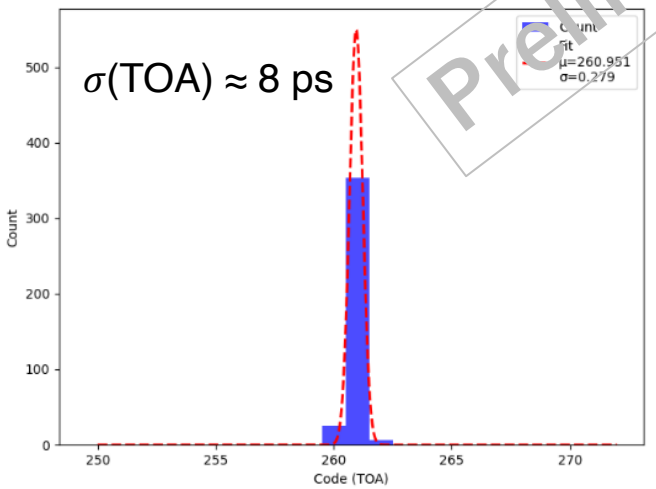
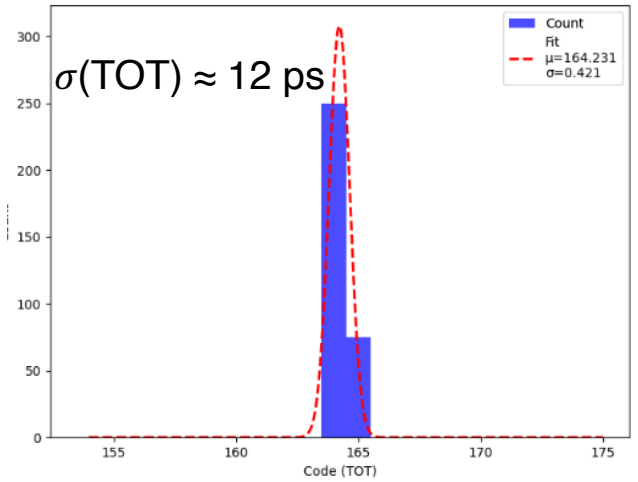
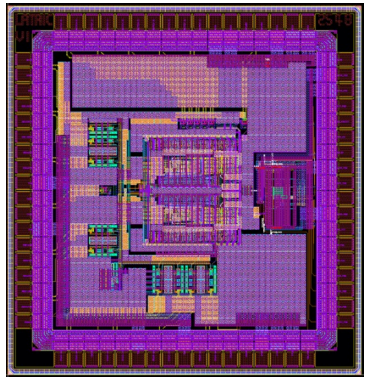
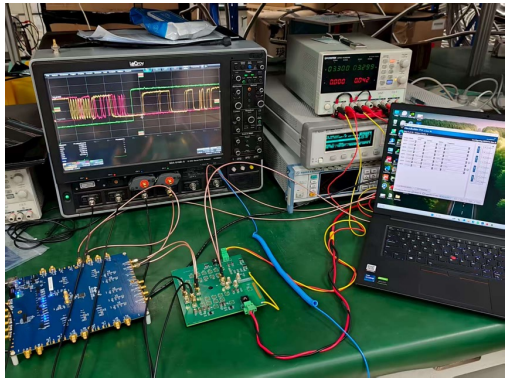




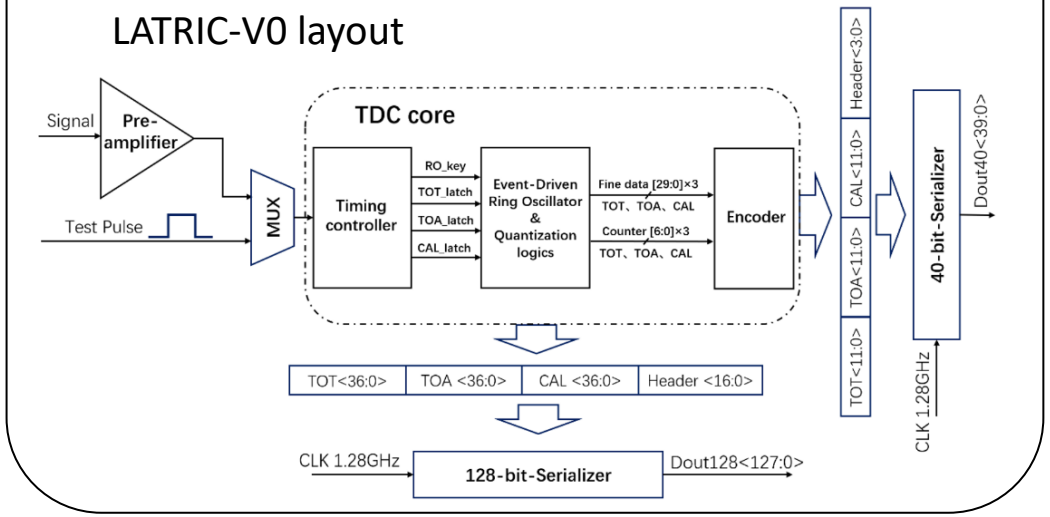








LATRIC-V0 layout



Comments from Ivan on Draft v0.4

- C-B-5-1: Concerning the chapter organization, this is significantly improved, facilitating the reading. The ITK and OTK dedicated sections now share the same subsection structure (design,electronics, mechanics, sensor technology and ASIC, and future plans); they also cover the important aspects of alignment, background estimations, and performance. As mentioned, the removal of the alternative sensor technologies for ITK and OTK has greatly improved the draft's readability.

Your suggestions have greatly improved the clarity and organization of our paper. We appreciate your positive feedback on the chapter structure and the revisions implemented.

Comments from Ivan on Draft v0.4

- C-B-5-2: The remaining content is very similar to the previous version; I noticed that the background hit rates are now lower than those presented in April's version, and the major missing part remains the definition of an approach to tackle the TPC performance degradation due to ion back-flow, but this will likely require considerably more time to address.

We are actively studying and improving the shielding design to mitigate beam induced background. Since the last review, the MDI shielding design has been updated, resulting in a further reduction in background levels.

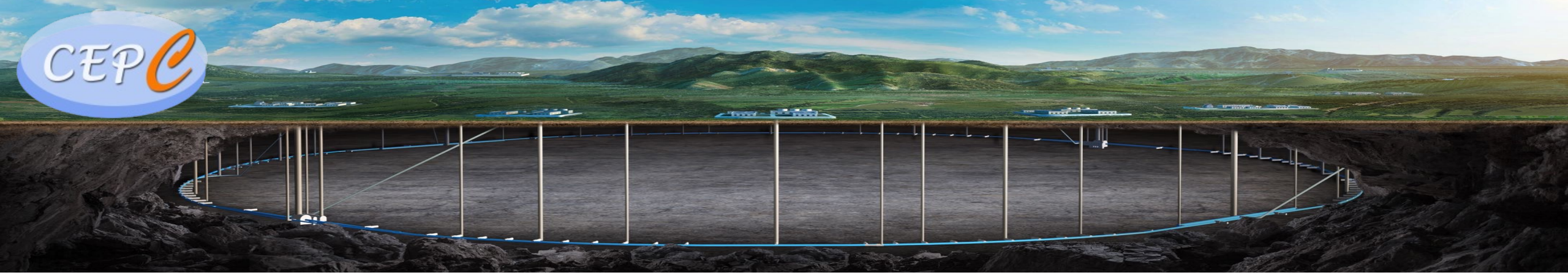
Concerning the issue of TPC performance degradation due to ion back-flow, please refer to the detailed responses provided in the TPC section.

Findings

- F-A-5-4: The Outer Tracker (OTK) of the CEPC is a large area tracking system designed to provide precision timing and position measurements, complementing the inner tracking systems and the central Time Projection Chamber (TPC). It plays a critical role in improving momentum resolution for high-momentum tracks and mitigating performance degradation of the TPC in high-luminosity operations, where ion backflow-induced space charge can distort the drift field and impair tracking accuracy. The OTK is based on AC-coupled Low-Gain Avalanche Detectors (AC-LGADs) arranged as microstrip sensors, capable of delivering ~10 μm spatial and ~50 ps timing resolution, covering approximately 85 m² across the barrel and endcap sections.
- F-A-5-5: Since the October 2024 IDRC review, the CEPC OTK system has made significant progress in response to the committee's recommendations. The AC-LGAD sensor design was updated, reducing the baseline size from approximately 8 × 5 cm² to 4 × 5 cm² to improve timing performance and manage higher particle rates. A new prototype sensor layout was submitted for tape-out in February 2025, featuring a variety of strip lengths, pitches, and electrode widths to optimize capacitance, noise, and spatial resolution. In parallel, the LATRIC readout ASIC was finalized and submitted for tape-out in April 2025, integrating all main functionalities. Mechanical and thermal simulations were also updated, confirming stable operation under a heat flux of 300 mW/cm².

Comments

- C-A-5-3: The latest submission of the redesigned AC-LGAD sensor marks a key step toward determining the optimal strip geometry and layout for the OTK system. By systematically varying strip length, p-well doping, electrode width, pitch, and implementing isolation structures (e.g., trenches) to reduce capacitance, this prototype will provide crucial data to balance timing resolution, position resolution, power dissipation, and occupancy, ensuring the final design meets the stringent performance and rate requirements of the CEPC detector.
- C-A-5-4: The LATRIC ASIC is a critical demonstrator, consolidating all essential functionalities required in the OTK readout chain into a single chip. It includes a low-jitter analog frontend, clock generation via PLL, coarse-fine TDCs, internal calibration circuits, and a data readout architecture with serializer and control interfaces. Its successful validation will be essential to confirm the feasibility of a compact, low-power, fully integrated readout solution for the AC-LGAD-based OTK system



Thank you for your attention!

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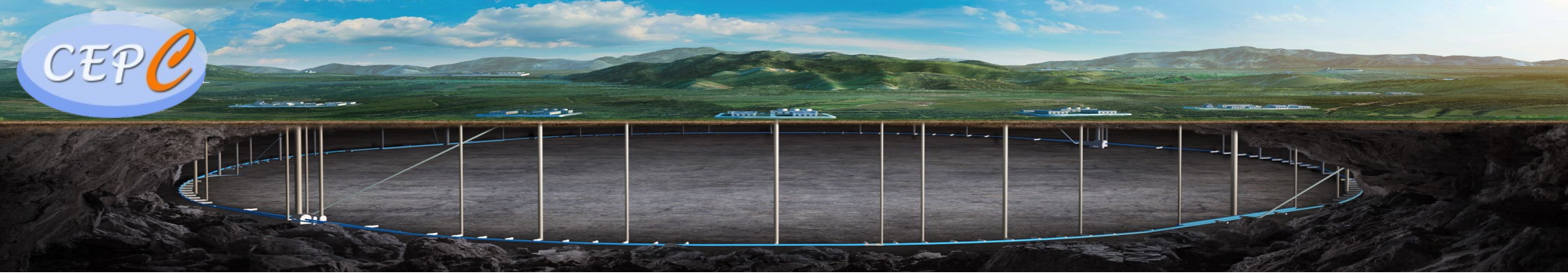

BACKUP

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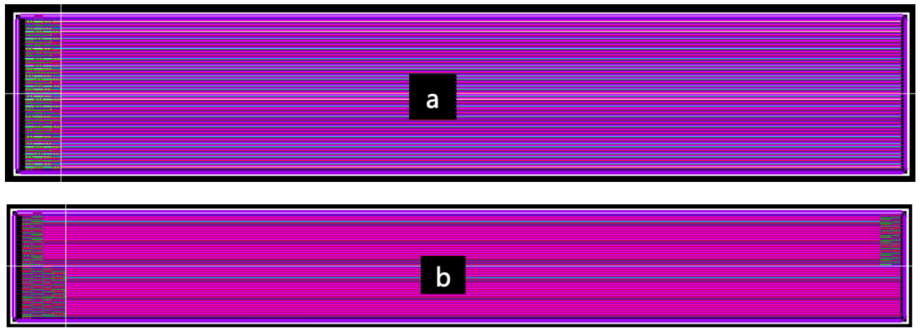
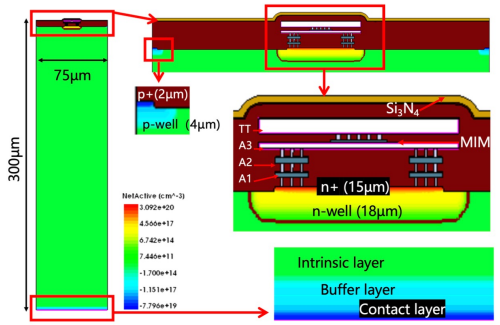
Summary of Answers to Review Comments

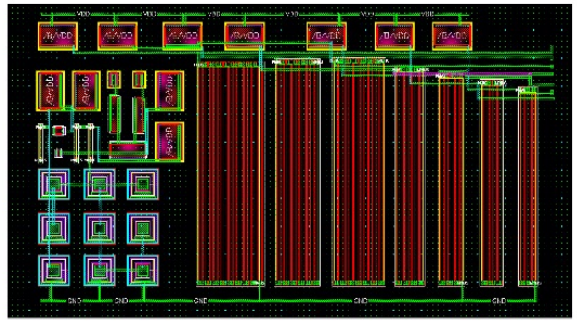
- There is currently no dedicated effort focused specifically on developing CMOS strip sensors for the Inner Tracker (ITK).

In our Ref-TDR, we delicate an entire section (Section 5.3.1.2) to describe efforts for the development CMOS strip sensor. In addition, the tape-out for the first CMOS chip (CSC1) is scheduled in April.



CSC1 sensor for CEPC





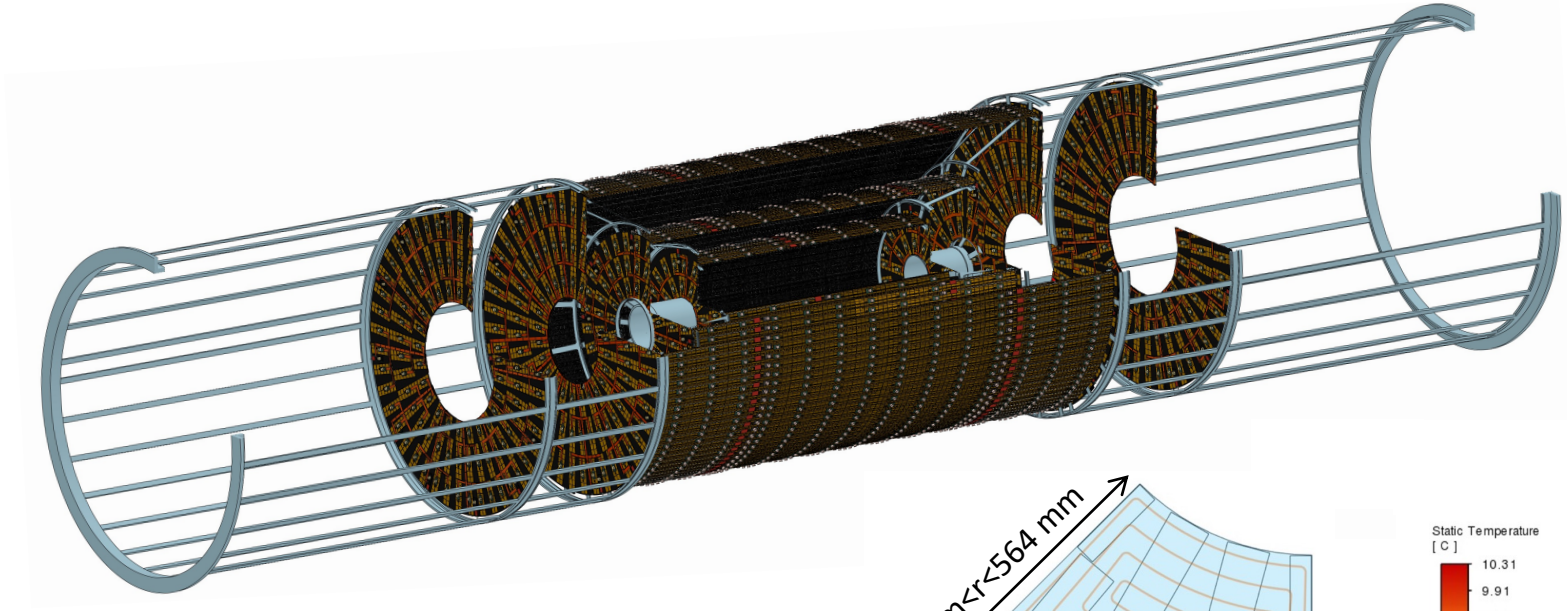
The design ASIC including preamplifier, the 1st stage amplifier, shaper, discriminator, and bandgap

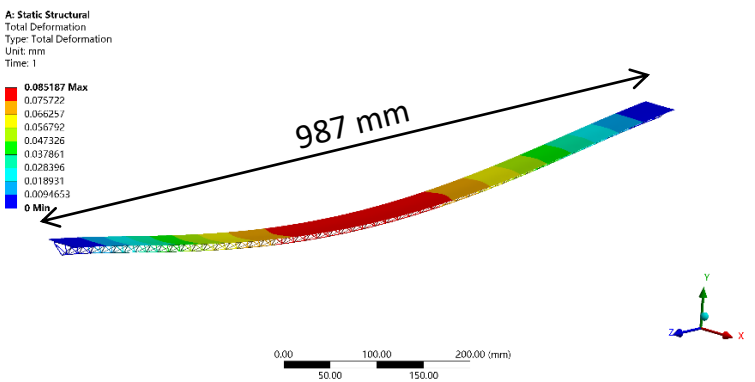
- The 180 nm process may face limited availability in the coming years, presenting a potential risk.

We spoke with the domestic foundry, and they preliminarily confirmed that 180 nm process will be maintained for a least the next 20 years. In parallel, we also have a plan to migrate to 55 nm, after the functional test of the 180 nm process.

ITK

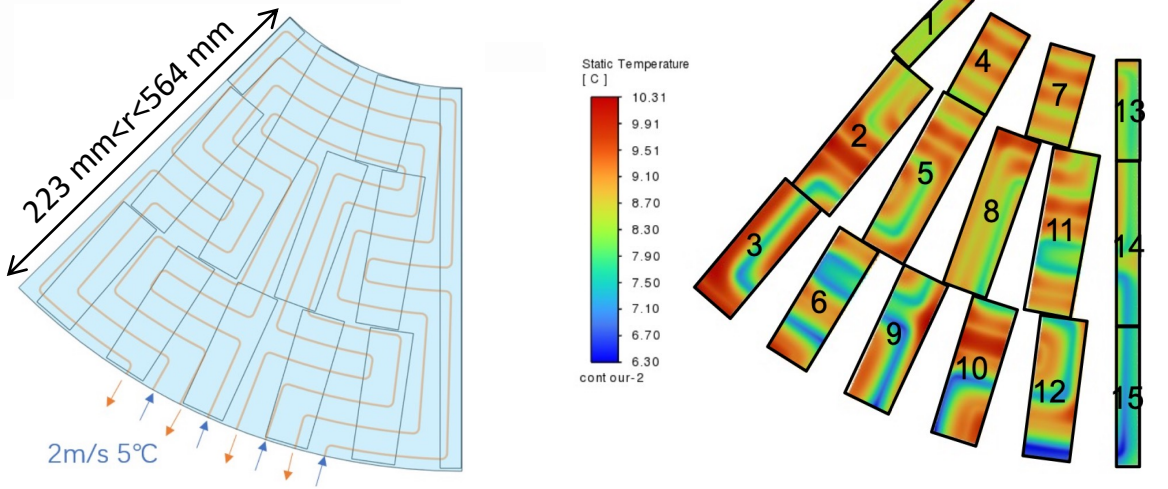
Mechanical and Thermal Analysis of the ITK





Maximum sag for first ITK barrel stave is 85 µm

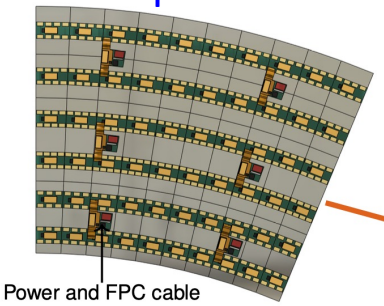
Heat flux: 200 mW/cm^2



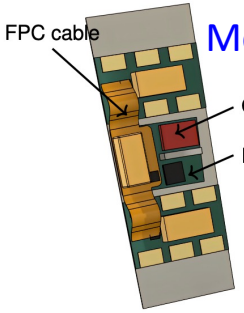
4-loops cooling for 1/8 endcap: with a cooling water flow of 2 m/s, a pipe inner diameter of 1.6 mm, and inlet temperature of 5°C, the temperature gradient across the endcap plane is <4°C, and the temperature difference for a single sensor is <2.5°C.

OTK Endcap Sensors with Readout Electronics

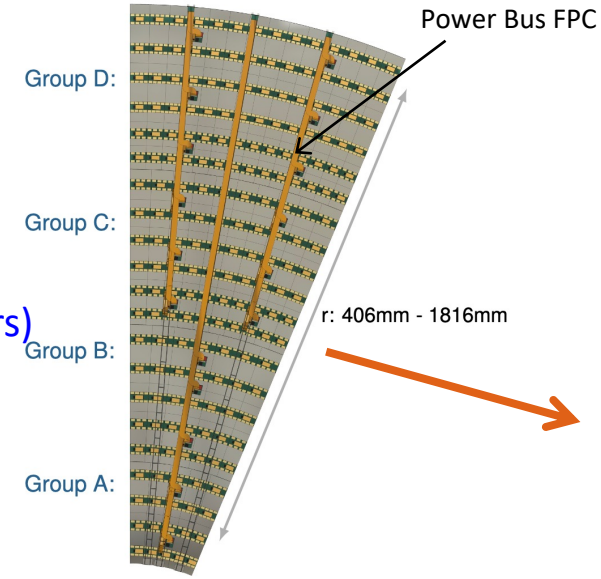
Group C sensors



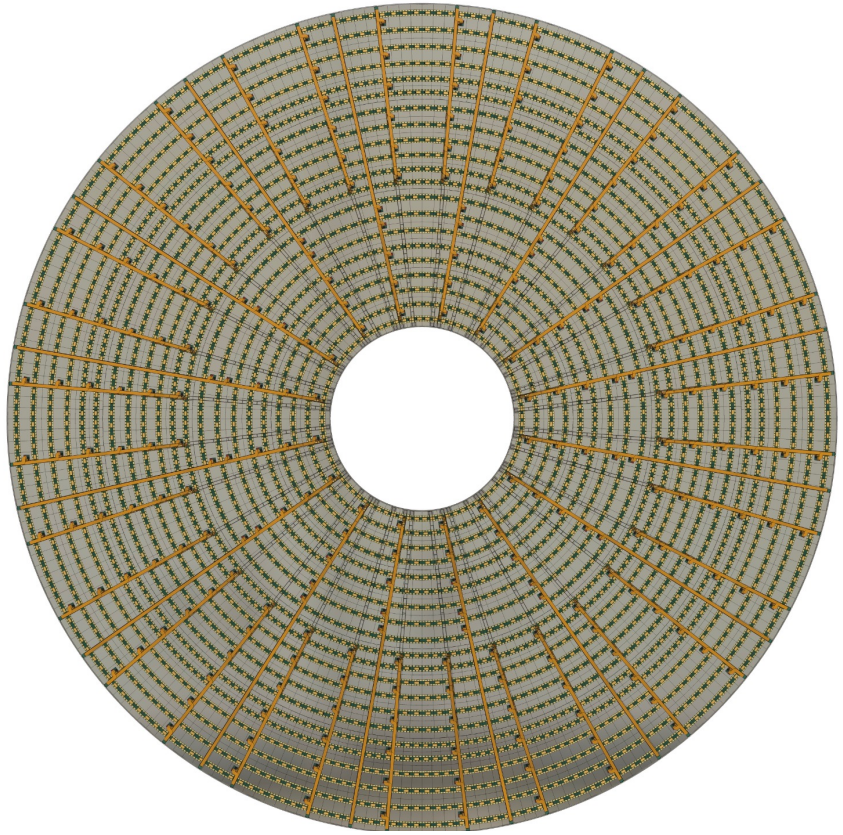
Module (2 sensors)

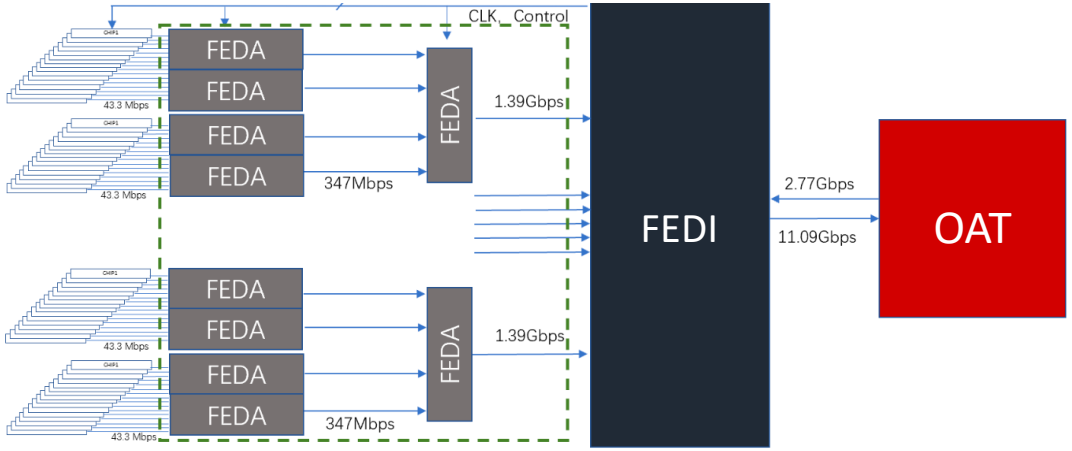


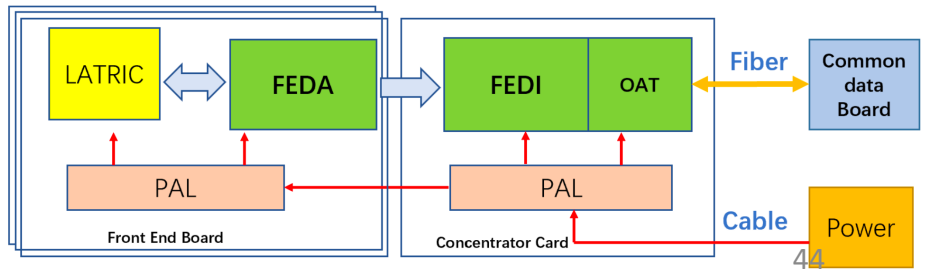
1/16 Sector



Endcap (16 sectors)



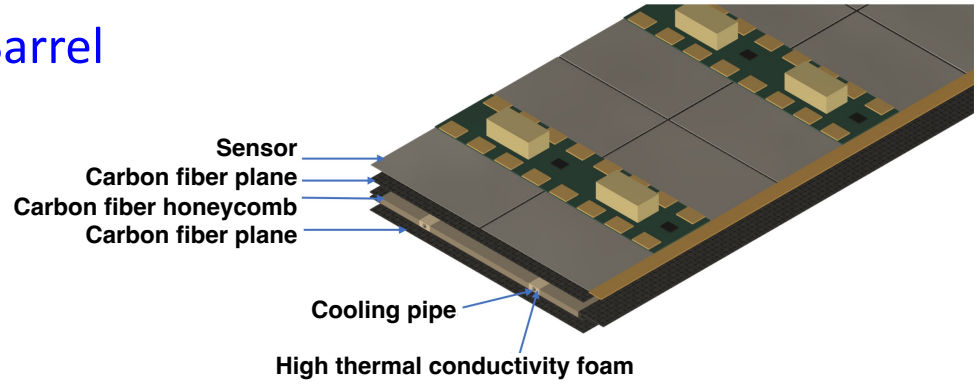




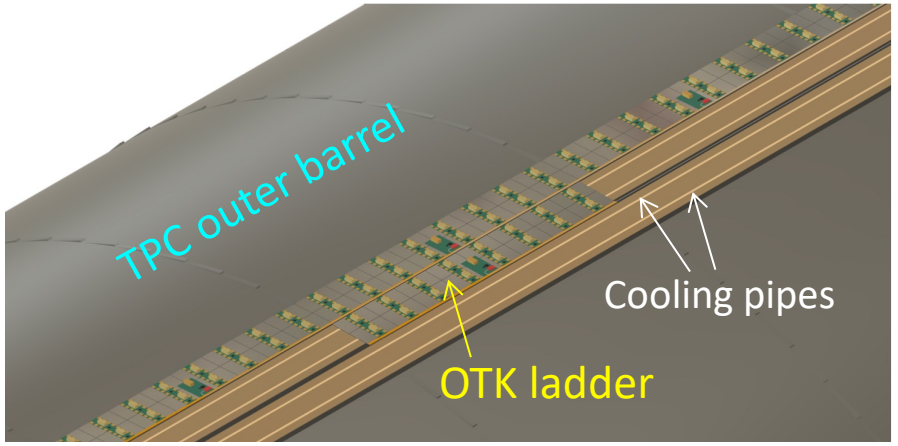
The FEDA, FEDI, OAT, and PAL chips are under development by the CEPC team.

Mechanical and Cooling Structure of the OTK

Barrel

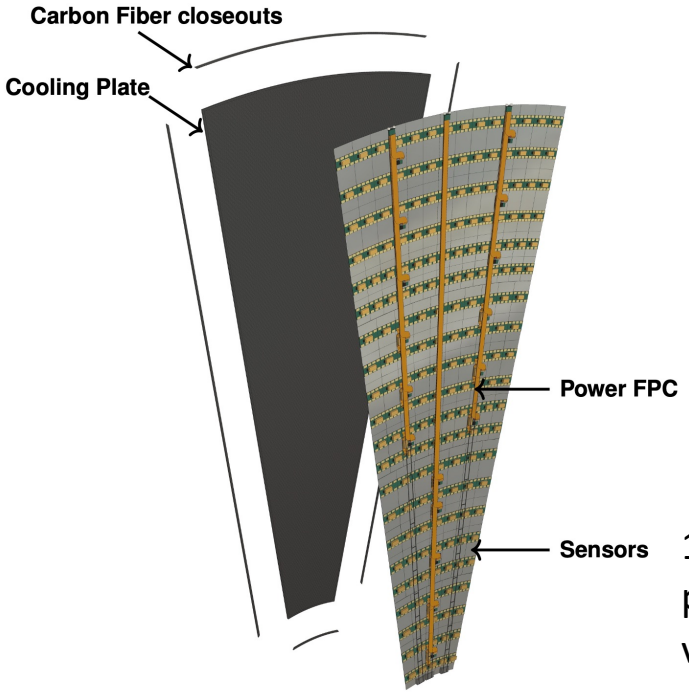


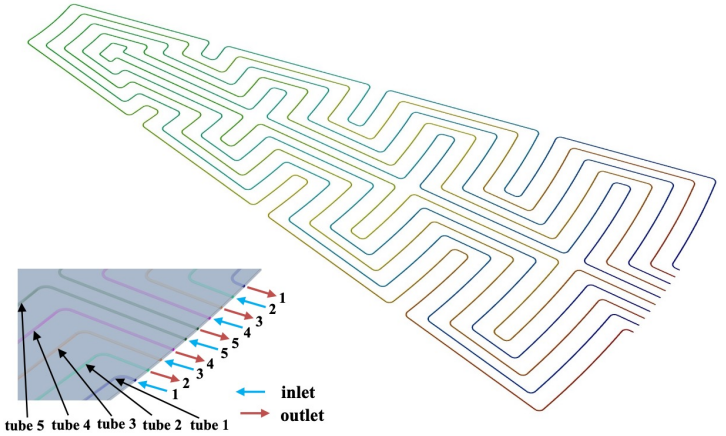
Stave Installation



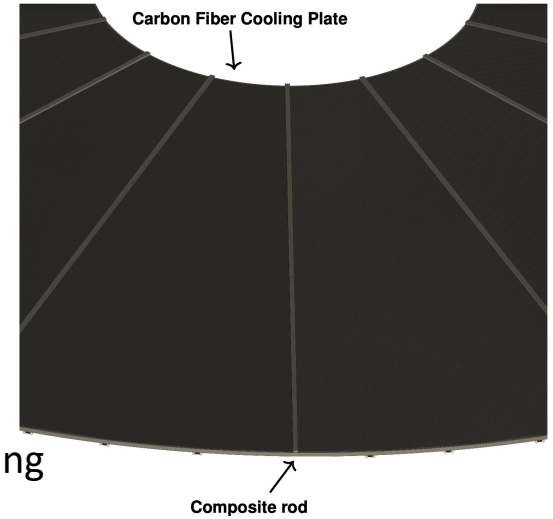
Endcap

1/16 OTK endcap sector





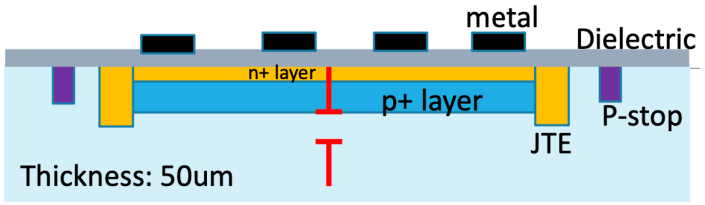
1/16 sector of the endcap uses 5-loop water cooling pipes: a pipe inner diameter of 2.3 mm, a flow velocity of 2 m/s, and an inlet temperature of 5°C.



Mounting 1/16 sectors

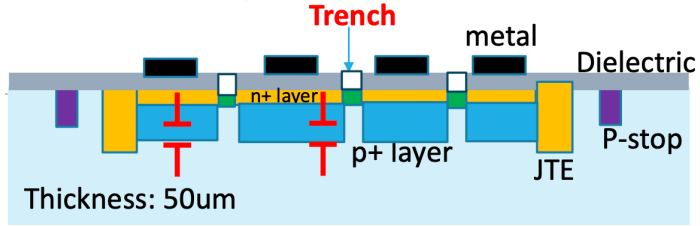
Latest Progress on AC-LGAD Sensor R&D

- New IHEP AC-LGAD strip sensor prototype: summitted for tap-out in March 2025.
  The new layout and design include:
  - Strip lengths： 1 cm, 2 cm, and 4 cm
  - Strip pitch sizes: 100 μm, 200 μm, and 500 μm
  - Electrode widths: 25 μm, 50 μm, and 100 μm
  - Optimized isolated structure design and EPI thickness to reduce sensor capacitance (correlated with power consumption)
  - Process design optimization (n+ layer dose) for better spatial resolution

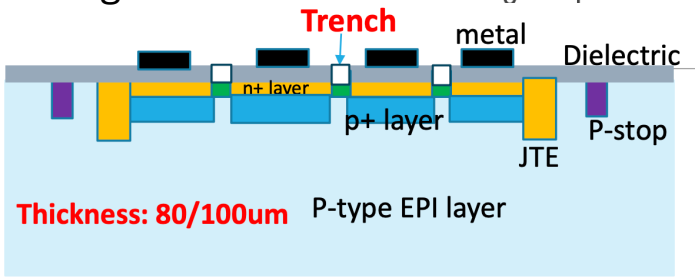


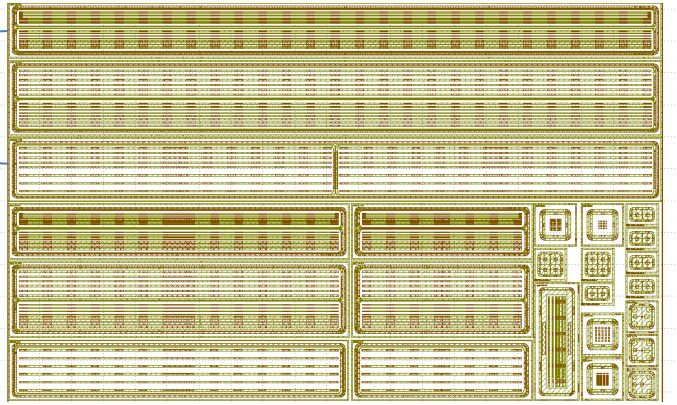
Introducing isolated structure:

$C = \varepsilon_0 * \varepsilon_r * A \downarrow / d$

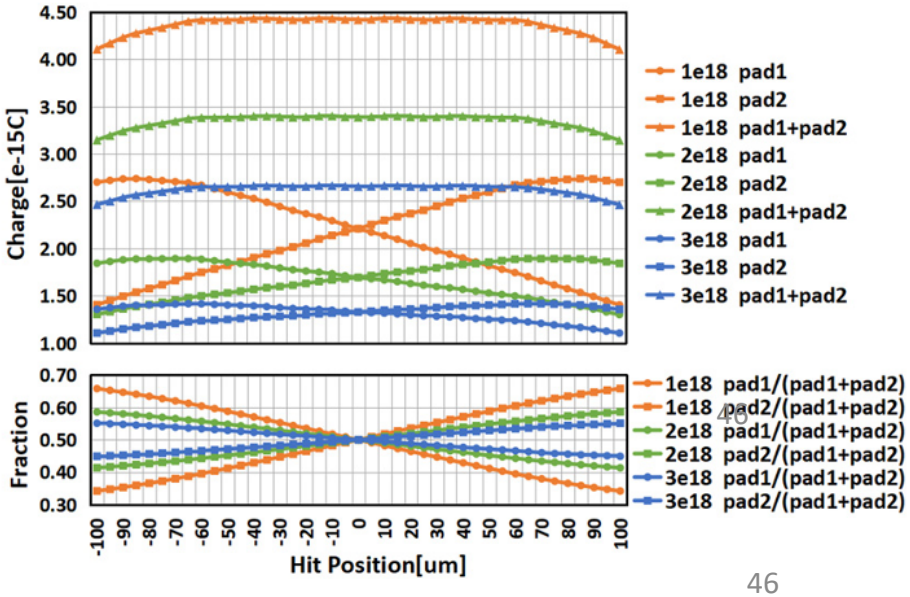


Increasing EPI thickness: $C = \varepsilon_0 * \varepsilon_r * A / \mathbf{d} \uparrow$





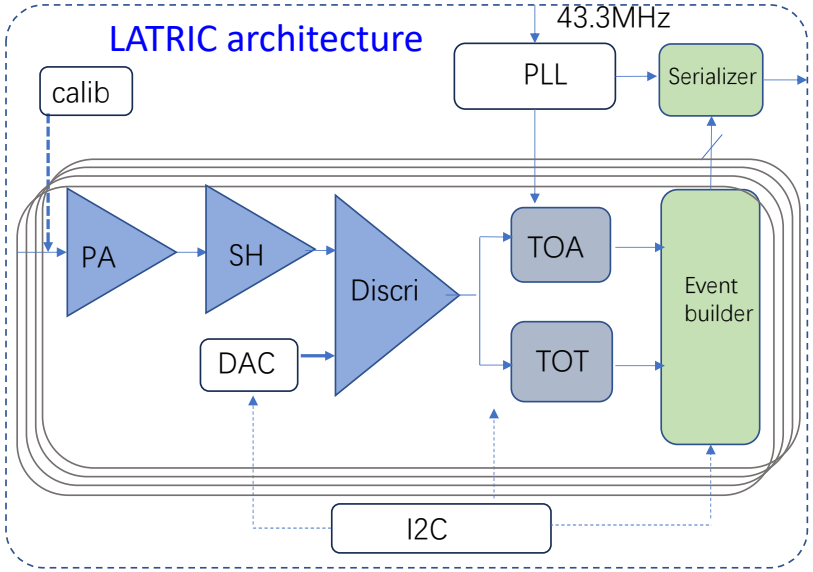
1cm AC-LGAD

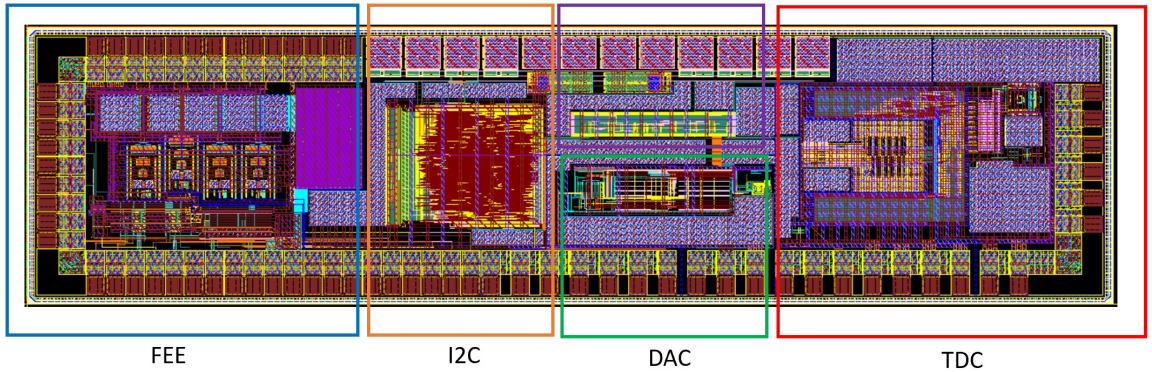


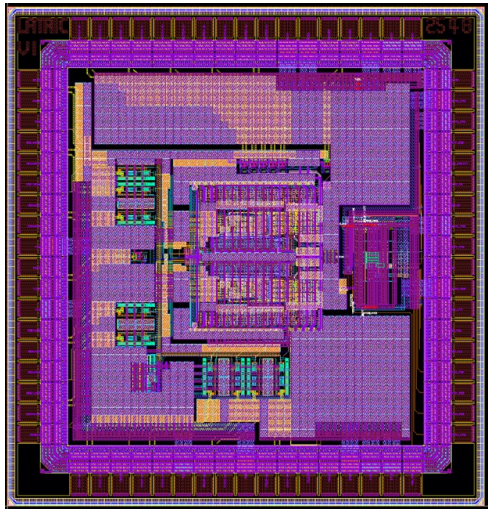
The sensor test will be launched once we received the latest tap-out.

LGAD ASIC (LATRIC) R&D

- LGAD ASIC (LATRIC) development: the prototype design was submitted for tap out in April 2025.
  - Several key elements in design are shared and verified with FPMROC (10 ps) chip
    - FEE: Preamplifier+Discriminator: jitter<7.8ps @ input 2.5mV, t_r=0.1ns, Cs=0 pF
    - PLL, Serializer verified
  - I2C Slave: ASIC parameter configuration
  - 12-bit DAC: threshold and calibration
  - TDC design:
    - Event driven delay line to reduce the power consumption
    - Power consumption: average current for single event: 443 µA, static current: < 5 µA
    - Real time calibration for PVT (Process, Voltage, Temperature)
    - LSB ~36 ps based on preliminary layout post-simulation (current version)



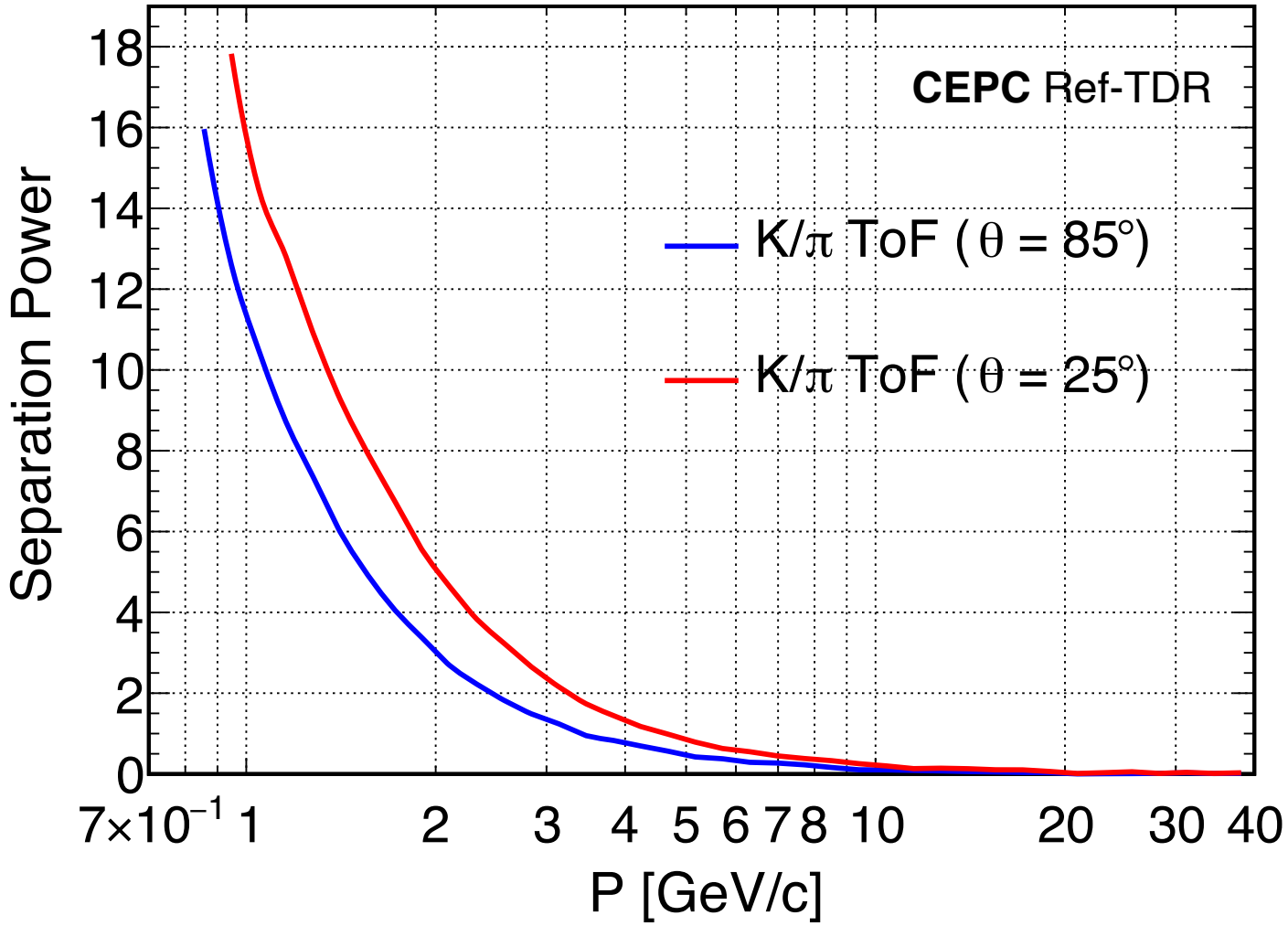


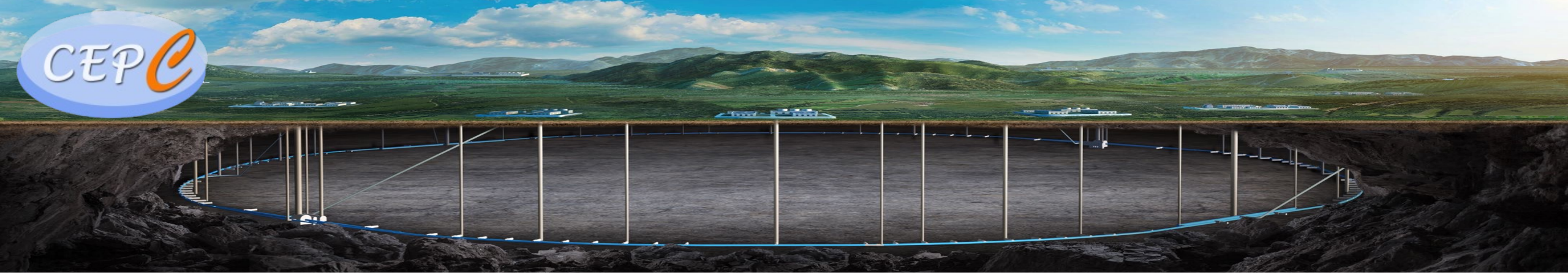


TDC delay line layout

Performance testing is scheduled to be completed by the end of 2025. In Q4 2025, the new design will be enhanced by incorporating a digital logic control section. The final chip will feature 128 readout channels and provide precise measurements of both time-of-arrival (TOA) and time-over-threshold (TOT).

PID Performance





Extra Slides

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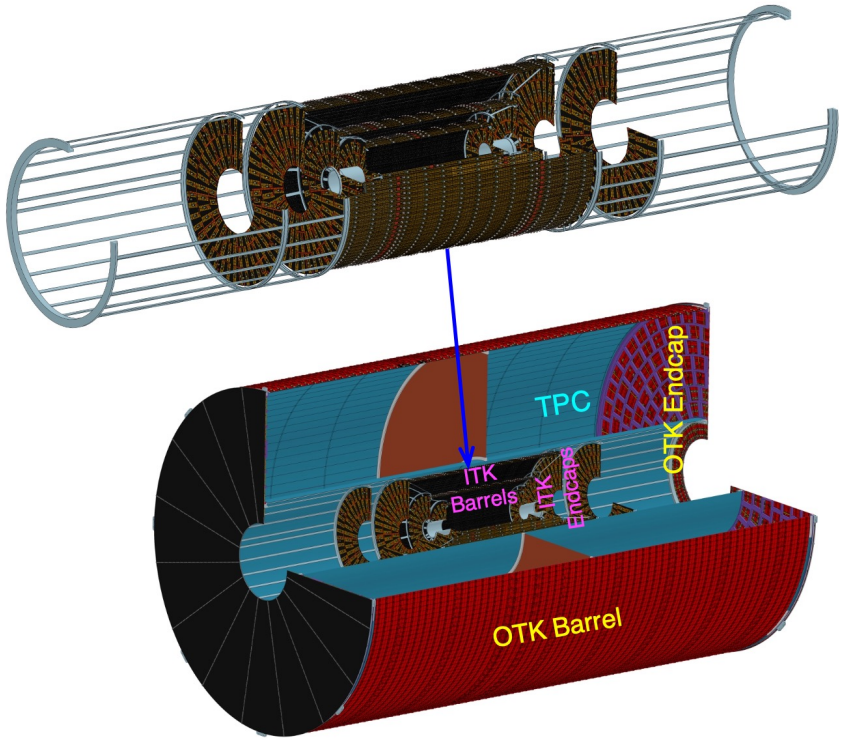


Figure 5.1: Layout of the Silicon Tracker (ITK and OTK). The ITK consists of three barrel layers and four endcap layers, together with two extended connection rings, forming the complete ITK assembly that is inserted into the inner barrel of the TPC. The OTK, as the outermost component of the tracker system, includes one barrel layer and one endcap layer, mounted outside of the TPC. It provides both high-precision spatial and timing measurements.

Table 5.1: Parameters and layout of the Silicon Tracker. The column labelled $\pm z$ shows the half-length of the barrel layers, and the z position of the end-cap disks. The column labelled σ_ϕ and σ_t represent the spatial resolution in the bending direction and time resolution, respectively.

Detector		**Radius R [mm]**		**$\pm z$ [mm]**	**Material budget [% X_0]**	**σ_ϕ [μm]**	**σ_t [ns]**
ITK Barrel	Layer 1 (ITKB1)	235.0		493.3	0.68	8	3-5
	Layer 2 (ITKB2)	345.0		704.8	0.68	8	3-5
	Layer 3 (ITKB3)	555.6		986.6	0.68	8	3-5
OTK Barrel	Layer 4 (OTKB)	1,800		2,840	1.6	10	0.05
		R_{in}	**R_{out}**				
	Disk 1 (ITKE1)	82.5	244.7	505.0	0.76	8	3-5
	Disk 2 (ITKE2)	110.5	353.7	718.5	0.76	8	3-5
ITK Endcap	Disk 3 (ITKE3)	160.5	564.0	1,000	0.76	8	3-5
	Disk 4 (ITKE4)	220.3	564.0	1,489	0.76	8	3-5
OTK Endcap	Disk 5 (OTKE)	406.0	1,816	2,910	1.4	10	0.05

Table 5.2: Estimated average and maximum hit rates of the Silicon Tracker [10^3 Hz/cm^2] for all layers across three operation modes.

$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	**Low Lumi Z** 26		**Higgs** 8.3		**High Lumi Z** 192	
	Average	Max	Average	Max	Average	Max
ITKB1	1.04	1.95	0.63	1.01	3.10	5.84
ITKB2	0.98	3.30	0.55	1.33	2.93	9.89
ITKB3	0.76	1.69	0.39	0.77	2.26	5.07
OTKB	0.66	1.11	0.37	0.58	1.96	3.32
ITKE1	3.46	15.78	2.35	11.70	10.37	47.28
ITKE2	3.99	24.50	2.06	9.82	11.95	73.38
ITKE3	2.29	17.26	1.14	7.46	6.86	51.71
ITKE4	2.54	8.55	1.26	3.71	7.59	25.61
OTKE	1.54	6.35	0.94	4.12	4.61	19.01

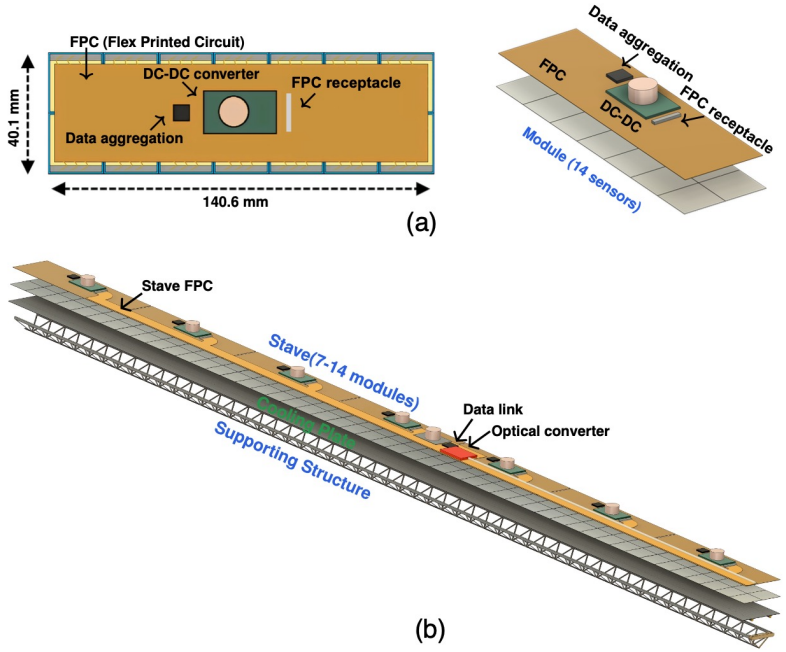


Figure 5.2: (a) ITK module and (b) ITK stave. The ITK module consists of 2×7 monolithic HV-CMOS pixel sensors, with their backside glued to a FPC board integrated with electronic components, including a DC-DC converter and a data aggregation chip. Each ITK stave is made up of 7, 10, or 14 modules, one or two long stave FPCs, a plate with embedded cooling tubes, and a truss supporting structure. A data link chip, an optical converter, and DC-DC converters are integrated at the center of each stave FPC.

Table 5.3: The HV-CMOS sensor key parameters

Parameter	Value
Sensor size	2 cm × 2 cm (active area: 1.74 cm × 1.92 cm)
Sensor thickness	150 µm
Array size	512 × 128
Pixel size	34 µm × 150 µm
Spatial resolution	8 µm × 40 µm
Time resolution	3-5 ns
Power consumption	200 mW/cm^2
Technology node	55 nm

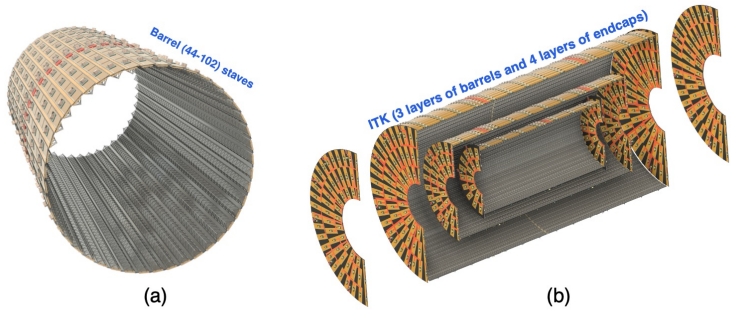


Figure 5.3: (a) ITK barrel and (b) ITK comprising three barrel layers and four endcap layers. Each ITK barrel contains 44, 64, or 102 staves arranged in a staggered structure to mimimize dead area.

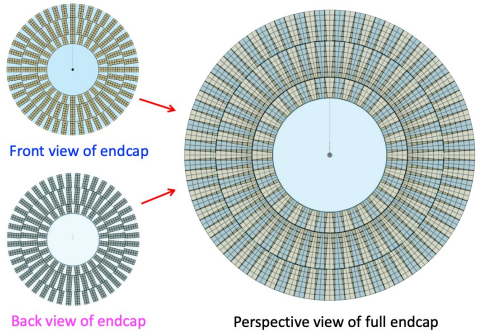


Figure 5.4: Perspective view of the sensor and module distribution for the fourth ITK endcap. The ITK endcap has double-sided detection surfaces, referred to as the "front view" (facing the interaction point) and the "back view" (facing away from the interaction point). The module layouts on the two sides are designed to complement each other to minimize dead detection areas. Overlapping detection regions between the two faces are highlighted as dark green triangles.

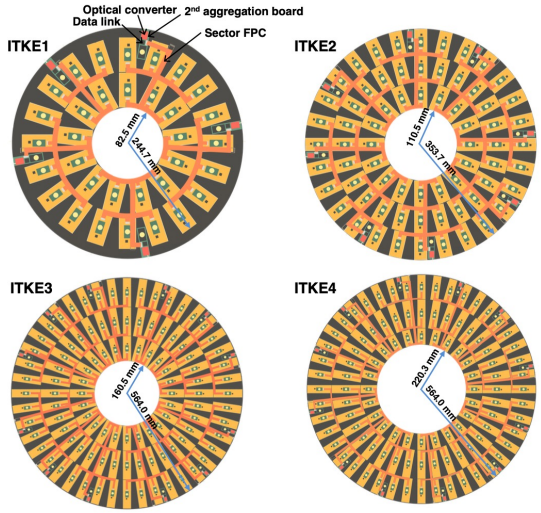


Figure 5.5: Module (yellow) layout of the four ITK endcaps: ITKE1, ITKE2, ITKE3, and ITKE4. Details are provided in Table 5.5. Secondary data aggregation boards — each integrating a data link chip, an optical converter, DC-DC converters, and optionally a data aggregation chip — are attached near the outermost rim of the endcap, with sector FPCs (shown in orange-red) connecting them to the modules.

Table 5.4: Information about the staves, modules, and sensors used for the construction of the three ITK barrels.

Barrel	Number of staves	Modules per stave	Sensors per module	Number of sensors	Sensor area [m^2]
ITKB1	44	7	14	4,312	1.72
ITKB2	64	10	14	8,960	3.58
ITKB3	102	14	14	19,992	8.00
Total	210			33,264	13.31

Table 5.5: Information about the module and sensor specifications for the four pairs of ITK endcap disks

Endcap	Number of rings per side	Number of modules per ring	Number of sensors per module	Total sensors
ITKE1	2	13,20	8,8	1,056
ITKE2	3	16,24,28	8,8,8	2,176
ITKE3	3	24,36,44	12,14,14	5,632
ITKE4	3	24,36,44	8,14,12	4,896
Total				13,760

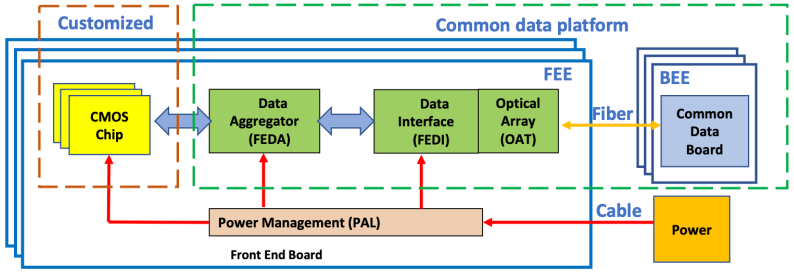


Figure 5.6: ITK readout and power supply scheme. The Front-End Data Aggregator (FEDA) chip collects data from multiple sensors and sends it to the Front-End Data Interface (FEDI) chip, which forwards it via the Optical Array Tranceiver (OAT) module to the Back-End Electronics (BEE). Power is supplied to both the sensors and readout chips through DC-DC converters (PAL).

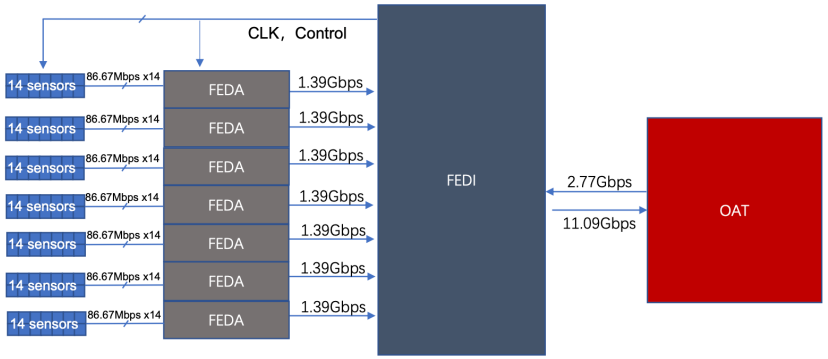


Figure 5.7: ITK readout electronics data flow. Data from 14 sensors are aggregated by a FEDA chip and transmitted via an e-link at 1.39 Gbps to the FEDI chip. Each FEDI chip collects and aggregates data from seven FEDA chips, serializes and encodes it, and forwards it to the OAT at an uplink rate of 11.09 Gbps. The OAT also provides a downlink of 2.77 Gbps for slow control, monitoring, and clock signals, which are distributed to the FEDI chip and then to the FEDA chips and sensors.

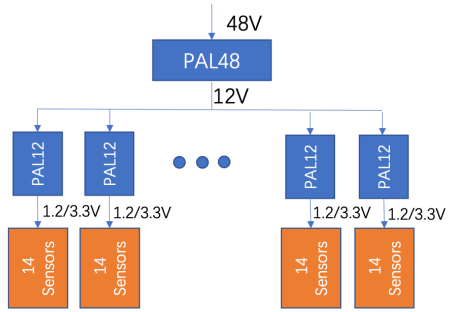


Figure 5.8: ITK readout electronics power distribution. The DC-DC converters operate in two stages: first, the PAL48 DC-DC converter reduces 48 V to 12 V; then, the PAL12 converter steps it down to 3.3 V for the Vertical-Cavity Surface-Emitting Laser (VCSEL) driver in the OAT and to 1.2 V for powering the sensor circuits and other readout electronics.

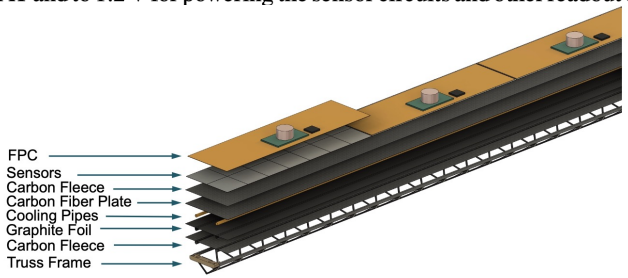
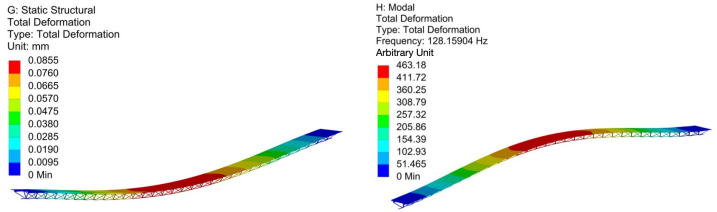


Figure 5.9: Structure of the ITK barrel stave. The stave consists of FPCs integrated with associated electronics and sensors, followed by a top carbon fleece layer, a carbon fiber plate, two cooling pipes, a graphite foil layer, a bottom carbon fleece layer, and a truss frame.



(a) Sag analysis (b) Modal analysis

Figure 5.10: Results of (a) gravitational sag analysis and (b) modal analysis for the stave of the first ITK barrel (ITKB1). Both ends of the stave were assumed to be fixed supports. The blue color indicates zero movement, while the red lines represent maximum movement.

Table 5.6: Estimation of the ITK stave material contributions. The wall thickness of the cooling tubes, averaged over the entire stave area and labeled with "†", is ~ 16 µm.

Functional unit	Component	Material	Thickness [µm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	150	28.41	0.053
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64†	28.41	0.006
	Cooling fluid	Water		35.76	0.028
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Truss Frame	Carbon rowing				0.080
Power Bus FPC					0.070
Total					0.677

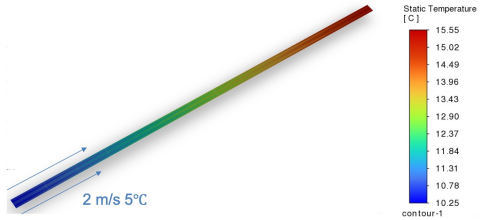


Figure 5.11: Simulation result of water cooling for the stave of the third ITK barrel (ITKB3), with a flow velocity of 2 m/s and a two-pipe inlet temperature of 5 °C. The temperature across the stave remains below 15.6 °C, and the temperature gradient along the stave is within 5 °C.

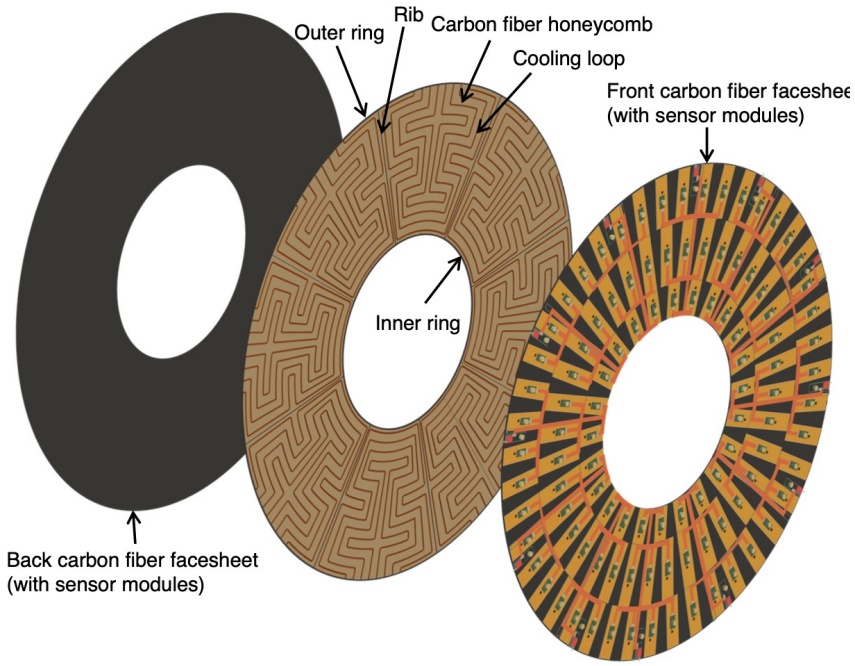


Table 5.7: Estimation of the ITK endcap material contributions. The wall thickness of the cooling tubes, averaged over the entire endcap area and labeled with "†", is ~ 24 μm.

Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	150	28.41	0.053
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Structure	Carbon fiber facesheet	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Titanium	100†	3.560	0.067
	Cooling fluid	Water		35.76	0.027
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	2000	186	0.108
	Carbon fiber facesheet	Carbon fiber	150	26.08	0.057
	Glue	Cyanate ester resin	200	44.37	0.045
Total					0.759