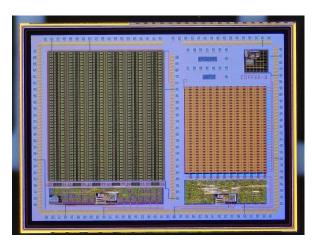
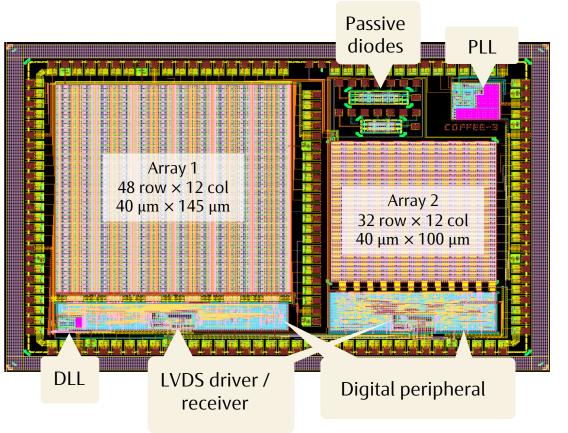
COFFEE3 chip

- Submission in Januaray 2025
 - $4 \text{ mm} \times 3 \text{ mm}$
- Two readout pixel arrays + a few function modules
 - Array 1: CMOS-based in-pixel circuit, fully exploiting 55nm potential for optimal timing performance (eg: with in-pixel TDC and coarse-fine delay line)
 - Array 2: optimized for triple-well process, only NMOS for in-pixel circuit to avoid cross-talk
 - Digital peripheral circuits: End of Column, function configuration, data scrambler, serializer
 - Passive diode array
 - PLL、LVDS modules, extendable for larger array
- Received in end May

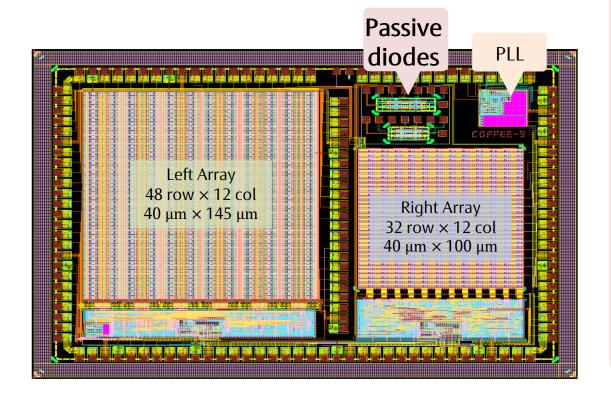




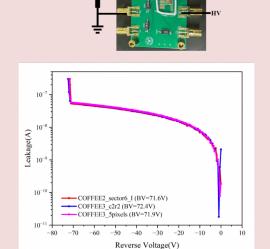


COFFEE3 layout

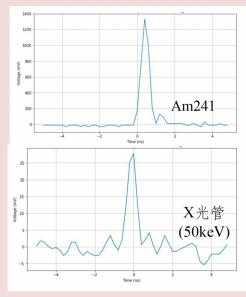
COFFEE3 tests



Passive diode array: validation of sensor performance; test result consistent with COFFEE2:

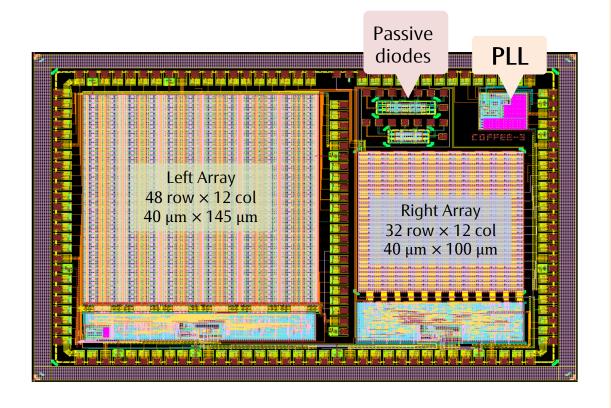


Breakdown voltage: -71V



Responsive to α -and X-rays

COFFEE3 tests

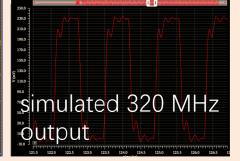


PLL: new module for clock synchronization.

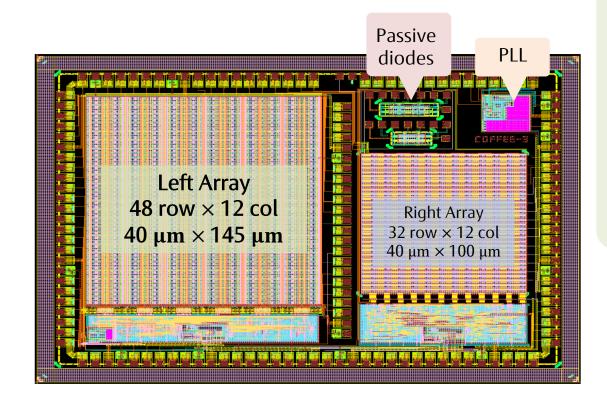
Test result consistent with simulation up to 320MHz output with 40MHz input → Module validated!







COFFEE3 tests



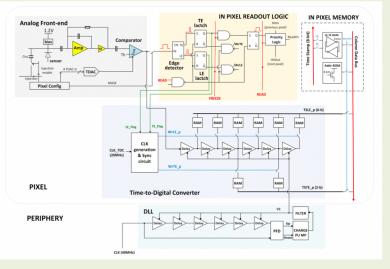
Testing team actively contributing to Car(ibou) community, with the latest software and firmware versions

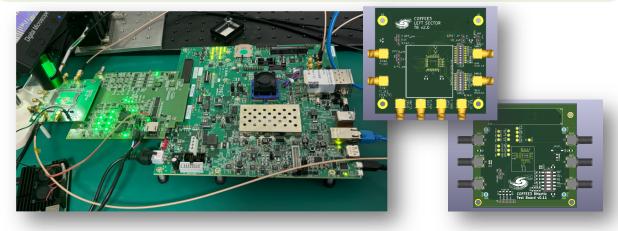
pixel array: full readout architecture validation

Testing goals:

In-pixel analog: CSA, comparator

- o In-pixel digital: TDC, me
- o Data-driven readout
- o DLL
- LVDS transceiver



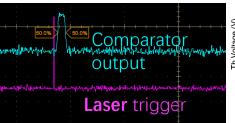


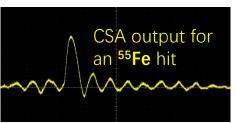
Dedicated test PCBs + CariBou readout board in place

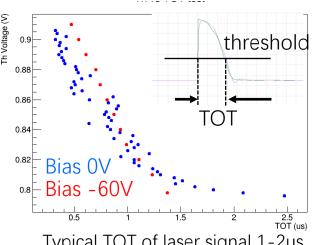
COFFEE3 pixel array test

Pixel response to laser & ⁵⁵Fe;

In-pixel CSA and comparator working as design







Typical TOT of laser signal 1-2us, consistent with simulation



LVDS transceiver works up to 640 MHz supporting 1.28 Gbps data transmission



DLL delivers clock phase decay as expected

Testing goals:

In-pixel analog: CSA, comparator



In-pixel digital: TDC, memory





- **LVDS** transceiver



Function configuration; serializer



End of Column; data scrambler WORKING

