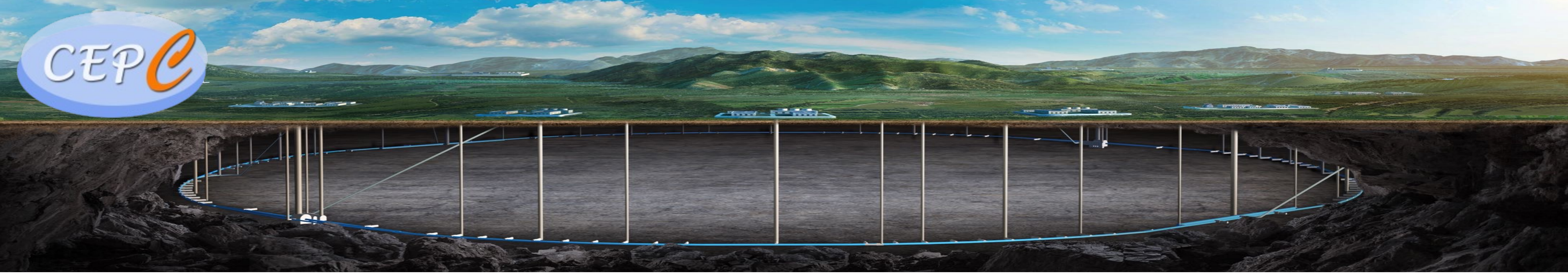


# CEPC Silicon Tracker Detector

Qi Yan
*On behalf of the CEPC Silicon Tracker Group*

中国科学院高能物理研究所
*Institute of High Energy Physics*
*Chinese Academy of Sciences*

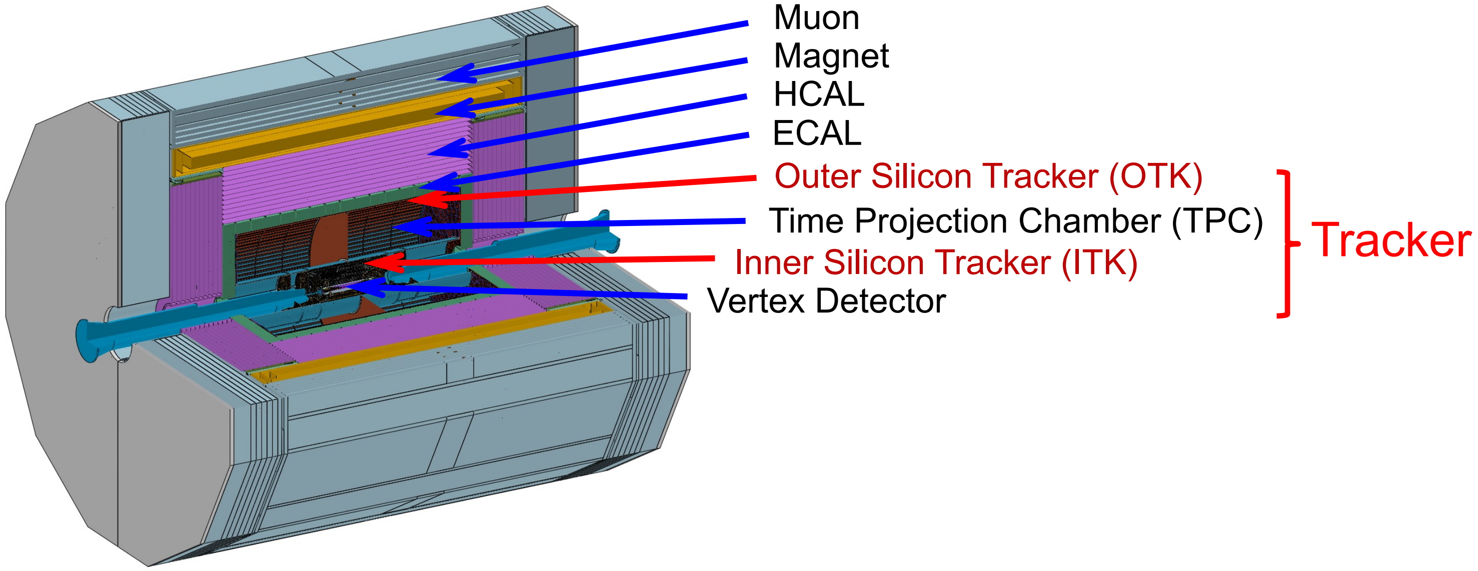
Nov 6, 2025, CEPC Workshop, Guangzhou

# Introduction

- The CEPC tracker system includes several detectors: the Vertex Detector, Inner Silicon Tracker, Time Projection Chamber (TPC), and Outer Silicon Tracker. My presentation will focus on the CEPC Inner Silicon Tracker (ITK) and Outer Silicon Tracker (OTK).

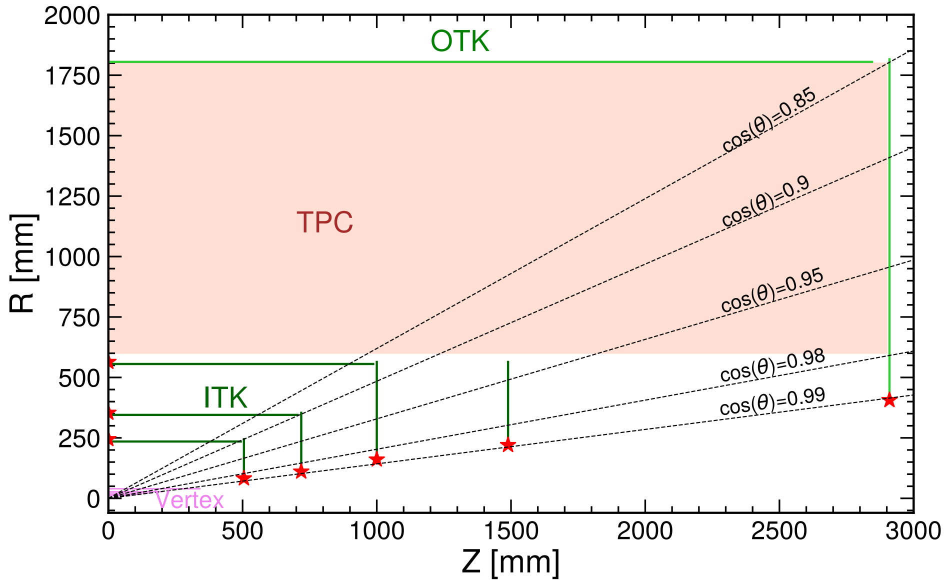
- The ITK employs advanced CMOS sensor technology to achieve precise position measurements for accurate particle trajectory determination.

- In addition to position measurement, the OTK integrates the AC-LGAD semiconductor detector for precision time measurement of charged particles, significantly enhancing particle identification capabilities.



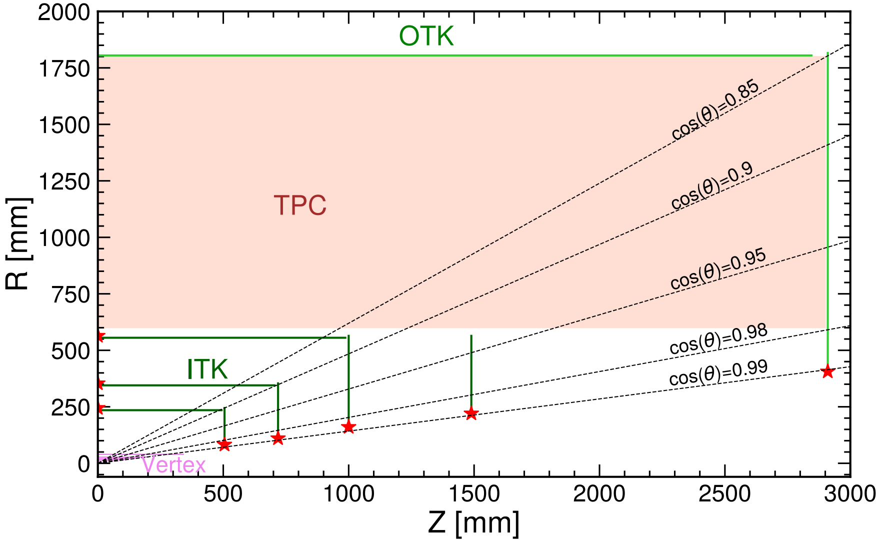
Muon
Magnet
HCAL
ECAL
Outer Silicon Tracker (OTK)
Time Projection Chamber (TPC)
Inner Silicon Tracker (ITK)
Vertex Detector

Tracker



- The CEPC overall track momentum resolution requirement: ~0.1% for momenta below 100 GeV/c.

# Baseline Configuration of Sensor for CEPC ITK

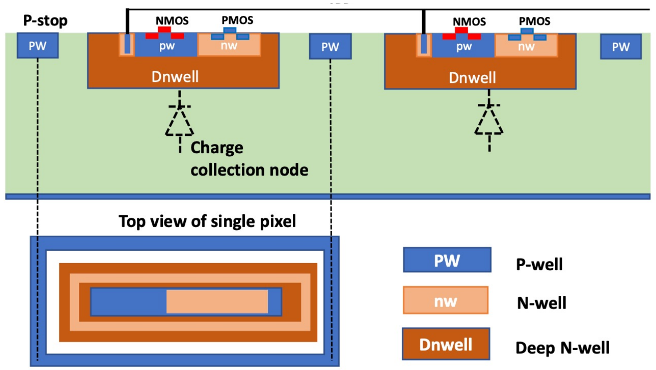


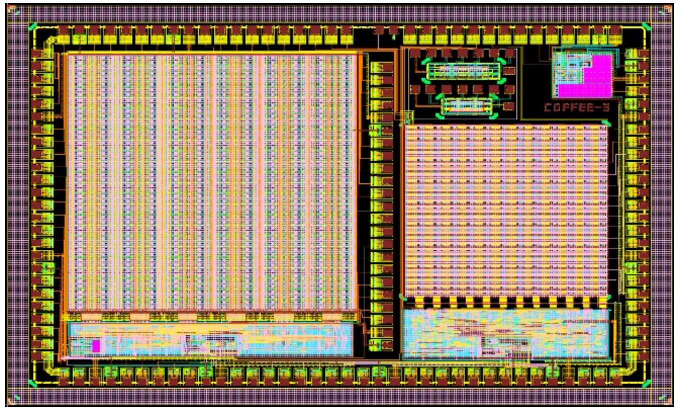
## Monolithic HV-CMOS pixel sensor:

- Large depletion depth and large signal.
- Good timing resolution (a few ns) to tag 23 ns bunches.
- Radiation hard.
- Low materials.
- Cost effectiveness.

## Key parameters of HV-CMOS pixel sensor for CEPC:

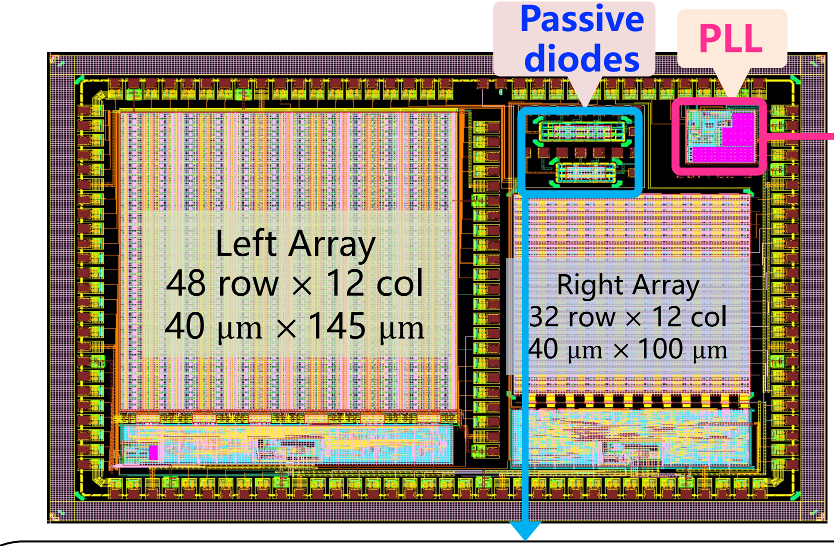
- Process node: 55 nm
- Chip size: 2 cm × 2 cm
- Sensor thickness: 150 μm
- Array size: 512 rows × 128 columns
- Pixel size: 34 μm × 150 μm
- Spatial resolution: 8 μm × 40 μm
- Time resolution: 3-5 ns
- Power consumption: 200 mW/cm$^2$





Latest HV-CMOS COFFEE3 chip (submitted for tap-out in Jan 2025)

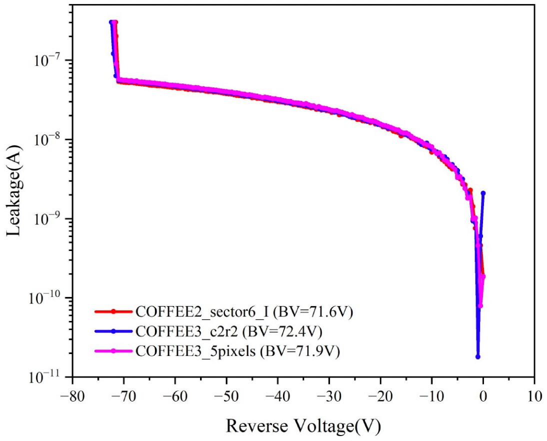
# Latest HV-CMOS Pixel Sensor COFFEE3 (1)



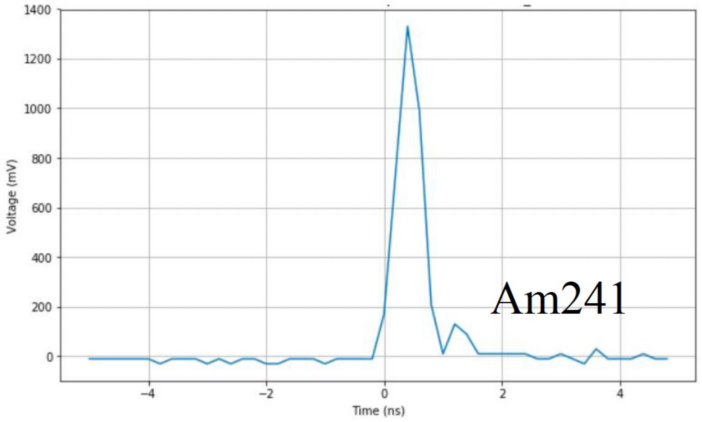
COFFEE3 sensor received at the end of May

See details in Yang Zhou's talk

**Passive diode array**: validation of sensor performance; test result consistent with COFFEE2.

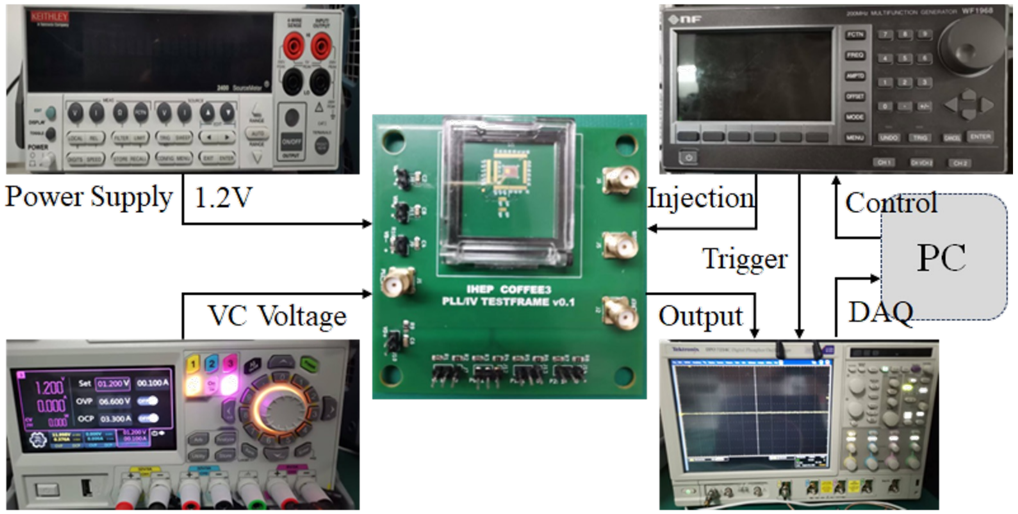


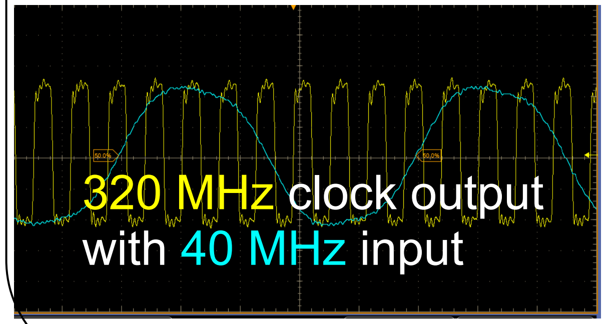
Breakdown voltage: -71V



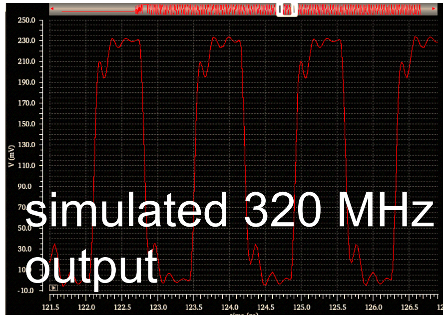
Responsive to $\alpha$ radioactive source

**PLL**: A new module for clock synchronization, providing up to 320 MHz output from a 40 MHz input (higher output limited by the test setup).





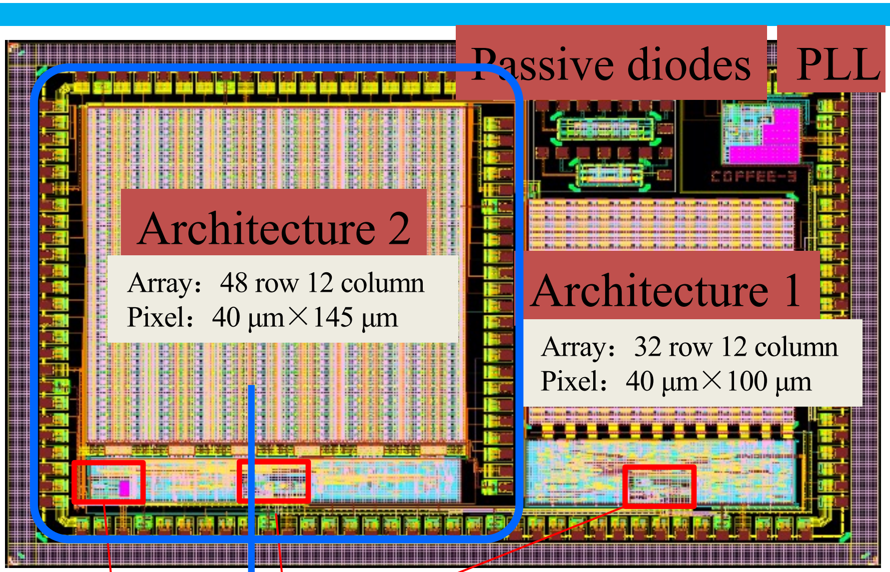
320 MHz clock output with 40 MHz input



simulated 320 MHz output

# Latest HV-CMOS Pixel Sensor COFFEE3 (2)

See details in Yang Zhou’s talk



Passive diodes

PLL

Architecture 2

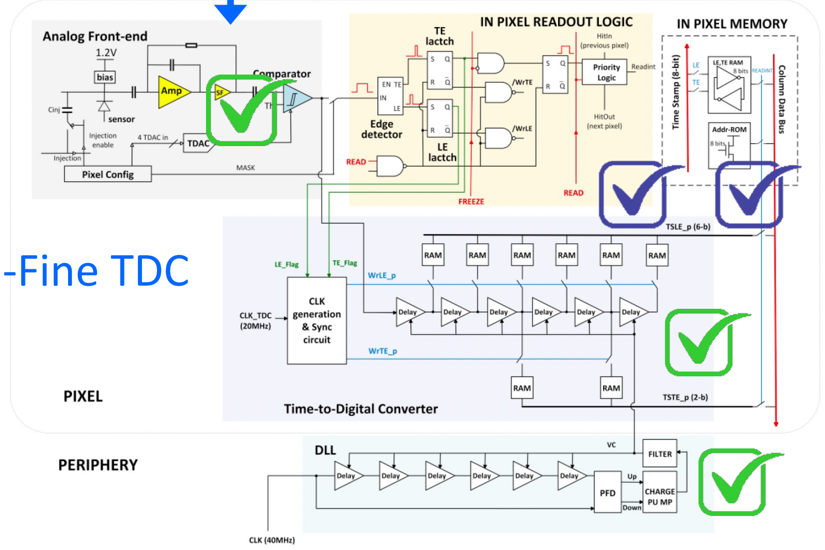
Array：48 row 12 column
Pixel：40 μm×145 μm

Architecture 1

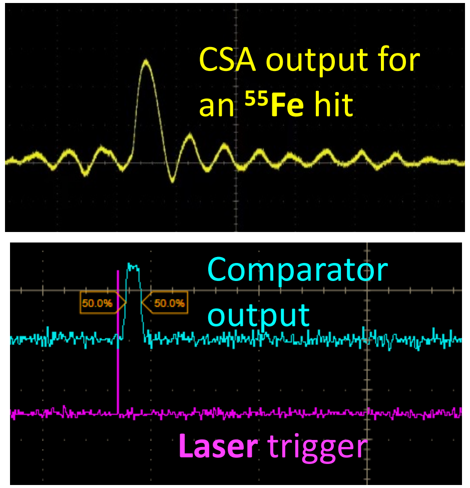
Array：32 row 12 column
Pixel：40 μm×100 μm

DLL

LVDS driver/receiver



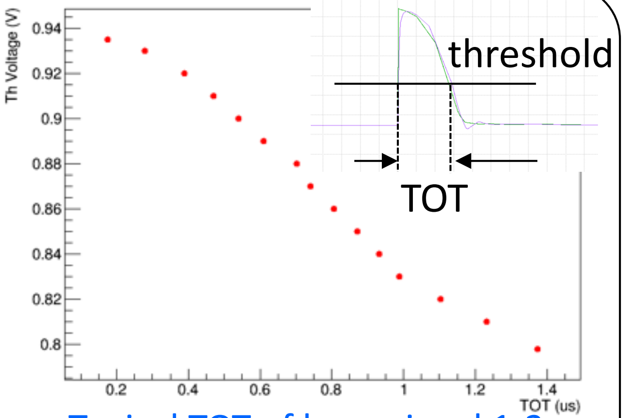
In-pixel Coarse-Fine TDC



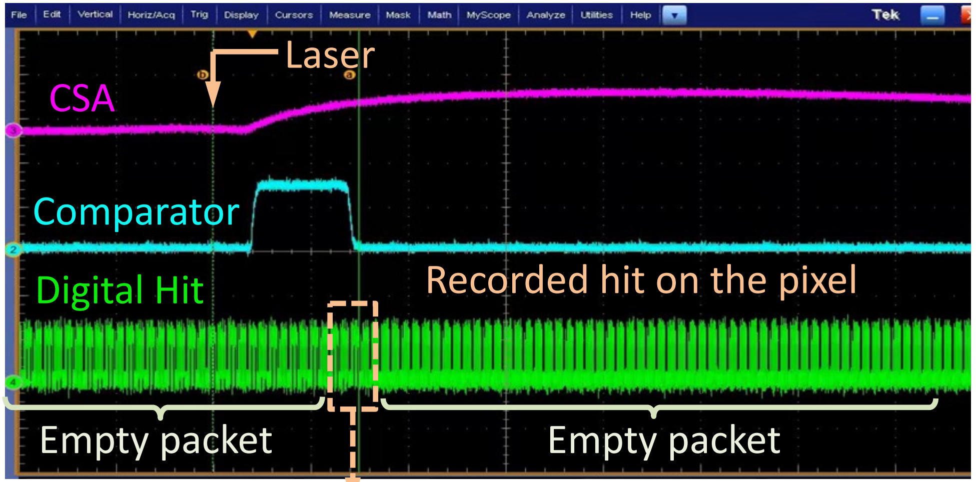
CSA output for an $^{55}$**Fe** hit

Comparator output

**Laser** trigger



Typical TOT of laser signal 1-2 μs, consistent with simulation



Laser

CSA

Comparator

Digital Hit

Recorded hit on the pixel

Empty packet

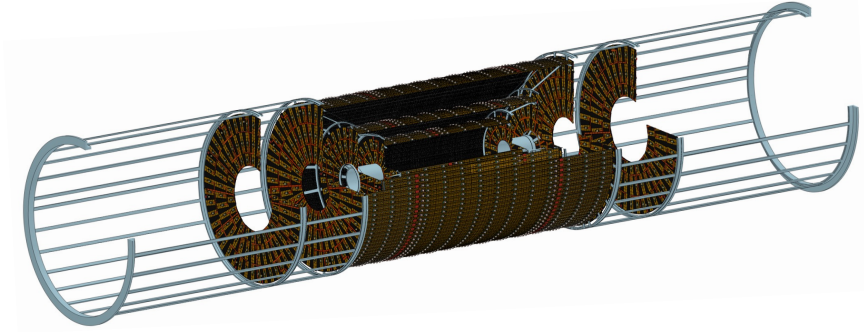
Empty packet

| 4 bit | 4 bit | 8 bit | 8 bit | 6 bit | 2 bit | 7 bit | 3 bit |
|---|---|---|---|---|---|---|---|
| header | CHIP_TS | LE_coarse | TE_coarse | LE_fine | TE_fine | Addr_Row | Add_Col |
| 0 1 1 0 | 0 1 0 1 | 0 0 0 1 0 1 1 0 | 0 1 1 0 1 0 1 1 | 1 1 0 0 0 0 | 0 0 | 0 0 0 0 0 0 1 | 0 0 0 |

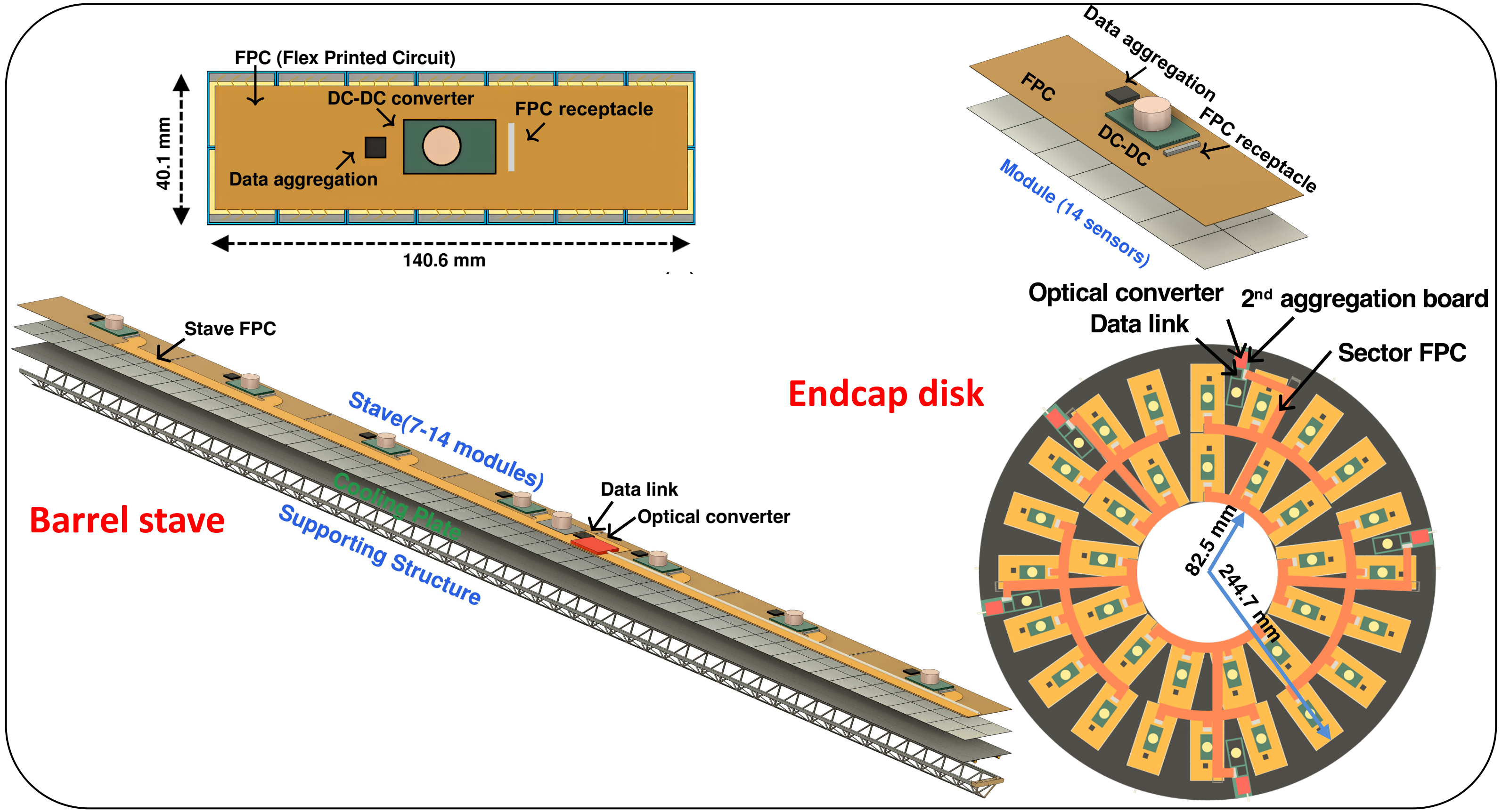
A valid transmission packet corresponding to a hit

Correct row & column address

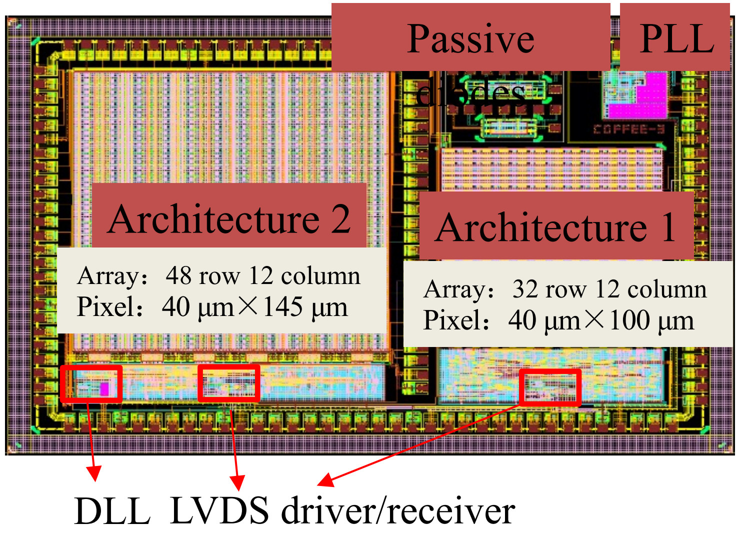
# ITK Design Based on HV-CMOS Pixel Sensor



- ❑ The designed inner tracker comprises three barrel layers and four endcap layers, with a total active area of 20 m² and 47,024 sensors in total.



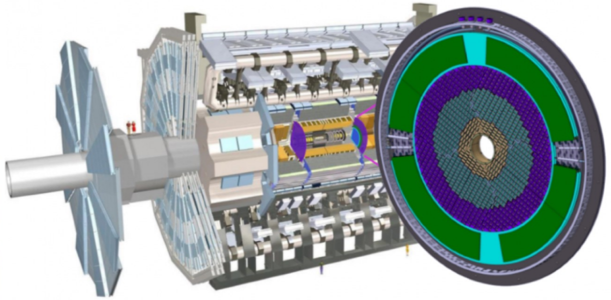
## HV-CMOS sensor prototype (COFFEE3)



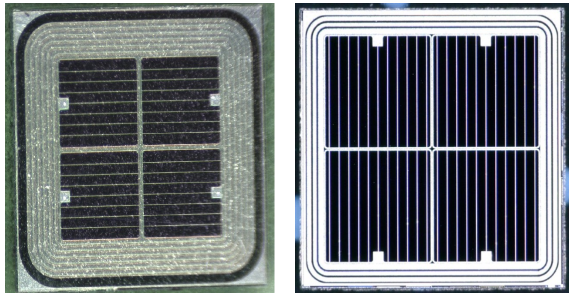
| HV-CMOS sensor specification for ITK | |
|---|---|
| Sensor size | 2 cm × 2 cm |
| Sensor thickness | 150 μm |
| Array size | 512 × 128 |
| Pixel size | 34 μm × 150 μm |
| Spatial resolution | 8 μm × 40 μm |
| Timing resolution | 3-5 ns |
| Power | 200 mW/cm² |
| Process node | 55 nm |

# LGAD Sensor Development at IHEP

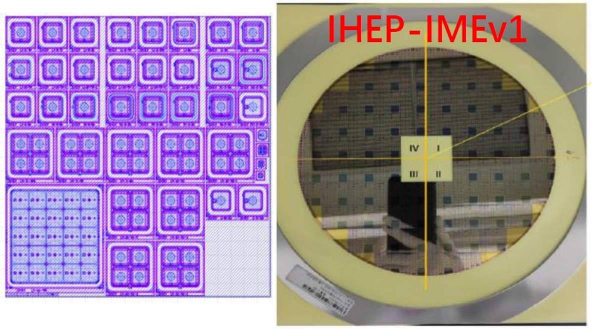
- The LGAD (Low Gain Avalanche Detector) sensor developed by IHEP achieves both precise position and time measurements under high radiation levels.



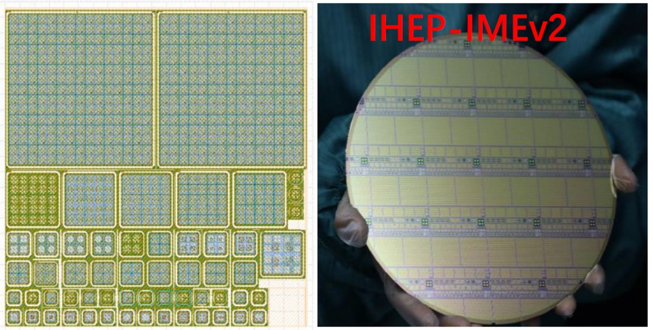
IHEP(2019)



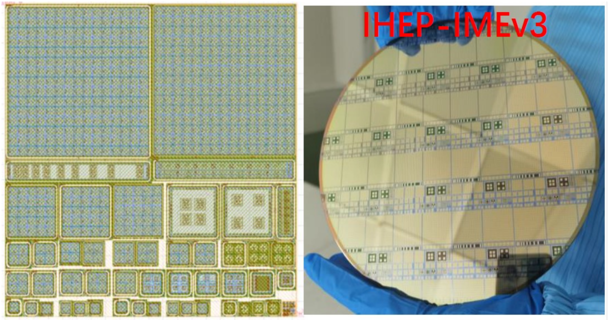
IHEP (2020.9)



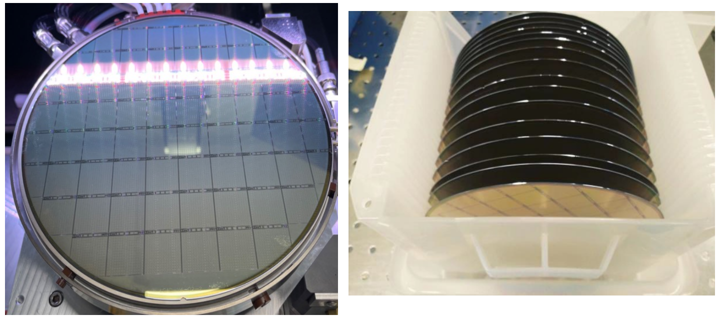
IHEP (2021.6)



IHEP (2022.5)

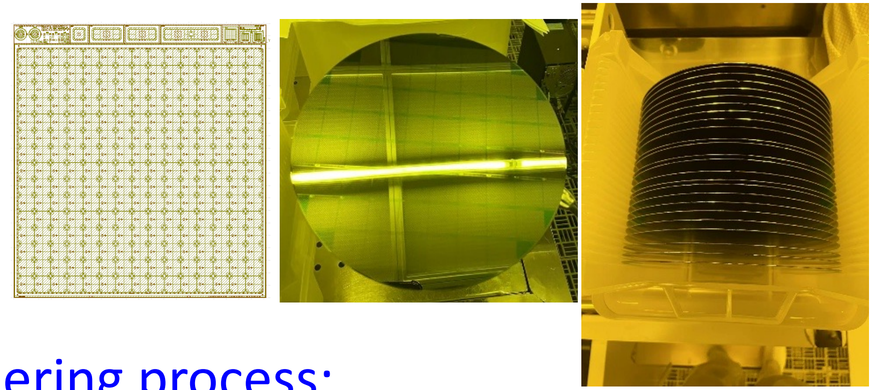


Pre-production for ATLAS (2023.7)



→

Mass production for ATLAS since 2024.6

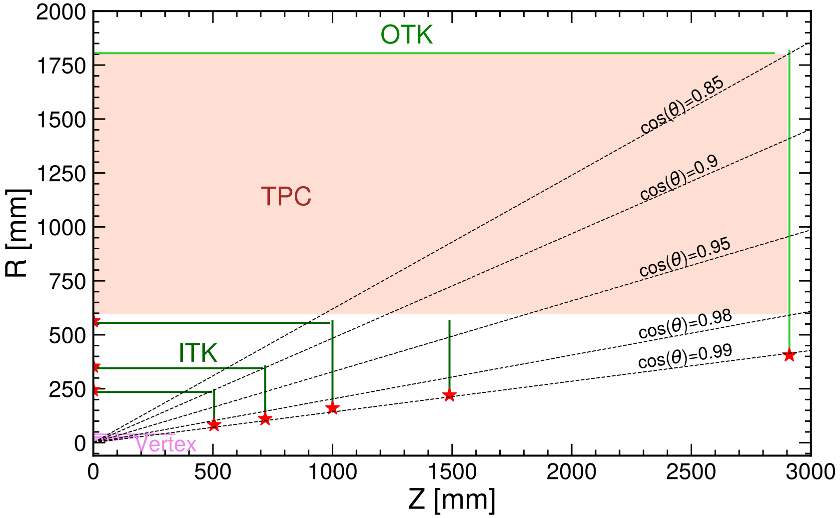


- In May 2023, CERN selected IHEP in the HGTD sensor tendering process:
  - First time a domestic silicon sensor was chosen by CERN for an LHC experiment.

# AC-LGAD for CEPC OTK with Precision Timing

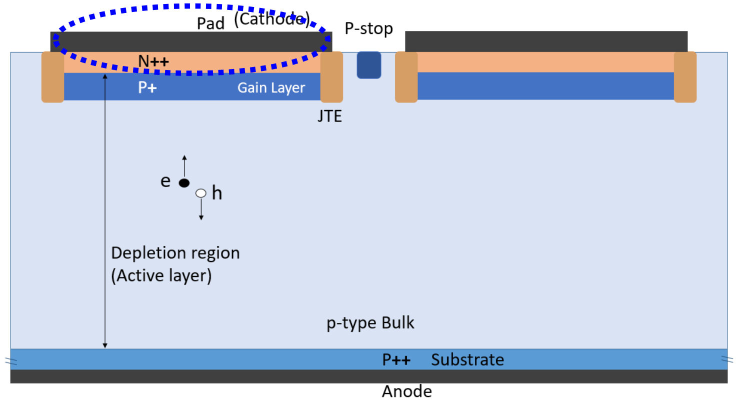
## Key parameters of AC-LGAD microstrip sensor for OTK:

| | |
|---|---|
| Sensor size: | (3-4.5) cm × (3-5) cm |
| Strip number: | 512 or 384 |
| Sensor thickness: | 300 µm |
| Pitch size: | ~100 µm |
| Spatial resolution: | 10 µm |
| Time resolution: | 50 ps |
| Power consumption: | 300 mW/cm$^2$ |



### LGAD (Low-Gain Avalanche Detector)

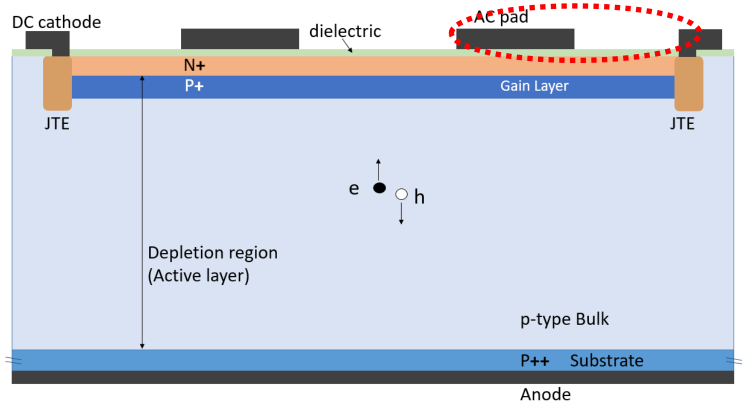
Segmented gain layer



- The read-out electrode is connected to the N++ layer.

### AC-LGAD (AC-coupled LGAD)

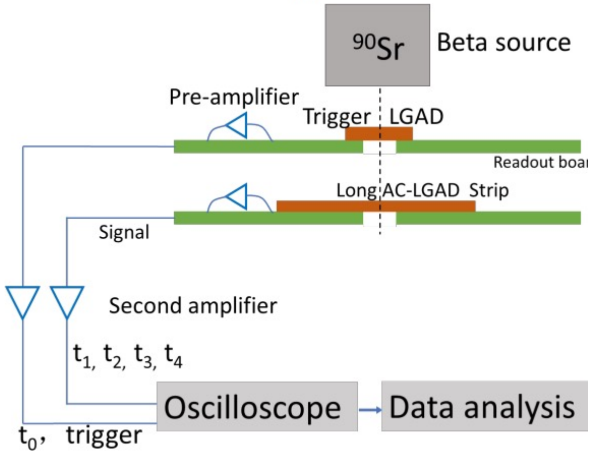
Bulk gain layer (less dead area)



- A thin dielectric layer ($Si_3N_4$ or $SiO_2$) separates the metal AC pads from the N+ layer.

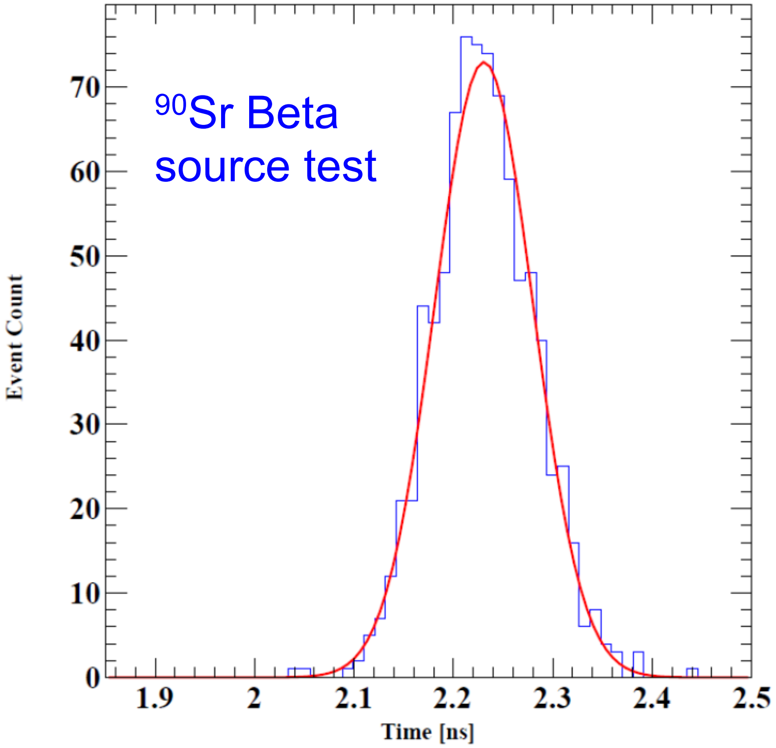
# AC-LGAD Performance: Time and Spatial Resolution

$^{90}$Sr test setup



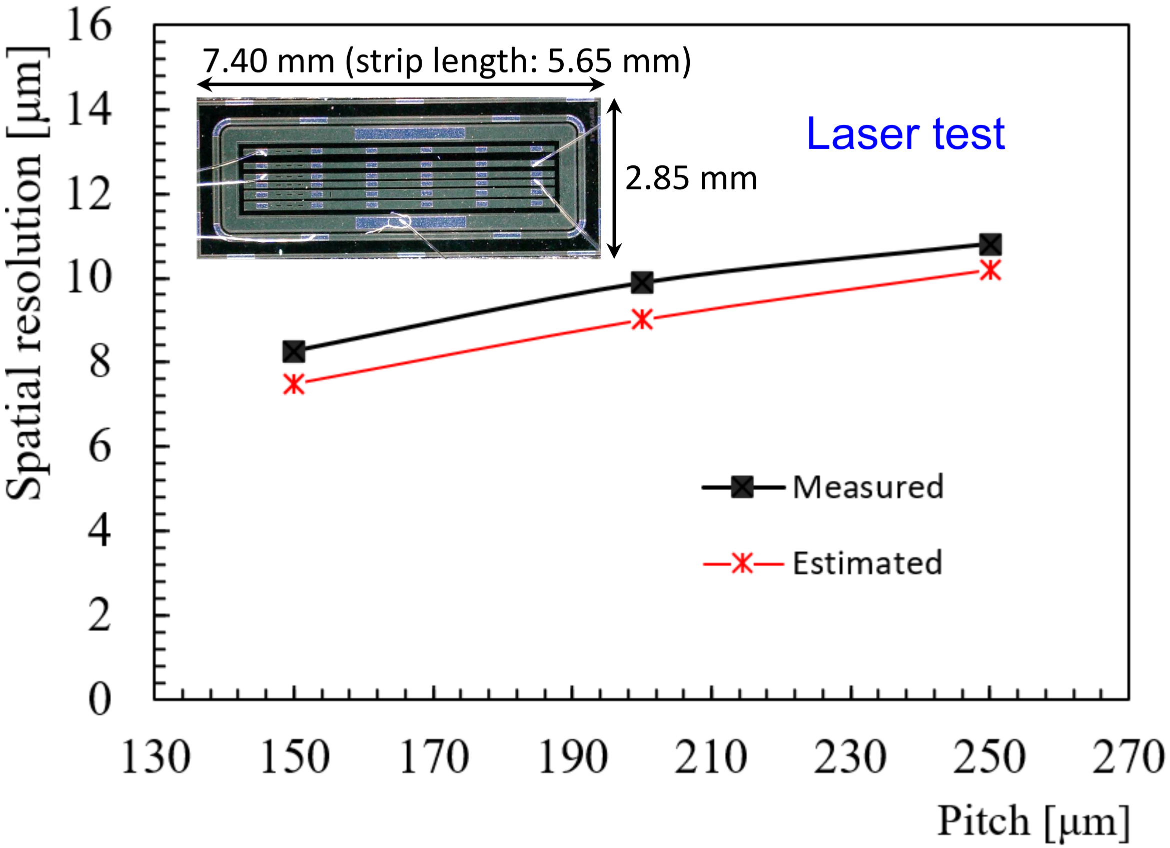
See details in Mei Zhao’s talk

$^{90}$Sr Beta source test



Time resolution: 38 ps

Laser test



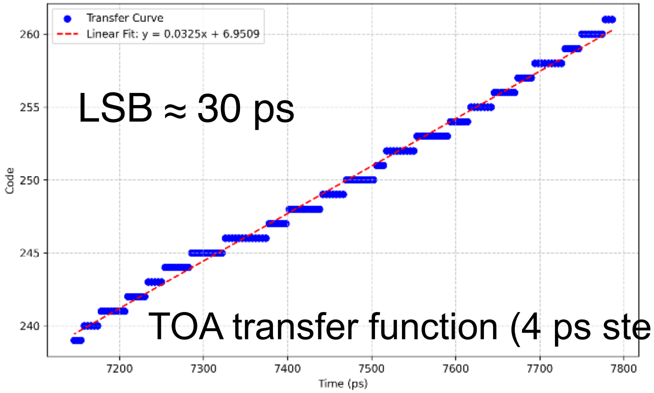
Spatial resolution: 8 μm for 150 μm strip pitch

# New Developed LGAD Readout ASIC (LATRIC)

The first LATRIC prototype, LATRIC-V0, submitted for tape-out in April, was delivered to IHEP in Aug:

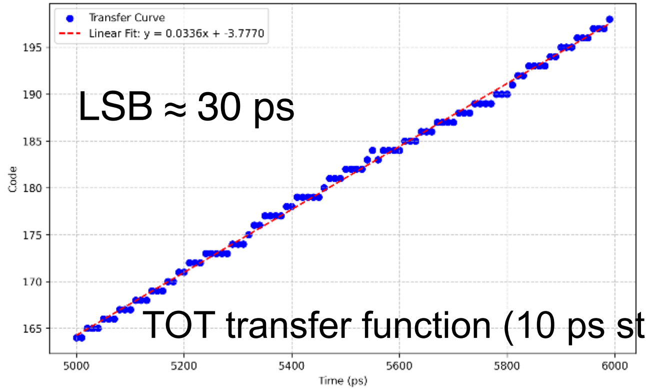
- The ASIC integrates a pre-amplifer, a discriminator, a TDC, and a serializer for data output.
- Tests find that the LSB is 29.8 ps, meeting the 30 ps design goal. The measured TDC power consumption is 0.1 mA (1.2 V) @ 0.5 MTPS (Mega-Trigger Per Second), 0.3 mA @ 1 MTPS, and 0.5 mA @ 2 MTPS, agreeing with the design.

The next 8-channel LATRIC-V1 was submitted for tape-out in October.



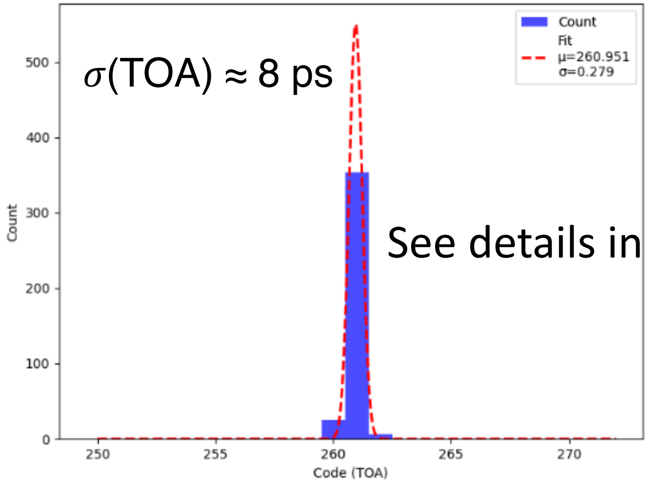
LSB ≈ 30 ps

TOA transfer function (4 ps step)

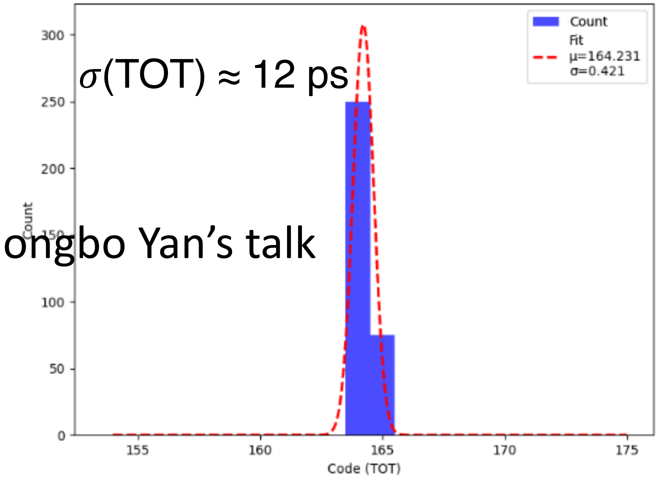


LSB ≈ 30 ps

TOT transfer function (10 ps step)

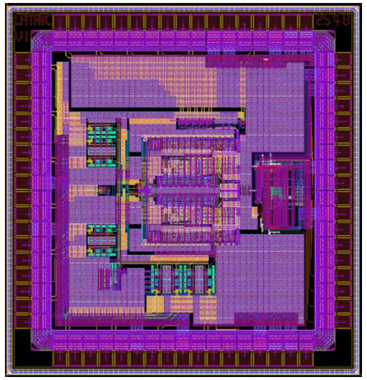


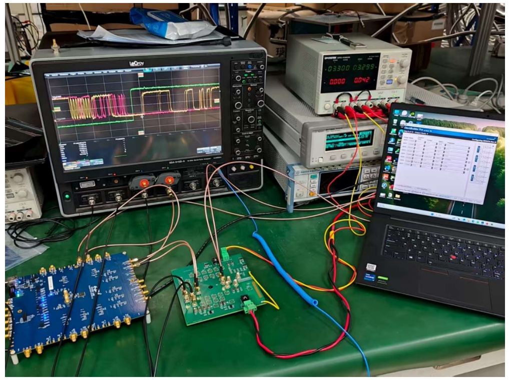
$\sigma$(TOA) ≈ 8 ps



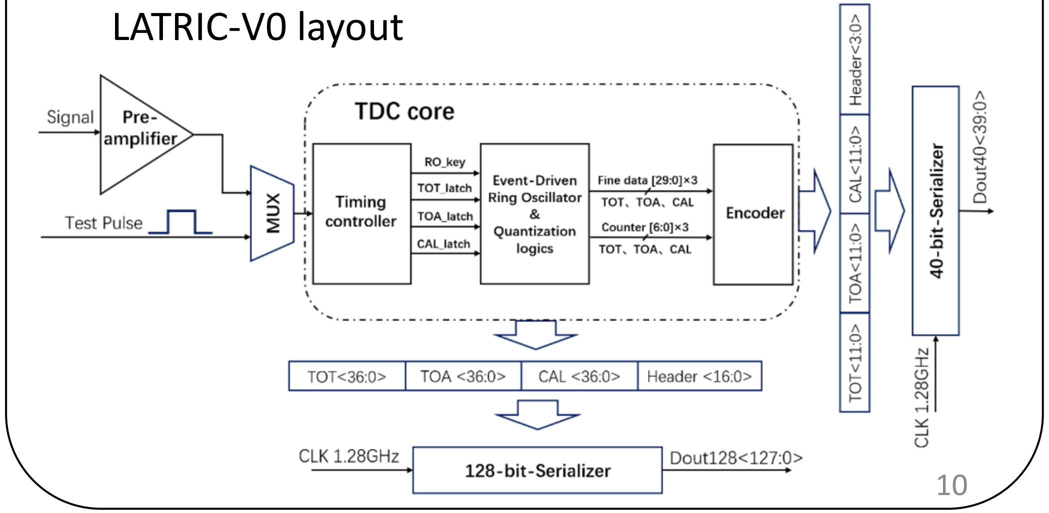
$\sigma$(TOT) ≈ 12 ps

See details in Xiongbo Yan's talk

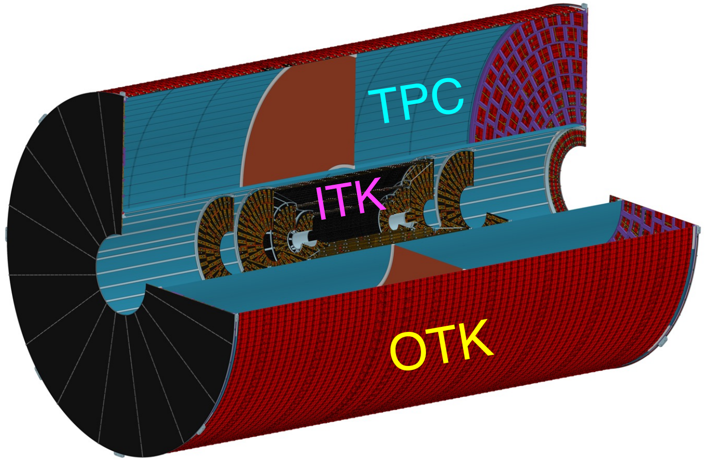




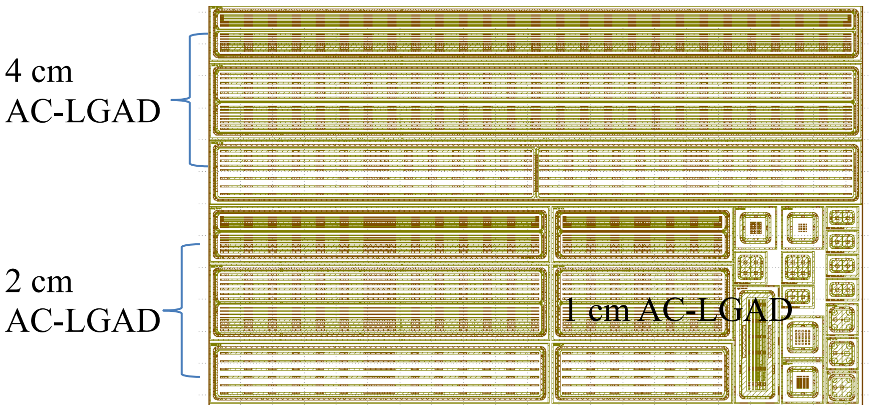
LATRIC-V0 layout



# OTK Design Based on LGAD Strip Sensor

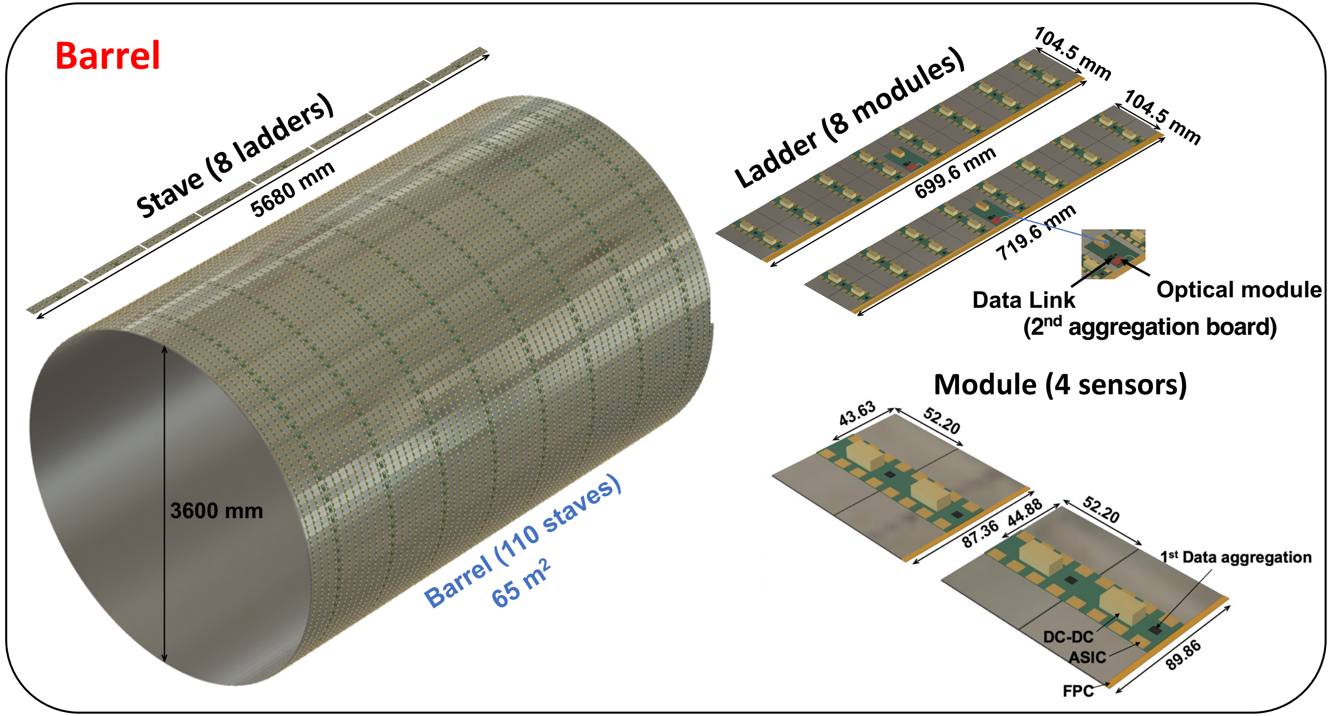


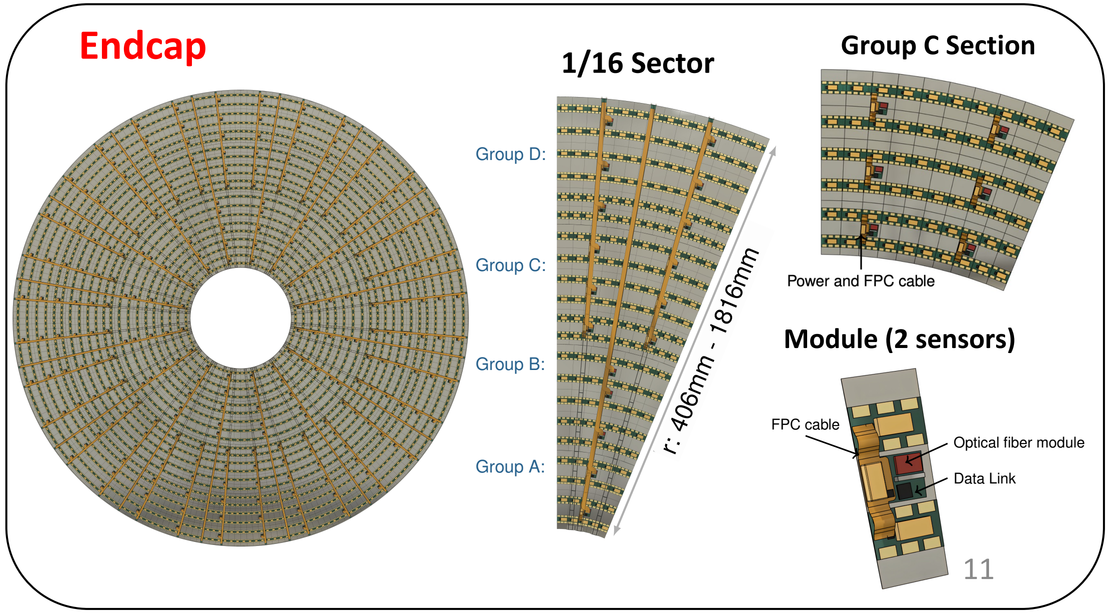
## AC-LGAD prototype (latest submitted)



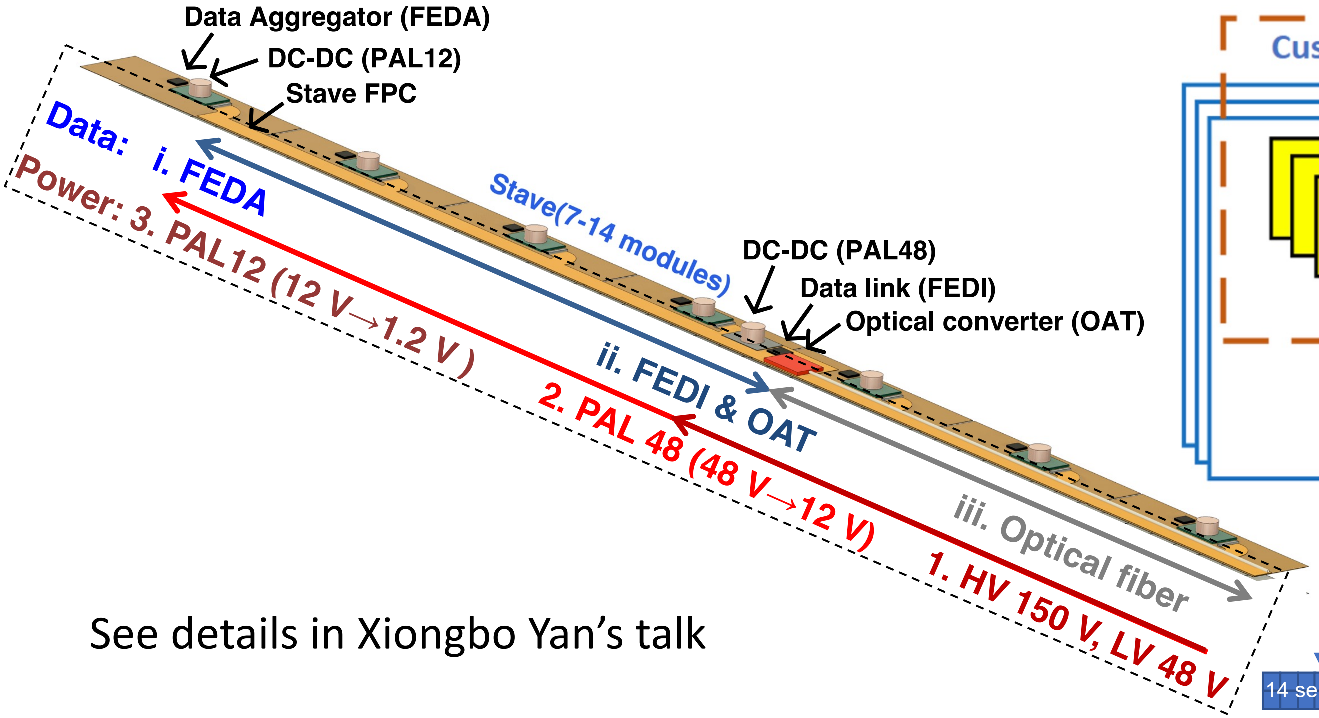
- One barrel layer and one endcap layer (~85 m$^2$).
- The latest LGAD sensor was submitted for tape-out in March and waiting for the return.

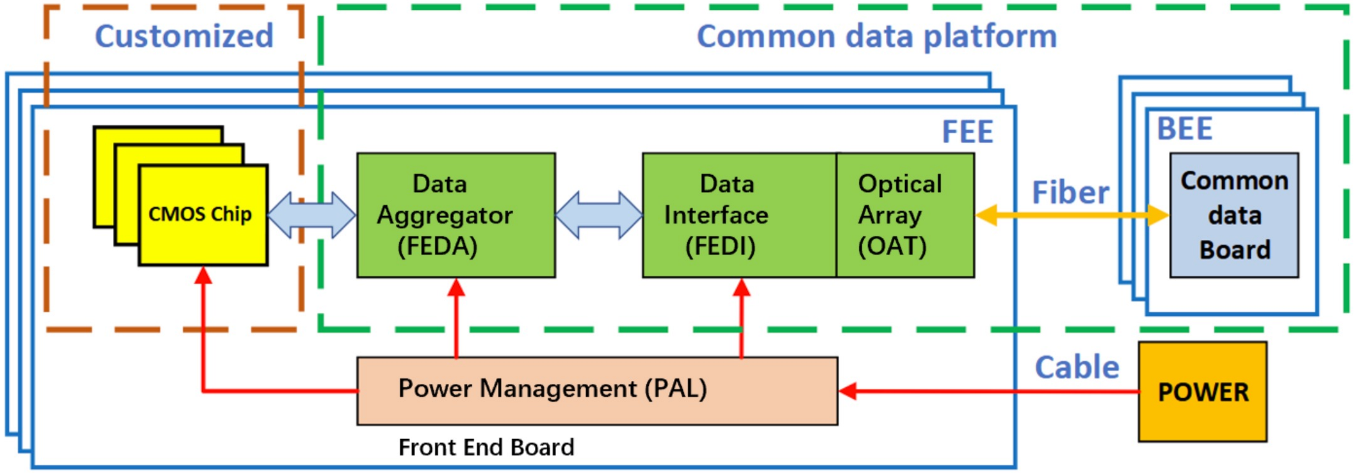
| LGAD sensor specification for OTK | |
|---|---|
| Sensor size | (3-4.5) cm × (3-5) cm |
| Strip pitch | ~100 µm |
| Spatial resolution | 10 µm |
| Timing resolution | 50 ps |
| Power | 300 mW/cm$^2$ |





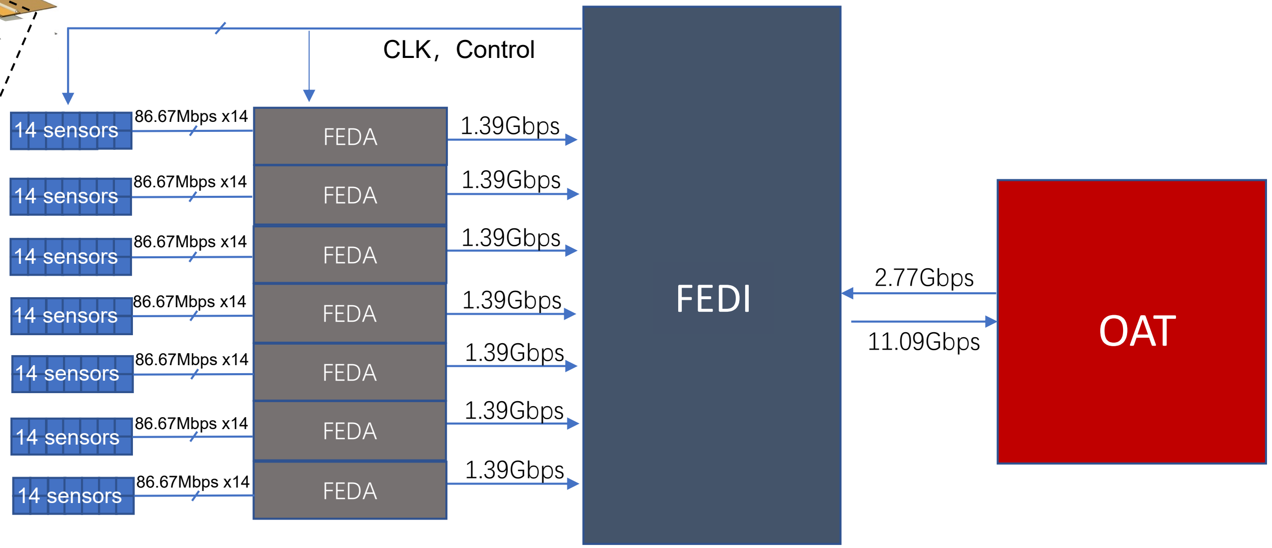
# Design Including Power and Readout Electronics





See details in Xiongbo Yan’s talk

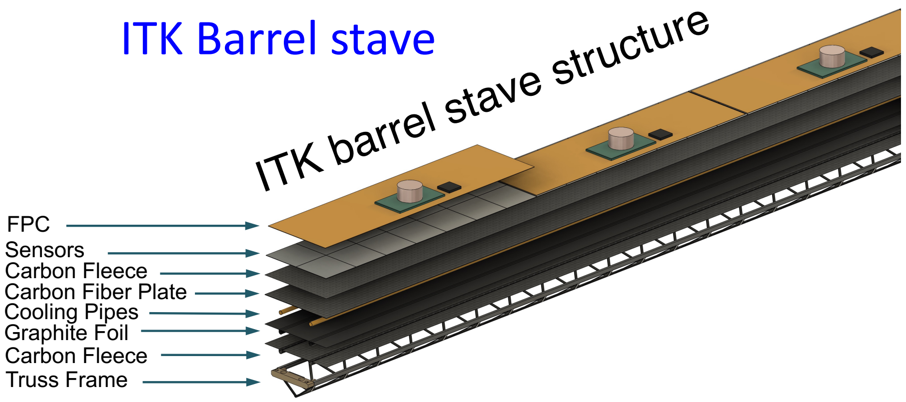
- ❑ In the readout design, each sensor can tolerate up to 86.67 Mbps, corresponding to a maximum hit rate of $4.1\times10^5$ Hz/cm$^2$ – about 42 times higher than the estimated peak background hit rates ($9.9\times10^3$ Hz/cm$^2$) under the most challenging high-luminosity $Z$-pole operation mode.



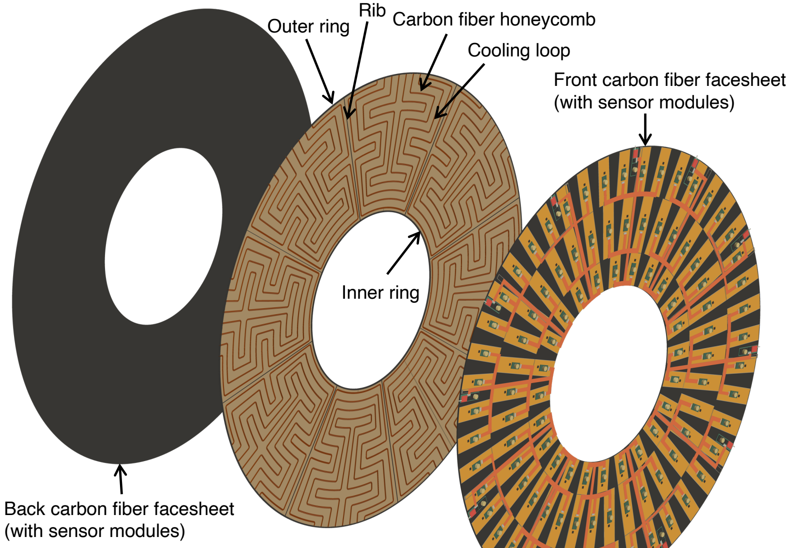
The FEDA, FEDI, OAT, and PAL chips are under development by the CEPC team.

# Design Including Cooling and Mechanics (1)

ITK Barrel stave

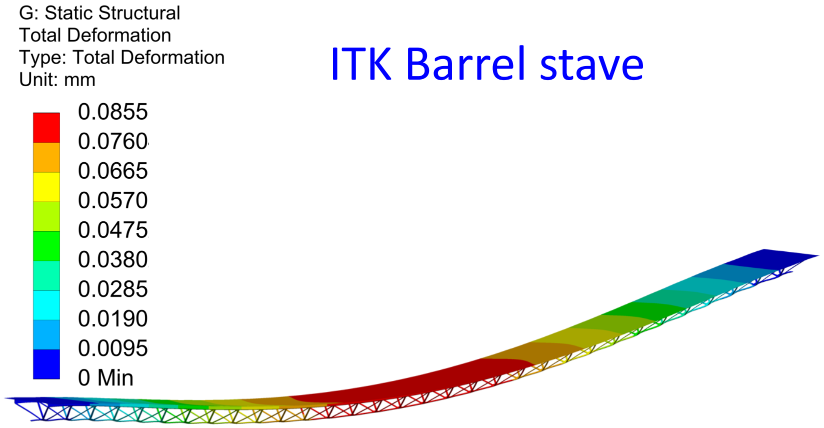


ITK Endcap



See details in Yujie Li's talk

ITK Barrel stave

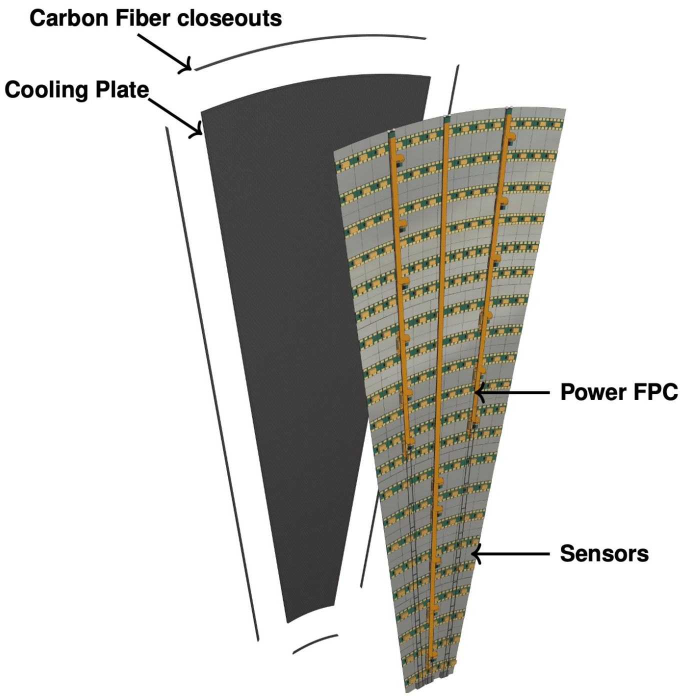


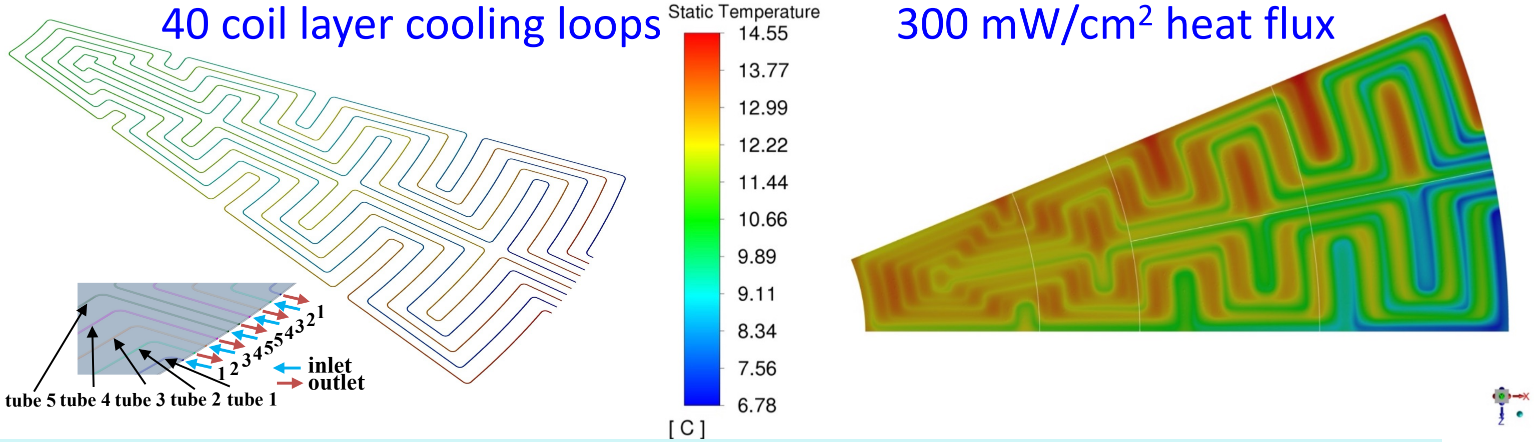
Maximum sag of first ITK barrel stave is 85 µm.

| Functional unit | Component | Material | Thickness [µm] | $X_0$ [cm] | Radiation Length [% $X_0$] |
|---|---|---|---|---|---|
| Sensor Module | FPC metal layers | Aluminium | 100 | 8.896 | 0.112 |
| | FPC Insulating layers | Polyimide | 150 | 28.41 | 0.053 |
| | Sensor | Silicon | 150 | 9.369 | 0.160 |
| | Glue | | 100 | 44.37 | 0.023 |
| | Other electronics | | | | 0.050 |
| Cooling Plate | Carbon fleece layers | Carbon fleece | 40 | 106.80 | 0.004 |
| | Carbon fiber plate | Carbon fiber | 150 | 26.08 | 0.057 |
| | Cooling tube wall | Polyimide | $64^\dagger$ | 28.41 | 0.006 |
| | Cooling fluid | Water | | 35.76 | 0.028 |
| | Graphite foil | Graphite | 30 | 26.56 | 0.011 |
| | Glue | Cyanate ester resin | 100 | 44.37 | 0.023 |
| Truss Frame | Carbon rowing | | | | 0.080 |
| Power Bus FPC | | | | | 0.070 |
| Total | | | | | 0.677 |

# Design Including Cooling and Mechanics (2)

OTK endcap 1/16 sector




40 coil layer cooling loops

300 mW/cm² heat flux

- ❑ The OTK endcap 1/16 sector uses 5-loop water cooling pipes with a pipe inner diameter of 2.3 mm, a flow velocity of 2 m/s, and an inlet temperature of 5°C. The sensor temperature is <15°C and sensor temperature gradient is <4°C.

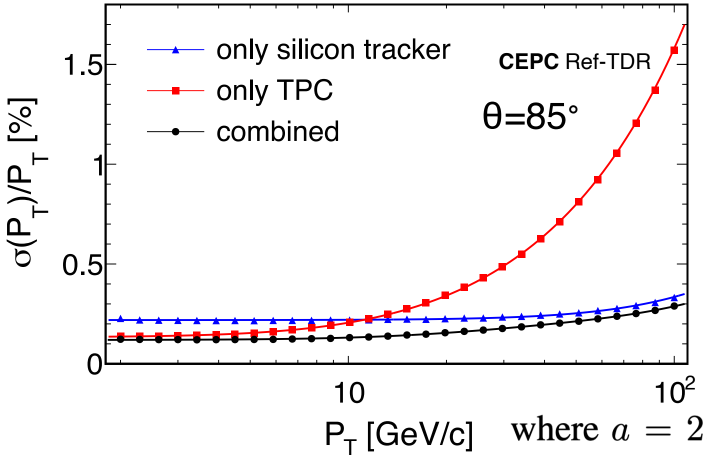
Although water cooling has been adopted as the baseline due to its overall system simplicity, we have recently initiated R&D on $CO_2$ cooling.

Technical Institute of Physics and Chemistry, CAS
(New $CO_2$ cooling collaborator)

See details in Yujie Li's talk

# Performance

Momentum resolution in the barrel region:



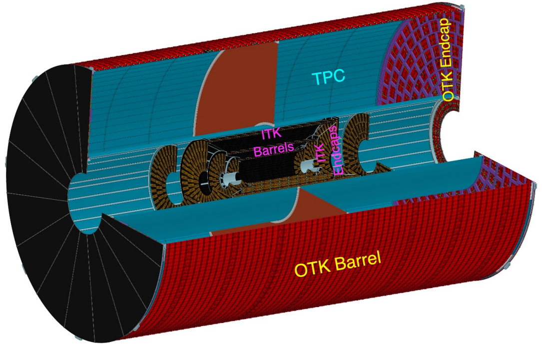
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Si}} = a p_t \oplus \frac{b}{\beta\sqrt{\sin\theta}}$$

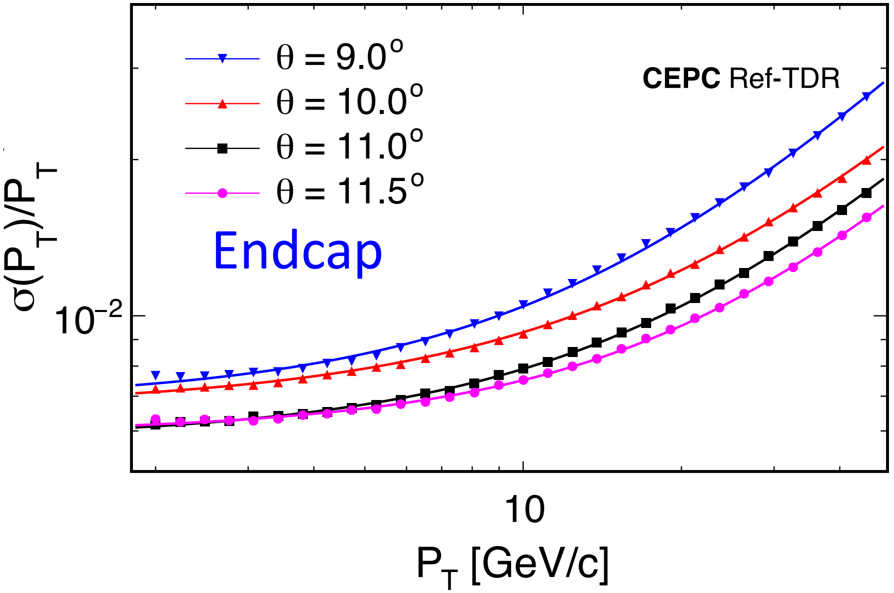
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{TPC}} = a s_1 p_t \oplus \frac{b s_2}{\beta\sqrt{\sin\theta}}$$

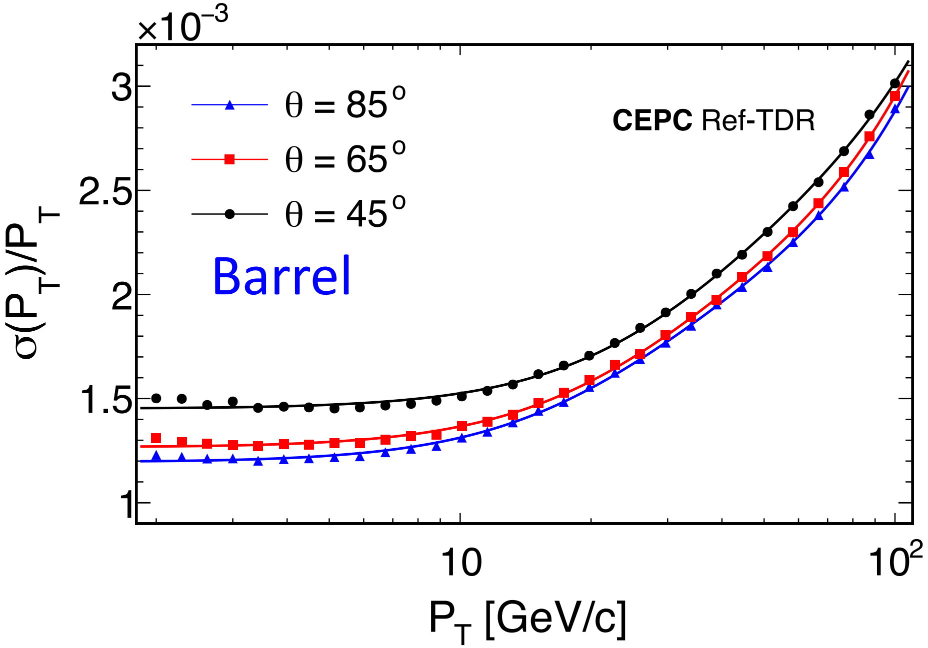
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Combined}} = \frac{1}{\sqrt{\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Si}}^{-2} + \left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{TPC}}^{-2}}}$$

where $a = 2.1 \times 10^{-5}$, $b = 2.2 \times 10^{-3}$, $s_1 \approx 4$, and $s_2 \approx 0.6$.

- ❑ Full simulation: systematic study of the tracker design and its performance







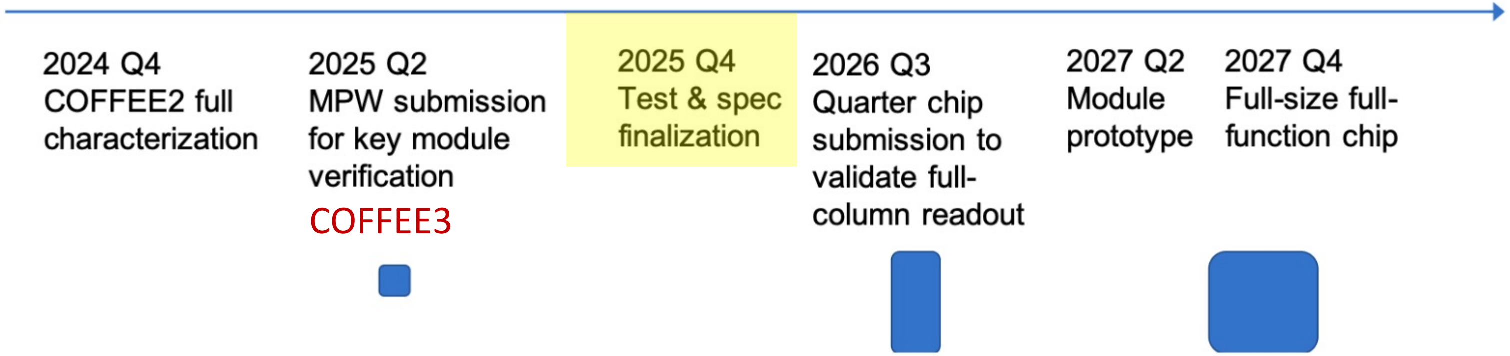
Momentum resolution in the endcap region:

$$\frac{\sigma_{p_t}}{p_t} = \frac{a' p_t}{(tan\theta)^2} \oplus \frac{b'}{\beta tan\theta\sqrt{\cos\theta}} \oplus \frac{c'\sqrt{p_t}}{\sqrt{\beta}(\tan\theta)^{\frac{3}{2}}(\cos\theta)^{\frac{1}{4}}}$$

where $a' \approx 1.1 \times 10^{-5}$, $b' \approx 1.1 \times 10^{-3}$, and $c' = 1.2 \times 10^{-4}$

# R&D Plan Following the Ref-TDR

- HV-CMOS pixels:



2024 Q4
COFFEE2 full characterization

2025 Q2
MPW submission for key module verification
COFFEE3

2025 Q4
Test & spec finalization

2026 Q3
Quarter chip submission to validate full-column readout

2027 Q2
Module prototype

2027 Q4
Full-size full-function chip

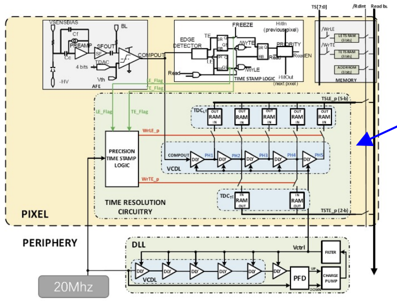
- AC-LGAD strips+ASIC:

| | 2024 Q4 | 2025 Q2 | 2025 Q4 | 2026 Q2 | 2026 Q4 | 2027 Q2 | 2027 Q4 |
|---|---|---|---|---|---|---|---|
| Sensor: | OTKLGAD 1st design | OTKLGAD 1st submission (4 cm long) | Sensor Test | OTKLGAD 2nd submission (optimization) | Test with ASIC Test beam radiation test | OTKLGAD 3rd submission (large array) | Sensor Test |
| ASIC: | | LATRIC ASIC 1st submission<br>LATRIC-V0 | ASIC Test | LATRIC ASIC 2nd submission<br>8 channel LATRIC-V1 | ASIC Test | LATRIC ASIC 3rd submission<br>64 channel LATRIC-V2 | ASIC Test |
| Module: | | | | Module built and test | Module built and test | | prototype built and test (large size) |

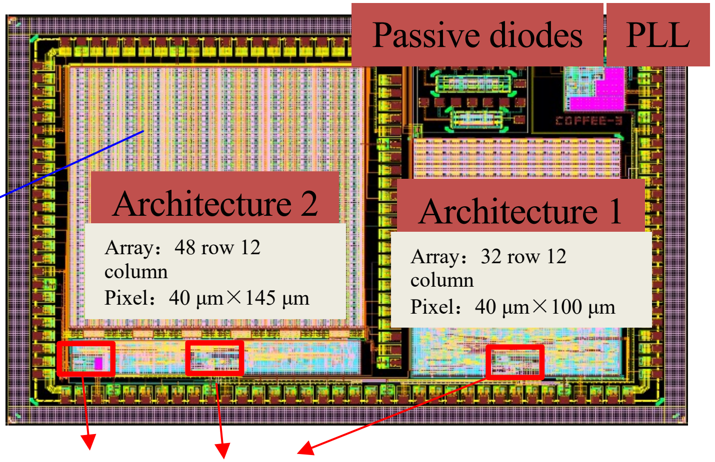
Development of the mechanical and cooling systems is progressing in parallel, with the goal of delivering a prototype detector by the end of 2027.

# Next HV-CMOS Sensor R&D

- The latest developed prototype sensor, COFFEE3, integrates two readout architectures:
  - A readout architecture using only NMOS within the pixel, supported by a triple-well process.
  - A digital CMOS (NMOS + PMOS) readout architecture within the pixel, which requires a quadruple-well process with an additional deep P-well.
- COFFEE3 has preliminarily validated the design of both analog and digital components, including:
  - Pre-amplifier, discriminator, in-pixel TDC, PLL, serializer, etc
- The next stage will mainly address process-related issues:
  - The currently used low-resistivity wafer (~10 Ω·cm) has a shallow depletion depth (~10 µm), resulting in a low S/N ratio (the current MIP signal is ~1120 e⁻).
  - The triple-well process currently in use cannot fully support complete in-pixel CMOS circuitry (both PMOS and NMOS): signal crosstalk.



- In-pixel coarse-fine TDC


Passive diodes

PLL

Architecture 2

Array：48 row 12 column

Pixel：40 µm×145 µm

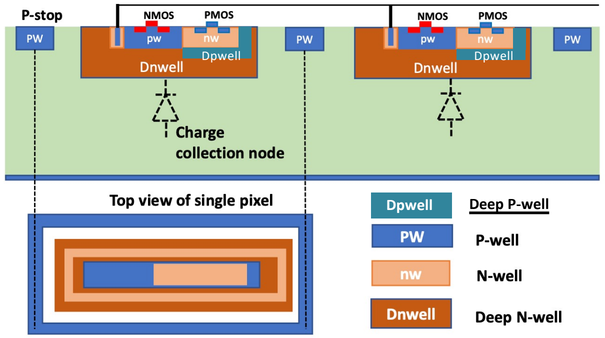
Architecture 1

Array：32 row 12 column

Pixel：40 µm×100 µm

DLL

LVDS driver/receiver

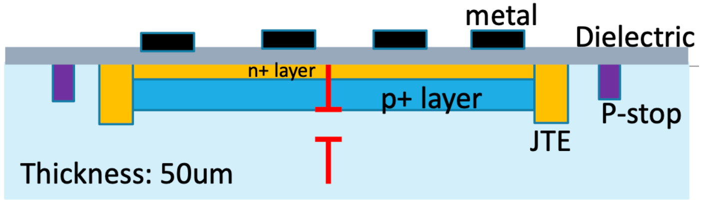


See details in Yang Zhou's talk

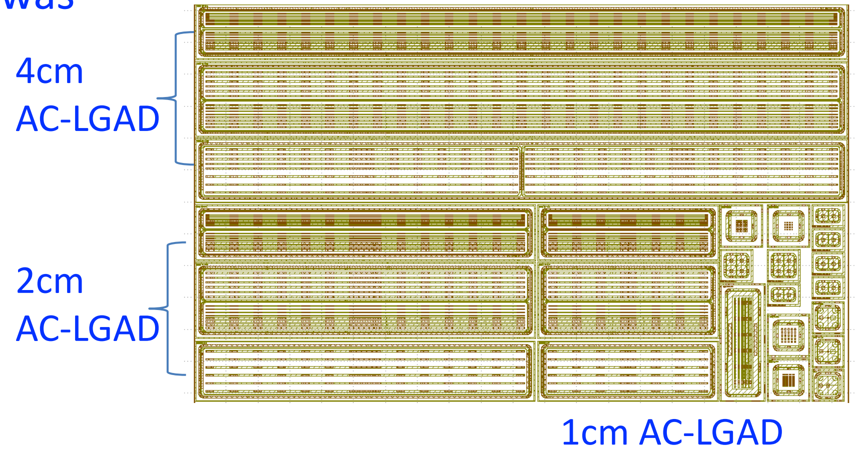
Cooperation with a new foundry on the use of high-resistivity wafers (>1000 Ω·cm) and the implementation of a quadruple-well process. A new tape-out is planned for the end of 2025.

# Next LGAD Sensor R&D

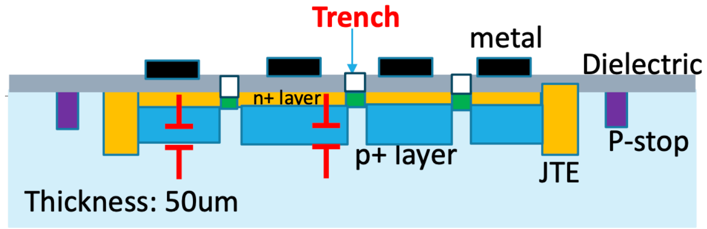
- The LGAD microstrip sensors are toward larger sizes, aiming for ultimate position and time resolution, as well as lower power consumption. The latest sensor tape-out was submitted in March, and the sensors will return soon:
  - Strip lengths：  1 cm, 2 cm, and 4 cm
  - Strip pitch sizes:  100 µm, 200 µm, and 500 µm
  - Electrode widths: 25 µm, 50 µm, and 100 µm
  - Optimized EPI thickness to reduce sensor capacitance (correlated with power consumption)
  - Process optimization (n+ layer dose) for better spatial resolution



LGAD layout submitted in March



- The next trenched-structure LGAD developed with SIMIT&SITRI is an essential step toward the ultimate LGAD design, as the capacitance has been greatly reduced to achieve the target power consumption. The sensor layout is already close to its final design and planed to tape-out recently.

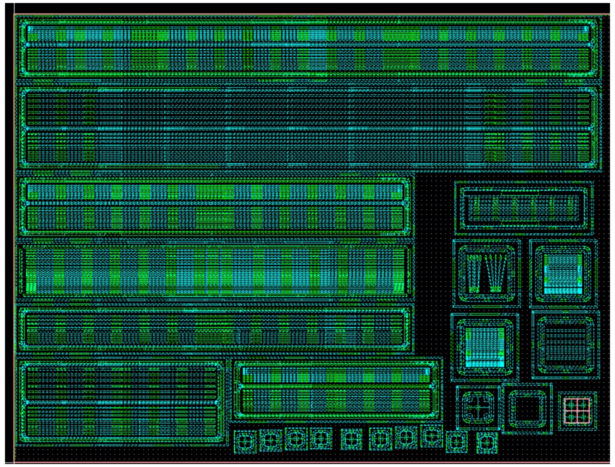


Introducing isolated structure

$$C = \varepsilon_0 * \varepsilon_r * A\downarrow / d$$

See details in Mei Zhao's talk

LGAD layout for tape-out with trench design
(to be submitted)



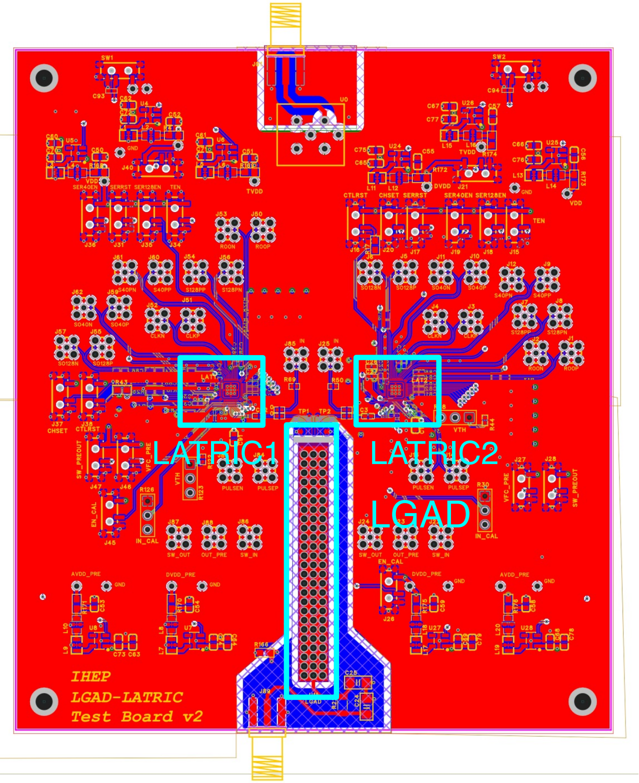
# Next LGAD Readout ASIC (LATRIC-V1) R&D

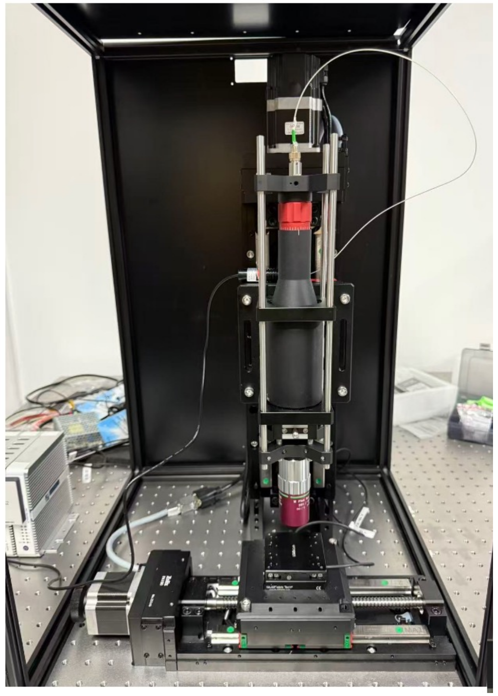
- The design of the new 8-channel LATRIC-V1 chip has been completed and was submitted for fabrication in mid-October.

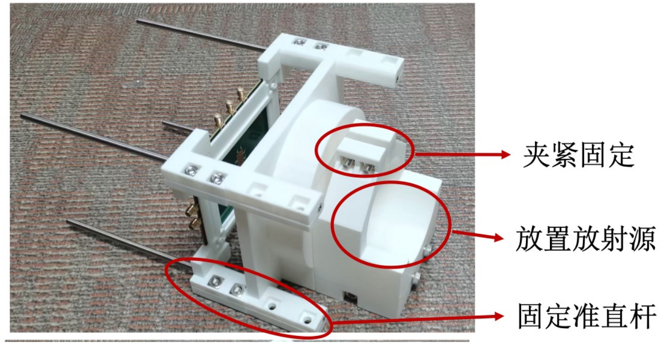
See details in Xiongbo Yan’s talk

# LGAD and LATRIC Combined Test

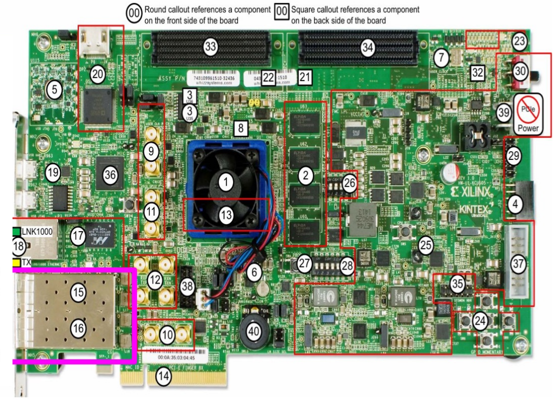
- The combined test of the LGAD and LATRIC ASIC is currently on going:
  - The first test board, integrating two LATRIC (V0) chips and one LGAD sensor, has been fully designed and fabricated.
  - The DAQ firmware supporting high-speed data readout of LATRIC is ready.
  - Laboratory setups for laser and β-source measurements, used to evaluate time and position resolutions, have been completed.
  - The complete beam test is schedule for mid-2026 .




laser setup

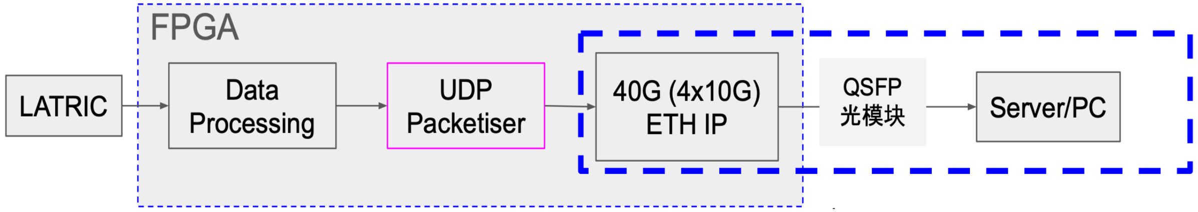


β-source setup



**KCU105**

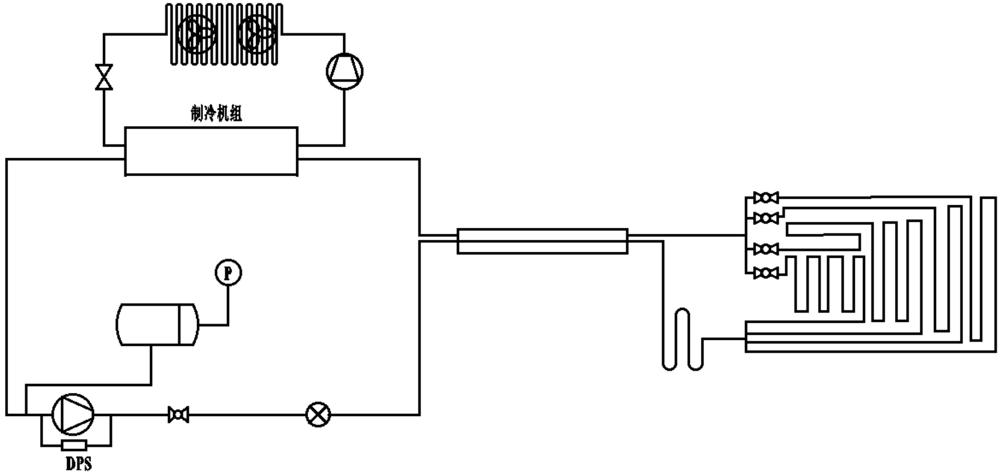
Kintex UltraScale
XCKU040-2FFVA1156E Device


FPGA

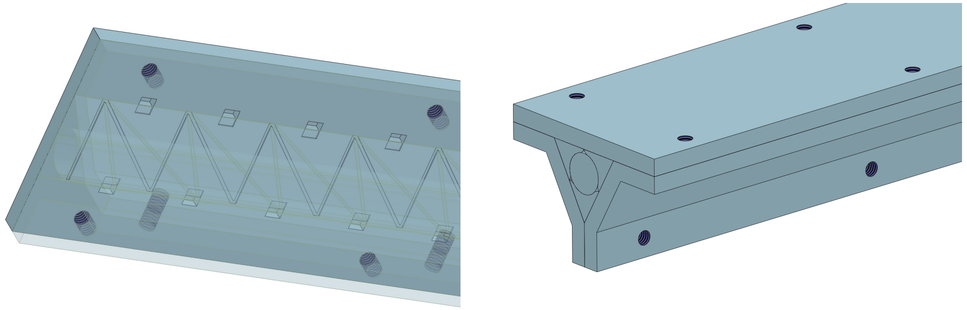
LATRIC → Data Processing → UDP Packetiser → 40G (4x10G) ETH IP → QSFP 光模块 → Server/PC

# Two-Phase $CO_2$ Cooling and Mechanical Module Development

- We aim to develop the first two-phase $CO_2$ cooling system prototype by mid-2026, in collaboration with the Technical Institute of Physics and Chemistry (TIPC), CAS. This prototype is designed to be compact and portable, capable of handling a nominal heat dissipation power of 2 kW (up to 4 kW), with a $CO_2$ inlet temperature adjustable between –40 °C and 20 °C, and a temperature control accuracy of <0.5 °C. Key components includes:
  - Two-stage cascaded cooling (Freon–$CO_2$ or Methanol–$CO_2$)
  - Accumulator (hydraulic type selected)
  - Pump (gear pump selected)
  - Pressure regulating valve



- We have recently established a dedicated mechanical team develop a high-quality, lightweight carbon-fiber mechanical structures integrated with cooling. This effort aims to establish a complete in-house carbon fiber production chain at IHEP, covering the entire process from design to manufacturing. It will support the R&D activities and the delivery of realistic detector mock-ups.



See details in Yujie Li’s talk

# Our Research Team

- Currently active: 29 institutes, 50 staff, and 50+ postdocs & students

Shanghai Institute of Microsystem and Information Technology, CAS
(New semiconductor collaborator, together with foundry SITRI)

Technical Institute of Physics and Chemistry, CAS
(New $CO_2$ cooling collaborator)

中国科学院微电子研究所
INSTITUTE OF MICROELECTRONICS OF THE CHINESE ACADEMY OF SCIENCES

SIMIT

IPC

张江实验室
ZHANGJIANG LABORATORY

山东高等技术研究院
SHANDONG INSTITUTE OF ADVANCED TECHNOLOGY

上海交通大學
SHANGHAI JIAO TONG UNIVERSITY

INFN

KIT
Karlsruher Institut für Technologie

Lancaster University

Jožef Stefan Institute
Ljubljana, Slovenia

UCG
Univerzitet Crne Gore

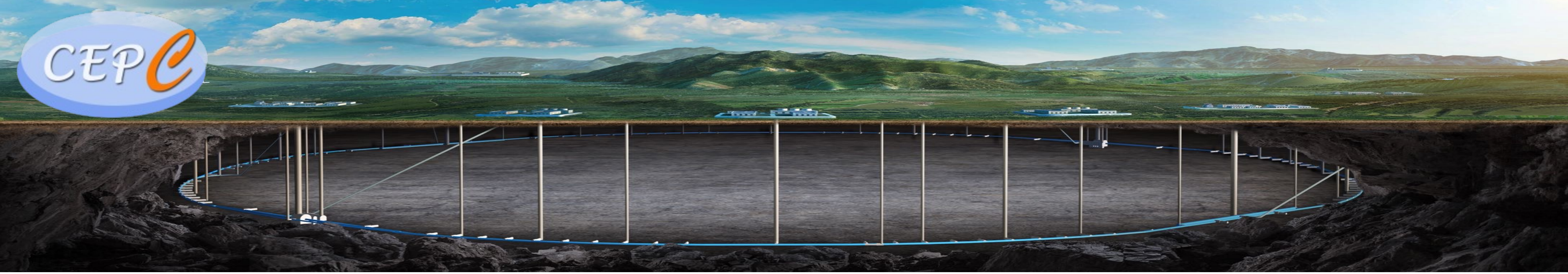
We welcome collaboration with partners worldwide.

# Summary

- The complete design of the CEPC Silicon Tracker and the latest R&D progress have been presented.

- Our next major focus will be on R&D, aiming key technology achievements and prototype detector development. Ongoing efforts in sensor technology, readout electronics, mechanical prototypes, and cooling systems are steadily advancing toward this goal.

- These advancements are crucial to meet the stringent performance requirements of the CEPC Silicon Tracker and ensuring the overall success of the CEPC project.



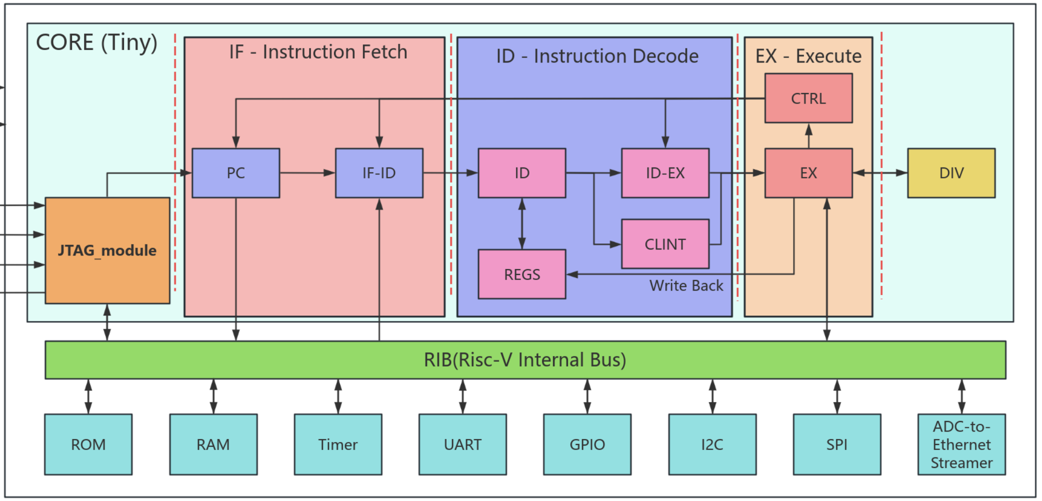
# Thank you for your attention!

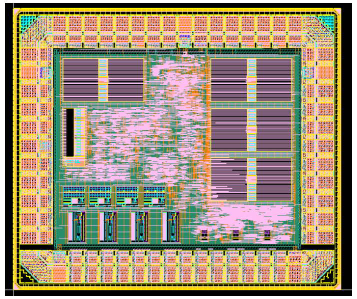
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# Development of a System on Chip (SoC)

- ASIC development is costly, offers limited configurability, and difficult to implement on-chip algorithm integration. System-on-Chip (SoC) architectures—including CPU, memory, bus, and peripherals—represent the future trend of ASIC development. RISC-V–based ASICs offer unique advantages in flexibility and rapid iteration, enabling better support for the diverse requirements of HEP experiments, as well as configurable control and complex on-chip algorithms. The first RISC-V chip developed was submitted for tape-out in October, with testing planned next. The next R&D phase will focus on radiation-hardening, full integration with the LATRIC ASIC, and further applications in system-level control, front-end on-chip computing, and AI integration for HEP experiments.

- Core (Tiny RiscV)
  - RV32IM Core
  - 3 stage pipeline
  - CoreMark/MHz = 2.4
- JTAG Interface
  - OpenOCD support
  - GDB debugging support
- Peripherals
  - 4 KB ROM, 32 KB RAM
  - Supports multiple serial communication protocols, such as I2C, UART, and SPI
  - Integrated sensor data processing and UDP forwarding


CLK
RST
TCK
TMS
TDI
TDO
CORE (Tiny)
IF - Instruction Fetch
ID - Instruction Decode
EX - Execute
JTAG_module
PC
IF-ID
ID
ID-EX
CLINT
REGS
Write Back
CTRL
EX
DIV
RIB(Risc-V Internal Bus)
ROM
RAM
Timer
UART
GPIO
I2C
SPI
ADC-to-Ethernet Streamer



- 55 nm process technology
- Frequency 50 MHz
- Size 1020 x 1196 um
- Supply Voltage 1.2 V
- Characterization will be performed in Q1 2026

See details in Cui Yuxin’s talk