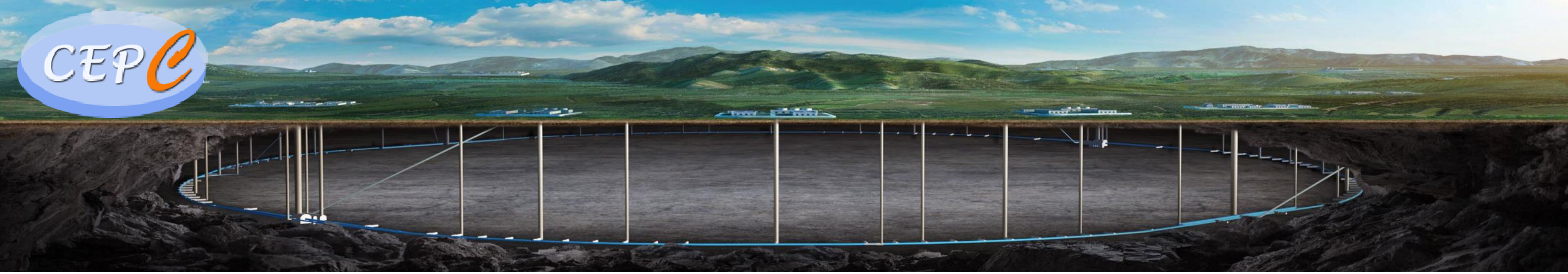

Status of CMOS pixel sensor chips for the CEPC VTX

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Content

- CEPC Vertex detector requirements
- Working plan for the TDR
- Design status of the first stitched chip
- Discussion on spatial resolution

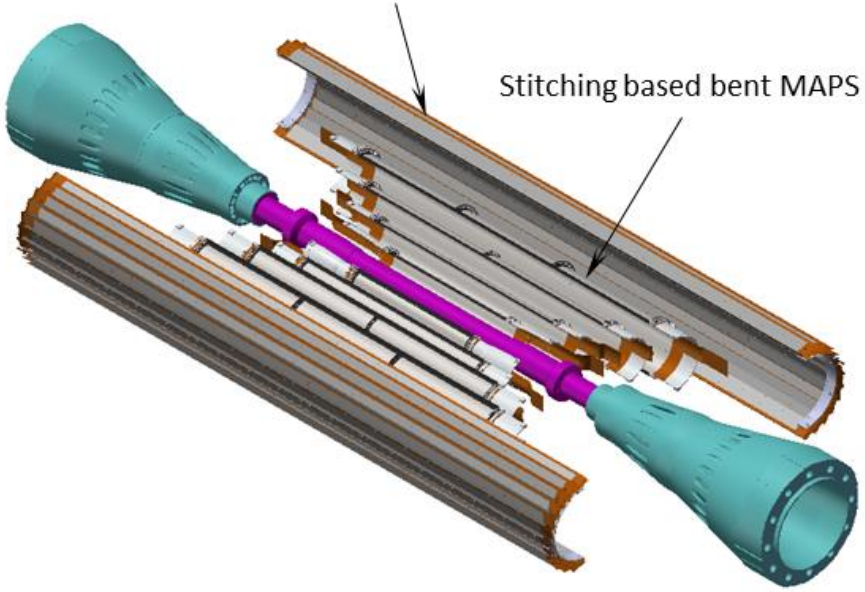
Vertex Requirement

- Inner most layer need to be positioned as close to beam pipe as possible
  - Challenges: Radius (11.1 mm) is smaller compared with ALICE ITS3 (18 mm)

    Requiring wafer-scale stitched Monolithic Active Pixel Sensors (MAPSs)

Table 4.2: Vertex Detector Design Parameters

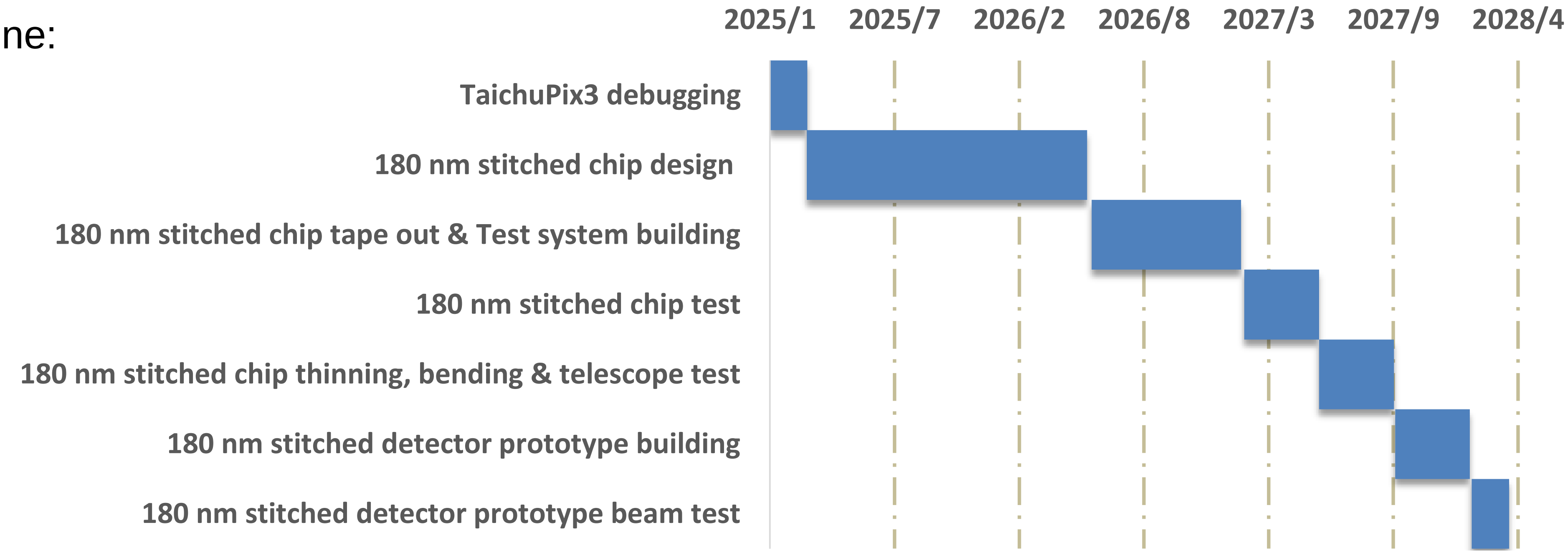
Parameter	Design
Spatial Resolution	$\sim 5\ \mu m$
Detector material budget	$\sim 0.8\%\ X_0$
First layer radius	11.1 mm
Power Consumption	$< 40\ mW/cm^2$ (air cooling requirement)
Time stamp precision	100 ns
Fluence	$\sim 2 \times 10^{14}\ Neq/cm^2$ (for first 10 years)
Operation Temperature	$\sim 5\ °C$ to $30\ °C$
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert \cos\theta \rvert < 0.99$



Ref: CEPC Detector Ref-TDR

Working plan for the TDR

- Development of wafer-scale stitched MAPSs
  - Develop a wafer-scale stitched sensor prototype with 180 nm process to keep R&D risks and costs within reasonable bounds.
  - Timeline:

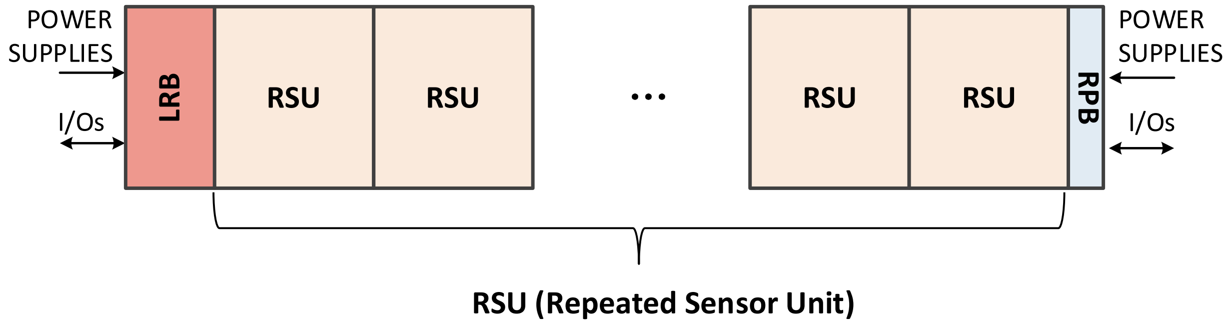


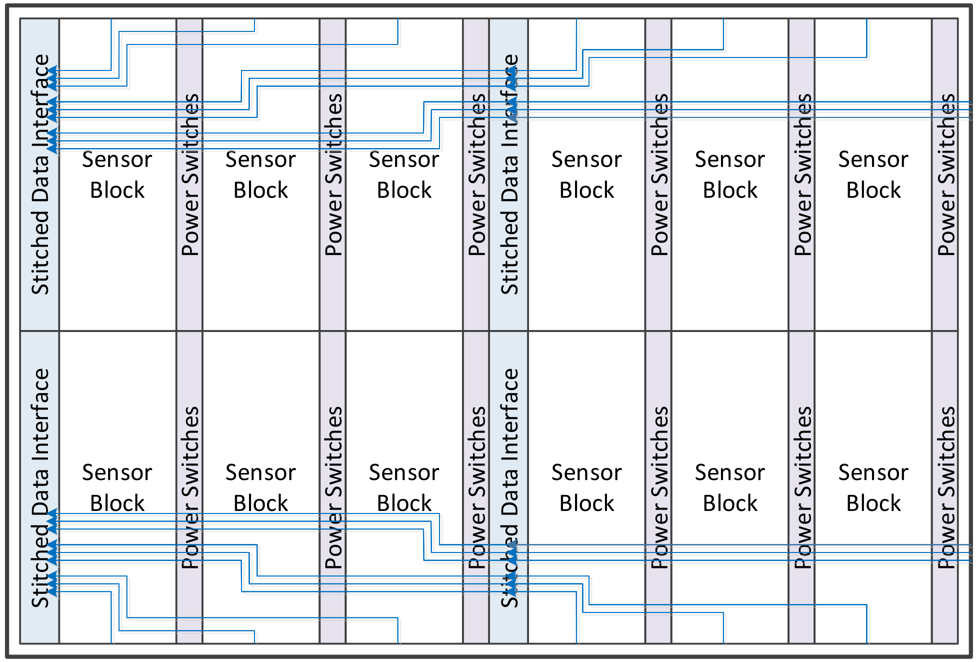
  - The second-generation stitching chip will transition to 65 nm/55 nm process
    - Baseline: TPSCo's 65 nm technology
    - Alternative: HLMC's 55 nm technology
    - Timeline: Depending on available time of the technology

Design of the first 180 nm stitched chip

- Main goal: feasibility validation of the stitching technology.
- Chip architecture:
  - 1D stitching along the beam direction.
  - Each chip consists of multiple RSUs (Repeated Sensor Unit), 1 LRB (Left-end Readout Block) and 1 RPB (Right-end Power Block).
  - An RSU is composed of multiple independent sensor blocks, each transmits low-speed serialized data to the left edge of chip.
    - Most of RSU circuits derived from TaichuPix-3.
  - LRB acts as data collector and high-speed data interface with external, needing new design.
  - REB contains only pads for power supply.

Floorplan of a stitched chip

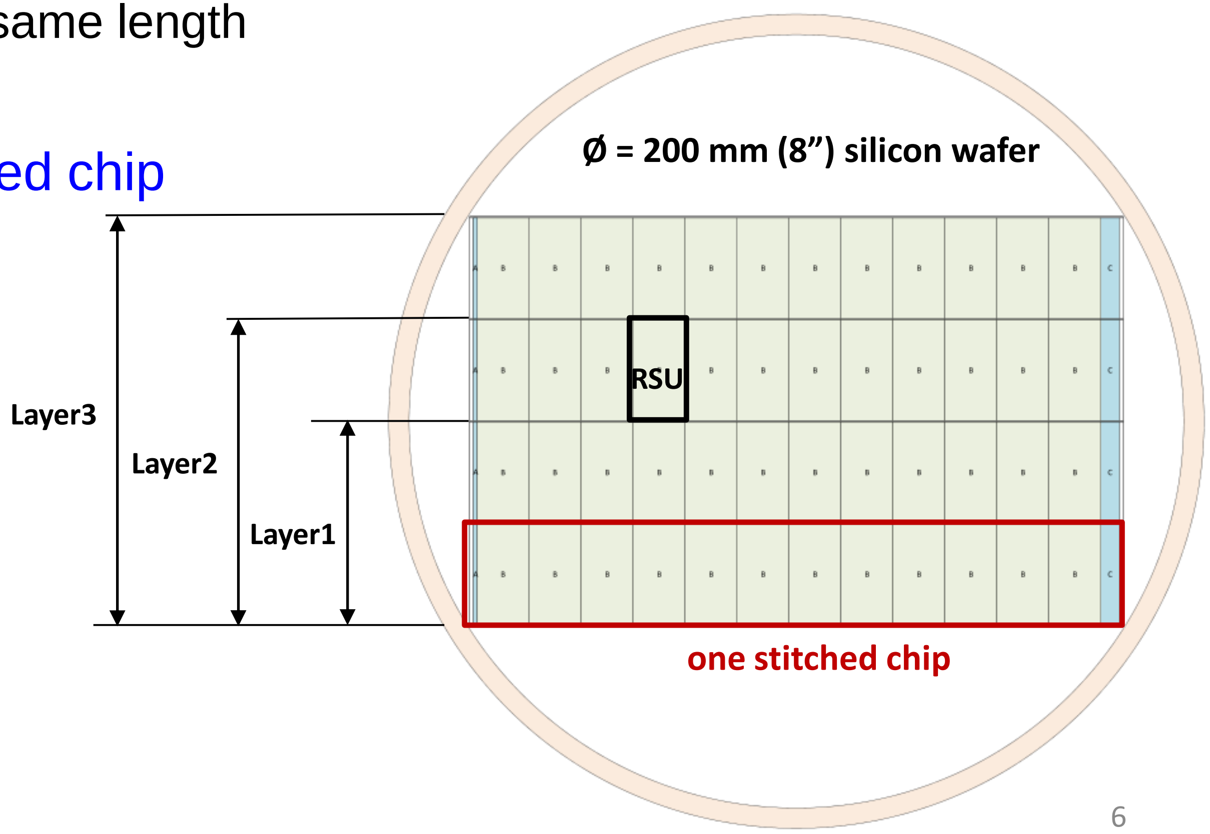




Design of the first 180 nm stitched chip

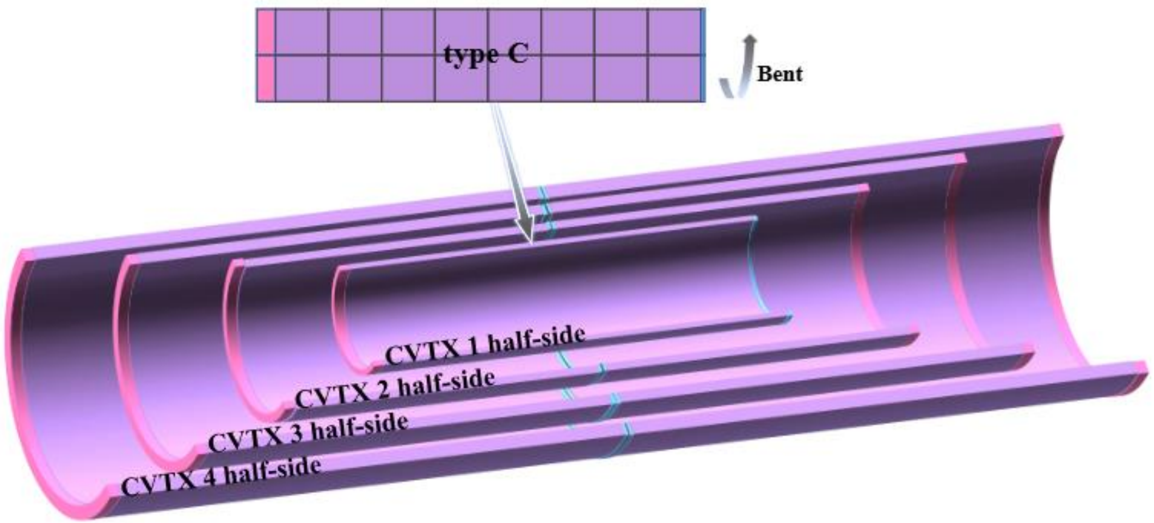
- Design status
  - Preliminary design of stitching floorplan done
    - Four stitched chips per wafer
    - Forming three semi-cylinder layers with the same length
  - Preliminary architecture design of the stitched chip finished
    - Chip size
    - Specific RSU floorplan
    - Data transmission scheme
  - Detailed circuit design ongoing

Stitching plan for a 200 mm wafer

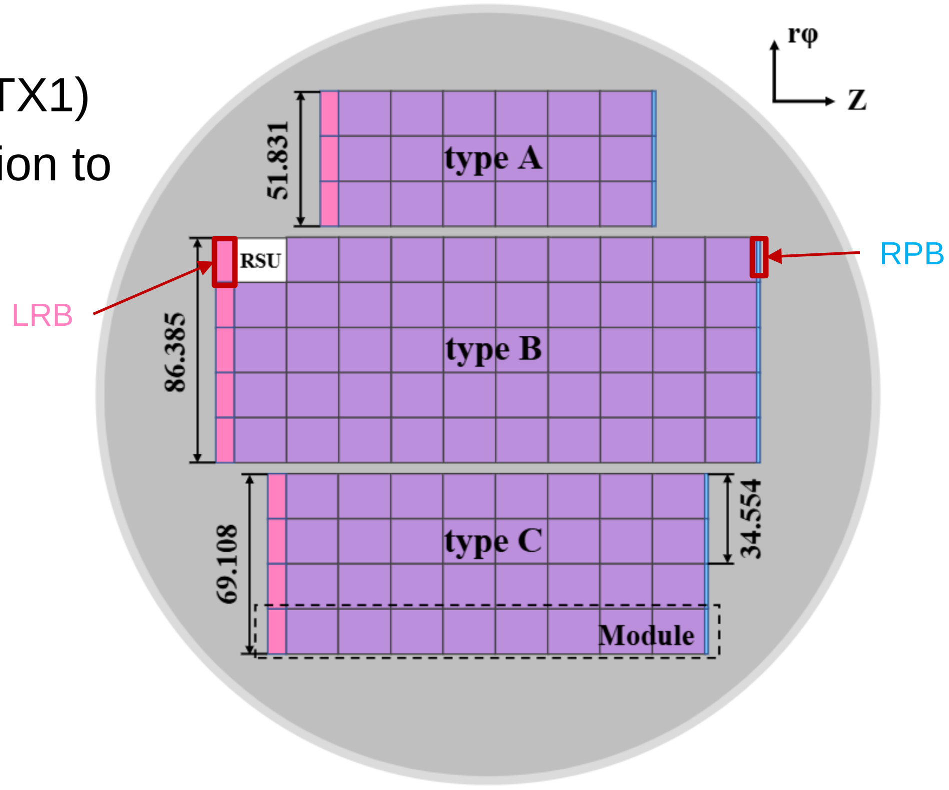


Design of the final stitching plan

- Vertex detector design for TDR
  - Inner four layers are constructed by curved stitched sensors
  - Three types stitched sensors with different sizes on a wafer
    - Sharing same components (RUS, LRB, RPB)
    - One Type C sensor forms a semi-cylindrical for layer1 (CVTX1)
    - Two Type A/Type C/Type B sensors oriented along z-direction to form halves for Laye2/Layer3/Layer4



Layout for the inner four half layers



Stitching plan for a 300 mm wafer

Design team

- Overall architecture
  - Backbone data & power: Wei Wei, Ying Zhang, Siqi Deng

Most faculties from TaichuPix & JadePix design teams

- RSU
  - IHEP: Wei Wei(overall + digital), Ying Zhang (pixel), Siqi Deng(pixel), Mujin Li(digital)
  - CCNU: Ping Yang (biasing)
- LRB
  - Data interface: Xiaomin Wei + std(3) (NPU)
  - Slow Control + Monitoring: Liang Zhang (SDU)
  - Digital: Yunpeng Lu + std(1) (IHEP)
- Verification & test

Floorplan of a stitched chip

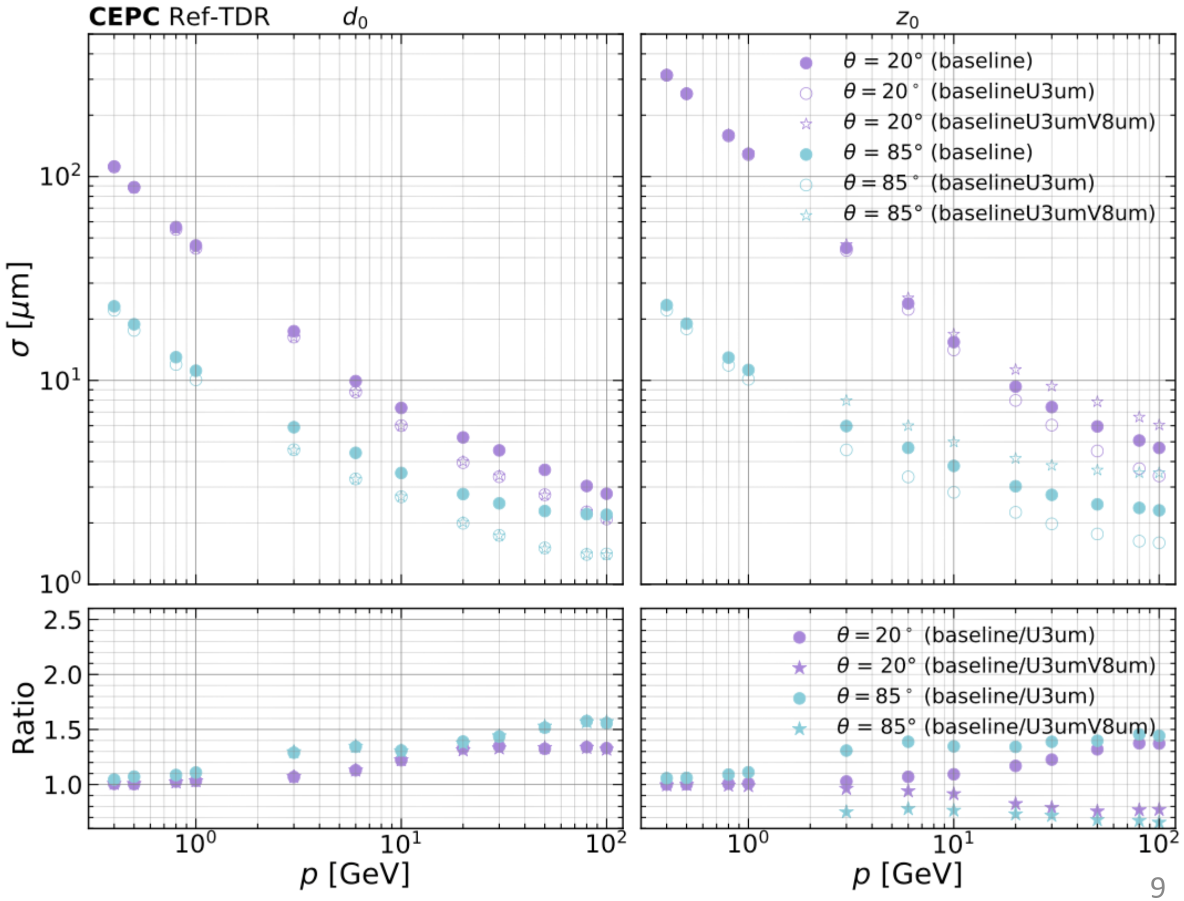
Study on spatial resolution

- Impact parameter resolution simulations with different spatial resolutions: U3V8/U3V3 vs. U5V5 (Baseline)

From Tianyuan Zhang

  – Motivation: choosing pixel size according to requirements of spatial resolution
    - U represent $r\varphi$ direction, V represent z direction

- The differences are more noticeable at high momentum.
- For U3V8, $\boldsymbol{\sigma_{d_0}}$ improved up to 55%, $\boldsymbol{\sigma_{z_0}}$ decreased up to 35%.
- For U3V3, $\boldsymbol{\sigma_{d_0}}$ improved up to 55%, $\boldsymbol{\sigma_{z_0}}$ increased up to 52%.

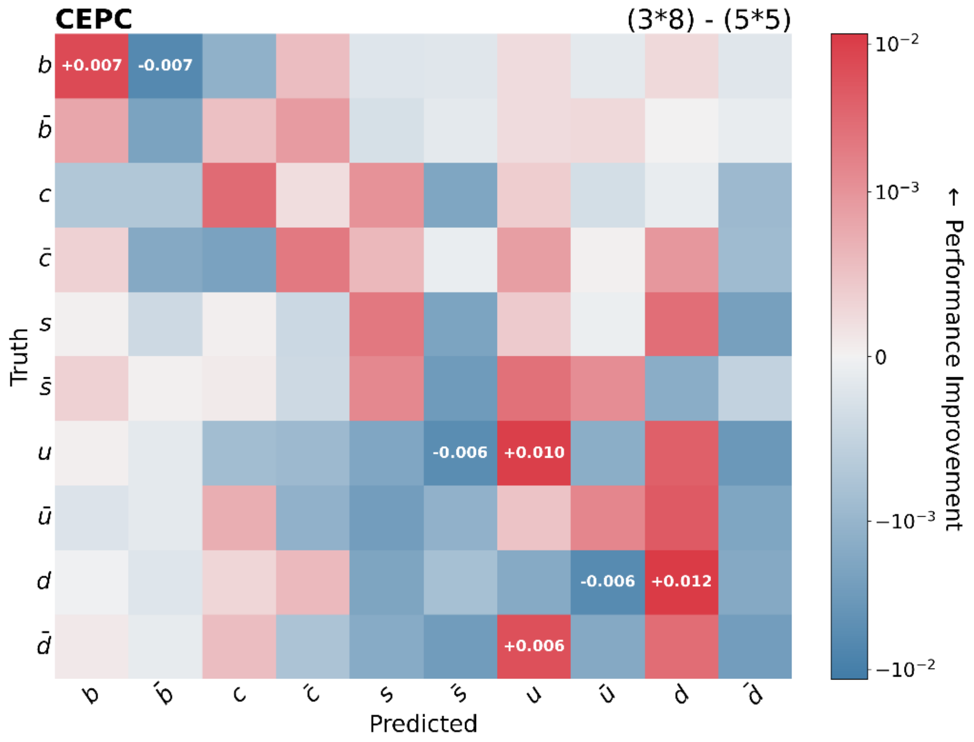


Study on spatial resolution

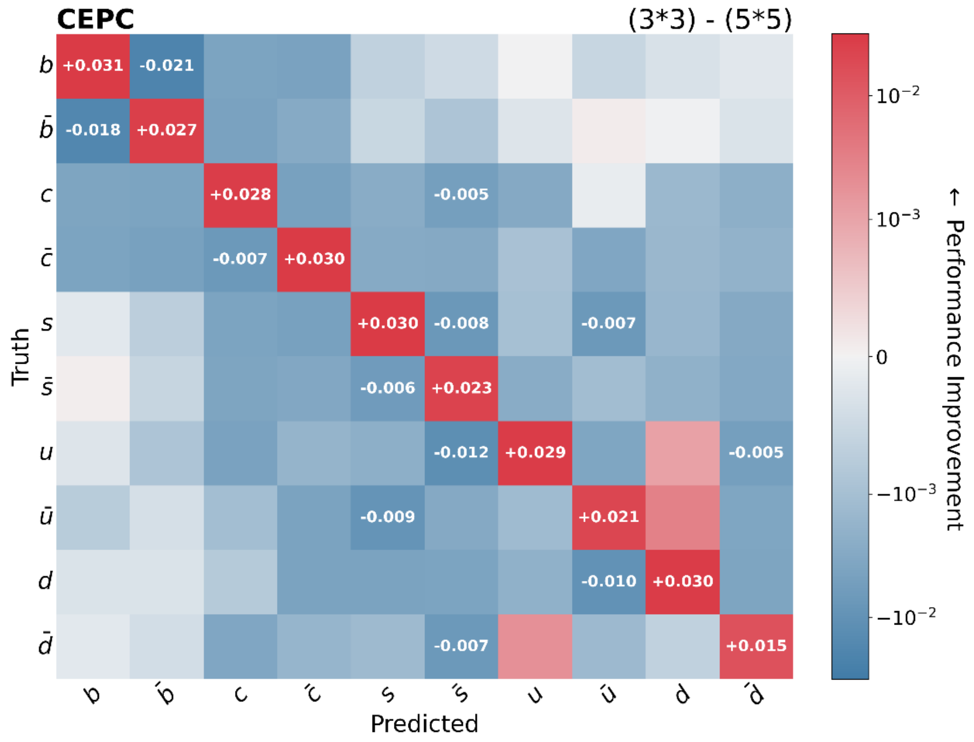
- Flavor tagging with different spatial resolutions: U3V8/U3V3 vs. U5V5 (Baseline)

From Kaili Zhang

(U3V8) - (U5V5)



(U3V3) - (U5V5)



- Performance of U3V8 is comparable with U5V5 (baseline).
- Performance of U3V3 improved about 3% comparing to U5V5.

Study on spatial resolution

- Performance comparison of different choices

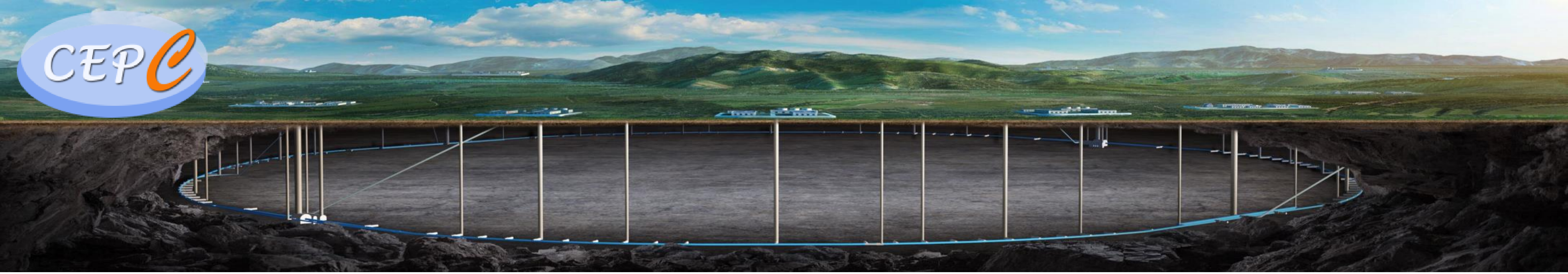
	Spatial resolution	Pixel size (theoretical)	Impact parameter resolution	Metric (Ave. M_{11})	RSU Power density*
Baseline	U5V5	25 μm x 25 μm	< 3 μm @ d_0 < 5 μm @ z_0	0.5865	40 mW/cm^2
	U3V8	16 μm x 40 μm	Increased max. 55% @ d_0 Decreased max. 35% @ z_0	0.5895	40 mW/cm^2
	U3V3	16 μm x 16 μm	Increased max. 55% @ d_0 Increased max. 52% @ z_0	0.6127	56 mW/cm^2

*Calculated with same sensitive area
Only pixel power differences considered

- Open discussion
  - Is a spatial resolution of 3 μm necessary for $r\varphi/z$ directions?

Summary

- CEPC vertex detector requires wafer-scale monolithic pixel sensors for the inner four layers.
  - First stitched chip based on 180 nm process under designing
    - Feasibility validation of the stitching technology
    - Architecture and functionality validation of the main circuits
    - Pixel pitch is 25 μm
  - Next generation stitched chip expected to transition to 65/55 nm
    - Process availability needs to be further confirmed
    - Final pixel size needs to be decided



Extra slides

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Submission cost

- TJ 180 nm process: 0.3-1 M RMB for MPW; 4.0 M RMB for NRE.
- TPSCo 65 nm process: 7.0 M RMB for NRE ; No MPW.