Feedback of 2025 2nd IDRC Review Report

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Outline

Machine Detector Interface

Recommendations

- The committee recommends continuing the study of discrepancies observed between data and simulation from BESIII. Understanding these differences is important for validating the assumptions underlying the CEPC machine–detector interface design.
- Answer: Sure. The study of the BIB at BESIII are important and are sure to be continued. For the future work, we will have improvements both on the simulation and the experiments.
  - In simulation, we plan to improve the generator, the tracking, and the detector simulation.
    - For generator, we will introduce whole ring generation of the single beam backgrounds, introducing the real profile of the vacuum distribution alongside the ring, etc…
    - For tracking, since we already have some results using APES-T with real-turn of the beam-beam effects considered, which is important to implement the beam-beam blow-up at the IP, we plan to move all our studies to APES-T/APES, and perform the cross-check with current and future SAD results.
    - For detector simulation, we are learning from the BESIII experts, to make our simulation right with the BOSS framework, especially for the MDC.
  - In experiments, we will continue the analysis of the data collect during the 2024 experiments, and also waiting for the machine time to collect more data.

Recommendations

- Closer collaboration with the accelerator team should be established to explore the full range of possible beam steering scenarios. This coordination is especially important for refining the design and placement of synchrotron radiation (SR) masks and collimators, ensuring that they remain effective across realistic operational conditions.
- Answer: Sure. We know that our current results are only based on the ideal beam in the uni-form solenoid field assumption, therefore we plan to simulate the beam-orbit change in next stage, as well as the real working scenarios. We still use three steps, which includes generation, accelerator tracking and detector simulation. The initial plans are briefly listed below:
  - Beam-orbit scenario: We are working with acc. colleagues to get a list of the possible scenarios of the beam-orbit changing which will affect the BIB. We are also planning to move the lattice to the one with correction. Then we can perform the dedicated study case by case. These might affect all three steps.
  - The improvements planned in the generation step(in one dedicated beam conditions):
    - Pair Production: We plan to continue study the uncertainties of the generator(including the study using BDK), and the effects of the magnetic field in the generator and the threshold. We also plan to integrate the GP++ into APES-T to study the beam-beam effects turn-by-turn.
    - SR: We plan to study in parallel if possible. We are implementing the anti-solenoid to the CEPCSW generator and separate the SR generated in different locations(last bending, QF1, QDb, Qda, -5 T anti-solenoid, etc). We plan to adjust the masks accordingly, change the design of the last collimator at -19.07 m to make it also a SR collimator, then we can relax the masks, and introduce weight in SR simulation to improve statistics. We are also evaluating BDSIM again to use it as generator.

Recommendations

- Closer collaboration with the accelerator team should be established to explore the full range of possible beam steering scenarios. This coordination is especially important for refining the design and placement of synchrotron radiation (SR) masks and collimators, ensuring that they remain effective across realistic operational conditions.
- Answer(continued):
  - The improvements planned in the generation step:
    - Photon backgrounds: Continue study on the photons generated with the BS and RBB.
    - Single beam: We are done with the lattice with solenoid and anti-solenoid for Higgs and Low-Lumi-Z. We are introducing the generator built-in in the tracking tool, the real profiles similar to BESIII cases, also the variation of the min and max values of the acceptance to consider the change in DA introduced by the collimator.
  - The improvements planned in the accelerator tracking step: We are improving the model of collimators in SAD, and introducing SAD-FLUKA coupling simulation. We also plan to introduce APES-T/APES in simulation for turn-by-turn study of the beam-beam.
  - The improvements planned in detector simulation step: We are improving the model in FLUKA, and optimize the shielding in detail, like partial shielding for the hotspots.
  - Other issues: We will continue the design and study of the photon dumps together with the accelerator colleagues. We agreed to modify the first bending magnet downstream to accommodate it.

Recommendations

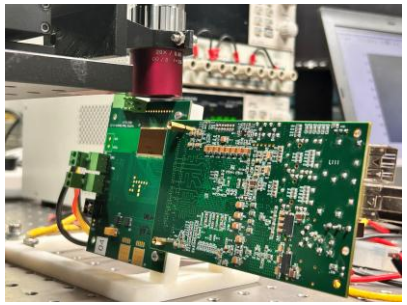
- The detailed mechanical design of the region surrounding the IP beam pipe should proceed as a priority, as its geometry and integration will directly impact the layout and feasibility of several adjacent components, including the luminosity monitors, final-focus magnets, and vertex detector. Early completion of this design will help prevent costly downstream revisions.
- Answer:
  - The design of the this region, including the LumiCal, and the cables for readout of the LumiCal are presented in the TDR. The improvements of the cooling and cables design of the LumiCal is on-going based on the experiments results and test beams in next stage.
  - Taken into account the recent changes in this region, though we already have a lot discussions on this issue, but we still need to work together with the colleagues from the sub-detectors, mechanical and accelerator group to improve further.

- The current description of the diamond-based Fast Lumi detector in the reference TDR lacks sufficient technical detail. The documentation should be expanded to include the detector architecture, segmentation, readout scheme, and performance expectations, supported by relevant prototype or test-beam results where available.
- Answer:
  - I contacted Suen Hou and Lei Zhang. It would be done as soon as possible. We have a design including some of the topics mentioned above, while some of them are addressed in current version.
  - We plan to re-organize the existing materials, and add more detail descriptions, to make the technical details of the diamond-based Fast Lumi detector comparable with the LumiCal.

Vertex Detector

Recommendations

- The committee commends the inclusion of a laser alignment system, which will enable continuous monitoring of mechanical deformations of the vertex detector. It is recommended to construct an early demonstrator that incorporates this feature and reflects the realistic properties of the sensors.
  - A preliminary laser system is made, and a more realistic system is in preparation.
  - This is included in future plan in Ref-TDR

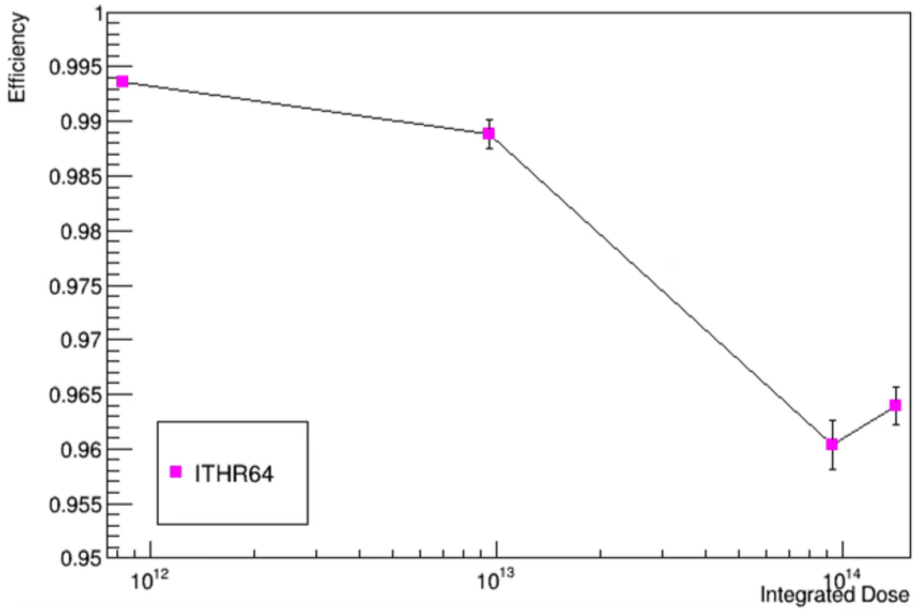


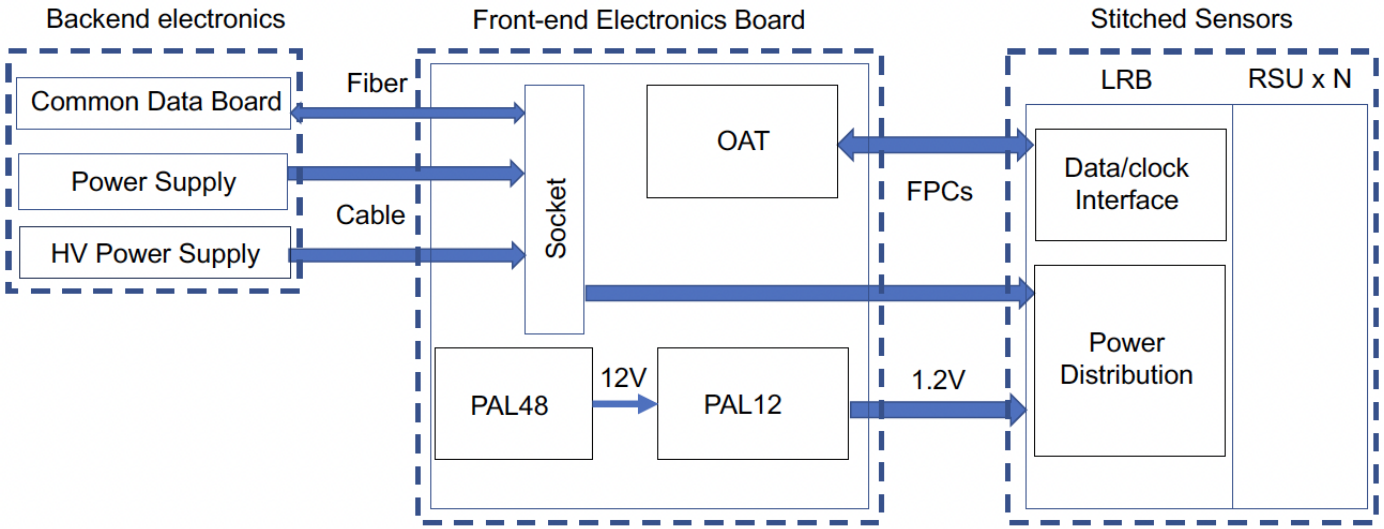
- The calculations for cooling performance (required flow rate and pressure drop) should be revisited, taking into account the non-uniform nature of heat dissipation. Building a detailed and realistic thermal mock-up will be essential.
  - A realistic thermal mock-up is top priority in our to-do-list.
  - Will validate the thermal calculation with thermal mock-up test result
- The design of power and data lines across the Readout Support Units (RSUs) must ensure sufficient shielding to minimize electromagnetic pickup.

  •Answer: We will perform simulations on the stitching design when we are about to tape out the next version of the sensor by the end of 2025. Most of these potential challenges can be simulated using the design kits once the stitching design is finalized.

Recommendations

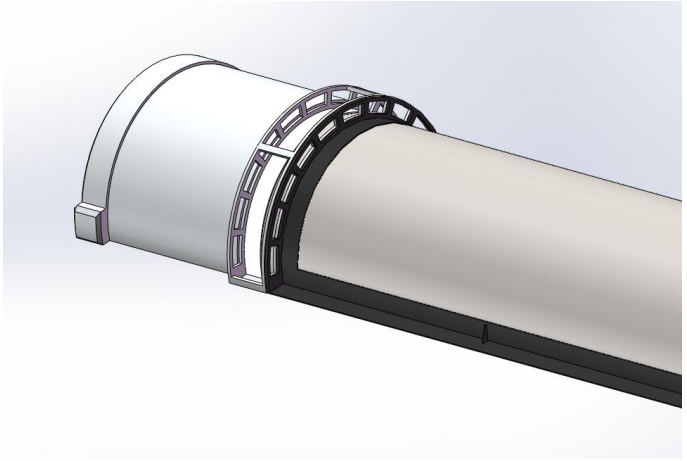
- Finally, the expected radiation fluence of approximately 2×10^{14} n_eq/cm^2 is significant for unbiased substrates relying on diffusion charge collection and could strongly impact operation. Since the ITS-3 project faces nearly an order of magnitude lower requirement, dedicated irradiation studies should be undertaken without delay. If substrate biasing proves necessary, the power-service design—particularly at the front-end boards—will need to be adapted accordingly.
  - Proton Irradiation tests up to 2×10^{14} n_eq/cm^2 has been performed. Efficiency is larger than 95% after irradiation
  - High voltage supply is added in electronics design



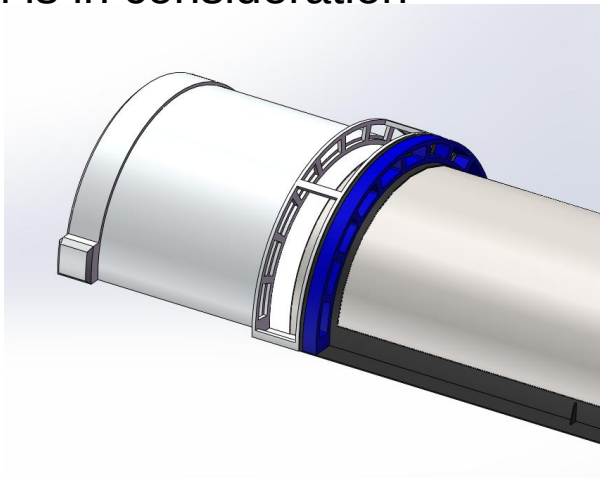


Recommendations

- Reevaluate the VTX air-cooling design. Recent studies (Section 4.3.2) indicate that the airflow had to be increased from 3.5 m/s to 5 m/s to maintain performance, yet the temperature of Layer 1 remains close to 30 ° C.
  - To further increase cooling power, adding thermal conductive foam is in consideration



adding thermal conductive foam



- Validate the thermal simulations presented in Figure 4.18 through the construction and testing of a VTX mock-up with dummy wafers and heaters. This will provide an essential experimental cross-check of the simulated results.
  - A realistic thermal mock-up is top priority in our to-do-list.
  - Will validate the thermal calculation with thermal mock-up test result

Inner Tracker (ITK)

Recommendations

- Complete characterisation of the COFFEE ASICs remains a high priority. While functional validation of COFFEE3 has confirmed the operation of key building blocks, a systematic programme of laboratory tests, radioactive-source studies, and beam campaigns is still required to demonstrate full detector performance. This is essential for validating the ITK baseline technology and guiding the design of subsequent ASIC generations.

We are working on that. A comprehensive characterisation is ongoing to validate the full performance of the COFFEE3 ASICs.

- A comprehensive COFFEE ASIC development roadmap should be defined, including a detailed and realistic schedule covering testing, redesign, and fabrication steps, to ensure timely achievement of key milestones and transparent progress tracking.

Following COFFEE3 verification in late 2025, the focus will shift to process modification. In collaboration with the foundry, a new MPW submission using the "quadruple-well process" is planned for early 2026, followed by testing around mid-2026 to evaluate the modified process. In parallel, a quarter-size chip will be designed and submitted for tape-out after process verification. Testing of this chip, from late 2026 to mid-2027, will serve as an intermediate validation step before full-scale development.

From late 2026 through 2027, the project will advance to the full-size chip design, integrating all validated circuit and process improvements. The designed chip is scheduled for submission by the end of 2027. Final full-size chip testing is planned for 2028 to confirm complete functionality, performance, and production readiness. By the end of 2028, a fully validated, high-performance, and scalable HV-CMOS sensor is expected to be delivered for mass production.

Recommendations

- The evolution of the COFFEE ASIC family must address the limitations of the current N-MOS–only readout. A timely decision on adopting a quadruple-well technology to allow both N-MOS and P-MOS devices is crucial, given the short submission timeline.

The NMOS-only readout architecture within the pixel cannot support complex digital circuit designs, which limits its ability to handle high hit-density scenarios. During the R&D of the COFFEE series, we have made substantial progress and plan to complete our first tape-out using the 55 nm quadruple-well process within a few months. This tape-out will provide critical information for evaluating both NMOS and PMOS devices and offer valuable guidance for future R&D directions.

- Elongated diode structures, omitted from COFFEE2 due to process constraints, remain an important design goal for achieving the required position resolution. The feasibility of implementing these structures in future submissions should be clarified.

Regarding the position resolution requirement, the 40 μm pixel size in COFFEE3 refers to the layout dimension. Due to the 55 nm fabrication process, the actual pixel size will be reduced by a factor of ~0.9, yielding an effective production size of ~36 μm. Without accounting for charge sharing, this corresponds to a worst-case intrinsic position resolution of ~10 μm ($36/\sqrt{12}$). Future COFFEE3-based designs will further optimize pixel geometry to enhance spatial resolution, although the margin allowed by the process remains limited.

Recommendations

- The transition toward per-pixel TDC architectures for time stamping is innovative but significantly impacts the data-readout design. Maintaining continuity of personnel and expertise across ASIC generations will be critical to ensure design consistency and effective knowledge transfer.

The team has a stable core of staff, supported by PhD and master's students at various stages of training. We will continue to strengthen the team to ensure effective knowledge transfer and the consistent accumulation of experience throughout the ASIC R&D process.

Recommendations

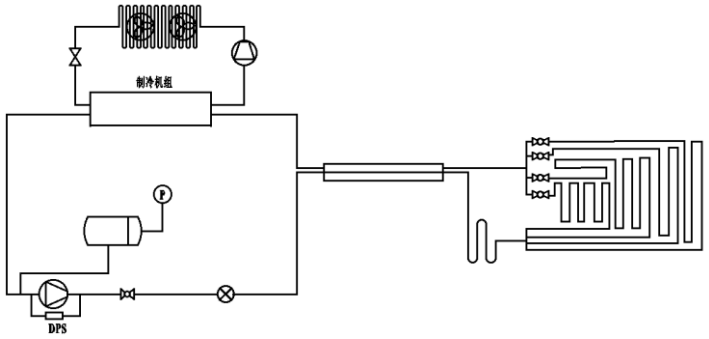
- A dedicated thermomechanical mock-up of the stave and endcap structures should be developed and tested to experimentally verify the cooling system's performance and mechanical stability under realistic operating conditions. This is essential both for validating thermal simulations and for quantitatively comparing water and CO_2 cooling strategies.

We have collaborated with the Technical Institute of Physics and Chemistry (TIPC), CAS, on the development of the CO_2 cooling system. This effort involves four senior TIPC staff with extensive experience in CO_2 cooling system development. Regular collaborative meetings have been established, with the most recent held on September 28.

Several rounds of detailed discussions have been conducted on key aspects, including the accumulator (hydraulic type selected), pump (gear pump selected), two-stage cascaded cooling (Freon–CO_2 or Methanol–CO_2), the pressure regulating valve, overall cooling system dimensions, etc. The first CO_2 cooling system prototype is designed to be compact and portable, handle a nominal heat dissipation power of 2 kW (up to 4 kW), with a CO_2 inlet temperature adjustable between –40 °C and 20 °C, and maintain a temperature control accuracy of <0.5 °C.

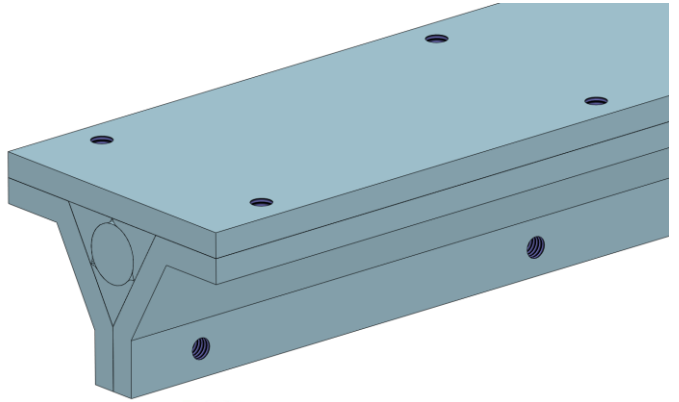
In parallel, a bundle of small-diameter titanium tubes (outer diameter: 1.6 mm, length: 1500 mm) have been procured. These will be integrated with heaters to create a detector mock-up for thermal load testing. We aim to complete the first CO_2 cooling system prototype in 2026.

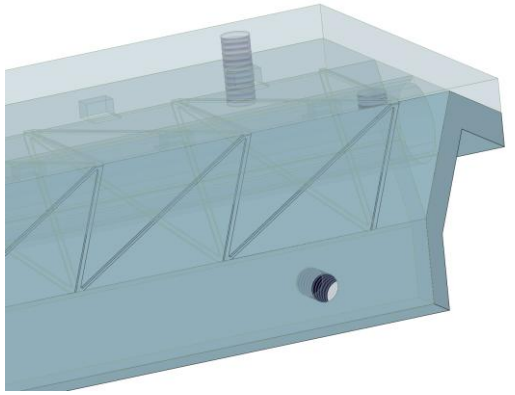
CO2 laboratory of the TIPC in Langfang

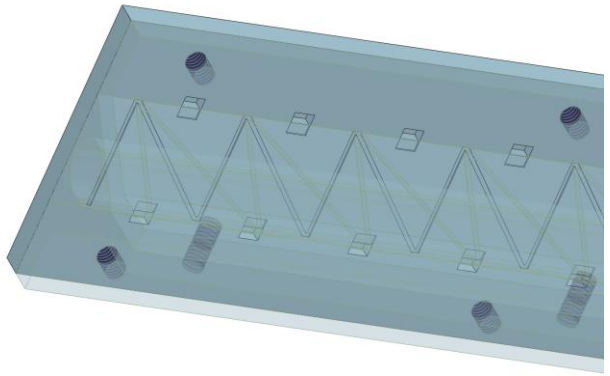


We have recently established a dedicated mechanical team develop a high-quality, lightweight carbon-fiber mechanical structures integrated with cooling. This effort aims to establish a complete in-house carbon fiber production chain at IHEP, covering the entire process from design to manufacturing. Most of the design work, raw material procurement, and tooling have been prepared, which will accelerate the R&D process and the delivery of realistic detector mock-ups.

项目	型号/详细信息	物资类型	单价(元)	备注
M40J碳纤维预浸料单向带	厚0.05mm 宽 6/8mm (得定制)	耗材	0.8元/米	威海光威复合材料股份有限公司， **5000米起订** M40J
M40J碳纤维预浸料单向布	厚0.05mm 宽1m		88元/㎡	
M40J碳纤维预浸料单向丝束 中简科技 ZJ-M50J, 中复神鹰 QZ50系列	厚0.4mm， 宽1mm	耗材		可通过变截面工装将宽幅碳纤维预浸料带（如8mm×0.05mm）变形加工为更细窄 https://www.zfsycf.com.cn/#/productIntroduce/top
		耗材		
四氟乙烯PTFE脱模布	CPTFEG特氟龙透气布T6007， 可耐260C, 0.07m	耗材	1143	CPTFEG特氟龙透气布T6007单光面 泰州市晨光塑业
透气毡（Bleeder Cloth）	150g/㎡ 1.5mx100m	耗材	699	萨姆森复合材料 复材供应链 JHL聚汇联
真空袋膜（Vacuum Bag Film）	真空袋膜DPT1000 (宽2.03m x 10m）热压罐	耗材	609	萨姆森复合材料 130度 复材供应链 130/200/230度 JHL聚汇联 130/
脱模蜡	牛邦脱模蜡N102, 适用于高温固化（<230°C）	耗材	45	萨姆森复合材料 复材供应链 “脱模蜡”和“脱模剂”功能类似，但蜡更适用于手工操作，脱模剂更适合自动化或大批量。
脱模剂		耗材		萨姆森复合材料 复材供应链 JHL聚汇联
隔离膜（Release Film）	肯天Chemlease41-90EZ （580） 或 肯天Zy	耗材	580	萨姆森复合材料 复材供应链 如 PET薄膜，铺设在预浸料之间或与模具接触面，防止粘连，保持界面清晰。
热压罐（Autoclave）（若需要）	或自制	核心设备		
烘箱（Oven）	甲机械组现有1米的	核心设备		
桁架成型模具		模具		
桁架支腿预制件模具		模具		
变截面工装(若需要)		核心设备		
模具抽芯工装		辅助设备		
线割加工设备		核心设备		







Outer Tracker(OTK)

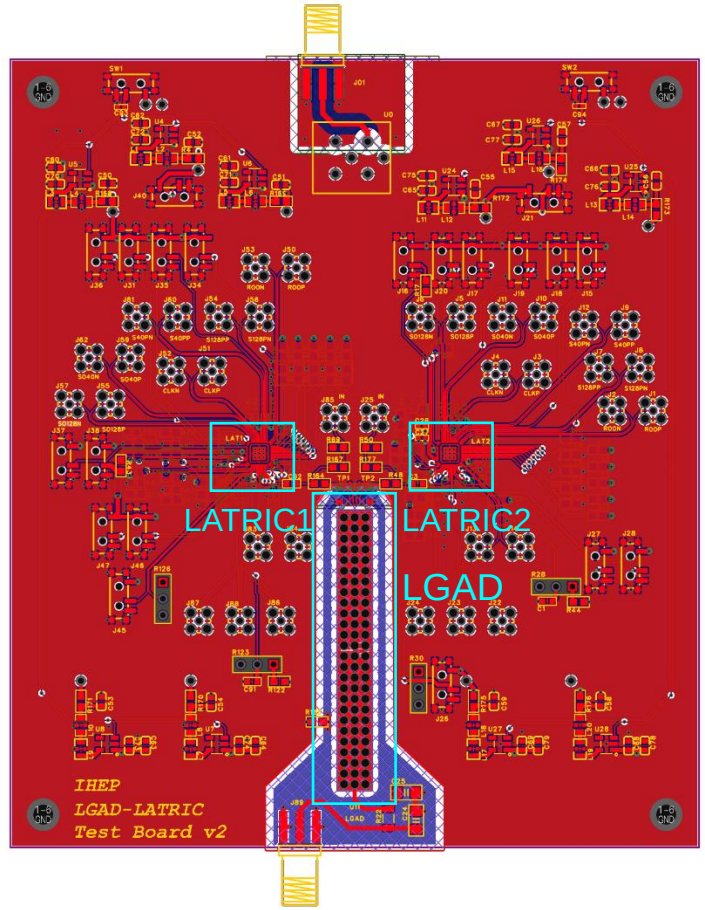
Recommendations

- Complete characterisation of the AC-LGAD sensors wire-bonded to the LATRIC ASIC remains a high priority. Integrated testing under realistic operating conditions will be essential to establish detector performance in terms of timing and spatial resolution, hit efficiency, noise, and power consumption.

We have devoted significant effort to the combined LGAD–LATRIC testing over the past few weeks. A dedicated LGAD–LATRIC test board has been designed, capable of integrating two LATRIC ASICs with an AC-LGAD sensor, with each LATRIC providing independent readout channels.

The test board layout has been optimized to minimize components on the reverse side, allowing two boards to be coupled back-to-back for β-source measurements.

In parallel, the laser and β-source test setups for timing and spatial resolution measurements are nearly complete, and the combined ASIC–sensor tests will be launched as soon as possible.



Recommendations

OTK

- A comprehensive LATRIC ASIC development roadmap should be defined, including a detailed and realistic schedule covering iterative design, testing, and validation steps leading to the final multi-channel version. This plan should also include auxiliary front-end and back-end electronics to ensure system-level readiness.

Following the successful development and testing of the single-channel LATRIC V0, an 8-channel ASIC (LATRIC V1) will be developed in Q4 2025, incorporating a digital logic control section. This integrated ASIC design will then be submitted for wafer fabrication. By the first half of 2026, the test system design for this ASIC will be finalized. In mid-2026, the performance of the 8-channel ASIC will be evaluated, including crosstalk studies, followed by connection, debugging, and radiation-hardness testing in conjunction with the LGAD sensor.

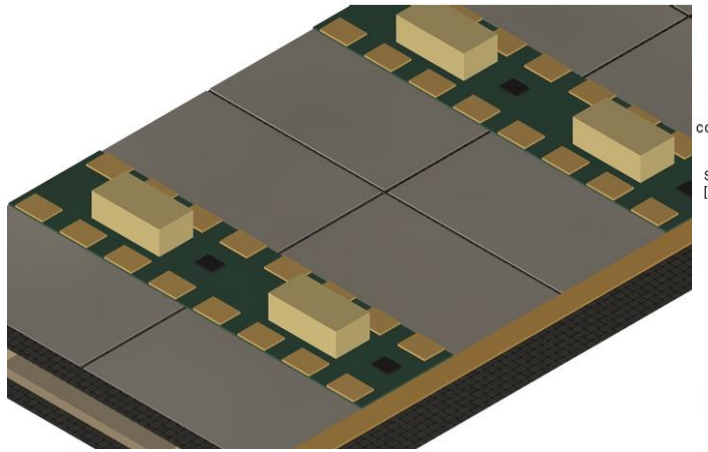
By the end of 2026, the ASIC design will be refined, and the 64-channel ASIC (LATRIC V2) will be submitted for wafer fabrication. Simultaneously, a prototype of the LGAD readout frontend electronic system will be developed. In the mid-2027, performance tests of the 64-channel ASIC will be conducted, along with evaluations of the frontend prototype, ensuring seamless integration with the LGAD sensor.

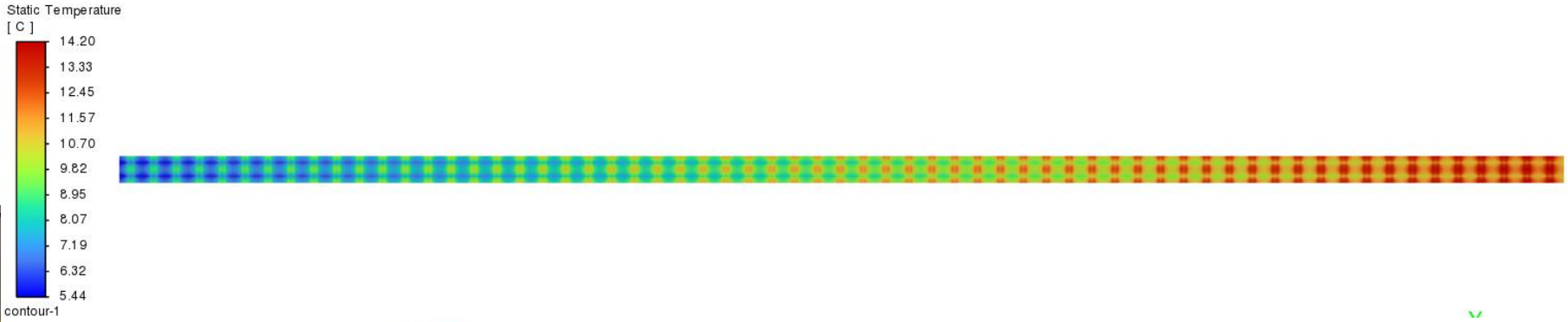
By the end of 2027, the 128-channel LATRIC will be designed, integrated, and finalized for submission, paving the way for mass production.

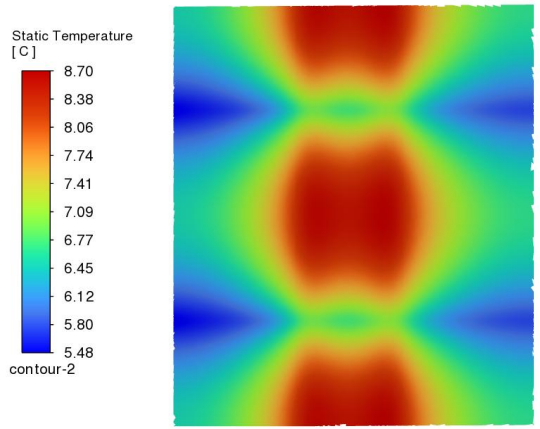
Recommendations

- The highly non-uniform heat dissipation, dominated by the LATRIC ASIC region, should be carefully evaluated for its implications on mechanical design, service routing, and overall detector stability.

Heat dissipation per ASIC:
1.5 W (2.5 W/cm^2)







With water cooling using 5 mm diameter pipe and 5 °C inlet, the latest simulation incorporating all ASIC details shows that the temperature difference within a single sensor is 3–4 °C, meeting the <5 °C requirement, with the maximum ASIC temperature reaching 40 °C.

Recommendations

OTK

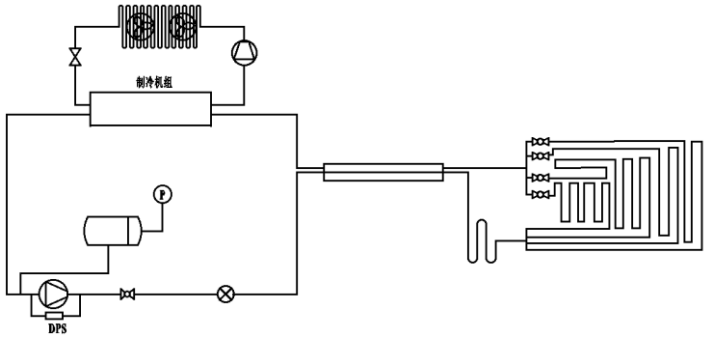
- A dedicated thermomechanical mock-up of the OTK cooling system should be developed and tested to experimentally validate thermal simulations, quantify temperature gradients across large-area assemblies, and provide a solid benchmark for comparing water and CO_2 cooling strategies.

We have collaborated with the Technical Institute of Physics and Chemistry (TIPC), CAS, on the development of the CO_2 cooling system. This effort involves four senior TIPC staff with extensive experience in CO_2 cooling system development. Regular collaborative meetings have been established, with the most recent held on September 28.

Several rounds of detailed discussions have been conducted on key aspects, including the accumulator (hydraulic type selected), pump (gear pump selected), two-stage cascaded cooling (Freon–CO_2 or Methanol–CO_2), the pressure regulating valve, overall cooling system dimensions, etc. The first CO_2 cooling system prototype is designed to be compact and portable, handle a nominal heat dissipation power of 2 kW (up to 4 kW), with a CO_2 inlet temperature adjustable between –40 °C and 20 °C, and maintain a temperature control accuracy of <0.5 °C.

In parallel, a bundle of small-diameter titanium tubes (outer diameter: 1.6 mm, length: 1500 mm) have been procured. These will be integrated with heaters to create a detector mock-up for thermal load testing. We aim to complete the first CO_2 cooling system prototype in 2026.

CO2 laboratory of the TIPC in Langfang



Recommendations

OTK

- The estimated wafer count (~3,250) does not currently include yield effects. Although the collaborating groups have extensive LGAD production experience, potential challenges—distinct from those encountered at the HL-LHC—must be anticipated and incorporated into production planning.

Yield is a major consideration for our next R&D phase and depends heavily on the foundry. In addition to IME, previously used for LGAD production, we have recently established a close collaboration with the Shanghai Institute of Microsystem and Information Technology (SIMIT), CAS, and the Shanghai Industrial μTechnology Research Institute (SITRI). SITRI operates on a much larger scale than IME and is expected to provide improved quality control. They will collaborate with us long-term to support R&D and process improvement. Our first tape-out of LGADs at SIMIT & SITRI is currently in preparation.

- Demonstration of large-area sensor stitching remains essential. Both TI-LGAD and RSD-LGAD variants (AC and DC) should be systematically studied in laboratory and beam environments to confirm uniformity, gain stability, and operational reliability.

The final large-area sensor will not use stitching but will be fabricated using wafer-scale contact lithography. We will perform a systematic and comprehensive study of both TI-LGAD and RSD-LGAD variants to evaluate their performance, including uniformity, gain stability, and operational reliability, in laboratory and beam tests.

Recommendations

OTK

- The team is encouraged to apply lessons learned from the ALTIROC and ETROC developments to maximise design efficiency, streamline ASIC integration, and ensure continuity of expertise across design generations.

We will pay close attention to these aspects and incorporate the lessons from ALTIROC and ETROC into our future ASIC developments.

TPC

Recommendation

- Reassess the choice of 500 × 500 μm² pad size in combination with the T2K gas mixture, as this configuration appears suboptimal for dE/dx-based particle identification.
- Extend the beam-induced background studies, incorporating recent improvements in simulation and mitigation methods to refine background estimates and design margins.
- Conduct more detailed investigations of space-charge distortions, ensuring that correction strategies are validated for all expected running conditions.
- Prototype ion backflow suppression techniques, independently of the selected solution (e.g., double mesh or graphene filter), to verify feasibility and performance.
- Demonstrate experimentally the effectiveness of spark-protection measures for the readout electronics.
- Evaluate CO_2 cooling as a potential alternative to water, taking advantage of its dielectric properties and ability to maintain constant-temperature heat removal without electrical risk.

Answer:

- The first four items have been included in Section 6.6 “summary and future plan”. These studies are either in progress or about to begin.
- Spark-protection measures will be included in the next version of the readout ASIC and will be tested and verified later.
- Descriptions of CO_2 cooling as a potential alternative to water was added in Section 6.2.5. The detailed design will be guided by thermodynamic FEA.

ELECTROMAGNETIC CALORIMETER

HADRONIC CALORIMETER

Recommendations

- Address intra-tile response variations, particularly given the design choice of using a single SiPM per tile, as these variations could significantly affect detector uniformity and calibration stability.
- Establish a robust and efficient QA/QC chain, building on the experience and methodologies developed for the PS-HCAL QA/QC programme.
- Answer to the recommendations:
  - For the three vendors new GS tiles and QA/QC, we added a subsubsection "8.4.2.4 Quality Control" under "8.4.2 Glass Scintillator" to describe the new batches of GS tiles from three venders, describes the GS tiles qualities, fractions of yields with light yields greater than 1000 ph/MeV, etc.. . Also in the subsubsection "8.4.2.1 Light Yield" the results are updated to the new GS tiles, and 150 GS tiles mass produciton test has been mentioned.
  - For the "intre tile variation", we added a some text in the "8.4.2.4 Quality Control" and in the "8.4.6 Calibration" section telling that non uniform responses from different tiles can be aligned to have uniform response through MIP inter-calibration using cosmic rays or muon beams, and also can be aligned using the LED monitoring system.

MUON

Recommendations

- Construct and test a full-length detector sector (barrel or endcap) using final strips, SiPMs, front-end boards, and services, to demonstrate 1 ns timing, threshold performance, and position uniformity under realistic conditions.
- Finalise the SiPM choice between HPK and NDL using a transparent, quantitative scorecard including photon detection efficiency, gain, dark count rate versus temperature, cross-talk, timing, radiation tolerance, ageing, cost, and production readiness.
- Freeze the optical design parameters and thresholds, including fibre size, routing, coupling, and reflective terminations; document a complete QA/QC chain linking energy deposition, photoelectron yield, and hit threshold calibration.
- Define and validate L1 trigger primitives based on PSU timing and topology (time windows, majority logic, sector overlap), assess latency and bandwidth requirements, and benchmark HLT performance combining muon, calorimeter, and tracking data.
- Explore the detector's performance for long-lived particle signatures, including displaced and delayed muons, by exploiting the six-layer geometry and precise timing. Establish timing windows and buffer depths at L1 and HLT, and develop benchmark analyses to quantify expected sensitivity gains.
- Finalise integration readiness by completing routing, grounding, and shielding layouts; validate access and maintenance plans; and prepare detailed procedures for calibration, timing alignment, and synchronization across large detector areas.

SUPERCONDUCTING SOLENOID

Recommendations

- Verify the magnetic field uniformity in the TPC region to ensure compliance with the stringent requirements for trajectory reconstruction, maintaining close coordination between the TPC detector and magnet groups.
- Accelerate the development of the Al-stabilised superconductor to demonstrate its industrial-scale production feasibility with sufficient length and performance margins. This should be prioritised to enable its application in the model coil winding within the planned timescale.
- Establish a comprehensive model coil development, qualification, and performance test programme. This should include cooldown and excitation tests to verify fabrication techniques, cooling efficiency, superconducting performance, and quench protection characteristics.
- Further optimise the cryogenics and cryostat design, including the implementation of a control dewar that integrates current leads and cooling pipes into a single unit, providing redundancy and robustness in emergency or failure modes.

Recommendations

- Verify the magnetic field uniformity in the TPC region to ensure compliance with the stringent requirements for trajectory reconstruction, maintaining close coordination between the TPC detector and magnet groups.

■ After preliminary calculations by IHEP colleagues, the current magnet field uniformity meets TPC requirements. We will continue to work closely with the TPC team and IHEP team to further validate the magnetic-field uniformity and detector performance.

Recommendations

- Accelerate the development of the Al-stabilized superconductor to demonstrate its industrial-scale production feasibility with sufficient length and performance margins. This should be prioritized to enable its application in the model coil winding within the planned timescale.

■ The development of the Al-stabilized superconductor is of great importance, and we are currently making effort to develop the superconductor. We planed to develop the short sample by 2025, and 100 m conductor by 2026.

Recommendations

- Establish a comprehensive model coil development, qualification, and performance test programme. This should include cooldown and excitation tests to verify fabrication techniques, cooling efficiency, superconducting performance, and quench protection characteristics.

■ We proposed a preliminary design for the model coil and are now refining and optimizing the design. We are developing detailed procedures for coil fabrication, assembly, and performance testing, including cooling and excitation tests.

Recommendations

- Further optimize the cryogenics and cryostat design, including the implementation of a control Dewar that integrates current leads and cooling pipes into a single unit, providing redundancy and robustness in emergency or failure modes.

■ We are optimizing the compactness of the cryogenic structure, along with the process and related components, to add more functions, including the ability to cool the coils and current leads only by gravity in the event of the failure modes. A 5000 L liquid helium Dewar is positioned on the magnet to handle emergency situations, such as power failures and cryogenics failures.

ELECTRONICS

Recommendations

- Clarify the chip development plan by identifying the different versions of each ASIC, specifying which version corresponds to the final size and functionality, and indicating the expected timeline.
- Provide a detailed timeline for testing, iteration, and qualification of the final prototypes, including expected milestones.
- Define the schedule for formal review stages, including the Final Design Review (FDR) and Production Readiness Review (PRR).
- Identify an independent verification team—particularly for the digital design components—to ensure comprehensive coverage. Employ modern verification methodologies and tools to manage the increasing complexity of the ASICs.
  - Each ASIC will not only match with its own development plan, but will also match with the detector prototype development. As the FDR and PRR were updated on the overall schedule map, these two nodes mark the critical timeline for each ASIC's development.
    - Most FEE-ASIC, including Taichu, COFFEE, TEPIX, LATRIC, and SIPAC, by the end of 2027/12, the full size full functionality version will be ready for FDR; then they will be co-tested with the detector prototype and should be qualified before 2029/12 for PRR
    - For the data interface ASIC (FEDI, FEDA, OAT) and dc-dc controller (PAL), they should also be ready for the full functionality before 2027/12, before this, the detector R&D will be based on COTS, but module development will be proceed in parallel; after the FDR, all the ASICs should be integrated on modules to replace COTS, and provided to the detector development for a real prototype.
  - Testing and qualification will be accompanied in all the lifetime of the chip development.
    - Before 2027/12, the test will be more focused on the chip functionality. The team will be grouped more with electronics engineers.
    - After the FDR, the test will be more focused on the detector co-test and chip interface refine. More people on the detector and even physics side will be involved into the test team.
  - The verification team, particularly the digit design, are already organized and will be enlarged. The advanced UVM technology for verification has been established for some complex chips (including Taichu, FEDI). This methodology will be evaluated in the early tapeouts of these chips, and will be introduced globally to all the digital designs.

Recommendations

- Monitor and benchmark the radiation performance of the SMIC 55 nm process using small, dedicated test chips submitted alongside each ASIC production batch.
  - This has been considered in previous tapeouts, and will be continued to keep track in future ASIC production phase.
  - The radiation performance of the SMIC 55nm has been preliminarily verified in previous R&D, we will further establish a methodology for the design kit development based on the statistics and further modelling.

TDAQ

SOFTWARE AND COMPUTING

Recommendations

- Establish well-defined reference performance benchmarks and corresponding validation plots to qualify simulation and reconstruction quality, as well as detector performance. Integrate these benchmarks into the new monitoring system.

  We will implement reference benchmarks and validation plots as suggested, and integrate them into the new monitoring system to ensure robust qualification of simulation, reconstruction, and detector performance.

- Define sub-detector–specific performance plots while maintaining a common set of global physics performance benchmarks to ensure consistent validation of software improvements.

  We will establish sub-detector–level performance plots and retain global physics benchmarks to ensure coherent and consistent validation of software improvements.

Recommendations

- Once consolidated, establish clear reference detector performance baselines within the Ref-TDR so that future detector and physics studies use consistent software versions, calibration constants, and conditions (e.g., ensuring that jet resolution and b-tagging results are derived under identical configurations).

  We will establish clear reference detector performance baselines within the Ref-TDR. This will ensure that future detector and physics studies are conducted under consistent software versions, calibration constants, and conditions, enabling reproducible results—particularly for metrics such as jet resolution and b-tagging performance.

- Provide more quantitative details in the resource estimate, including the ratio of Monte Carlo to data events used, expected number of events, and average file sizes per event.

  The version to be published will include a detailed formula to specify the resource estimation, including the ratio of Monte Carlo to data events, expected event numbers, and average file sizes per event.

MECHANICAL INTEGRATION

Recommendations

- Continue and extend the routing-path studies toward the inner detectors (TPC, OTK, ITK, and VTX). While Table 14.5 lists the number and dimensions of cables and cooling pipes, it remains unclear whether the available space is fully adequate—particularly since the routing volume is considered only from the Barrel ECAL outward.

The service is still in optimization and refinement. The space allocation for services to the inner detectors requires a more comprehensive evaluation. We will do a detailed integration check to confirm if the available space is adequate for the cables and cooling pipes listed in Table 14.5. A detailed 3D integration check is plan to identify any potential clashes or space constraints within the allocated volume.

- Pursue further studies on refrigerant choice across the various sub-detectors. The use of supercritical CO_2 (sCO_2) should be carefully evaluated as an alternative to water, given its dielectric nature, higher heat-transfer coefficient, and reduced piping requirements, which could offer clear technical and operational advantages.

This is already part of our next plan. We will conduct a comparative study between supercritical CO_2 and water cooling systems. The evaluation will focus on thermal performance, system complexity, and integration constraints to determine the optimal solution.

Recommendations

For VTX

- Reevaluate the VTX air-cooling design. Recent studies (Section 4.3.2) indicate that the airflow had to be increased from 3.5 m/s to 5 m/s to maintain performance, yet the temperature of Layer 1 remains close to 30 ° C.
- Validate the thermal simulations presented in Figure 4.18 through the construction and testing of a VTX mock-up with dummy wafers and heaters. This will provide an essential experimental cross-check of the simulated results.

(Answers in Vertex)

DETECTOR PEREORMANCE

Recommendations

- While the detector performance section (15.1) is well advanced, the physics benchmark studies (15.2) — and in particular the treatment of essential experimental aspects such as luminosity determination, resonant depolarization, and alignment strategy (15.3) — remain at an early stage. The committee recommends that, following the established roadmap, the promising work already initiated be further developed to achieve a more comprehensive qualification of the Reference TDR detector performance, including realistic modelling of operational conditions.
  - Agree.
- The TDR places notable emphasis on the new JOI algorithm compared with the standard BDT XGBoost approach. The quark-flavour separation power achieved by JOI, as illustrated in Figure 15.15, is particularly promising. The committee encourages the collaboration to demonstrate its impact on sensitivity to the H → ss decay channel — a novel and distinctive measurement beyond the reach of current LHC experiments.
  - More studies on H->ss with more channels, and comparison with different approaches are onging.
- Since Figure 15.7 indicates that charged kaons can be efficiently identified at the Z pole, the committee further recommends exploring the potential for measuring the forward–backward asymmetry (AFB) in the Z → ss channel.
  - AFB_s analysis is already under development

OVERALL CONSTRUCTION COST AND TIMELINE