Inner Tracker (ITK)

Recommendations (10/2)

- With respect to cooling, the TDR should provide more detailed information about the thermal studies, in particular the origin and justification of the sensor thermal requirements, and should better quantify the motivation for considering CO_2 cooling. As the text currently acknowledges the sufficiency of the water-based solution, a clearer quantitative comparison of the two approaches would help to assess whether parallel R&D is needed

Recommendations

- The “Future Plans” subsection of the TDR should include a much more detailed schedule for the testing, redesigning, and manufacturing of the COFFEE ASIC family. This would provide a way to track progress and ensure that critical milestones for the ITK baseline are met in a timely manner.

In the coming years, substantial efforts will be dedicated to developing the full-size HV-CMOS sensor, evolving from small MPW productions to full reticle size. In parallel, module level and system level integration, including R&D on supporting electronics, mechanical structures, cooling systems, and detailed integration methodologies, will also be carried out.

Among the target sensor design specifications listed in Table 5.3, achieving a timing resolution of a few nanoseconds to tag the 23 ns bunch crossings is particularly challenging, especially when combined with the requirement for moderate power consumption and high hit density tolerance. To address this, a novel data-driven readout architecture featuring in-pixel Coarse-Fine Time-To-Digital Converters (TDCs) has been implemented in the latest sensor prototype, COFFEE3 (see Figure 5.21). This design fully exploits the 55 nm process’s small feature size, enabling more functionality within the limited pixel area. The chip has been recently submitted and is currently undergoing comprehensive characterization.

Continuous efforts are also focus on improving the sensor design and fabrication processes. In the current HV-CMOS process used for the COFFEE series, the n-well of the PMOS transistor is directly in contact with the charge-collecting deep n-well (Figure 5.15). This configuration can induce voltage variations in the deep n-well due to PMOS transistor flipping, which are further amplified by the front-end electronics. To mitigate this cross-talk effect, a deep p-type layer has been proposed to separate the n-well from the charge collection electrode. Efforts are ongoing to enable such separation through a “quadruple-well process”. As an alternative to process modification, cross-talk can also be avoided by designing the pixel circuitry using only NMOS transistors. Both a CMOS-based array and an NMOS-only pixel array have been designed in COFFEE3, as shown in Figure 5.21. However, process modification remains the preferred solution, as it provides greater flexibility and enhanced pixel circuitry functionality.

Following COFFEE3 verification in late 2025, the focus will shift to process modification. In collaboration with the foundry, a new MPW submission using the “quadruple-well process” is planned for early 2026, followed by testing around mid-2026 to evaluate the modified process. In parallel, a quarter-size chip will be designed and submitted for tape-out after process verification. Testing of this chip, from late 2026 to mid-2027, will serve as an intermediate validation step before full-scale development.

From late 2026 through 2027, the project will advance to the full-size chip design, integrating all validated circuit and process improvements. The designed chip is scheduled for submission by the end of 2027. Final full-size chip testing is planned for 2028 to confirm complete functionality, performance, and production readiness. By the end of 2028, a fully validated, high-performance, and scalable HV-CMOS sensor is expected to be delivered for mass production.

Prototyping of ITK detector modules, along with their mechanical and cooling support structures for integration, will proceed in parallel with the development of the sensor chips. This includes the development of electronic components, methodologies, and tools for detector module assembly, studying support structures to optimize manufacturing procedures, and designing an efficient cooling system.

As the full-sized sensor prototype will only become available after several submissions, small-scale sensor chips together with the evolving off-chip electronic components, will serve as key intermediate steps for the system level R&D for both electrical and mechanical functionalities. Extensive prototyping studies — particularly on the mechanics, assembly and tooling — can be conducted using dummy silicon sensors. Specific traces can be added to these dummy sensors to define assembly procedures, especially when using an automatic gantry system. Dummy sensor modules, and other mechanical and cooling mockups, incorporating additional components that dissipate heat or generate external stress loads, will be useful for thermal and mechanical studies. Prototyping of the cooling system for the ITK and OTK using coolants such as CO_2 or water is currently underway.

Others

- L3151 - conventional partly depleted CMOS are probably meant as MAPS without external HV bias, which more accurately describes these devices.
- A sentence on proposed HV distribution/granularity plan and associated services would be welcome.
- Fig. 5.19 and L 3559-3571: It would be highly welcome to estimate the depletion depth from the capacitance measurement. This is essential to understand the minimum ionizing particle signal one can expect with this process using standard wafers.
- L4172 - for mip particle

Outer Tracker (OTK)

Recommendations

OTK

- Similarly to the case of the ITK, the OTK section of the TDR would benefit from the inclusion of more detailed information about the thermal simulations, in particular the assumptions underlying the sensor thermal requirements. This would help clarify the design margins of the cooling system and provide a stronger justification for pursuing alternatives such as CO_2 cooling in parallel with the water-based baseline.

Recommendations

OTK

- The heat dissipation is very inhomogeneously distributed (dominated at the place of the LATRIC). It is not clear to us if it was taken into account with all the implications to the mechanics/services.

Recommendations

OTK

- In addition, the “Future Plans” section should present a more explicit and detailed schedule for the development, testing, redesign, and validation of the LATRIC ASIC family, to reach the final multi-channel version, as well as the other auxiliary chips required for both the front-end and back-end electronics chain.

The development timeline of the LGAD readout ASIC (LATRIC) is closely aligned with that of the LGAD sensor, with the main focus on the design of a multi-channel ASIC, as shown in Figure 5.42.

Following the successful development and testing of the single-channel LATRIC V0, an 8-channel ASIC (LATRIC V1) will be developed in Q4 2025, incorporating a digital logic control section. This integrated ASIC design will then be submitted for wafer fabrication. By the first half of 2026, the test system design for this ASIC will be finalized. In mid-2026, the performance of the 8-channel ASIC will be evaluated, including crosstalk studies, followed by connection, debugging, and radiation-hardness testing in conjunction with the LGAD sensor.

By the end of 2026, the ASIC design will be refined, and the 64-channel ASIC (LATRIC V2) will be submitted for wafer fabrication. Simultaneously, a prototype of the LGAD readout frontend electronic system will be developed. In the mid-2027, performance tests of the 64-channel ASIC will be conducted, along with evaluations of the frontend prototype, ensuring seamless integration with the LGAD sensor.

By the end of 2027, the 128-channel LATRIC will be designed, integrated, and finalized for submission, paving the way for mass production.

Throughout the development process, the performance of the sensor–ASIC module will be thoroughly evaluated. A key focus will be on verifying whether the TOA and TOT metrics provide sufficient information to achieve the required timing and spatial resolutions. Additional efforts will aim to identify improvements in both the ASIC and the sensor to enhance the overall performance of the OTK detector.

Currently, wire bonding is the commonly used technique for connecting sensors and ASICs. This mature and reliable technology has been extensively applied in numerous experiments. However, alternative packaging and interconnection methods, such as solder-ball connections to the sensor or via an interposer board, will also be explored to further optimize the detector design and functionality.

In addition, to construct an OTK detector prototype, auxiliary chips — including the prototypes of data-link chip series (FEDI, FEDA, and OAT) and the power management DC-DC converters (PAL) — are scheduled for demonstration before 2027, while their final versions will be completed in the subsequent years.

Others

OTK

- Similarly to ITK a sentence on proposed HV distribution/granularity plan and associated services would be welcome. 200V may not be enough to achieve optimum time resolution given the close to room temperature operation and the fact that you are not going to optimize the performance for radiation hardness as for HL-LHC.
- L3781 - please mention the process in which LATRIC is made.
- L3928 - sensor heat dissipation will be much less than that. 300 mW/cm^2 (<1mW/cm^2).
- Fig. 34 - units of charge are not correct
- Table 5.12 - please put also the size of the LATRIC (dimensions)

Table 5.12: Configuration for the LATRIC ASIC (assuming a detector capacitance C_d = 8 pF)

Parameter	Value
Chip size	1.2 cm × 0.5 cm
Voltage	1.2 V
Number of channels	128
Channel pitch	< 100 µm
Single channel noise (ENC)	0.8 fC
Cross-talk	< 10%
Maximum jitter	30 ps at 16 fC
Minimum threshold	4 fC
Dynamic range	8 fC–50 fC
TDC conversion time	< 23 ns
Power dissipation per ASIC	1.5 W (for occupancy < 1%)
Data size per fired channel	48 bits
e-link driver bandwidth	43.33 Mbps or 86.67 Mbps
Technology node	55 nm

A water cooling fluid structure coupled finite element model was established to study the temperature distribution along the entire longitudinal length of the stave, considering a specific water cooling flow rate. The following configurations were used in the model:

- The detector dissipates heat at a flux of 300 mW/cm^2.
- Cooling water enters the stave with a flow velocity of 2 m/s and a temperature of 5 °C.
- Natural convection and radiative heat transfer were not considered.

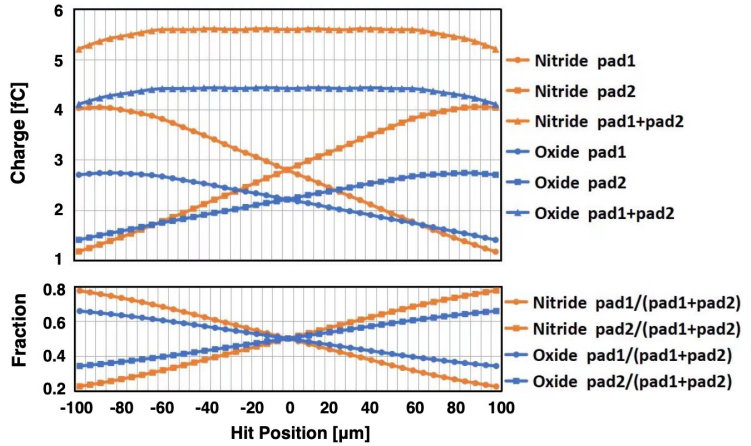

Figure 5.34: Charge collection of two neighboring pads (pad1 and pad2) as functions of hit position for two different dielectric materials: oxide (blue curve) and nitride (orange curve).