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CEPC Reference Detector

Technical Design Report

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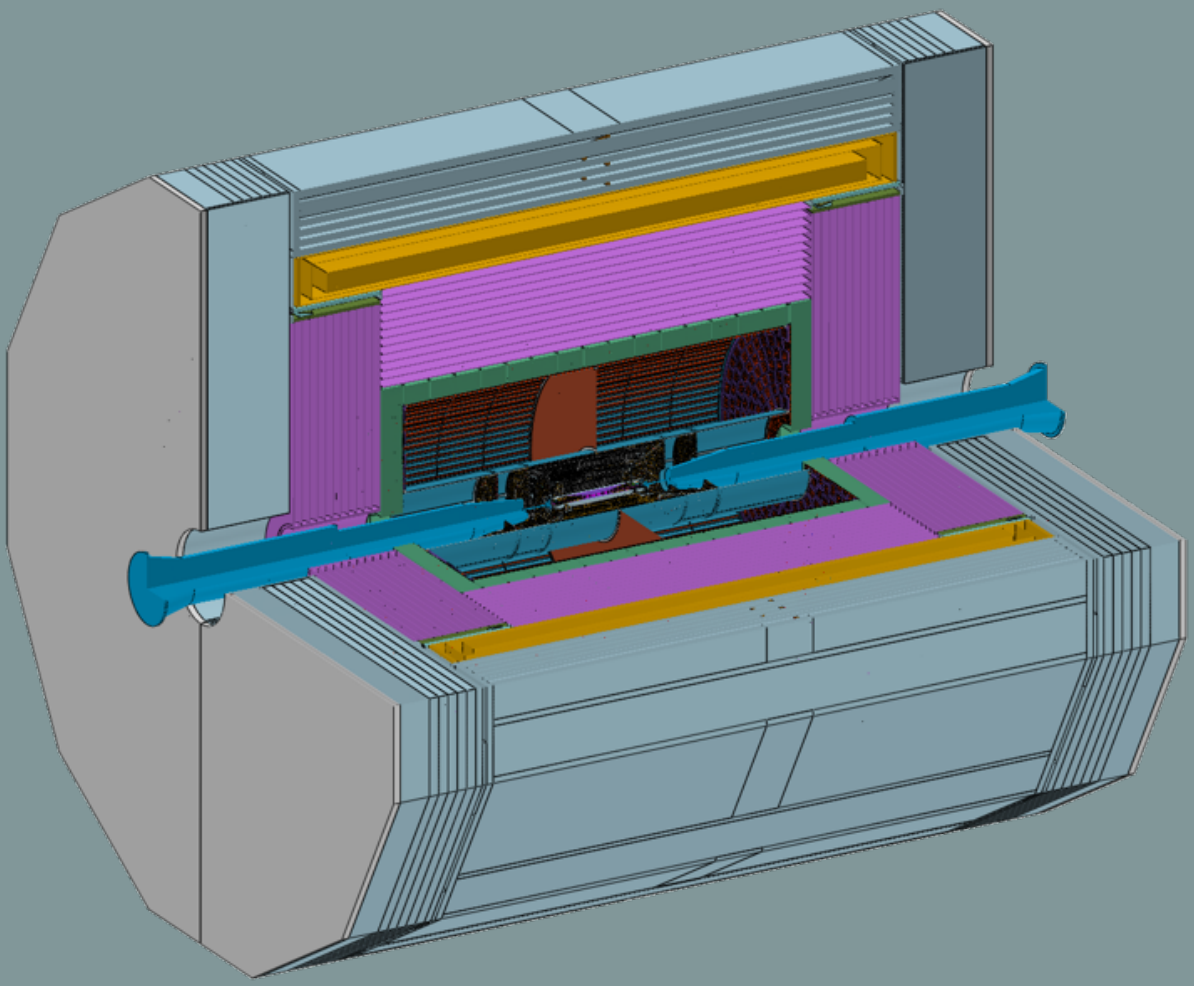


The CEPC Study Group

October, 2025

Contents

Part I

CEPC Reference Detector

Chapter 5 Silicon Tracker

The Silicon Tracker (STK) is primarily designed to provide precise tracking for momentum measurements, as required by the Circular Electron Positron Collider (CEPC) physics programme across all data-taking modes. Located outside the Vertex Detector (VTX), the STK comprises the Inner Silicon Tracker (ITK) and the Outer Silicon Tracker (OTK), with the Time Projection Chamber (TPC) positioned between them.

The baseline design of the ITK employs monolithic High Voltage Complementary Metal-Oxide-Semiconductor (HV-CMOS) pixel sensors, achieving high spatial resolution and sufficient timing resolution for accurate bunch tagging. As the outermost tracking detector, the OTK — based on innovative microstrip AC-coupled Low Gain Avalanche Detector (AC-LGAD) technology — provides precise spatial measurement and extends the tracking lever arm, enhancing overall tracking performance, particularly in momentum resolution. In addition, it functions as a high-granularity Time-of-Flight (ToF) detector, offering precise timing measurement for particle identification.

This chapter begins with an overview of the Silicon Tracker in Section 5.1, followed by detailed descriptions of the ITK and OTK in Sections 5.2 and 5.3, respectively. Section 5.4 discusses the alignment strategies. Performance studies are presented in Section 5.5, and the chapter concludes with a summary and outlook in Section 5.6.

5.1 Overview

To support precise measurements of Higgs boson properties and other key physics objectives, the tracking system must deliver permille-level momentum resolution for charged particles with momenta below 100 GeV/c. In addition, ToF measurements are essential for particle identification in flavor physics studies and jet substructure analyses, particularly for hadron and jet (b or c) tagging.

To meet these requirements, the baseline design of the STK includes three barrel layers and four endcap layers in the ITK, and one barrel layer and one endcap layer in the OTK, as shown in Figure 5.1. This layout enables precise determination of particle trajectories, with a bending lever arm of $\sim 1.6\,\mathrm{m}$ in the barrel region, spanning from the innermost ITK layer to the OTK. Additionally, the OTK provides precise timing measurement as a ToF detector for particle identification. The total surface area of the STK is $\sim 100\,\mathrm{m}^2$.

Each detector layer is required to achieve a spatial resolution of $10\,\mu\mathrm{m}$ or better in the bending direction. At the same time, the detector material budget must be minimized to reduce multiple scattering, which is critical for maintaining good resolution at low momenta. The material thickness per ITK layer is constrained to be $< 1\%$ of a radiation length (X_0), while the OTK allows slightly more material, as it is the outermost tracking layer.

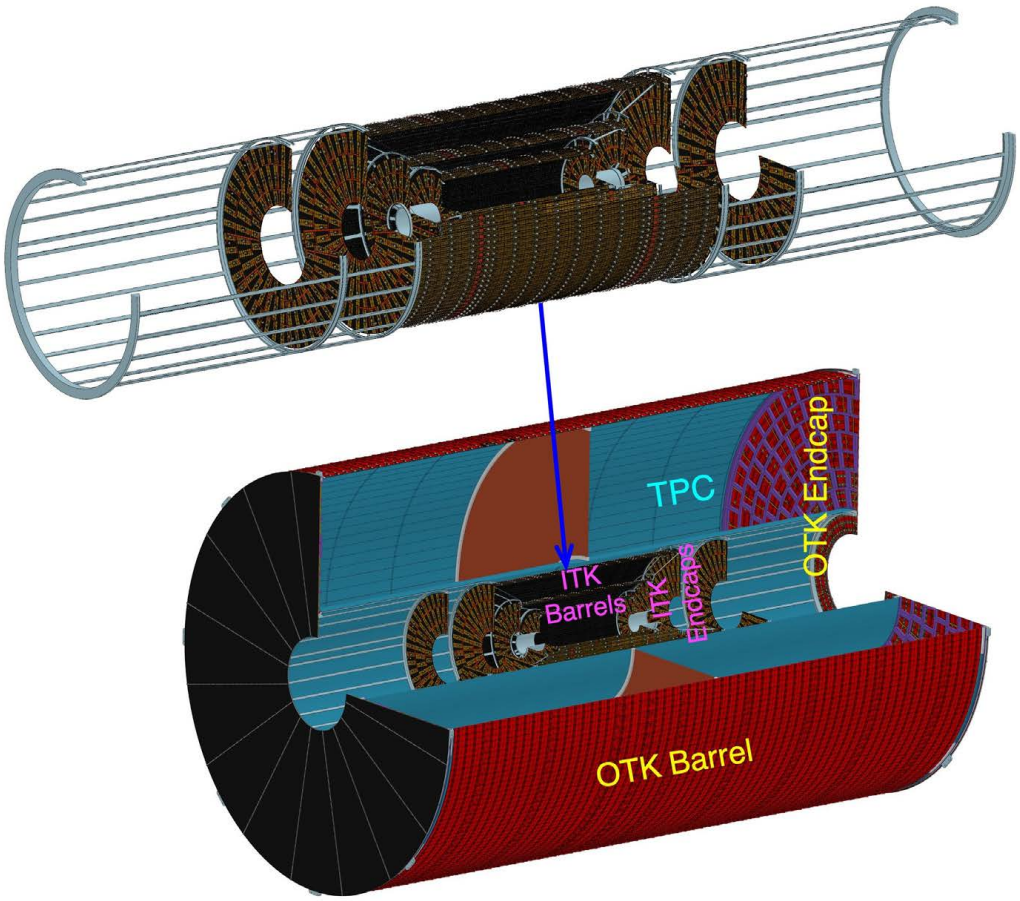


Figure 5.1: Layout of the Silicon Tracker (ITK and OTK). The ITK consists of three barrel layers and four endcap layers, together with two extended connection rings, forming the complete ITK assembly that is inserted into the inner barrel of the TPC. The OTK, as the outermost component of the tracker system, includes one barrel layer and one endcap layer, mounted outside of the TPC. It provides both high-precision spatial and timing measurements.

To meet these constraints, the ITK adopts a 150 µm-thick monolithic Complementary Metal Oxide Semiconductor (CMOS) sensor, which integrates both the sensor and readout circuitry on a single chip. Under the high-luminosity Z-pole operation with 23 ns bunch spacing, a timing resolution of a few nanoseconds or better is required for bunch tagging. Accordingly, monolithic High Voltage Complementary Metal-Oxide-Semiconductor (HV-CMOS) pixel sensor technology has been selected for the ITK. For the CEPC specification, this sensor provides a spatial resolution of $\sim$ 8 µm in the bending direction and a timing resolution of 3–5 ns, thanks to fast and large charge collection in a fully depleted sensor. This performance, achieved with moderate power consumption, significantly outperforms conventional CMOS sensors with shallow depletion, as in typical CMOS Image Sensor (CIS) processes. Common module designs are employed across the barrel and endcap regions to facilitate mass production. The mechanical structures are optimized for a low material budget and high stiffness, incorporating efficient embedded cooling, achieving a material budget of $\sim 0.7\%$ X_0 per layer. Key ITK detector parameters are listed in Table 5.1.

For the OTK, the baseline technology is advanced microstrip AC-coupled Low Gain Avalanche Detector (AC-LGAD), which provides both high-precision spatial resolution (~ 10 μm) for momentum measurement and high-precision timing (~ 50 ps) for particle identification. Unlike the monolithic ITK sensor, the OTK uses a hybrid sensor design, where the sensor and readout Application Specific Integrated Circuit (ASIC) are implemented as separate chips and then bonded together. The AC-LGAD sensor, combined with a dedicated readout ASIC chip currently under development, aims to deliver robust K/π/p separation below a few GeV/c, complementing the TPC's particle identification capability. The sensor modules, mechanical supports, and cooling structures of the OTK are specifically designed to meet the challenges of its large size, limited installation space, and strict material budget constraints (~ 1.5% X_0). Key OTK parameters are also listed in Table 5.1.

Table 5.1: Parameters and layout of the Silicon Tracker. The column labelled $\pm z$ shows the half-length of the barrel layers, and the z position of the endcap disks. The column labelled σ_ϕ and σ_t represent the spatial resolution in the bending direction and time resolution, respectively.

Detector		**Radius R [mm]**		**$\pm z$ [mm]**	**Material budget [% X_0]**	**σ_ϕ [μm]**	**σ_t [ns]**
ITK Barrel	Layer 1 (ITKB1)	235.0		493.3	0.68	8	3–5
	Layer 2 (ITKB2)	345.0		704.8	0.68	8	3–5
	Layer 3 (ITKB3)	555.6		986.6	0.68	8	3–5
OTK Barrel	Layer 4 (OTKB)	1,800		2,840	1.6	10	0.05
		R_{in}	R_{out}				
	Disk 1 (ITKE1)	82.5	244.7	505.0	0.76	8	3–5
	Disk 2 (ITKE2)	110.5	353.7	718.5	0.76	8	3–5
ITK Endcap	Disk 3 (ITKE3)	160.5	564.0	1,000	0.76	8	3–5
	Disk 4 (ITKE4)	220.3	564.0	1,489	0.76	8	3–5
OTK Endcap	Disk 5 (OTKE)	406.0	1,816	2,910	1.4	10	0.05

As in the VTX, the STK hit rates are dominated by beam induced backgrounds, including pair production and single-beam backgrounds. Based on full simulations that incorporate all relevant background sources and the final detector layout, the average and maximum beam-induced background hit rates have been estimated for each STK layer across the three main operation modes, with a safety factor of 2 applied, as summarized in Table 5.2. The ITK and OTK readout systems are designed with sufficient safety margin to handle these rates under all operating conditions, including the most demanding high-luminosity Z-pole mode.

5.2 Inner silicon tracker (ITK)

The ITK is located between the VTX and the TPC. It consists of three barrel layers and four endcap layers, as detailed in Table 5.1, covering an area of ~ 20 m^2.

Table 5.2: Estimated average and maximum hit rates of the Silicon Tracker (safety factor 2 applied) [10^3 Hz/cm^2] for all layers across the three operation modes described in Chapter **??**.

	Low Lumi. Z		**Higgs**		**High Lumi.** Z	
$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	26		8.3		192	
	Average	Max	Average	Max	Average	Max
ITKB1	2.0	3.9	1.2	2.0	6.2	11.7
ITKB2	2.0	6.6	1.1	2.6	5.9	19.8
ITKB3	1.5	3.4	0.8	1.5	4.5	10.1
OTKB	1.3	2.2	0.7	1.2	3.9	6.6
ITKE1	6.9	31.6	4.7	23.4	20.7	94.6
ITKE2	8.0	49.0	4.1	19.6	23.9	146.8
ITKE3	4.6	34.5	2.2	14.9	13.7	103.4
ITKE4	5.1	17.1	2.5	7.4	15.2	51.2
OTKE	3.1	12.7	1.9	8.2	9.2	38.0

5.2.1 ITK design

The ITK design employs monolithic HV-CMOS pixel sensors fabricated using a 55 nm CMOS process to meet the requirements for performance, including power consumption. Key parameters are summarized in Table 5.3, and further details on the sensors are provided in Section 5.2.4.

Table 5.3: The HV-CMOS sensor key parameters

Parameter	**Value**
Sensor size	2 cm × 2 cm (active area: 1.74 cm × 1.92 cm)
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Time resolution	3–5 ns
Power consumption	200 mW/cm^2
Technology node	55 nm

5.2.1.1 ITK barrel design

The ITK barrel design begins with the barrel module, which consists of 14 monolithic HV-CMOS pixel sensors arranged in two rows and seven columns, with their backside glued to a Flexible Printed Circuit (FPC) board that holds electronic components, including a radiation-tolerant Direct Current-Direct Current (DC-DC) converter and a data aggregation chip. The sensors are also electrically connected to the FPC via wire bonds, which transmit clock and command inputs, data output, and both low and high voltages for the sensors.

A schematic of a barrel pixel module is shown in Figure 5.2 (a). Each sensor has dimensions of 20 mm × 20 mm, with an active area of 17.4 mm × 19.2 mm, as listed in Table 5.3. The inactive area of each sensor mainly results from the region reserved for peripheral electronics along one edge, as well as from the guard rings designed to shape the electric field and protect against edge breakdown. Within the module, sensors are oriented such that most inactive regions are positioned along the two long edges of the module, as indicated by the grey areas in Figure 5.2 (a).

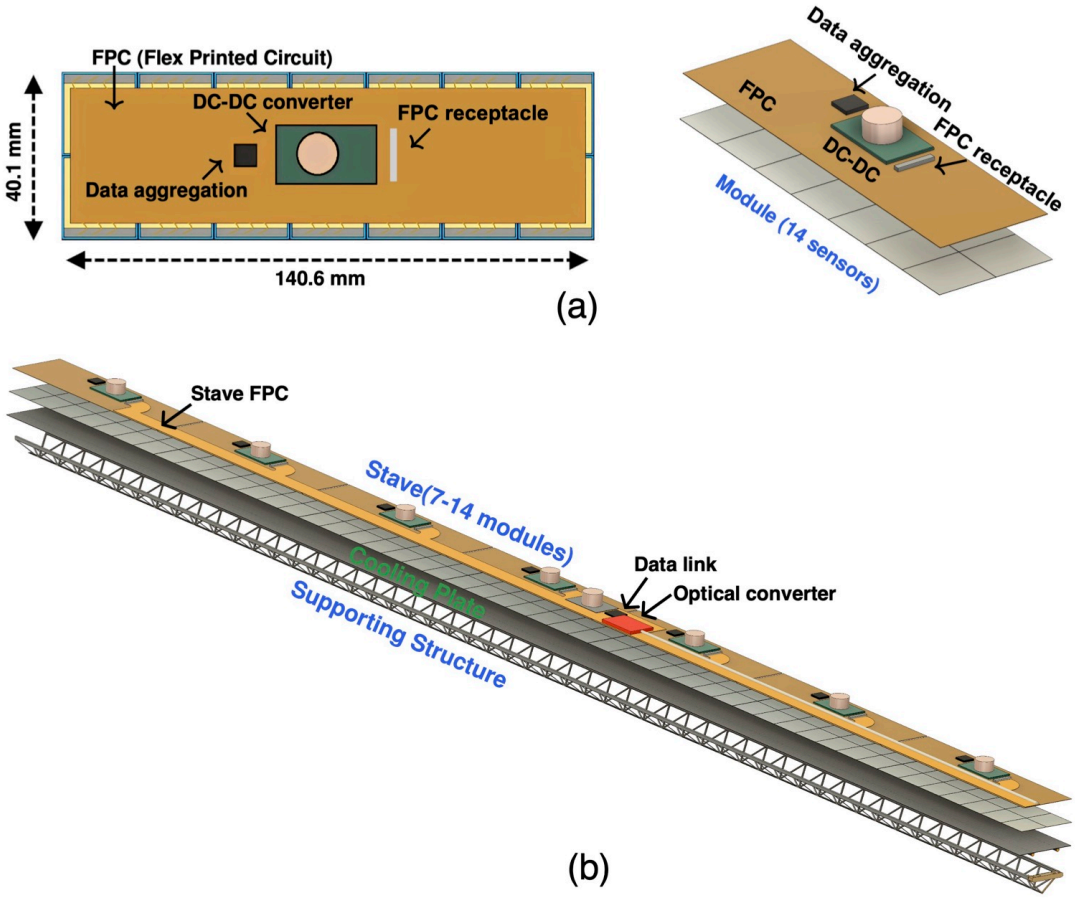


Figure 5.2: (a) ITK module and (b) ITK stave. The ITK module consists of 2 × 7 monolithic HV-CMOS pixel sensors, with their backside glued to a FPC board integrated with electronic components, including a DC-DC converter and a data aggregation chip. Each ITK stave is made up of 7, 10, or 14 modules, one or two long stave FPCs, a plate with embedded cooling tubes, and a truss supporting structure. A data link chip, an optical converter, and DC-DC converters are integrated at the center of each stave FPC.

Within each module, sensors are powered in parallel from a common low voltage input on the FPC, supplied by a DC-DC converter. A single downlink data line connects to the module, from which clock and command signals are extracted and distributed in parallel to each sensor. The uplink data streams from all sensors in a module are aggregated by a data aggregation chip and then transmitted off-module.

Every set of 7, 10, or 14 modules is assembled onto long supporting and cooling structures,

forming three types of staves with a width of 40.1 mm and lengths of 986.6 mm, 1,409.6 mm, and 1,973.2 mm, respectively, as illustrated by a stave in Figure 5.2 (b). These staves are used to construct the three ITK barrels (ITKB1, ITKB2, and ITKB3).

Modules for each stave are mounted on a carbon fiber supporting plate using a specialized assembly system with precision optical metrology and vacuum pick-up tools. The pick-up tools include adjustment mechanisms that allow fine-tuning of the module's position, achieving a placement accuracy better than 10 μm in the local coordinate system. A specific glue, characterized by its radiation resistance and high thermal conductivity, is used to establish robust mechanical and thermal contact between the modules' backside and the surface of the supporting structure.

After gluing all the modules onto a carbon fiber plate of a stave, one or two long FPCs (stave FPCs) are attached on top of the modules to transmit high voltage, low voltage, data, clock signals, and chip commands. For the innermost barrel layer (ITKB1), each stave uses a single FPC to connect all 7 modules, as shown in Figure 5.2 (b). For ITKB2 and ITKB3, each stave uses two stave FPCs, with each serving 5 (ITKB2) or 7 modules (ITKB3) from one end. Each stave FPC integrates a data link chip, an optical converter, and DC-DC converters, all located at its center.

The 150 V High Voltage (HV) and the original 48 V Low Voltage (LV) are both supplied from the end of the stave and transmitted along the stave FPC. The HV is delivered directly to individual modules for sensor biasing. To allow isolation of individual malfunctioning sensors, High-Voltage Multiplexers (HVMUXs) are planned for possible integration into each module FPC. The LV is stepped down to 12 V by the DC-DC converter at the center of the stave FPC, and then distributed to individual modules. Within each module, a local DC-DC converter further reduces the 12 V to 1.2 V to power the sensor circuits.

Uplink data from all sensors in a module are aggregated and sent through the stave FPC to the data link chip, which forwards the data to the optical converter. An optical fiber then transmits the data to the Back-End Electronics (BEE). The same optical fiber cable also carries downlink signals, enabling a bidirectional data link between the stave and the BEE. Details of the ITK electronics are further discussed in Section 5.2.2.

The overall stave, employing a truss structure and a plate with embedded cooling tubes, is designed for low mass (with a radiation length of 0.68% X_0) while providing high stiffness and effective heat dissipation, efficiently removing the heat generated by the modules. The details about the ITK mechanical and cooling design, as well as the performance, are presented in Section 5.2.3.

The three ITK barrels have radii of 235.0 mm, 345.0 mm, and 555.6 mm. Since the inactive regions of the modules (see Figure 5.2 (a)) are concentrated along the two long edges of a stave, the staves in a barrel are mounted in a staggered structure. With this arrangement, each stave is aligned parallel to the z-axis and tilted by 55.85 mrad around it to allow sufficient overlap between neighboring staves, as illustrated in Figure 5.3 (a). To minimize dead space,

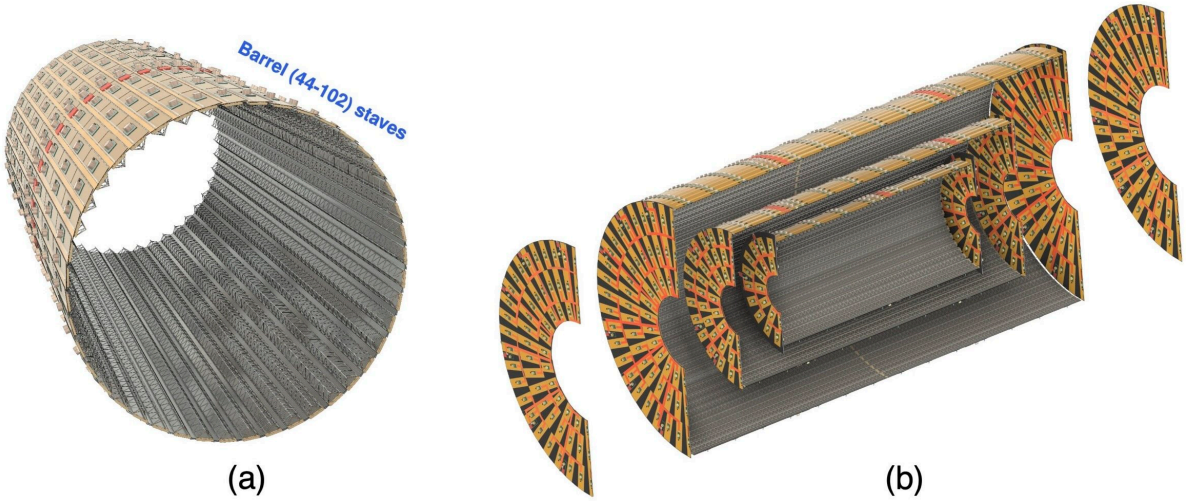


Figure 5.3: (a) ITK barrel and (b) ITK comprising three barrel layers and four endcap layers. Each ITK barrel contains 44, 64, or 102 staves arranged in a staggered structure to minimize dead area.

there are 44, 64, and 102 staves required for the three individual barrels (see Figure 5.3 (b)). Table 5.4 summarizes the detailed information about the staves, modules, and sensors used for the construction of the 3 ITK barrels.

Table 5.4: Information about the staves, modules, and sensors used for the construction of the three ITK barrels.

Barrel	Number of staves	Modules per stave	Sensors per module	Number of sensors	Sensor area [m^2]
ITKB1	44	7	14	4,312	1.72
ITKB2	64	10	14	8,960	3.58
ITKB3	102	14	14	19,992	8.00
Total	210			33,264	13.31

5.2.1.2 ITK endcap design

The ITK endcap consists of four pairs of endcap disks — ITKE1, ITKE2, ITKE3, ITKE4 — with detailed layouts provided in Table 5.1. It uses the same monolithic HV-CMOS pixel sensors as the barrel and adopts similar module design concepts to streamline production. The endcap modules come in three variations containing 8, 12 or 14 sensors, with the 14-sensor module being identical to the one used in the barrel. The longer edge of modules are oriented along the radial (r) direction to optimize the position resolution in the azimuthal direction (ϕ).

Modules are precisely positioned and glued to both sides of a carbon fiber honeycomb support disk for each endcap. Figure 5.4 (left panel) shows the module layout on the front side (facing the interaction point) and back side (facing away from the interaction point) of the fourth ITK endcap (ITKE4). As shown, there are three rings of modules on each side of the endcap. Each module in the outermost ring contains 12 sensors, those in the middle ring contain 14

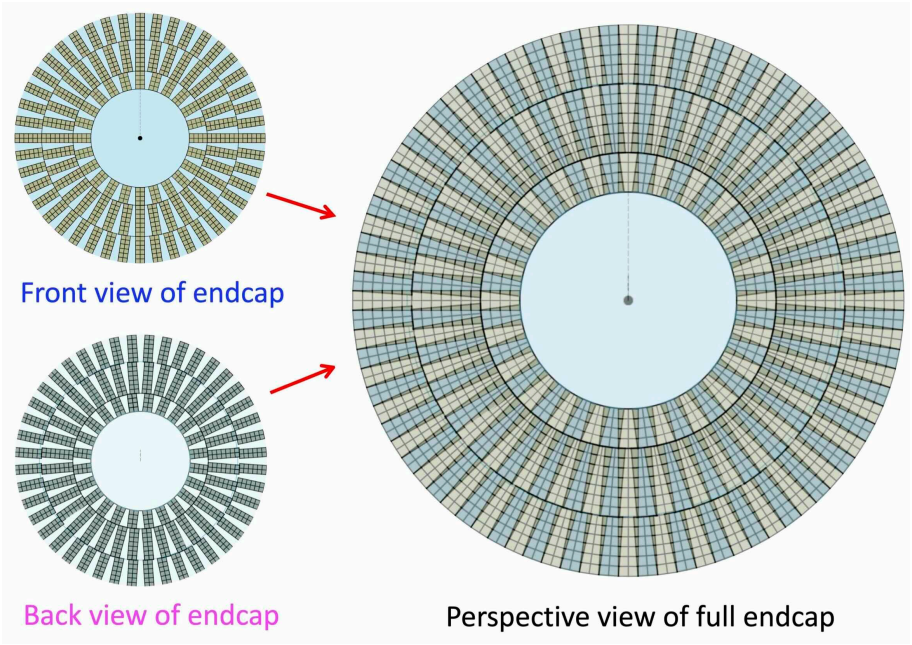


Figure 5.4: Perspective view of the sensor and module distribution for the fourth ITK endcap. The ITK endcap has double-sided detection surfaces, referred to as the "front view" (facing the interaction point) and the "back view" (facing away from the interaction point). The module layouts on the two sides are designed to complement each other to minimize dead detection areas. Overlapping detection regions between the two faces are highlighted as dark green triangles.

sensors, and those in the innermost ring contain 8 sensors. To minimize dead detection area in the endcap, the modules on the back side are offset in the layout relative to those on the front side, creating overlapping coverage between the two surfaces. Figure 5.4 (right panel) provides a perspective view of the complete fourth ITK endcap, where the overlap regions are highlighted in dark green triangles.

The layouts of the modules and their electronic components for the four ITK endcaps (ITKE1, ITKE2, ITKE3, and ITKE4) are displayed in Figure 5.5, with key details summarized in Table 5.5. In total, the four-disk pairs comprise 13,760 sensors and 1,236 modules used in the construction of the ITK endcaps.

Table 5.5: Information about the module and sensor specifications for the four pairs of ITK endcap disks

Endcap	Number of rings per side	Number of modules per ring	Number of sensors per module	Total sensors
ITKE1	2	13,20	8,8	1,056
ITKE2	3	16,24,28	8,8,8	2,176
ITKE3	3	24,36,44	12,14,14	5,632
ITKE4	3	24,36,44	8,14,12	4,896
Total				13,760

After the modules are glued onto the carbon fiber disks, secondary data aggregation Printed Circuit Boards (PCBs) are mounted around the disk periphery, as shown in Figure 5.5 (e.g., four secondary boards on the front side of ITKE1). Each secondary board integrates a data

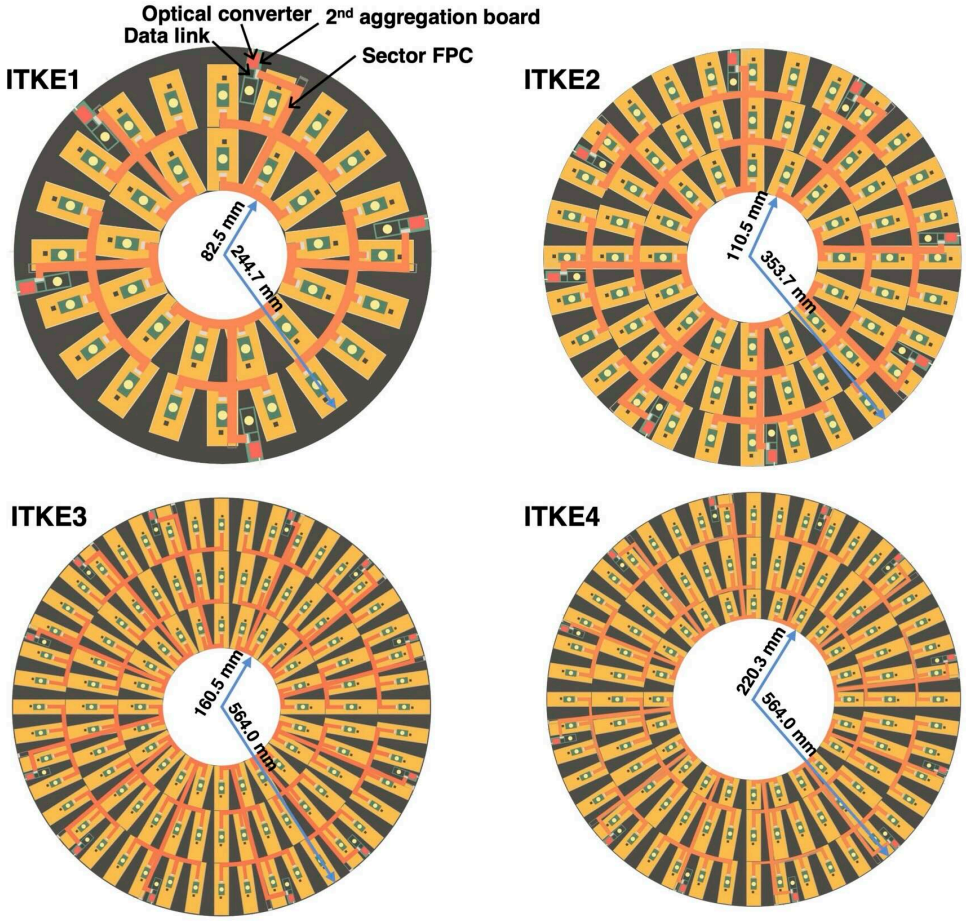


Figure 5.5: Module (yellow) layout of the four ITK endcaps: ITKE1, ITKE2, ITKE3, and ITKE4. Details are provided in Table 5.5. Secondary data aggregation boards — each integrating a data link chip, an optical converter, DC-DC converters, and optionally a data aggregation chip — are attached near the outermost rim of the endcap, with sector FPCs (shown in orange-red) connecting them to the modules.

link chip, an optical converter, DC-DC converters, and optionally a data aggregation chip. The modules connect to these secondary boards via sector FPC connectors (shown in orange-red in Figure 5.5), which transmit power, data, clock signals, and control commands between the modules and the secondary aggregation boards.

The original 150 V HV supply, together with the 12 V LV output stepped down from the 48 V input by the DC-DC converter on the secondary board, provides power to the modules from the outermost rim of the ITK endcap. Readout data from each module is transferred through the sector FPC to the corresponding secondary board, where it is aggregated, converted into an optical signal, and sent via optical fiber to the BEE.

5.2.2 Readout electronics

In each ITK barrel module, 14 monolithic HV-CMOS pixel sensors are bonded to a common FPC, as shown in Figure 5.2. The module FPC transmits digital signals from the sensors to a

data aggregation chip, and then via a long stave FPC to a data link chip, which subsequently sends the data out through the optical converter. To enable flexible data transmission, two ASICs are used for data aggregation: the data aggregation chip, called the Front-End Data Aggregator (FEDA), and the data link/interface chip, called the Front-End Data Interface (FEDI).

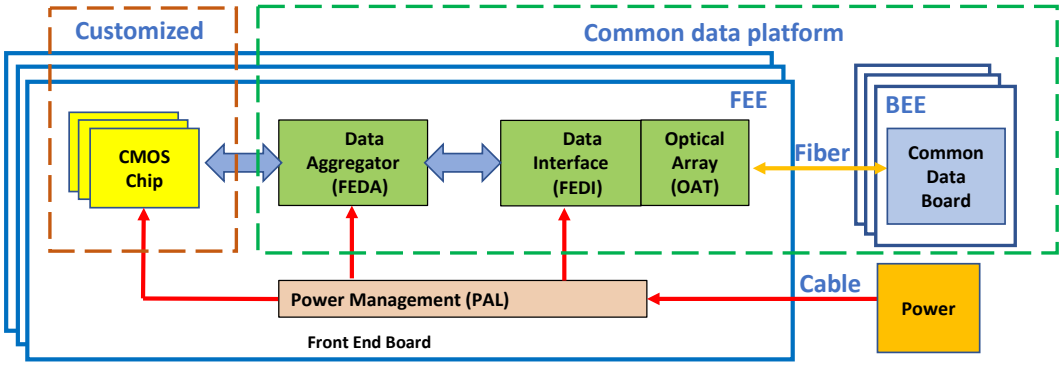


Figure 5.6: ITK readout and power supply scheme. The Front-End Data Aggregator (FEDA) chip collects data from multiple sensors and sends it to the Front-End Data Interface (FEDI) chip, which forwards it via the Optical Array Tranceiver (OAT) module to the Back-End Electronics (BEE). Power is supplied to both the sensors and readout chips through DC-DC converters (Power-at-Load (PAL)).

As illustrated in Figure 5.6, the FEDA chip collects data from multiple sensors and transfers it serially. The FEDI chip [1] then gathers data from several FEDA chips and routes it to the Optical Array Tranceiver (OAT) module for optical readout. The hit rate varies across different radial regions as shown in Table 5.2 for different beam modes. To manage this variation, each aggregation ASIC includes a dedicated buffer. This buffer helps average the rate fluctuations and optimizes the speed of the e-link transceiver inputs. The aggregated data is transmitted via optical fiber from the detectors to the Back-End Electronics (BEE) and Trigger and Data Acquisition (TDAQ) system.

As shown in Figure 5.7, data from each module (up to 14 sensors) is first aggregated by a FEDA chip and then routed to the FEDI chip. The FEDI chip is designed to support a maximum valid data rate of 9.71 Gbps. It collects and aggregates data from seven uplinks, each operating at 1.39 Gbps (e-link), serializes it, and encodes it for high-speed transmission at 11.09 Gbps through an optical fiber.

Considering an average of $\sim$ 1.5 pixels firing per hit, with each fired pixel generating 42 bits of data, the designed per-sensor data bandwidth of 86.67 Mbps (applied to all barrel sensors and the inner radial endcap sensors) corresponds to a maximum hit rate of 4.1×10^5 Hz/cm^2 for a sensor with an active area of 1.74×1.92 cm^2. This is about 21 times higher in the barrel region and 3 times higher in the endcap region than the estimated peak background hit rates (after applying a safety factor of 2), under the most challenging high-luminosity Z-pole operation mode, as shown in Table 5.2.

For the synchronization of different detectors, a reference clock signal is distributed through

optical fiber from the BEE to the FEDI chip. Clock recovery is managed by the FEDI's clock and data recovery circuit. The FEDI chip offers six clock output options: 43.33 MHz, 86.67 MHz, 173.33 MHz, 346.67 MHz, 693.33 MHz, and 1.39 GHz, which are used by the front-end electronics of the various detectors.

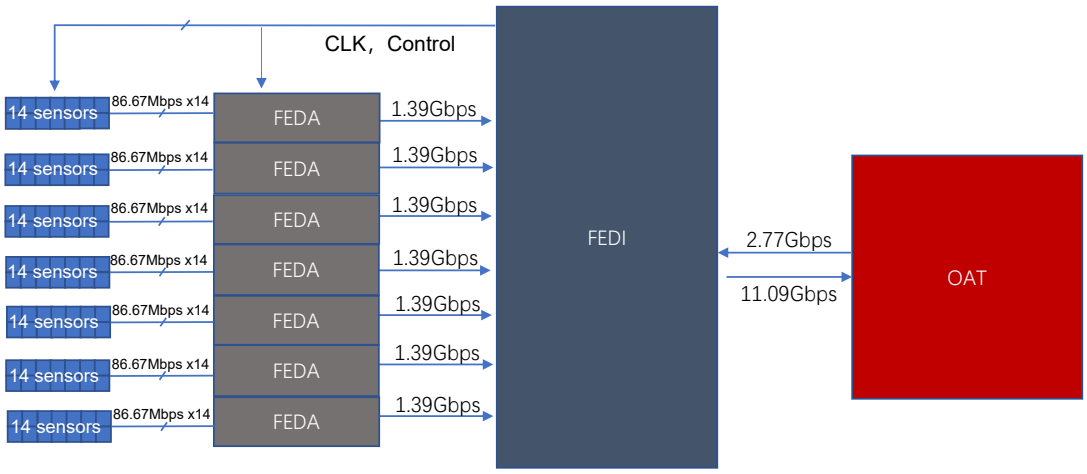


Figure 5.7: ITK readout electronics data flow. Data from 14 sensors are aggregated by a FEDA chip and transmitted via an e-link at 1.39 Gbps to the FEDI chip. Each FEDI chip collects and aggregates data from seven FEDA chips, serializes and encodes it, and forwards it to the OAT at an uplink rate of 11.09 Gbps. The OAT also provides a downlink of 2.77 Gbps for slow control, monitoring, and clock signals, which are distributed to the FEDI chip and then to the FEDA chips and sensors.

The FEDI chip also provides a range of slow control and monitoring features, including Inter-Integrated Circuit (I2C) master controllers, bidirectional Input/Output (I/O) ports, and a memory-like bus master controller for data and address management. The preliminary slow control implementation encompasses power control bits, configuration settings for the sensors, and monitoring functions such as DC-DC status and temperature measurements.

Considering a total power consumption of 200 mW/cm^2 and a sensor area of 2 cm $\times$ 2 cm, each module with 14 sensors requires $\sim$ 9 A at 1.2 V. A DC-DC converter (PAL12) is mounted on the module FPC to meet this current demand. The 48 V LV supplied from the power crate is first stepped down to 12 V using a DC-DC converter (PAL48), and further reduced to 1.2 V by the PAL12 converter, as illustrated in Figure 5.8.

As shown in Figure 5.2 (b) for a barrel stave and Figure 5.5 for endcap disks, the PAL48 converter is located at the center of the stave or the outer rim of the endcap. It steps down the 48 V LV input to 12 V, which is subsequently distributed to the individual modules via the long FPC. In each module, a dedicated PAL12 converter further reduce the 12 V LV to 1.2 V to supply power to the sensor circuits.

FPCs are used to transmit both low voltage and high voltage from the end of the barrel or endcap to the modules. These FPCs, together with optical fibers, are connected to composite cables from outside to deliver power and signals. In the ITK barrel, every three neighboring

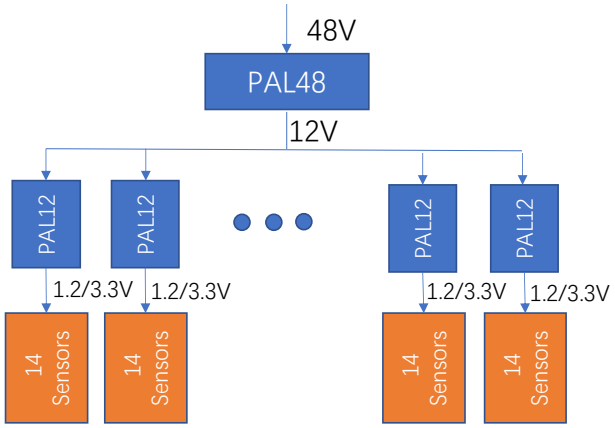


Figure 5.8: ITK readout electronics power distribution. The DC-DC converters operate in two stages: first, the PAL48 DC-DC converter reduces 48 V to 12 V; then, the PAL12 converter steps it down to 3.3 V for the Vertical-Cavity Surface-Emitting Laser (VCSEL) driver in the OAT and to 1.2 V for powering the sensor circuits and other readout electronics.

stave FPCs and their corresponding three fibers on the same side of the stave are grouped into one composite cable. Similarly, in the ITK endcap, every two neighboring sector FPCs and two fibers are connected to one composite cable. In total, the three ITK barrel layers use 128 composite cables, while the four pairs of ITK endcaps use 74.

5.2.3 Mechanical and cooling design

The ITK barrel layers are azimuthally segmented into mechanically independent units called staves, which are mounted onto two end-wheel structures to form three barrel layers, as shown in Figure 5.1. Neighboring staves are partially overlapped to ensure the detector hermeticity, as illustrated in Figure 5.3. Four pairs of assembled ITK endcap disks are also mounted on the same end-wheel structures. Together with two extended connection rings, they form the complete ITK assembly. This entire ITK structure is inserted into the inner barrel of the TPC, with the extended connection rings fixed to the TPC end-wheels. The staves and endcap disks serve as the local support structures of the ITK. They are specifically designed to meet stringent requirements, including a low material budget, high structural rigidity, and efficient cooling.

5.2.3.1 Barrel local support

The ITK stave, a long structure spanning the full length of the ITK barrel, acts as the fundamental building block, integrating both structural and electrical components, as illustrated in Figures 5.2 (b) and 5.3. The design of the ITK stave is similar to that of the ITS2 used in ALICE [2]. The stave structure consists of three main units, as shown in Figure 5.9:

- Sensor Modules: These consist of sensors glued onto FPCs integrated with associated electronics.
- Cooling Plate: A carbon fiber plate embedded with cooling pipes that are in direct thermal

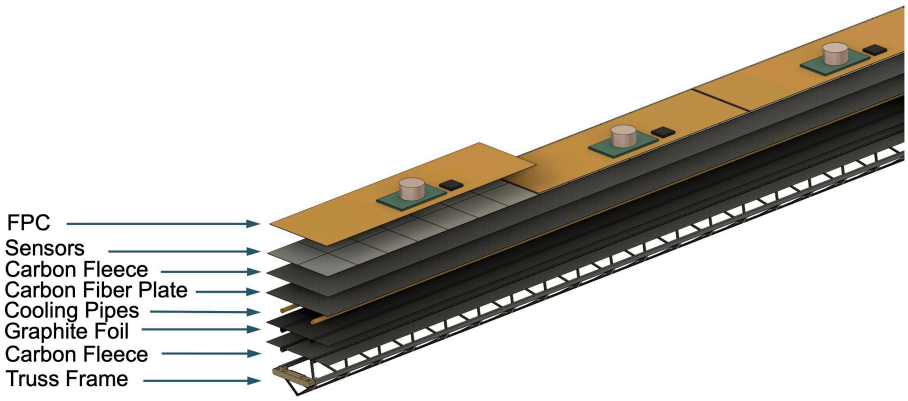


Figure 5.9: Structure of the ITK barrel stave. The stave consists of FPCs integrated with associated electronics and sensors, followed by a top carbon fleece layer, a carbon fiber plate, two cooling pipes, a graphite foil layer, a bottom carbon fleece layer, and a truss frame.

contact with the sensors to efficiently dissipate heat. The cooling pipes are glued to the carbon plate, and the thermal contact is enhanced by a layer of graphite foil. To increase the structural rigidity, an additional thin layer of carbon fleece is added to both the top and bottom sides of the cooling plate.

- Truss Frame: A carbon fiber support structure that provides mechanical support and enhances the stiffness of the stave.

Materials The ITK stave design must meet strict requirements to minimize the material budget. The Cooling Plate is stiffened by the Truss Frame, which has a triangular cross section made from carbon fiber with a high modulus, such as K13C2U [3], with a tensile modulus of up to 900 GPa. Other options, like M60J [4] with a tensile modulus of 588 GPa and M55J [5] with a tensile modulus of 540 GPa, may also be considered in the future. For the Cooling Plate, the carbon fiber used for the plate has high thermal conductivity, such as K13D2U, with a thermal conductivity of up to 800 W/(m·K). Additionally, the thermal performance is enhanced by a layer of graphite foil, which has high thermal conductivity in the horizontal direction, reaching over 1500 W/(m·K). This helps to maintain a more uniform temperature field across the plane.

Water with polyimide cooling pipes has been selected as the baseline cooling medium for the ITK stave. Polyimide possesses excellent properties such as high temperature resistance, corrosion resistance, radiation resistance, and high strength. Additionally, it has a low coefficient of friction and good sliding performance, which reduces frictional losses when transporting fluids or gases, thereby effectively improving the efficiency of the water-cooling system.

Table 5.6 lists the estimated contributions of the ITK stave to the material budget. The overall estimated material budget for a stave is 0.68% X_0. The overlap area between neighboring staves accounts for 8% of the stave area, corresponding to 6% of the stave materials.

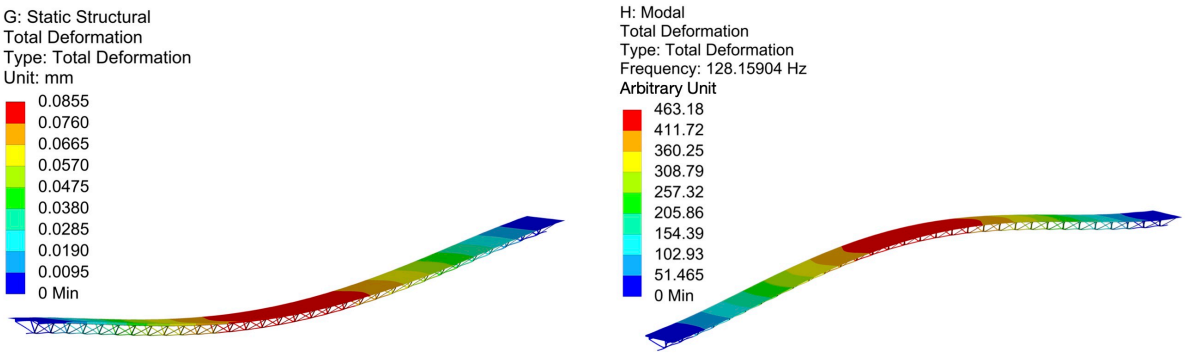
Structural characterization The structural characterization is performed using finite element simulations. The two key structural parameters that define the achievable accuracy and stability in the position of the sensors are the stave sag under its own weight and the first natural

Table 5.6: Estimation of the ITK stave material contributions. The wall thickness of the cooling tubes, averaged over the entire stave area and labeled with "†", is ~ 16 µm.

Functional unit	Component	Material	Thickness [µm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	150	28.41	0.053
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64†	28.41	0.006
	Cooling fluid	Water		35.76	0.028
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Truss Frame	Carbon fiber roving				0.080
Power Bus FPC					0.070
Total					0.677

frequency of the stave. The sag provides information on the deviation of the sensors' final positions relative to the nominal positions, while the first natural frequency indicates the frequency at which an external impulse can induce resonance phenomena in the structure, resulting in oscillations of the sensor positions.

Both the sag and the natural frequency for a given stave mass depend on the stave stiffness, which is mainly provided by the Truss Frame. As a conservative assumption, the contribution of the FPC and cooling pipes to the overall stiffness is not included in this analysis.



(a) Sag analysis (b) Modal analysis

Figure 5.10: Results of (a) gravitational sag analysis and (b) modal analysis for the stave of the first ITK barrel (ITKB1). Both ends of the stave were assumed to be fixed supports. The blue color indicates zero movement, while the red lines represent maximum movement.

Static and modal analyses were performed to evaluate the maximum deflections and the first natural frequencies, as shown in Figure 5.10 for the stave in the first ITK barrel (ITKB1). The results indicate sag values of 85 µm, 289 µm, and 896 µm for the staves in the three ITK

barrels (ITKB1, ITKB2, and ITKB3), with corresponding first natural frequencies of 126 Hz, 69 Hz, and 34 Hz.

Thermal characterization Heat transfer simulation analysis is conducted to optimize the cooling design. The sensor specifications for ITK requires:

- The overall sensor operating temperature should not exceed 30 °C.
- The temperature uniformity across a single sensor should be maintained within 5 °C.

A water cooling fluid structure coupled finite element model was developed to study the temperature distribution along longitudinal length of the stave with the following configuration:

- The heat generated by sensors is uniformly distributed on the carbon fiber plate, with a magnitude of 200 mW/cm^2 (sensor heat flux).
- The cooling water enters the stave with a flow velocity of 2 m/s and a temperature of 5 °C.
- The two cooling polyimide pipes for the ITK stave have an inner diameter of 1.6 mm.
- Natural convection and radiative heat transfer are not considered.

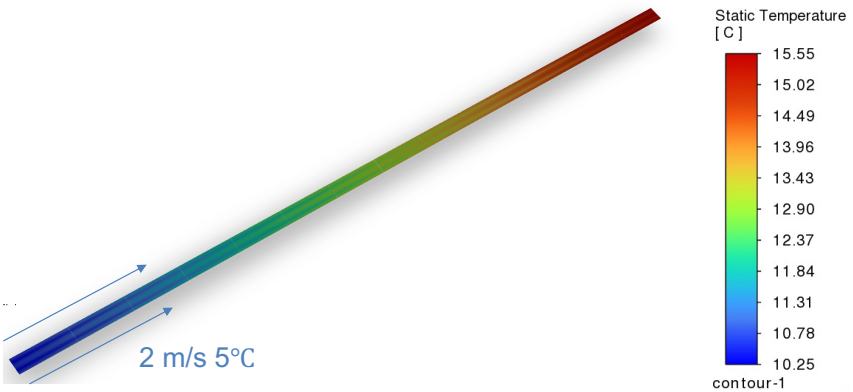


Figure 5.11: Simulation result of water cooling for the stave of the third ITK barrel (ITKB3), with a flow velocity of 2 m/s and a two-pipe inlet temperature of 5 °C. The temperature across the stave remains below 15.6 °C, and the temperature gradient along the stave is within 5 °C.

The simulation result, shown in the Figure 5.11, demonstrates that with both pipe inlets placed on the same side, the temperature gradient along the longest stave — ITKB3, with a length of 1,973 mm — can be controlled within 5 °C. The maximum temperature across the stave remains below 15.6 °C. With this configuration, the water cooling strategy meets the thermal requirements of the detector.

5.2.3.2 Endcap local support

Figure 5.12 illustrates the structure of a single endcap layer (ITKE4). It consists of front and back layers of sensor modules — each glued to a carbon fiber plate (facesheet) — and a central opened cooling plate layer with mechanical and cooling structures, all sandwiched together. The sensor modules are attached to the front and back carbon fiber facesheets using thermal adhesive.

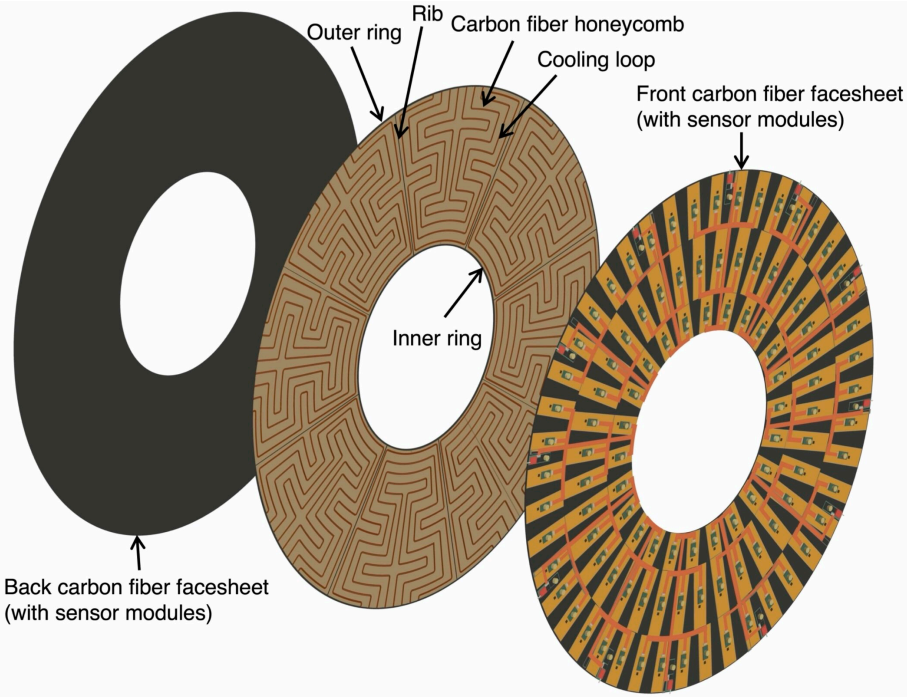


Figure 5.12: Structure of the ITK endcap (ITKE4). It consists of two facesheets with glued sensor modules, and a central supporting and cooling structure composed of an inner ring, an outer ring, eight connecting radial ribs, carbon fiber honeycomb, and integrated cooling loops.

The main mechanical skeleton (frame) of the opened cooling plate consists of an inner ring and an outer ring, connected by eight radial ribs. In addition, carbon fiber honeycomb cores are embedded within the frame to enhance overall bending stiffness and maintain the flatness of the two facesheets. Serpentine grooves are machined into the honeycomb cores to accommodate cooling pipes. The outer ring interfaces with the inlets and outlets of the cooling loops. The gaps between the carbon fiber honeycomb and the cooling loops are sealed with low-mass, high thermal conductivity foam. Finally, the two carbon fiber facesheets (with the sensor modules) and the opened cooling plate are bonded using an adhesive infused with thermally conductive carbon particulates.

Materials The two facesheets are constructed from layers of high-modulus unidirectional carbon fiber material combined with cyanate ester resins. The interface between the cooling tubes and the facesheets is formed using thermally conductive carbon foam, such as Allcomp K9. Water circulating through cooling loops of the cooling plate serves as cooling medium for the ITK endcap.

The frame, comprising the inner ring, outer ring, and eight radial ribs, is made from stiff materials. The primary candidate material for these components is carbon fiber. For the outer ring, high performance Polyether Ether Ketone (PEEK) polymer may also be considered as an alternative material.

Table 5.7 lists the estimated contributions of the ITK endcap to the material budget. The overall estimated material budget is 0.76% X_0.

Table 5.7: Estimation of the ITK endcap material contributions. The wall thickness of the cooling tubes, averaged over the entire endcap area and labeled with "†", is ∼ 24 µm.

Functional unit	Component	Material	Thickness [µm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	150	28.41	0.053
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Structure	Carbon fiber facesheet	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Titanium	100†	3.560	0.067
	Cooling fluid	Water		35.76	0.027
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	2000	186	0.108
	Carbon fiber facesheet	Carbon fiber	150	26.08	0.057
	Glue	Cyanate ester resin	200	44.37	0.045
Total					0.759

Structural characterization The stiffness of the ITK endcap is primarily provided by the carbon fiber facesheets, honeycomb, eight radial ribs, inner ring, and outer ring. Finite element simulations, similar to those performed for the barrel, were also conducted for the endcap structural characterization. Analyses were carried out to evaluate the deformations for the ITK endcaps in both the nominal and flat-lying positions.

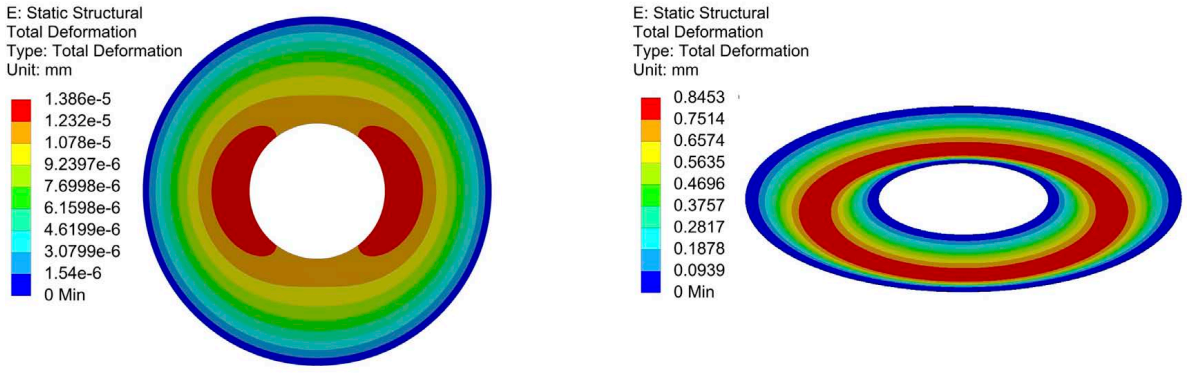


Figure 5.13: Deformations of the fourth ITK endcap in (a) the nominal position, with the outer ring of the endcap assumed to be a fixed support, and (b) the flat-lying position, with both the inner and outer rings of the endcap assumed to be fixed supports. The maximum sag is 0.8 mm in the flat-lying position (b), and negligible (< 1 µm) in the nominal position (a).

As an example, Figure 5.13 shows the deformation for the fourth endcap (ITKE4). A maximum sag of 0.8 mm is found for the ITKE4 in the flat-lying position. In the nominal position, it becomes negligible (< 1 µm). Overall, the stiffness of the ITK endcaps is adequate to ensure they can operate under various conditions.

Thermal characterization The operating temperature of the sensors in the ITK endcaps should meet the same requirements as those in the barrels, as previously discussed. Considering

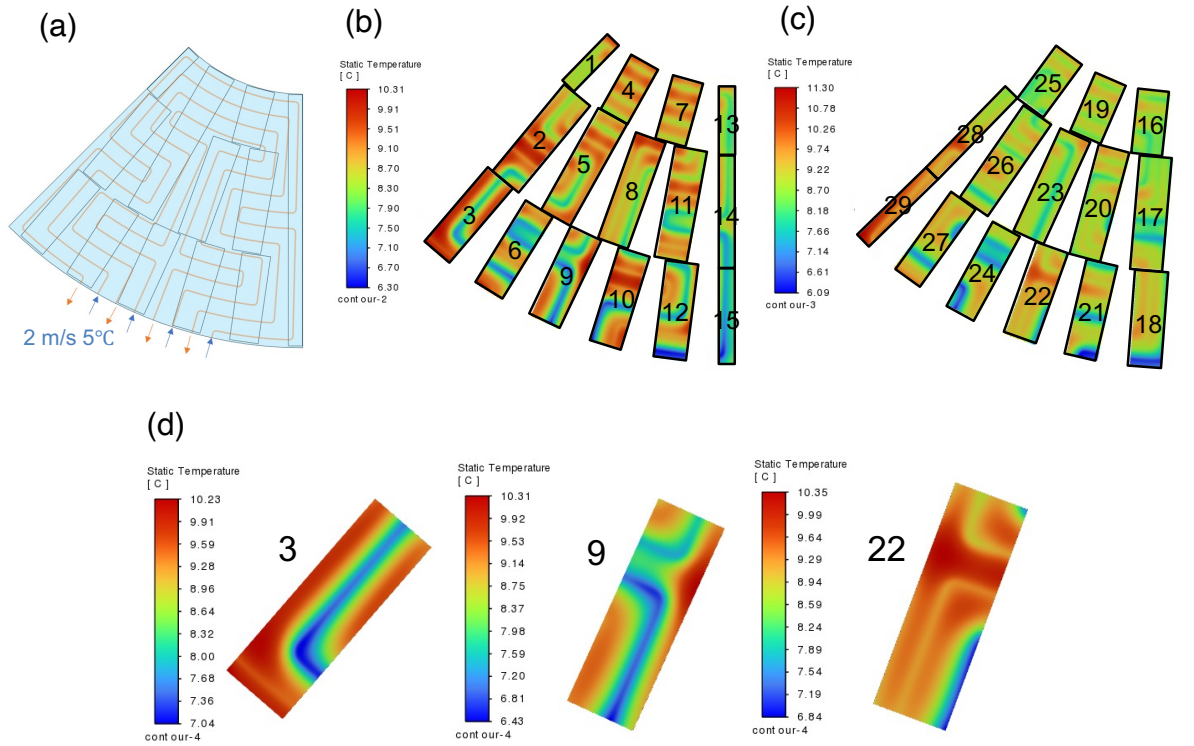


Figure 5.14: (a) Designed cooling loops for one eighth of the ITK endcap, featuring four closed loops arranged radially across 16 coil layers. Sensor temperature distributions for one eighth of the ITK endcap: (b) front-side sensors from 15 modules (numbered 1 to 15), (c) back-side sensors from 14 modules (numbered 16 to 29), and (d) selected temperature profiles from three modules (No. 3, 9, and 22).

the compressive mechanical strength required for the detector on both faces and its ductility, titanium has been chosen as the material for the cooling pipes. Titanium offers high corrosion resistance, low weight, excellent radiation hardness, and high pressure resistance.

The cooling loops for the ITK endcaps are custom-designed to achieve a small temperature gradient across the entire endcap disks. One eighth of the endcap is defined as a cooling unit. Figure 5.14 (a) shows the designed layout of the cooling loops for one eighth of the ITK endcap. This design employs four closed loops arranged radially across 16 coil layers. To ensure uniform temperature distribution across the endcap, the cooling loop design optimizations include radial layering, sector partitioning, and alternating inlet/outlet configurations. Titanium cooling pipes, adopted for the ITK endcaps, have an inner diameter of 1.6 mm and a wall thickness of 0.1 mm. The cooling water enters the ITK endcaps at 2 m/s and 5 °C, the same as in the barrel.

A finite element model was established to study the temperature distribution across the endcaps. Thermal simulations incorporate the thermal conductivity of cooling water, cooling pipes, graphite foam, carbon fiber facesheets, and detector sensors.

Figures 5.14 (b) and (c) show the simulation results for the temperature distributions across both faces of the one eighth of the fourth ITK endcap (ITKE4). The temperature of all sensors on both faces were found to be below 11.3 °C (well below the operation limit of 30 °C). The

maximum temperature difference across the plane is below 5 °C, across one ITK module is below 4 °C (see Figure 5.14 (d)), and across one ITK sensor is below 2.5 °C (satisfying the requirement of < 5 °C). In all aspects, the effective cooling loop design with water cooling meets the detector's requirements in both thermal uniformity and operational functionality.

5.2.4 HV-CMOS pixel sensor

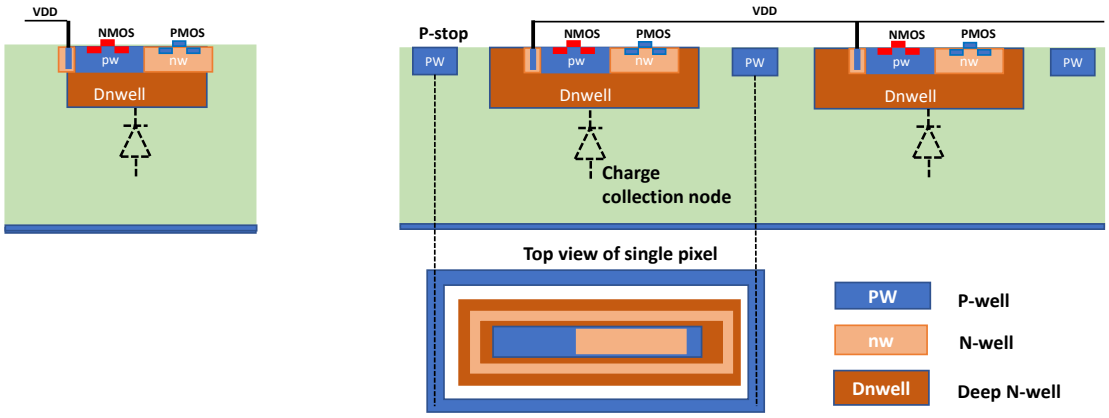
Over the past two decades, monolithic CMOS sensor technologies have rapidly evolved for precise tracking by integrating sensing and readout electronics onto a single substrate. The introduction of deep n-well structures as charge collection electrodes in High Voltage Complementary Metal-Oxide-Semiconductor (HV-CMOS) sensors marked a significant advancement, enabling larger depletion volumes for efficient and fast charge collection as well as enhanced radiation hardness.

Most HV-CMOS sensors in high energy physics utilize 180 nm or 150 nm technology processes, such as those deployed in Mu3e [6] and planned for the LHCb upgrades [7]. However, HV-CMOS technology with a 55 nm feature size has been chosen as the baseline for the ITK for two key reasons. First, a smaller feature size offers the potential for better performance, including lower power consumption, while allowing more functionalities to be integrated within the same area, particularly benefiting digital circuits. Equally important is the reliability of the process access. Since the most advanced processes in industry often lead high energy physics applications by one or two decades, the processes used during the Research and Development (R&D) phase may not be available during mass production. Therefore, starting with more advanced processes is more secure. This choice also aligns with the general trend in Monolithic Active Pixel Sensor (MAPS) development using the CIS process, which is moving from 180 nm to 65 nm, such as the TaichuPix sensor developed by the CEPC team for the VTX detector, and front-end electronics are advancing even further to 28 nm processes.

For ITK R&D, a series of small-scale sensors (COFFEE1, COFFEE2) have been designed, submitted, and fabricated in Multi-Project Wafers (MPWs) using the 55 nm process. Notably, COFFEE2 was the first sensor prototype in the 55 nm HV-CMOS process worldwide. The performance of these small-scale sensor chips are evaluated to provide crucial input for the final detector design, as listed in Table 5.3. A small-scale prototype with full readout functionalities (COFFEE3) has also been designed, and further prototyping toward a full-size chip is planned, both of which are covered in Section 5.2.5.

The COFFEE1 chip was fabricated in a 55 nm Low-Leakage process in an MPW in 2022. While this is not a High-Voltage process, it features a similar deep n-well structure underneath the electronics, which could serve as a large electrode, as illustrated in Figure 5.15 (a). The default wafers with low resistivity of a few $\Omega \cdot$ cm are used. This chip has an area of 3 mm $\times$ 2 mm, including arrays of passive diode sensors. The current-voltage curve shows a breakdown voltage at around -9 V, and a clear signal generated in the sensor in response to laser is observed.

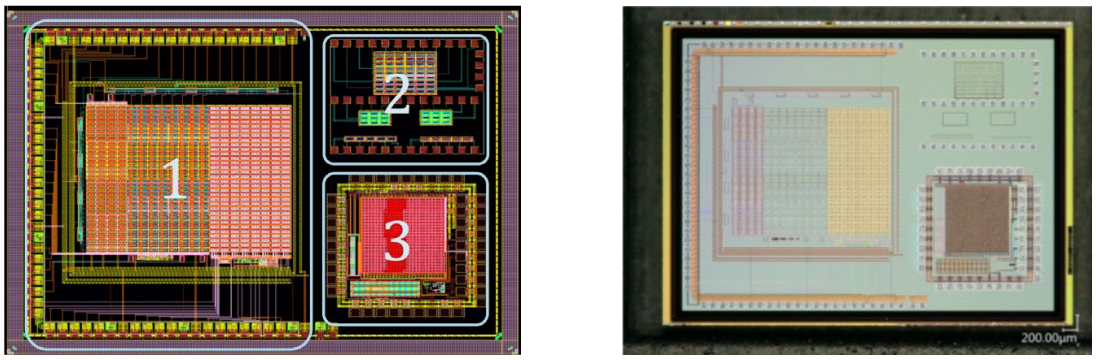
More results can be found in Ref. [8].



(a) Low-Leakage process (b) High-Voltage process

Figure 5.15: Cross-sections of the 55nm (a) Low-Leakage and (b) High-Voltage CMOS processes. The Low-Leakage process was used in the COFFEE1 chip, while the High-Voltage CMOS process was adopted in the COFFEE2 chip.

With the experience accumulated with COFFEE1, the first proof-of-principle sensor chip in 55 nm HV-CMOS process, COFFEE2, was developed. Figure 5.15 (b) shows the cross-section of this process, which is triple-well process including n-, p-, and deep n-wells. Up to ten metal layers can be used for fine pitch routing, including two thick metal layers for power. In this MPW, six metal layers are used, where one thick metal layer is used for power lines.



(a) (b)

Figure 5.16: (a) Floorplan and (b) photo of the COFFEE2 chip. The chip comprises three sections: Section "1" contains diode arrays and in-pixel circuits; Section "2" consists of passive diode arrays similar to those in COFFEE1; Section "3" is designed for imaging applications with small pixels and is not directly relevant to the CEPC use case.

The COFFEE2 chip has an area of 4 mm × 3 mm, with its floorplan and a photo shown in Figure 5.16. It is divided into three sections addressing different design purposes:

- Section “1” has a 32×20 pixel matrix with in-pixel circuits.
- Section “2” consists of passive diode arrays similar to COFFEE1 with the same pixel sizes as in the Section “1”.
- Section “3” is designed for imaging application with small pixels for external applications outside of CEPC.

The pixel pitch was initially planned to be $25 \times 150\,\mu m^2$ as in COFFEE1. However, this would be extremely challenging, as the narrower areas require a few micrometers of clearance to be kept from the edge of the deep n-well, leaving no more than 10 μm on one side for the circuit. Therefore, a less elongated pixel shape was adopted while keeping a similar pixel area, resulting in a pixel size of $40 \times 80\,\mu m^2$.

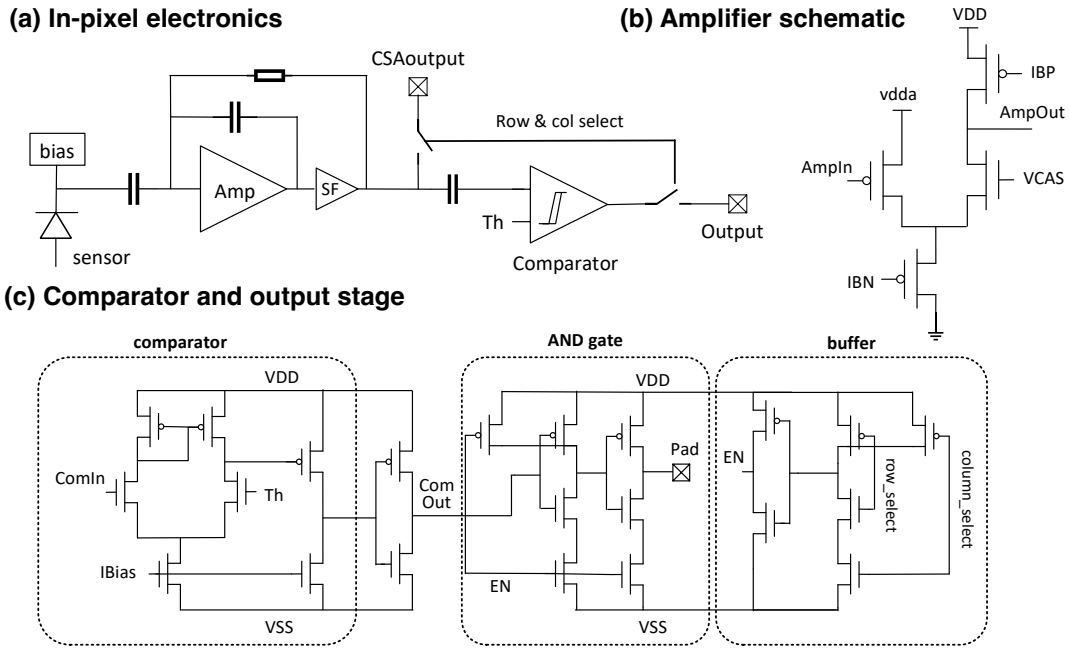


Figure 5.17: Schematic diagram of in-pixel electronics in Section “1” of COFFEE2. (a) The sensor generates a signal that is amplified by a charge-sensitive amplifier, consisting of a gain stage (Amp) and a source follower (SF). The amplified signal, labeled as “CSAoutput”, is Alternating Current (AC)-coupled to a comparator, which converts the analog signal into a digital output. This output is routed to the exterior of the pixel via a shared output bus per column, with row and column select signals managing the pixel address. (b) Schematic of the amplifier (Amp), which operates using the current bias “IBN” and the voltage bias “VCAS”. (c) Detailed circuit elements of the comparator and output stage. The comparator compares the input signal “ComIn” with the threshold reference “Th”, using “IBias” as the current bias. The output signal “ComOut” passes through an AND gate and a buffer before reaching the external output pad. This configuration ensures robust digital signal readout, controlled by enable signals “EN”, and facilitates row and column selection via “row_select” and “column_select”. All bias signals are externally controlled, allowing fine-tuning of the amplifier during testing.

Figure 5.17 shows the schematic design of the in-pixel electronics in Section “1”. A

pixel consists of a Charge-Sensitive Preamplifier (CSA) connected to the front-end collection electrode through AC coupling. A comparator, via another AC coupling stage, is connected to the output stage of the CSA. This arrangement ensures the transmission of the analog signal while isolating the different stages electrically. Only one pixel in the array can be read out at a time when both the "column" and "row" are selected.

Several variations in diode or in-pixel electronics are implemented in Section "1", including:

- Gaps between neighboring deep n-wells are 10, 15, or 20 µm.
- With or without p-stop between pixels.
- Pixels with only amplifiers or with both amplifiers and comparators.
- By default, the comparators are implemented using both Positive channel Metal-Oxide-Semiconductor (PMOS) and Negative channel Metal-Oxide-Semiconductor (NMOS). However, in the left four columns, only NMOS-based comparators are designed. This NMOS-only design aims to mitigate potential crosstalk between the deep n-well and n-well.

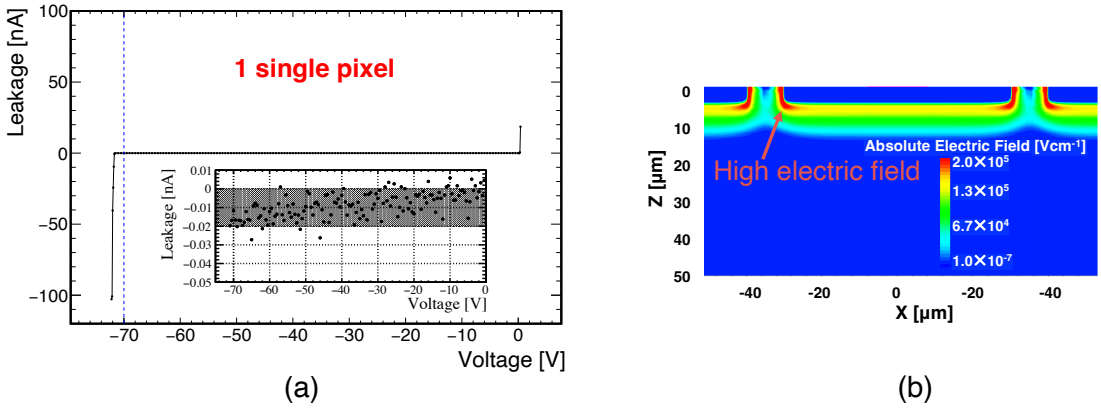


Figure 5.18: (a) IV curve of a pixel in COFFEE2 chip; (b) Technology Computer Aided Design (TCAD) simulation of the passive diode under a reverse bias of −70 V. The breakdown voltage of the COFFEE2 chip is around −70 V, and the leakage current is at the pA level before breakdown.

The IV curve of a typical diode in Section "2" is shown in Figure 5.18 (a). The breakdown voltage can be as large as −70 V. The increase of breakdown voltage of COFFEE2 with respect to COFFEE1 is due to the different CMOS processes. The sudden increase in current beyond the breakdown voltage may indicate that the breakdown occurs at the edge of the deep n-well, which is consistent with the TCAD simulation shown in Figure 5.18 (b). The simulation also demonstrates that the breakdown voltage can be significantly increased by using higher resistivity wafers. The leakage current is at the pA level at low bias.

The capacitance as a function of bias voltage is shown in Figure 5.19 for (a) a single pixel and for (b) 8 connected pixels. Full depletion is not reached when the breakdown occurs. The capacitance should be proportional to pixel area; however, an offset exists due to various

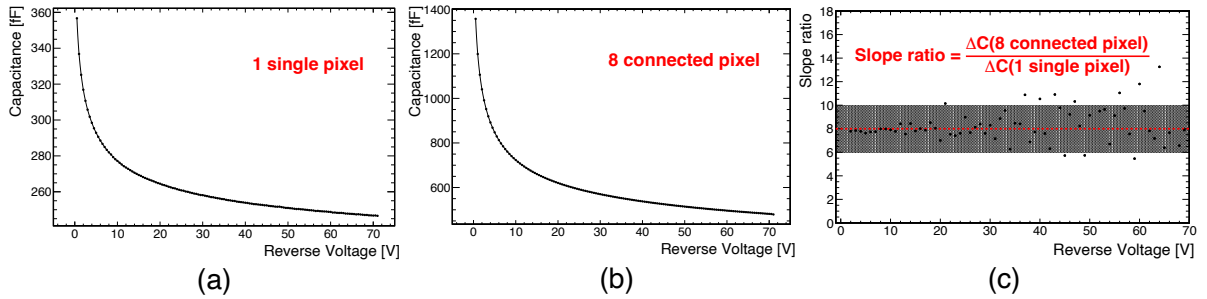


Figure 5.19: CV curves of (a) a pixel, (b) 8 connected pixels in the COFFEE2 chip, and (c) the ratio of capacitance of 8 pixels with respect to 1 pixel as a function of reverse bias. With the offset subtracted, the capacitance of a single pixel is 30–40 fF at a bias of −70 V.

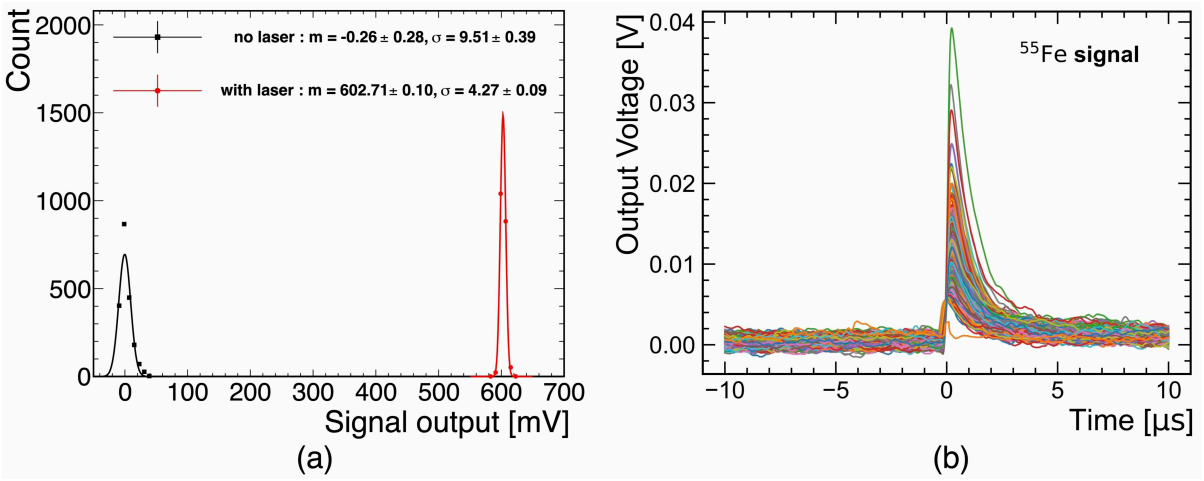


Figure 5.20: Responses to (a) red laser signals (red histogram) compared with no laser (black histogram), and (b) X-rays from ^{55}Fe in a pixel of COFFEE2. Clear signal responses were observed for both the red laser and the ^{55}Fe radioactive source.

reasons, such as the parasitic capacitance of metal routing. To eliminate the offset, the derivative of the CV curves is taken, and the ratio of the capacitance for 8 pixels versus a single pixel is extracted. The ratio agrees well with the ratio of their areas, as shown in Figure 5.19 (c). The raw capacitance of a single pixel at −70 V is about 200 fF, which becomes 30–40 fF after subtracting the offset.

A dedicated carrier board for the test setup was designed and fabricated, which is connected to the general-purpose control and readout board [9], an Field-Programmable Gate Array (FPGA) board, and a personal computer. Clear responses to laser signals and radioactive sources, such as ^{55}Fe, were observed from the amplifier output, as shown in Figure 5.20.

Following the successful verification of the sensor process and the in-pixel analog circuitry of COFFEE2, the subsequent COFFEE3 was designed and submitted for tape-out in early 2025, with fabricated devices received in May 2025. COFFEE3 incorporates an almost complete ASIC readout framework, which can be further extended toward the final chip implementation.

Comprehensive characterization of the chip is ongoing and is expected to be completed by the end of 2025. Further details on COFFEE3 and the HV-CMOS sensor R&D plan are provided in Section 5.2.5.

5.2.5 Future plan

In the coming years, substantial efforts will be dedicated to developing the full-size HV-CMOS sensor, evolving from small MPW productions to full reticle size. In parallel, module level and system level integration, including R&D on supporting electronics, mechanical structures, cooling systems, and detailed integration methodologies, will also be carried out.

Among the target sensor design specifications listed in Table 5.3, achieving a timing resolution of a few nanoseconds to tag the 23 ns bunch crossings is particularly challenging, especially when combined with the requirement for moderate power consumption and high hit density tolerance. To address this, a novel data-driven readout architecture featuring in-pixel Coarse-Fine Time-To-Digital Converters (TDCs) has been implemented in the latest sensor prototype, COFFEE3 (see Figure 5.21). This design fully exploits the 55 nm process's small feature size, enabling more functionality within the limited pixel area. The chip has been recently submitted and is currently undergoing comprehensive characterization.

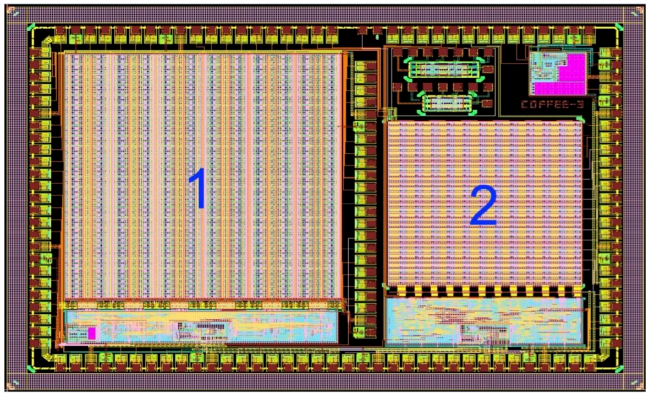


Figure 5.21: Layout of the COFFEE3 sensor chip, consisting of two distinct pixel array sections: Section "1" features a CMOS-based array, utilizing both PMOS and NMOS transistors, while Section "2" contains an NMOS-only pixel array, using exclusively NMOS transistors. Section "1" incorporates in-pixel Coarse-Fine TDCs, fully exploiting the small feature size of the 55 nm process.

Continuous efforts are also focus on improving the sensor design and fabrication processes. In the current HV-CMOS process used for the COFFEE series, the n-well of the PMOS transistor is directly in contact with the charge-collecting deep n-well (Figure 5.15). This configuration can induce voltage variations in the deep n-well due to PMOS transistor flipping, which are further amplified by the front-end electronics. To mitigate this cross-talk effect, a deep p-type layer has been proposed to separate the n-well from the charge collection electrode. Efforts are ongoing to enable such separation through a "quadruple-well process". As an alternative

to process modification, cross-talk can also be avoided by designing the pixel circuitry using only NMOS transistors. Both a CMOS-based array and an NMOS-only pixel array have been designed in COFFEE3, as shown in Figure 5.21. However, process modification remains the preferred solution, as it provides greater flexibility and enhanced pixel circuitry functionality.

Following COFFEE3 verification in late 2025, the focus will shift to process modification. In collaboration with the foundry, a new MPW submission using the "quadruple-well process" is planned for early 2026, followed by testing around mid-2026 to evaluate the modified process. In parallel, a quarter-size chip will be designed and submitted for tape-out after process verification. Testing of this chip, from late 2026 to mid-2027, will serve as an intermediate validation step before full-scale development.

From late 2026 through 2027, the project will advance to the full-size chip design, integrating all validated circuit and process improvements. The designed chip is scheduled for submission by the end of 2027. Final full-size chip testing is planned for 2028 to confirm complete functionality, performance, and production readiness. By the end of 2028, a fully validated, high-performance, and scalable HV-CMOS sensor is expected to be delivered for mass production.

Prototyping of ITK detector modules, along with their mechanical and cooling support structures for integration, will proceed in parallel with the development of the sensor chips. This includes the development of electronic components, methodologies, and tools for detector module assembly, studying support structures to optimize manufacturing procedures, and designing an efficient cooling system.

As the full-sized sensor prototype will only become available after several submissions, small-scale sensor chips together with the evolving off-chip electronic components, will serve as key intermediate steps for the system level R&D for both electrical and mechanical functionalities. Extensive prototyping studies — particularly on the mechanics, assembly and tooling — can be conducted using dummy silicon sensors. Specific traces can be added to these dummy sensors to define assembly procedures, especially when using an automatic gantry system. Dummy sensor modules, and other mechanical and cooling mockups, incorporating additional components that dissipate heat or generate external stress loads, will be useful for thermal and mechanical studies. Prototyping of the cooling system is currently underway.

5.3 Outer silicon tracker (OTK) with precision timing

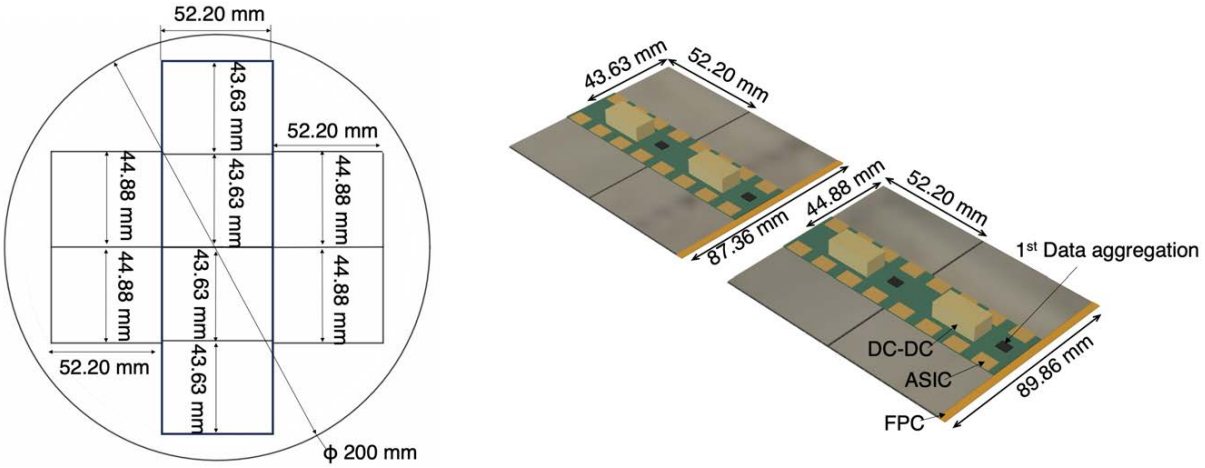
Positioned close to the calorimeter, the OTK is the outermost tracking detector, covering an area of $\sim 85\,\mathrm{m}^2$. It is primarily designed to improve the momentum resolution by extending the tracking level arm with high spatial resolution, while also functioning as a precision ToF detector. This is achieved through the integration of novel microstrip AC-LGAD technology. Together with a high-resolution readout ASIC, the OTK is designed to provide a spatial resolution of $\sim 10\,\mu\mathrm{m}$ and a time resolution of ~ 50 ps.

5.3.1 OTK design

The baseline design of the OTK consists of one barrel detector layer with a radius of $\sim 1,800$ mm and a length of 5,680 mm, along with a pair of endcaps positioned at $|z| = 2,910$ mm, covering a radial range of 406 mm – 1,816 mm. Both the barrel and endcap are constructed from AC-LGAD microstrip sensors with a strip pitch size of ~ 100 μm. These sensors are diced from 8-inch silicon wafers, having a rectangular shape for the barrel and a trapezoidal shape for the endcaps.

5.3.1.1 OTK barrel design

The OTK barrel has two sensor types, with surface dimensions of 43.63 mm × 52.20 mm and 44.88 mm × 52.20 mm, which correspond to an active area of 43.03 mm × 51.60 mm and 44.28 mm × 51.60 mm, respectively. These two sensor types — differ only in length — are diced from a common 8" silicon wafer, as shown in Figure 5.22 (a). The thickness of the sensors is 300 μm. Each sensor contains 512 parallel strips with a strip pitch of 100 μm and strip lengths of 43.03 mm and 44.28 mm for the two sensor types, respectively.



(a) 8" wafer **(b) Module (4 sensors)**

Figure 5.22: (a) Sensors and (b) modules for the OTK barrel. Eight sensors are diced from a single 8-inch silicon wafer, comprising four sensors with dimensions of 43.63 mm × 52.20 mm and four with dimensions of 44.88 mm × 52.20 mm. Each module consists of four sensors arranged in a 2×2 configuration, together with a low-mass PCB that integrates DC-DC converters, readout ASICs, and data aggregation chips. The two sensor lengths correspond to two types of modules, as illustrated in (b).

A barrel strip module consists of four sensors arranged in a 2×2 configuration and a low-mass PCB equipped with radiation-tolerant DC-DC converters, readout ASICs, and data aggregation chips, as illustrated in Figure 5.22 (b). The two sensor lengths correspond to two module types. A module is assembled by gluing the PCB to the silicon sensors using conductive epoxy. Thermal vias are included in the PCB design to improve vertical heat transfer from the

ASICs to the sensor through the PCB. Each readout ASIC has 128 channels, connected to the silicon strips via wire bonding. The DC-DC converters provide low voltage (1.2 V) to two rows of readout ASICs (see Figure 5.22 (b)), with each row of ASICs wire-bonded to a set of strips on one half of a module. Each module contains 16 ASICs to read out 2,048 strips.

Every 8 modules (32 sensors) are glued to a common carbon fiber support plane with a thickness of 0.3 mm, forming a mechanical and electronic unit called a ladder, as shown in Figure 5.23 (a). There are two types of ladders, with lengths of 699.6 mm for short ladders and 719.6 mm for long ladders, assembled using the two types of sensors, respectively. A secondary data aggregation PCB, integrating an aggregation chip, a data link chip, an optical converter, and DC-DC converters, is glued near the middle of the ladder. At the edge of the ladder, a long kapton flexible printed circuit (ladder FPC) is connected (see Figure 5.23 (b)) to transmit high voltage (200 V) for sensor bias, low voltage for DC-DC, data, clock signals, and chip commands. Signals collected from the strips are digitized in the ASICs, aggregated within each module, transmitted through the FPC, and then reach the secondary data aggregation board. Data from all the modules in a ladder undergo secondary aggregation, passes through a data link chip, and is subsequently converted to optical signals via the optical module for readout.

To match the length of the OTK barrel, four long ladders and four short ladders are placed on the TPC outer barrel in a row, forming a long structure called a stave, with a total length of 5,680 mm, as shown in Figure 5.23 (b). In each stave, the central four ladders are short, with two long ladders positioned at each end.

After the ladders mounted onto the TPC outer barrel, two long power bus FPCs per stave are connected to the stave side, with each power bus FPC serving four ladders per half stave from one end. As shown in Figure 5.23 (c), each long power bus FPC is soldering to the four secondary data aggregation boards of the four ladders, and is placed just above the four shorter ladder FPCs. The high voltage (HV, 200 V) and original low voltage (LV, 48 V) are transmitted to the secondary data aggregation boards through the long power bus FPC. The DC-DC converters in the secondary data aggregation boards step down the 48 V LV input to 12 V. The 12 V LV, along with 200 V HV for sensor biasing, is distributed from the secondary data aggregation boards to the primary aggregation boards via shorter ladder FPCs. The DC-DC converters in the primary aggregation board of each module further drops the LV from 12 V to 1.2 V to supply power to the sensor readout ASICs.

Data readout from the sensor ASICs is aggregated on the primary aggregation board and transmitted to the secondary data aggregation board. The secondary data aggregation board processes the data, converts it to an optical signal, and transmits it through an optical fiber. The four optical fibers from four ladders per half stave are attached above the power bus FPC.

The diameter of the OTK barrel is 3,600 mm, requiring 110 staves to cover the full detector area of 65 m^2, as shown in Figure 5.23 (b). Neighboring staves are designed to overlap in the transverse direction to reduce the dead area. The detailed mechanical supporting design for the OTK is elaborated in Section 5.3.3.

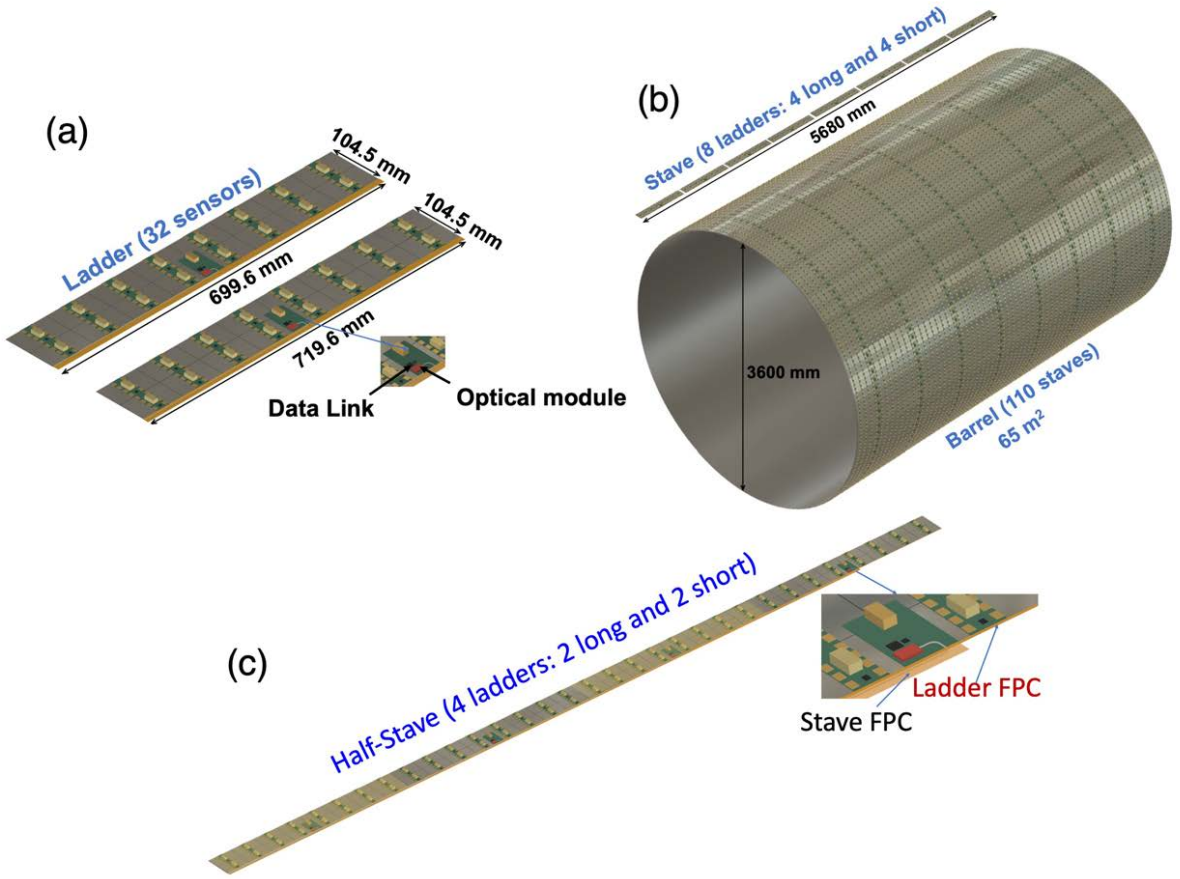


Figure 5.23: OTK (a) ladders, (b) barrel, and (c) half stave. Each ladder consists of eight modules (32 sensors) glued onto a carbon fiber support plane. A secondary data aggregation PCB — integrating an aggregation chip, data link chip, optical converter, and DC-DC converters — is attached near the ladder center, with a flexible printed circuit (ladder FPC) connected at the edge. Two types of ladders are used: short (699.6 mm) and long (719.6 mm). Four long ladders and four short ladders are arranged in a row on the TPC outer barrel to form a stave (5,680 mm). The OTK barrel contains 110 staves in total. The secondary data aggregation PCBs of the four ladders in each half stave are soldered to a power bus FPC (stave FPC) for power transmission from the stave end.

For the OTK barrel construction, the design of the OTK sensor mask and subsequent sensor dicing strategy from 8" silicon wafers, shown in Figure 5.22, have been optimized to maximize the usage efficiency of silicon wafers for the OTK barrel. For the entire OTK barrel, a total of 3,520 wafers are needed, with 15% greater silicon wafer utilization compared to conventional single-piece sensor dicing. Table 5.8 (a) summarizes the detailed information about the number of staves, modules, sensors, and readout ASICs used for the construction of the OTK barrel.

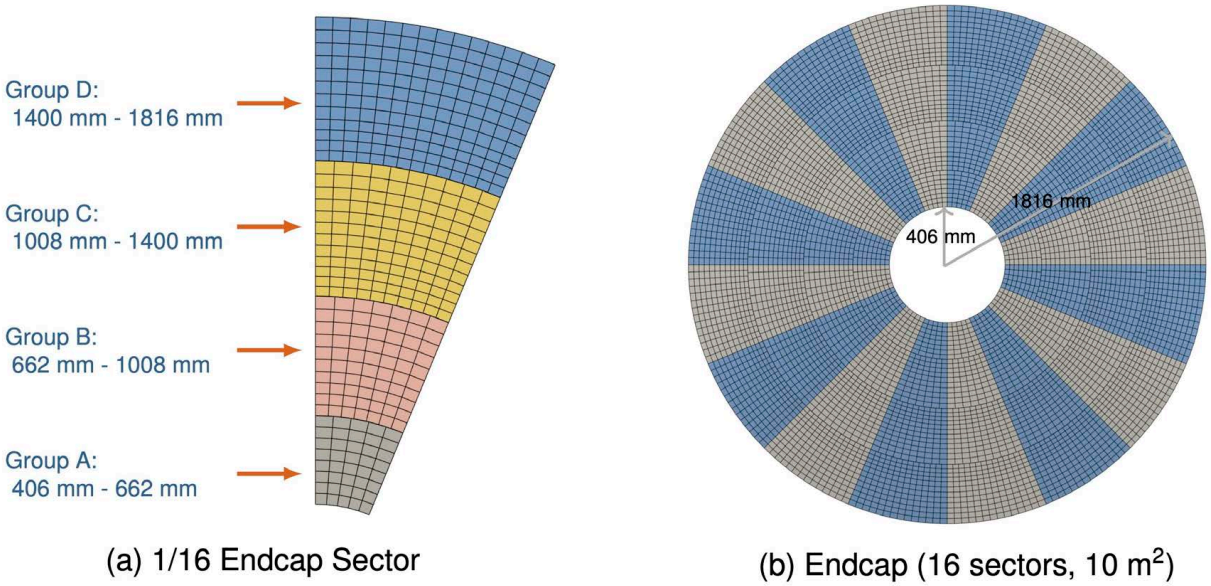
5.3.1.2 OTK endcap design

Each OTK endcap disk covers a surface area of $\sim 10\,\mathrm{m}^2$, corresponding to a radial range of 406 mm – 1,816 mm. Together with the barrel layer, the OTK provides full tracking coverage

Table 5.8: Information about the modules, sensors, and readout ASICs used for the OTK construction

(a) Number of components used for the OTK barrel				
Staves	Ladders	Modules	Sensors	Readout ASICs
110	880	7,040	28,160	112,640
(b) Number of components used for the OTK endcaps				
Sectors	Secondary aggregation boards	Modules	Sensors	Readout ASICs
32	544	6,368	12,736	46,336

up to a polar angle of $|\cos(\theta)| < 0.99$. To facilitate sensor production and assembly, and to maximize silicon wafer utilization, the OTK endcap was specifically designed with trapezoid sensors.



(a) 1/16 Endcap Sector (b) Endcap (16 sectors, 10 m^2)

Figure 5.24: OTK sensor layout for (a) the 1/16 endcap sector and (b) the full endcap. The 1/16 sector of the OTK endcap consists of 42 rings of trapezoidal sensors, which are arranged into four groups: Group A, Group B, Group C, and Group D, each indicated by a different color.

The OTK sensors are fabricated from 8” silicon wafers. Figure 5.24 (a) shows a 1/16 sector of the OTK endcap, which consists of 42 rings arranged into four groups: Group A, Group B, Group C, and Group D, each indicated by a different color. Each group contains 2–4 subgroups of trapezoidal sensors, designed to fit to a common 8” silicon wafer. Figure 5.25 displays the wafer layouts for sensors from individual groups.

As shown in Figure 5.25, the sensor groups — specifically A1 and A2 in Group A, B1 and B3 in Group B, C1 and C2 in Group C, and D3 and D4 in Group D — each contain 4 sensors. Other sensor groups, namely B2 in Group B, C3 and C4 in Group C, and D1 and D2 in Group D, each contain 2 sensors. Each sensor has a set of implanted strips. Trapezoidal sensors with a middle width below 43 mm are classified as narrow sensors, while those above 43 mm are classified as wide sensors, with narrow and wide sensor containing 384 and 512

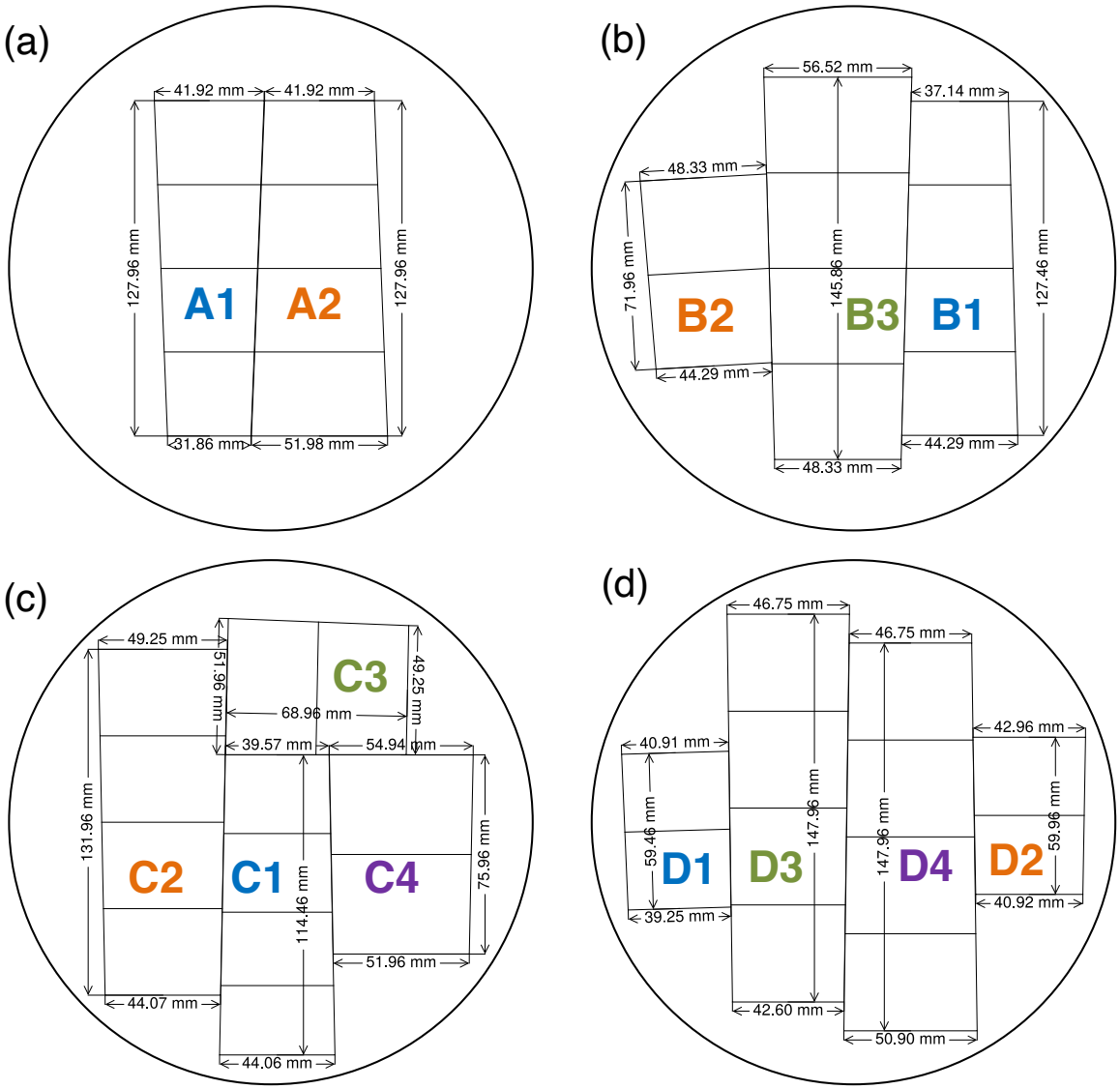


Figure 5.25: Four groups (A, B, C, and D) of OTK endcap sensors diced from 8" silicon wafer. Sensor subgroups B2, C3, C4, D1, and D2 each contain 2 trapezoidal sensors, while subgroups A1, A2, B1, B3, C1, C2, D3, and D4 each contain 4 sensors.

strips, respectively. The sensor geometric parameters are illustrated in Figure 5.25. For example, the surface dimensions of the top trapezoidal sensor of group A1 (A11) in Figure 5.25 (a) are 41.85 mm in top width, 39.34 mm in bottom width, and 31.90 mm in height. With a total of 384 strips, the radial strip pitch of the sensor A11 varies from a maximum of 107.4 µm at the top to a minimum of 100.9 µm at the bottom, while the strip length is ~ 31.2 mm.

In the OTK endcap design (see Figure 5.24), each group of sensors is aligned to a 1/16 sector, with 16 sectors constituting the full endcap. This unique design requires only four masks for sensor fabrication and maximizes wafer usage efficiency. Table 5.9 summarizes the sensors and silicon wafer usage per OTK endcap. For each endcap, 6,368 silicon sensors will be fabricated from a total of 576 silicon wafers.

Table 5.9: Usage of silicon wafers, sensors, and ASICs per OTK endcap

Mask	**A**		**B**			**C**				**D**			
Number of wafers	80		112			160				224			
Sensor subgroup	A1	A2	B1	B2	B3	C1	C2	C3	C4	D1	D2	D3	D4
Sensors per subgroup	4	4	4	2	4	4	4	2	2	2	2	4	4
Number of sensors	320	320	448	224	448	640	640	320	320	448	448	896	896
ASICs per sensor	3	4	3	4	4	3	4	4	4	3	3	4	4
Number of ASICs	960	1280	1344	896	1792	1920	2560	1280	1280	1344	1344	3584	3584

The basic assembly unit for the OTK endcap is the module. As shown in Figure 5.26 (a), each endcap module, similar to the barrel module, consists of two sensors and a low-mass PCB equipped with a DC-DC converter, readout ASICs, and a data aggregation chip. Each PCB, glued to the two sensors, serves as the primary data aggregation board, reading out two sets of strips. Each PCB has 6 ASICs for wide sensor modules and 8 for narrow sensor modules, with the ASICs wire-bonded to the strips.

For the OTK endcap, the 1/16 sector is designed as a complete mechanical and functional unit. To construct it, as shown in Figure 5.26 (b), 199 modules are glued on a 1/16 sector carbon fiber plane. Next, 17 secondary data aggregation boards are glued to the sensor surfaces of 1/16 sector, with each secondary data aggregation board connected to the two lateral rows of primary data aggregation boards. As illustrated in Figure 5.26 (a), each secondary data aggregation board includes a data aggregation chip, a data link chip, an optical module, and DC-DC converters. The primary aggregation board connects to the secondary aggregation board via a FPC connector. The lateral row of PCBs, or primary aggregation boards, in 1/16 sector are interconnected using compact connectors or wire soldering (the final method has yet to be decided). These connections enable the transmission of power, data, clock signals, and chip commands between the secondary aggregation board and any primary aggregation board.

As shown in Figure 5.26 (b) of a 1/16 OTK sector, 17 long power bus FPCs are arranged into three groups and fixed on three supporting frames. These FPCs extend from the outermost rim of the OTK sector to connect with the 17 secondary data aggregation boards. The high voltage (HV, 200 V) and original low voltage (LV, 48 V) are transmitted to the secondary data aggregation boards through these power bus FPCs. The DC-DC converter on the secondary data aggregation board steps down the 48 V LV input to 12 V and, along with the 200 V HV supply, distributes power to the primary aggregation boards. The 200 V is used for sensor biasing, while the DC-DC converter in the primary aggregation board of each module further drops the LV from 12 V to 1.2 V to supply power to the sensor readout ASICs.

Data readout from the sensor ASICs is aggregated on the primary aggregation board and transmitted to the secondary data aggregation board. The secondary data aggregation board processes the data, converts it to an optical signal, and transmits it through an optical fiber. The 17 optical fibers from the 17 secondary data aggregation boards in a sector are attached to the same mechanical frames as the power bus FPCs.

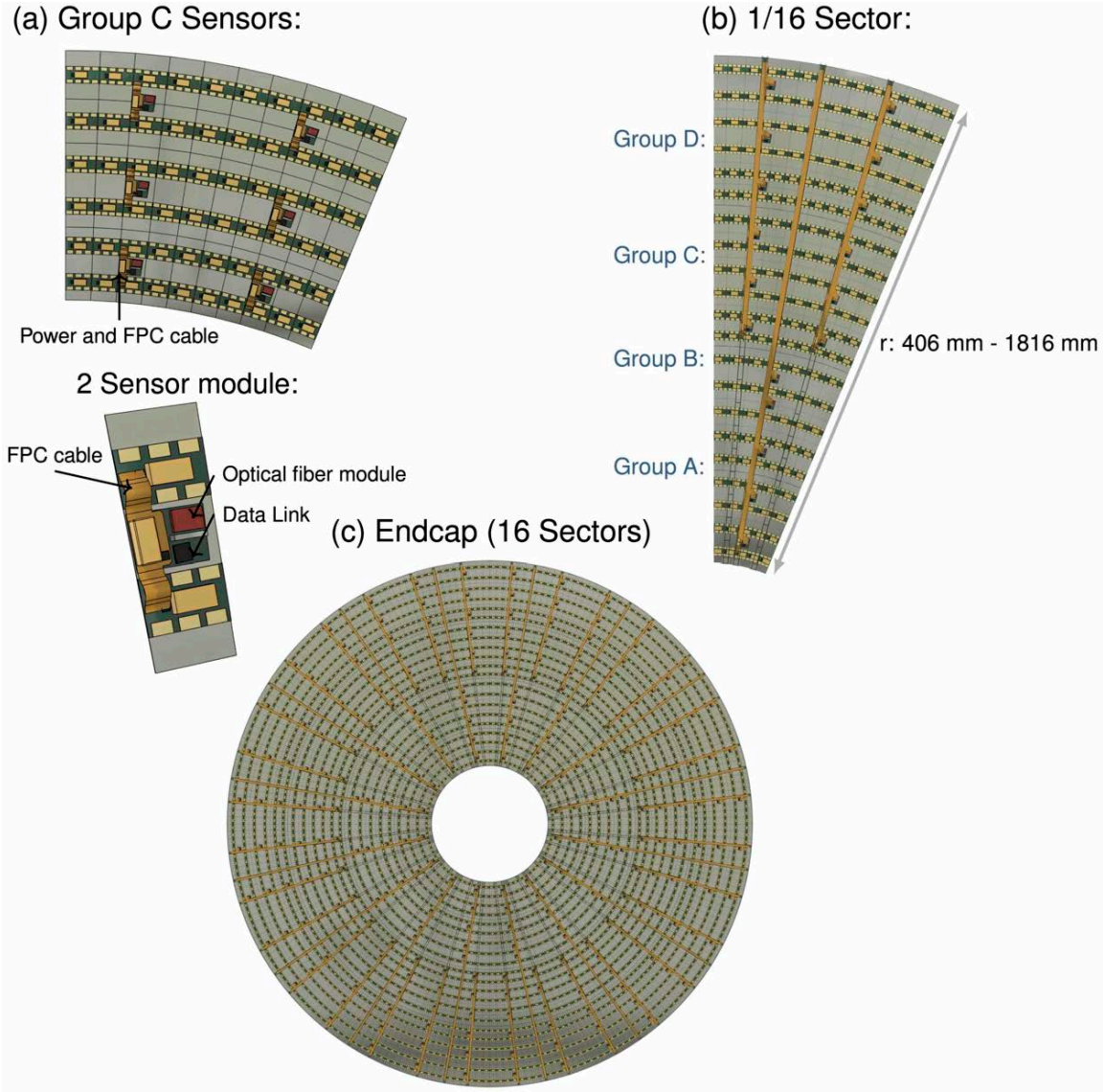


Figure 5.26: (a) The Group C sensors, (b) 1/16 sector of the OTK endcap, and (c) the full OTK endcap. Each endcap module consists of two sensors and a primary data aggregation board (a low-mass PCB equipped with a DC-DC converter, readout ASICs, and a data aggregation chip). Each secondary data aggregation board (a low-mass PCB integrated with DC-DC converters, a data aggregation chip, a data link chip, and an optical module) is glued to the sensors and connected to the two lateral rows of primary data aggregation boards via FPC connectors. The 1/16 OTK endcap sector contains 199 modules, 17 secondary data aggregation boards, and 17 long power bus FPCs arranged into three groups and fixed on three supporting frames for power transmission from the outermost rim of the endcap.

A complete OTK endcap consists of 16 sectors. Figure 5.26 (c) shows the OTK endcap with sensors and electronic components. Table 5.8 (b) summarizes the detailed information about the number of sectors, secondary data aggregation boards, sensors, and readout ASICs used for the construction of the OTK endcap pair. A detailed description of the OTK electronic design is provided in Section 5.3.2. The mechanical and cooling design for the OTK endcap is presented in Section 5.3.3.

5.3.2 Readout electronics

Figure 5.27 shows the overall readout electronics scheme of the OTK. The AC-coupled signals from the Low Gain Avalanche Detector (LGAD) strips in the sensor are processed and digitized by the 128-channel LGAD Timing and Readout Integrated Chip (LATRIC) readout ASIC, on the Front-End (FE) board, also referred to as the primary data aggregation board (Figures 5.22 (b) and 5.26 (a)). The LATRIC ASIC, designed for high-precision timing and charge measurements, is described in detail in Section 5.3.5.

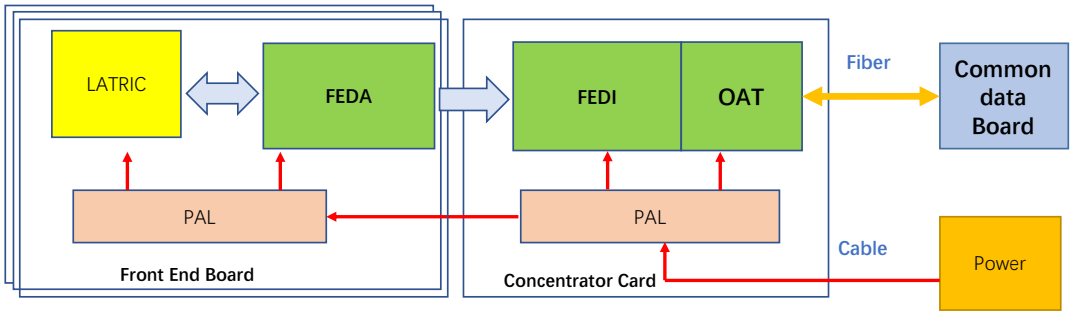


Figure 5.27: OTK readout electronics scheme. The Front-End Data Aggregator (FEDA) chip collects data from multiple LATRIC ASICs and transmits it to the Front-End Data Interface (FEDI) chip. The FEDI chip then forwards the data via the Optical Array Tranceiver (OAT) module to the Back-End Electronics (BEE). Power is delivered through DC-DC converters (PAL) to the LATRIC ASICs and other readout chips.

As illustrated in Figure 5.27, the data from the LATRIC ASICs is first aggregated by the FEDA chip on the FE board and the FEDI chip on the secondary data aggregation board (Concentrator Card), and then routed to the OAT module for fiber readout (Figures 5.23 (a) and 5.26 (a)). The fiber link transfers data between the backend electronics and the secondary data aggregation board.

Power is delivered from the crate via power cables and stepped down in two stages: from 48 V to 12 V, and then from 12 V to 1.2 V or 3.3 V by PAL DC-DC converters, which supply the LATRIC and other readout electronics.

5.3.2.1 Front-end board

In the OTK module, two rows of LATRIC ASICs are integrated on the FE board (Figures 5.22 (b) and 5.26 (a)), with each row wire bonded to a set of LGAD strips. For the LGAD

sensor, each fired strip generates 48 bits of data digitized by the LATRIC ASIC, with an average of about two strips firing per hit. The AC coupling design within the sensor [10] isolates the circuit from large leakage currents and protects the ASIC from potential damage caused by bias voltage in case of an LGAD failure.

The LATRIC ASIC operates on a 1.2 V power supply, which is regulated and filtered by the PAL12 (Power at Load for 12 V) ASIC — a radiation tolerant DC-DC converter capable of delivering up to 10 A of current, sufficient to power up to eight LATRIC ASICs.

On a barrel FE board (Figure 5.22 (b)), sixteen LATRIC ASICs are powered by two PAL12 converters, and their digitized data is aggregated by two FEDA chips. On an endcap FE board (Figure 5.26 (a)), six or eight LATRIC ASICs are powered by one PAL12, and their data is aggregated by one FEDA chip.

In the OTK baseline design, each FE board interfaces to the secondary data aggregation board, transferring the following signals:

- Clock: The FEDI provides 43.33 MHz e-clocks for the LATRIC ASICs.
- Data Readout:
  - Barrel FE board: Two uplink e-links (each at 346.67 Mbps) from two FEDA chips connect to the secondary data aggregation board, supporting a data rate of up to 43.33 Mbps LATRIC ASIC.
  - Endcap FE board: One uplink e-link (693.33 Mbps) from one FEDA chip connects to the secondary data aggregation board, supporting a data rate of up to 86.67 Mbps per LATRIC ASIC.
- Configuration/Sync/Reset:
  - Barrel FE board: Two downlink e-links (86.67 Mbps) are used for configuration, resynchronization, and reset, with each link shared by eight LATRIC ASICs.
  - Endcap FE board: One downlink is shared by six or eight LATRIC ASICs.
- Monitoring: Each FE board supports up to 16 temperature sensors, enabling real-time monitoring of both sensor and electronics temperatures.
- Power:
  - 200 V HV is used for sensor biasing, with HVMUXs considered for integration on the FE board to allow isolation of individual malfunctioning sensors.
  - 12 V LV is delivered from the secondary aggregation board to the PAL12 DC-DC converters on the FE board.

To enable multiple LATRIC ASICs to share a common configuration downlink, each ASIC is assigned a unique 4-bit address through dedicated Identification (ID) pins. The configuration protocol uses this address to configure each LATRIC chip individually via I2C. To ensure reliable reception of the downstream signals from the FEDI, the LATRIC chip can latch input signals on either the rising or falling edge of the clock.

5.3.2.2 Concentrator Card

The Concentrator Card (CC), also referred to as the secondary data aggregation board, is designed to interface the system readout with multiple FE boards. For the barrel, each CC connects to 8 FE boards, with each FE board equipped with two FEDAs (see Figure 5.23 (a)). For the endcap, each CC connects to either 10 or 14 FE boards, with each FE board containing one FEDA (see Figure 5.26 (b)).

The FEDI on CC provides the interface from e-links to an OAT module. Each optical module includes a single channel receiver and a single channel transmitter for optical signals. The command downlink operates at 2.77 Gbps, while the uplink bandwidth supports up to 11.09 Gbps.

In the barrel, 16 FEDA chips on 8 FE boards are aggregated and linked to a single FEDI chip via 346.67 Mbps e-links. In the endcap, 10 to 14 FEDA chips are similarly connected to one FEDI chip, with each e-link operating at 693.33 Mbps. Considering each FEDA chip connecting to 8 readout ASICs in the barrel and 6 or 8 ASICs in the endcap, the resulting data rate per ASIC is up to 43.33 Mbps in the barrel and up to 86.67 Mbps in the endcap. These data rates correspond to a maximum supported hit rate of 8.0×10^4 Hz/cm^2 in the barrel (with an active detector area of ~ 1.28 cm $\times$ 4.4 cm per ASIC) and 2.1×10^5 Hz/cm^2 in the endcap (~ 1.28 cm $\times$ 3.3 cm per ASIC). These supported hit rates are 12 times higher in the barrel and 6 times higher in the endcap than the estimated peak background hit rates (after applying a safety factor of 2), under the most challenging high-luminosity Z-pole operation mode, as shown in Table 5.2.

The distribution of a precise clock to the front-end is a critical requirement for the OTK system. The clocks in the backend system are recovered from the FEDI downlinks, synchronized to the 43.33 MHz frequency bunch crossing rate. An additional key feature of the FEDI is ensuring the precise clock distribution to the front-end system. This is achieved via a high-frequency clock noise filter in the Phase-Locked Loop (PLL) of the FEDI. However, low-frequency clock jitter and potential phase instability, particularly caused by temperature variations or the low-frequency response of the clock chain, will require special attention to ensure optimal system performance.

The FEDI also provides a set of slow control and monitoring features, including I2C master controllers, a Joint Test Action Group (JTAG) master controller, programmable and bidirectional I/O ports, and a memory-like bus master controller with data and address management.

Power is distributed through PAL DC-DC converters. To power both the CC components and the FE boards, two types of DC-DC converters are used: PAL48 (Power at Load for 48 V) and PAL12. As shown in Figures 5.23 (c) and 5.26 (b), long power bus FPCs transmit both 200 V HV and 48 V LV from the end of the barrel or endcap to the CCs. The PAL48 converters on the CC step down the 48 V to 12 V, which, along with the 200 V HV, is then distributed to each individual FE board. Each CC also integrates a PAL12 converter that steps down the 12 V

to either 1.2 V for FEDI and 3.3 V for the OAT.

The power bus FPCs, along with optical fibers, are connected to composite cables that deliver both power and signals from external sources. For each half stave in the barrel, four composite cables are connected to the FPC and four fibers. Similarly, each 1/16 endcap sector uses nine composite cables, with each cable connecting to two power bus FPCs and the corresponding two optical fibers. In total, the OTK barrel requires 880 composite cables, while the OTK endcaps use 288. To improve efficiency and compactness, serial powering is under consideration.

5.3.3 Mechanical and cooling design

Similar to the ITK, the OTK barrel is segmented in the azimuthal direction into structural units known as staves. Each stave is a long structure spanning the entire length (5,680 mm) of the OTK barrel. These staves are directly mounted on the TPC outer barrel — a carbon fiber cylinder integrally molded with a specifically designed support structure — to optimize support for the longer staves while minimizing material usage. The installation of the OTK barrel is illustrated in Figure 5.28 (a).

A pair of assembled OTK endcaps, together with the OTK barrel, form the complete OTK system, as shown in Figure 5.1 (b). The mechanical and cooling design of the OTK is driven by stringent requirements on material budget, structural robustness, and thermal efficiency.

5.3.3.1 Barrel support

The cross section of the internal structure of an OTK barrel stave is shown Figure 5.28 (b). The OTK stave structure can also be divided into three functional units:

- Sensor Modules: Sensors are glued to low-mass PCBs equipped with DC-DC converters, readout ASICs, and other components.
- Support Structure: This structure consists of two layers of 0.3 mm thick carbon fiber facesheets sandwiching a carbon fiber honeycomb core. The transverse edges of the stave are enclosed by side closeouts, which are C-shaped channels made of carbon fiber. These side closeouts are important mechanical interfaces to the global support structures, increasing the stave's stiffness and reducing deformation.
- Cooling Structure: Sensors in the modules are attached to the carbon fiber facesheet using thermal adhesive. The area around the cooling pipes and the honeycomb core is filled with low-mass, high thermal conductivity foam. The carbon fiber facesheet and honeycomb are bonded using an adhesive infused with thermally conductive carbon particulates.

To achieve hermetic coverage, neighboring staves are partially overlapped via the stepped ramp ring mounting structure, as illustrated in Figure 5.28.

Materials The facesheets are constructed from layers of high-modulus unidirectional carbon fiber material combined with cyanate ester resins, designed to meet the overall stiffness

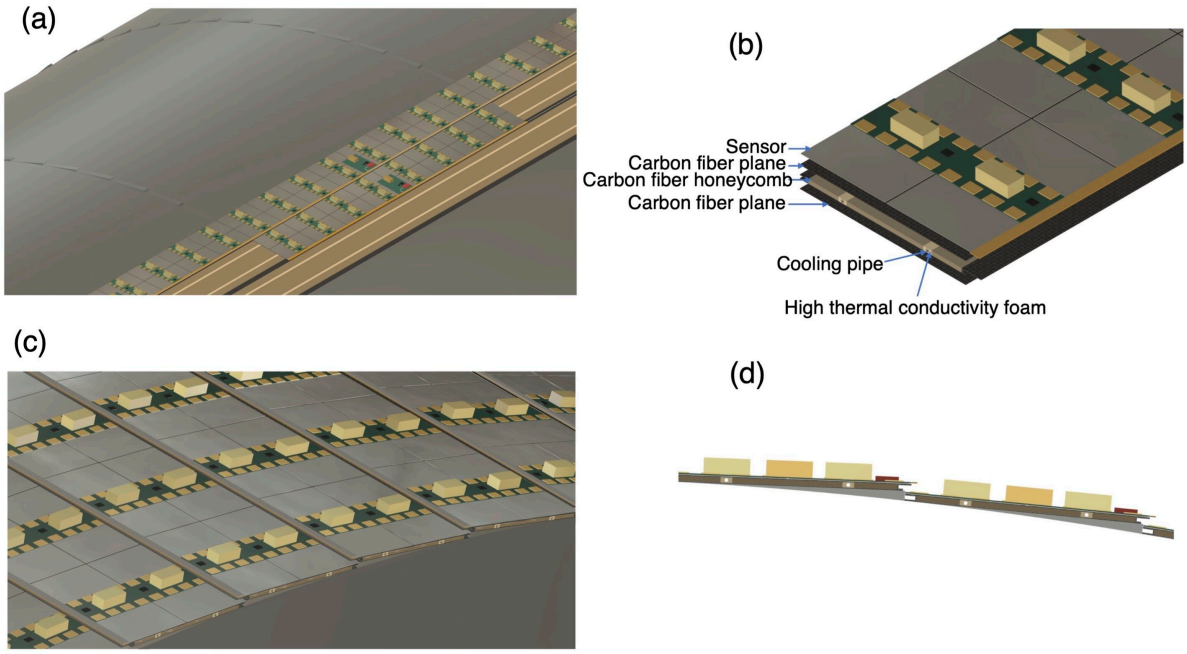


Figure 5.28: (a) Installation of the OTK barrel. Each stave is mounted onto the TPC outer barrel, a carbon fiber cylinder with stepped ramp rings. A lower carbon fiber facesheet (plane) with a honeycomb core is first attached, followed by the insertion of two ∼ 6 m cooling pipes sealed with high-conductivity foam. Finally, eight ∼ 0.7 m ladders are glued on top to complete the stave assembly. (b) Structure of the OTK barrel stave. Each stave contains sensor modules, top and bottom carbon fiber planes sandwiching a carbon fiber honeycomb core. Two cooling pipes are inserted into the honeycomb grooves, sealed with high-conductivity foam, and the transverse edges of each stave are enclosed by side closeouts. (c) Staggered structure of OTK staves and (d) cross section of two neighboring staves. Neighboring staves are staggered and partially superimposed to ensure the detector's hermeticity.

requirements for local support and the thermal demands of conducting heat generated in the modules to the cooling structures embedded in the core.

The honeycomb core is made of lightweight, high-performance carbon fiber material. It maintains the separation of the facesheets to ensure good bending stiffness and provides a sufficiently flat and robust surface for adhesive attachment of the modules without requiring excessively thick glue layers.

The interface between the cooling tubes and the facesheets is formed using thermally conductive carbon foam, such as Allcomp K9. Water with titanium cooling pipes (tube wall thickness of 0.2 mm and a diameter of 5 mm) has been selected as the baseline cooling medium for the OTK.

Table 5.10 lists the estimated contributions of the OTK stave to the material budget. The overall estimated material budget for a stave is 1.6% X_0. The overlap area between neighboring staves accounts for 8% of the stave area, corresponding to 6% of the stave materials. With 110 staves, the total weight of the OTK barrel is ∼ 300 kg.

Structural characterization The stiffness of the stave is provided by the carbon fiber

Table 5.10: Estimation of the OTK stave material contributions. The wall thickness of the cooling tubes, averaged over the entire endcap area and labeled with "†", is ~ 60 μm.

Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	PCB metal layers	Cu		1.436	0.200
	PCB Insulating layers	Polyimide		28.41	0.070
	Sensor	Silicon	300	9.369	0.320
	Glue		100	44.37	0.023
	Other electronics				0.100
Structure	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Cooling tube wall	Titanium	200†	3.560	0.169
	Cooling fluid	Water		35.76	0.105
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	6000	186	0.322
	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Glue	Cyanate ester resin	200	44.37	0.045
Total					1.584

facesheets, honeycomb, and C-shaped carbon fiber channels. Similar to OTK stave, the maximum sag of the OTK stave under its own weight and the first natural frequency are used to estimate the displacement and stability of the sensors' positions.

A finite element model of an OTK stave for structural analysis was created, similar to the one used for the ITK stave. Based on this model, structural analyses were performed to evaluate the maximum deformation and the first natural frequency. The results indicate a sag of 135 μm for the OTK stave, with a corresponding first natural frequency of 76 Hz.

Thermal characterization According to the specifications for the OTK sensor, the cooling design must meet the following requirements:

- The overall sensor operating temperature should not exceed 30 °C.
- The temperature uniformity across a single sensor should be maintained within 5 °C.

Based on numerical simulations for different pipe diameters, and considering cooling system simplification, a pipe with an inner diameter of 5 mm using water cooling was selected as the baseline for the OTK stave cooling.

A water cooling fluid structure coupled finite element model was established to study the temperature distribution along the entire longitudinal length of the stave, considering a specific water cooling flow rate. The following configurations were used in the model:

- The detector dissipates heat at a flux of 300 mW/cm^2, simply assumed to be uniformly distributed across the sensors.
- Cooling water enters the stave with a flow velocity of 2 m/s and a temperature of 5 °C.
- Natural convection and radiative heat transfer were not considered.

Figure 5.29 shows the simulation result with both pipe inlets placed on the same side. The temperature gradient along the full stave length is controlled within 8.6 °C, and the maximum temperature remains below 14.6 °, satisfying the preliminary requirement. The temperature variation across a single sensor is found to be below 3 °C, which is within the specified limit.

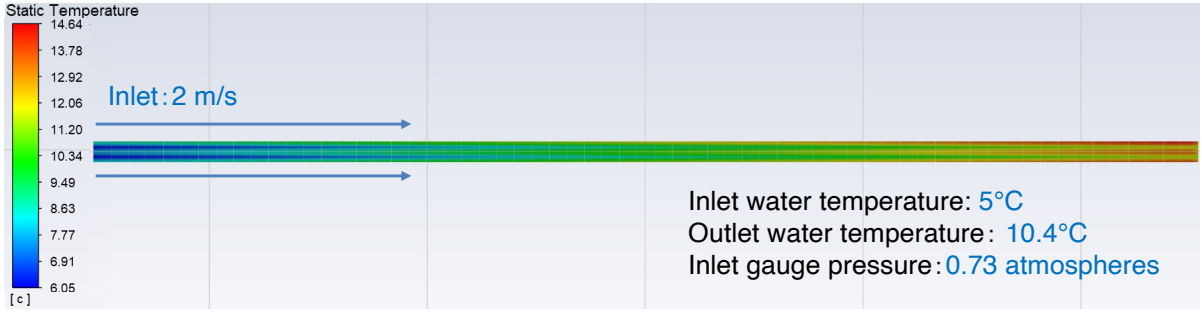


Figure 5.29: Simulation result of water cooling for the OTK stave, with a flow velocity of 2 m/s and a two-pipe inlet temperature of 5 °C. The temperature across the stave remains below 14.6 °C, and the temperature gradient along the stave is within 8.6 °C.

5.3.3.2 Endcap support

Figure 5.30 (a) illustrates the components of the OTK endcap, including a layer of sensor modules, a layer of cooling plates, connection rods, an inner structural ring, and an outer structural ring. To simplify the assembly and testing processes, the endcap is segmented into 16 sectors, each with its own dedicated detection, mechanical, and cooling structures. Figure 5.30 (b) shows a detailed view of one OTK sector, with main components summarized as follows:

- Sensor Modules: The sensors are glued to low-mass PCBs equipped with DC-DC converters, readout ASICs, and other components.
- Cooling Plate:
  - The cooling plate consists of two layers of high stiffness carbon fiber facesheets sandwiching a low-mass, carbon fiber honeycomb core with embedded serpentine cooling loops, sealed with high thermal conductivity foam. The composite pyrolytic graphite foam is the same as the one used in the OTK barrel stave.
  - The edges of the sector are enclosed by side closeouts, which interface with inlets and outlets of cooling loops. These closeouts, made of carbon fiber, serve as critical mechanical interfaces to the overall support structures, enhancing the sector's stiffness.
  - The sensors in the modules are attached to the cooling plate (more accurately, the carbon fiber facesheet) using thermal adhesive.

Sixteen composite rods are installed along the edges to join adjacent sectors, forming the complete OTK endcap disk. Figure 5.30 (c) illustrates the mechanical interface between neighboring sectors, where each composite rod extends from the inner to outer ring, connecting adjacent cooling plates. To reinforce the structural integrity of the assembly, inner and outer mounting rings are secured to the disk's perimeter, enhancing the connections between neighboring sectors. Together with the rods, these rings enhance the overall stiffness of the endcap and absorb induced stress. Additionally, the outer ring also serves as a routing structure for the cooling lines from the cooling plate.

Materials The two facesheets of the cooling plate for each 1/16 sector are constructed from

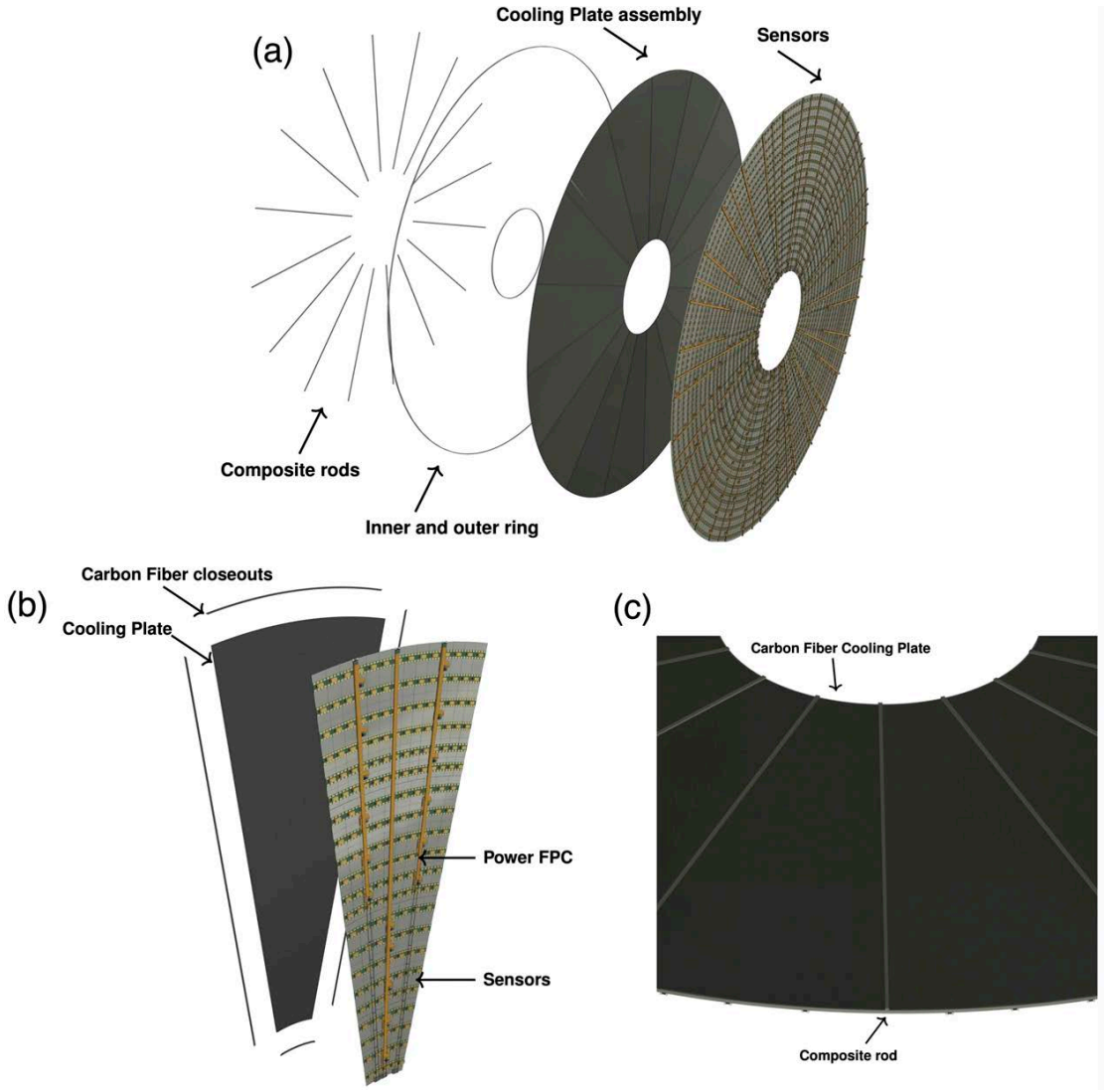


Figure 5.30: (a) Structure of the OTK endcap. It consists of a layer of sensor modules, a layer of cooling plates, connection rods, an inner structural ring, and an outer structural ring. (b) Structure of the OTK 1/16 sector, and (c) mechanical connection between sectors. Each sector consists of a sensor module layer and a cooling plate, enclosed by side closeouts. Sixteen composite rods are installed along the edges to join adjacent sectors, while inner and outer mounting rings are attached to the disk perimeter to reinforce inter-sector connections.

layers of high-modulus unidirectional carbon fiber material combined with cyanate ester resins. The interface between the cooling tubes and the facesheets is formed using thermally conductive carbon foam, such as Allcomp K9. Water circulating through cooling loops within the foam serves as the cooling medium for the OTK endcap.

The rods, inner ring, and outer ring, which connects sectors to an endcap disk, must be made from stiff materials. The rods are constructed from carbon fiber. For the inner ring and the outer ring, the primary candidate materials are the high-performance PEEK polymer and Torlon polyamide-imide technology.

Table 5.11 lists the estimated contributions of each OTK endcap disk to the material budget.

The overall estimated material budget is 1.4% X_0.

Table 5.11: Estimation of the OTK endcap material contributions. The wall thickness of the cooling tubes, averaged over the entire endcap area and labeled with "†", is ~ 60 μm.

Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	PCB metal layers	Cu		1.436	0.200
	PCB Insulating layers	Polyimide		28.41	0.070
	Sensor	Silicon	300	9.369	0.320
	Glue		100	44.37	0.023
	Other electronics				0.100
Structure	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Cooling tube wall	Titanium	200†	3.560	0.168
	Cooling fluid	Water		35.76	0.054
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	3000	186	0.161
	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Glue	Cyanate ester resin	200	44.37	0.045
Total					1.371

Structural characterization The stiffness of the OTK endcap is primarily provided by the carbon fiber facesheets, honeycomb, and frames (including closeouts, rods, inner ring, and outer ring).

Structural analyses similar to those performed for the ITK endcap, were conducted to evaluate the maximum deformation for the OTK endcap in both the nominal and flat-lying positions. The results indicate a negligible sag ($< 1\,\mu$m) in the nominal position, and a maximum of 1.4 mm in the flat-lying position. The OTK endcap is sufficiently stiff for both installation and operation.

Thermal characterization Similar cooling strategy to that of the OTK barrel is chosen as the baseline in the endcap, with the same water flow velocity and inlet water temperature. Similar to the ITK endcaps, the cooling loops for the OTK endcap are specifically designed to achieve a small temperature gradient across the entire surface of the endcap sensor plane. Figure 5.31 (a) shows the designed layout of the cooling loops for a 1/16 OTK endcap sector, consisting of five closed loops arranged across 40 coil layers. The inner diameter of the cooling coops is chosen to be 2.6 mm, with a wall thickness of 0.2 mm.

In the thermal simulations, the thermal conductivity of the cooling water, cooling pipes, graphite foam, carbon fiber face sheets, and detector sensors were taken into account.

Based on these configurations, Figure 5.31 (b) shows the simulation results for the temperature distributions of a 1/16 OTK endcap sector. As shown, the temperature of all OTK sensors remains below 15 °C. The maximum temperature difference across the sensor plane is below 8 °C, and the temperature difference across a single sensor is below 4 °C. Comparing the sensor operation limit of 30 °C and the temperature uniformity across a single sensor (< 5 °C), the OTK endcap cooling design meets the detector's requirements.

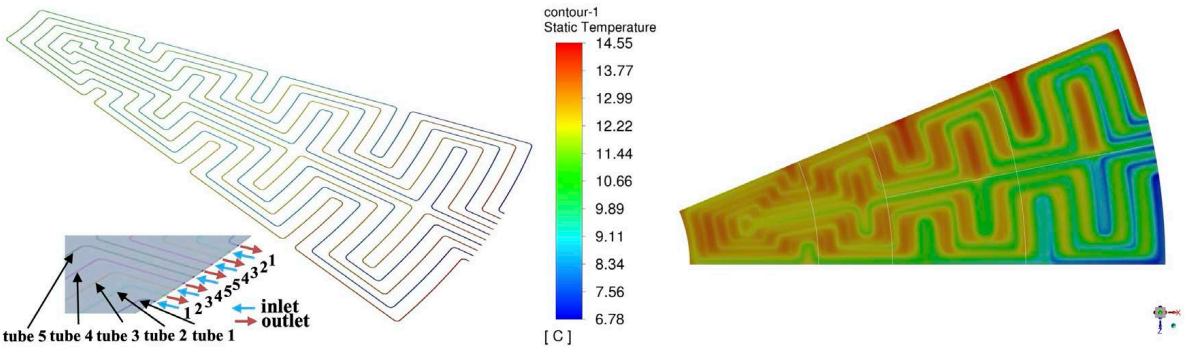


Figure 5.31: (a) Schematic of the 40 coil layer cooling loops designed for the 1/16 OTK endcap sector, featuring five closed loops arranged radially across the layers. (b) Simulated sensor temperature distributions for the 1/16 OTK endcap sector.

5.3.4 AC-LGAD sensor

Low Gain Avalanche Detector (LGAD) technology has been selected for use in the ATLAS High Granularity Timing Detector (HGTD) [11] and the CMS endcap timing layer [12] to mitigate pile-up effects in the HL-LHC experiment. LGAD sensors from several vendors have demonstrated timing resolutions of around 50 ps, both before and after irradiation. In particular, the LGAD developed by the Institute of High Energy Physics (IHEP) achieves a collected charge exceeding 15 fC and a timing resolution better than 35 ps before irradiation, and a charge of 4 fC with a timing resolution better than 50 ps after irradiation at a fluence of 2.5×10^{15} n_{eq}/cm^2 [13, 14].

However, despite their excellent timing capabilities, conventional LGADs face limitations in spatial resolution due to pixel size constraints. Furthermore, the presence of Junction Termination Extension (JTE) and P-stop structures between pixels introduces dead zones that reduce detection efficiency. To overcome these challenges and minimize the inactive area, AC-coupled LGADs (AC-LGADs) is being developed as an advanced evolution of LGAD technology.

In AC-LGADs, AC coupling electrodes and a dielectric layer are placed above the n+ layer of the LGAD, as illustrated in Figure 5.32. When a particle passes through the detector, the induced charge is distributed among electrodes near the impact position. By analyzing the signals collected from these adjacent electrodes, the particle's impact position can be precisely reconstructed. This enables AC-LGADs to deliver both high-precision timing and spatial measurements while achieving a nearly 100% fill factor, significantly enhancing their efficiency and performance in particle detection applications.

AC-LGADs have been extensively investigated by many research institutes and companies including National Institute for Nuclear Physics (INFN), Fondazione Bruno Kessler (FBK), Brookhaven National Laboratory (BNL), Hamamatsu (HPK), IHEP, and others [15–18]. These detectors enable four-dimensional (4D) tracking by combining precise spatial and temporal measurements, and can also serve as ToF detectors [19]. Specifically, AC-LGADs with strip-

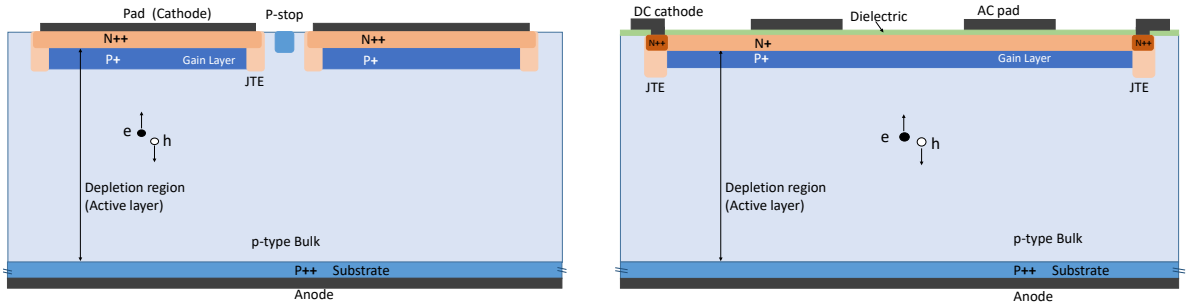


Figure 5.32: Structures of (a) standard LGAD and (b) AC-LGAD. In the standard LGAD (DC-LGAD), the readout electrode (pad) connects to the n++ layer, with Junction Termination Extension (JTE) and P-stop structures creating dead zones. In contrast, the AC-LGAD uses a thin dielectric layer to separate the metal AC-coupling electrodes from the n+ layer, achieving a nearly 100% fill factor.

shaped readout electrodes reduce the number of readout channels while maintaining exceptional spatial resolution along the bending direction [20], which has been adopted as the baseline design for the OTK.

Extensive R&D efforts have been undertaken at IHEP to advance the development of AC-LGADs. The process and structural parameters of these devices have been extensively simulated by using TCAD software, exploring the impact of various process parameters and structural configurations on detector performance.

5.3.4.1 AC-LGAD simulation

Simulations of AC-LGAD devices were performed using the TCAD software, incorporating all key structural components such as the n+ resistance layer dose, AC coupling dielectric material and thickness, and metal pad ratio. The simulated model structure is illustrated in Figure 5.33. These simulations focus on AC-LGAD specific structures that differ from standard LGADs and have a significant impact on both timing and spatial resolution.

Key findings include:

- **Dielectric material and thickness:** Variations in the dielectric material and its thickness significantly influence spatial performance (Figure 5.34). Silicon nitride, with its higher dielectric constant compared to silicon oxide, enhances capacitive coupling when the thickness remains the same. As a result, AC-LGADs using high-dielectric-constant materials such as silicon nitride for the AC coupling layer can achieve improved spatial resolution.
- **n+ layer dose:** The n+ layer dose affects the charge sharing between electrodes, signal shape, and spatial resolution. As the n+ dose decreases, the resistivity of the layer increases, resulting in more signal charge being collected by the electrode closest to the particle impact position. The signal also changes more rapidly with the impact position,

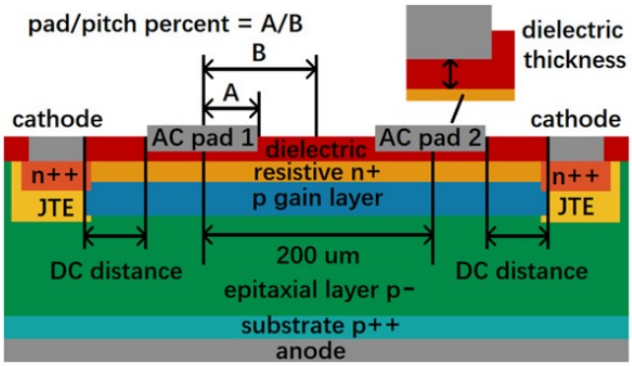


Figure 5.33: Sketch of the AC-LGAD simulation model with two AC pads, incorporating key structural components such as the n+ resistance layer dose, AC coupling dielectric material and thickness, and the metal pad ratio.

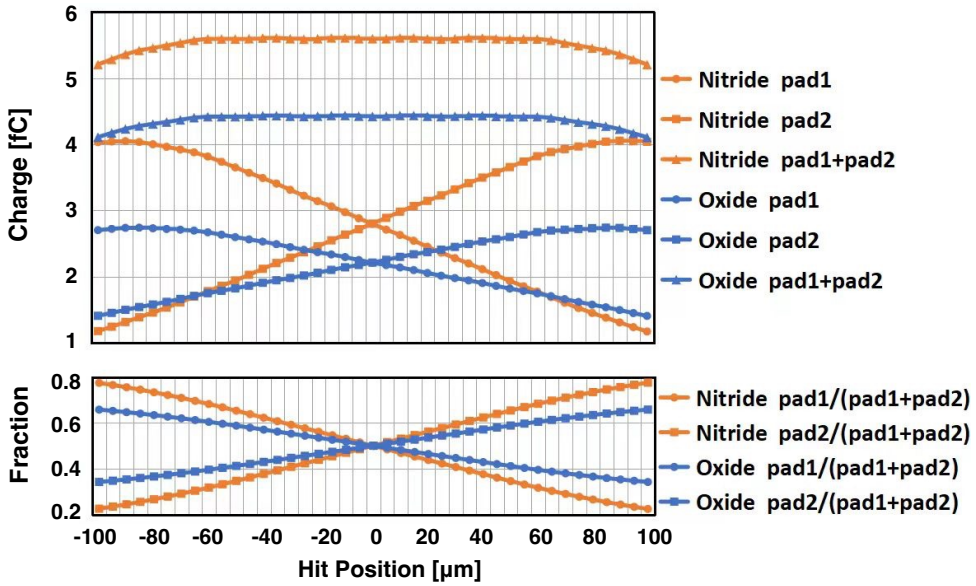


Figure 5.34: Charge collection of two neighboring pads (pad1 and pad2) as functions of hit position for two different dielectric materials: oxide (blue curve) and nitride (orange curve).

leading to improved spatial resolution [21].

- **Metal pad pitch size and other structural parameters:** Additional structural parameters, such as the metal pad pitch size, were also simulated to evaluate their effects on overall detector performance. More details are provided in Ref. [21].

Based on these findings, various R&D prototypes were fabricated to further explore AC-LGAD performance. Dedicated testing systems were designed and implemented to study the timing and spatial resolutions of the developed devices.

5.3.4.2 Testing setup

The testing platforms, utilizing Transient Current Technique (TCT) laser scans and Beta tests, are illustrated in Figure 5.35. These setups comprise readout boards, amplifiers, oscillo-

scopes (Teledyne LeCroy HDO9204 with 2 GHz bandwidth and 20 G/s sampling rate), laser sources, and Beta sources. The AC-LGAD electrodes were wire-bonded to a four-channel readout board, which was designed according to the single-channel readout board developed by the University of California Santa Cruz [22]. Signals from the AC-LGAD electrodes were processed through a two-stage preamplifier system and subsequently recorded by the oscilloscope.

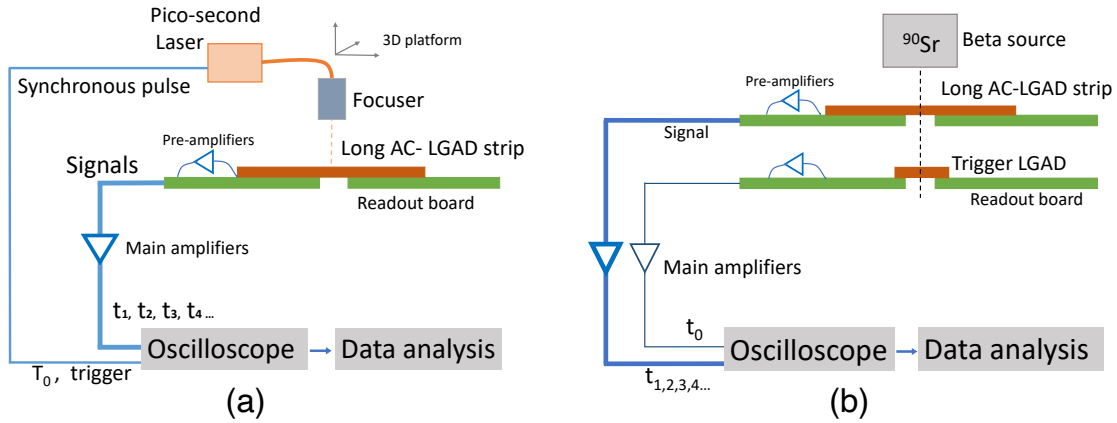


Figure 5.35: The schematics of the (a) TCT testing platform and (b) Beta testing platform. Each setup includes either laser or beta source, readout board, amplifiers, and oscilloscope. AC-LGAD electrodes are wire-bonded to a four-channel readout board, with signals processed through two-stage preamplifiers and recorded by the oscilloscope.

To evaluate the timing resolution of the Device Under Test (DUT), a trigger LGAD with a timing performance (σ_{trigger}) of 28.5 ps was employed as the reference device. Signals from both the trigger LGAD and the AC-LGAD strip were recorded, and the time difference of flight for a Minimum Ionizing Particle (MIP) between the two devices was determined and defined as ΔT. The standard deviation of ΔT ($\sigma_{\Delta T}$) was then calculated. Using this value, the timing resolution of the DUT sensor can be derived using the following equation:

$$\sigma_{\text{DUT}} = \sqrt{\sigma_{\Delta T}^2 - \sigma_{\text{trigger}}^2} \tag{5.1}$$

Transient Current Technique (TCT) laser scans were employed for highly accurate position resolution measurements. In this setup, a picosecond laser pulse with a wavelength of 1,064 nm strikes AC-LGAD sensor at a frequency of 20 MHz using a focuser. The focuser, mounted on a precision positioning table, ensures movement accuracy better than 1 µm. The laser systematically scans across the AC-LGAD sensor in µm steps. At each position, 1,000 waveforms are recorded before advancing to the next point. By analyzing the signals collected from electrodes near the laser hit position, the impact position is reconstructed. This enables the evaluation of spatial resolution through laser tests. The spatial resolution is defined as the standard deviation (σ) of the difference between the laser's actual position and the reconstructed position.

5.3.4.3 Strip AC-LGAD prototype

A strip AC-LGAD prototype has been designed by IHEP [18]. It comprises strip electrodes, a dielectric layer, Direct Current (DC) electrodes, an n+ layer, a p+ layer, a p-type bulk, a p++ layer, and a backside aluminum anode. Figure 5.36 shows its detailed layout and schematics. It has a total thickness of 775 μm, includes a 50 μm p-type epitaxial layer (active layer). The length of the strip electrodes is 5.65 mm. Three pitch sizes of 250 μm, 200 μm, and 150 μm were designed, with the width of the strip metal electrodes being 100 μm.

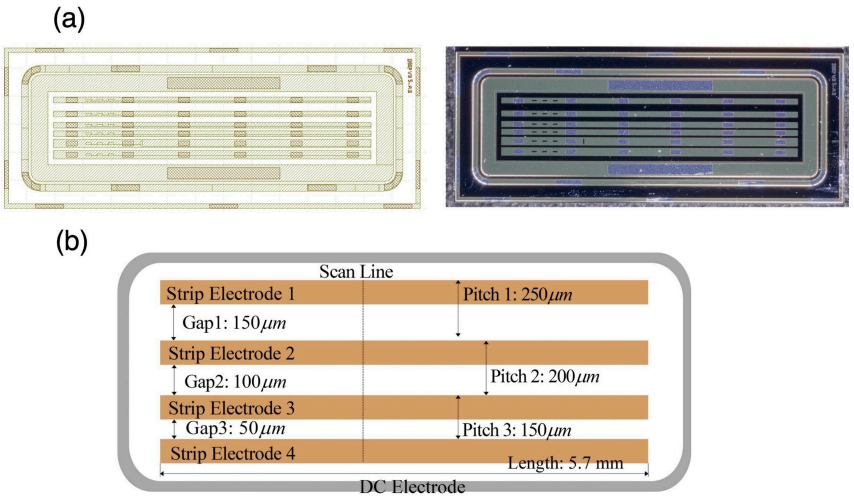


Figure 5.36: (a) The strip AC-LGAD layout and prototype, and (b) the schematic structure of the AC-LGAD prototype. The length of the strip electrodes is 5.65 mm, with three pitch sizes of 250 μm, 200 μm, and 150 μm. The width of the strip metal electrodes is 100 μm.

The breakdown voltage of the device is 385 V, with a leakage current on the order of 10 nA. The capacitance value is 28.9 pF when fully depleted. The gain layer depletion voltage (V_{gl}) is 21.5 V, while the full depletion voltage (V_{fd}) of the sensor is 34.8 V. The coupling capacitance between the strip electrodes and the DC electrode/n+ layer is measured to be 170 ± 0.2 pF.

Timing performance from Beta testing The timing resolution of the sensor was evaluated using a ^{90}Sr beta source, where a calibrated LGAD (trigger LGAD) was placed above the AC-LGAD strip sensor and serves as the timing reference. The ^{90}Sr beta source was positioned above the trigger LGAD to provide a stream of minimum ionizing particles.

Timing signals from the trigger LGAD and the AC-LGAD strip sensor were recorded. The time difference, denoted as ΔT, was calculated as the difference between the signal arrival time of the trigger LGAD and that of the AC-LGAD strip sensor:

$$\Delta T = T_{\text{trigger}} - \frac{\sum_i a_i^2 T_i}{\sum_i a_i^2} \tag{5.2}$$

where T_{trigger} is the arrival time measured by the trigger LGAD, while T_i and a_i are the arrival time and signal amplitude from strip electrode $i = 1, 2, 3$ of the AC-LGAD sensor, respectively. This amplitude weighting method enhances the contribution from the electrode closest to the particle

hit position, effectively reducing noise and improving the timing resolution. The measured standard deviation of the time difference is $\sigma_{\Delta T} = 47.1$ ps. Considering the timing resolution of the trigger LGAD is $\sigma_{\text{trigger}} = 28.5$ ps, the timing resolution of the AC-LGAD strip sensor is calculated using Equation 5.1 and found to be $\sigma_{\text{AC-LGAD}} = 37.6$ ps.

Spatial resolution The TCT was used to study the spatial resolution of the prototype. When a focused laser pulse hits the sensor surface, the amplitude of the induced signal varies with the distance from the electrodes. This causes variations in the collected charge across the electrodes, which can be used for precise position reconstruction.

The position reconstruction method relies on the relative signal amplitudes recorded by the two strip electrodes nearest to the laser hit position. For example, when the laser or a particle hits the region between electrodes 1 and 2 (referred to as "gap 1" in Figure 5.36 (b)), the signal amplitudes on these two electrodes vary as a function of the hit location. The reconstructed hit position is characterized the amplitude ratio $R = a_2/(a_1 + a_2)$.

To obtain the spatial resolution, 1,000 waveforms were recorded for each laser hit position, resulting in 1,000 reconstructed positions per scan point. The difference between the reconstructed and the actual laser hit positions was computed for each event. For each gap region (e.g., gap 1), these differences were collected and plotted as a histogram. The standard deviation of the fitted distribution was used to estimate the device's spatial resolution.

Figure 5.37 shows the differences between the reconstructed and true hit positions for three pad-pitch sizes. The spatial resolutions for the AC-LGAD strip sensor with pitch sizes of 250 µm, 200 µm, and 150 µm are found to be 12.8 µm, 10.9 µm, and 8.3 µm, respectively.

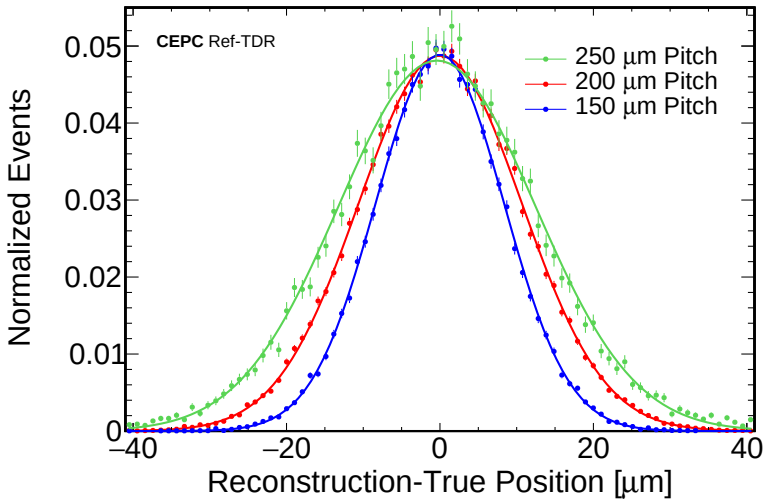


Figure 5.37: Distributions of difference in reconstructed and true hit positions for strip LGAD prototype with different pad-pitch sizes from TCT laser setup.

Summary Results from the 5.65 mm strip sensor prototype demonstrate a timing resolution of 37.6 ps and a spatial resolution of 8.3 µm (based on laser test with a strip pitch of 150 µm), fulfilling the performance requirements of the OTK system. This shows a great potential for the AC-LGAD strip as a promising candidate for 4D trackers in future particle physics experiments

such as the CEPC. However, further studies are necessary to evaluate the timing and spatial performance of the longer AC-LGAD strip sensors as required by the OTK layout. To optimize the design, an isolated structure will be introduced into the AC-LGAD configuration to reduce sensor capacitance. Careful attention will be paid to the potential impact of this modification on spatial resolution. These refinements aim to ensure the sensor's compliance with the stringent requirements of the OTK system.

5.3.5 LGAD readout ASIC

The LGAD readout ASIC, LGAD Timing and Readout Integrated Chip (LATRIC), is designed to achieve both high time resolution for precise timing and good charge resolution for accurate position reconstruction, to fully exploit the sensor's outstanding performance. This section outlines the performance requirements, design considerations, and recent prototype testing of LATRIC.

5.3.5.1 LATRIC architecture and requirements

LATRIC will feature 128 readout channels. The pitch between neighboring readout channels must be less than 100 μm to match the pitch of the LGAD strips. Each channel in LATRIC includes a preamplifier [23], a discriminator, and TDC for measuring both the Time-of-arrival (TOA) and Time-over-threshold (TOT), as illustrated in Figure 5.38. The ASIC also integrates common digital components, including a clock generator, data alignment logic, slow control configuration, and data transmission interfaces.

The requirements of the ASIC are driven by the electrical connections, targeted time resolution, and power constraint, etc. A summary of the final configuration for the LATRIC ASIC is presented in Table 5.12.

The time resolution of the OTK system depends on both the LGAD sensor and LATRIC. As the LGAD sensor exhibits a jitter of approximately 40 ps, to achieve an overall time resolution of 50 ps per hit, the contribution of LATRIC must be kept below 30 ps. Timing resolution is mostly limited by jitter and time walk. Given the small signal amplitude from the LGAD sensor, the analog front-end circuits — especially the preamplifier and discriminator — dominate the electronics' jitter contribution and are therefore critical for achieving OTK's precision timing performance. Time walk effects can be mitigated by applying corrections based on the correlation between TOA variations and TOT values.

The TOT serves as a charge indicator, as the signal amplitude is correlated with the duration of the signal above a specific threshold. Charge resolution depends on the intrinsic variations in the TOT width as well as time resolution. The Most Probable Value (MPV) of the charge collected from the LGAD sensor for a MIP is approximately 16 fC. Considering the charge sharing with adjacent strips, the expected operating charge range is 8–50 fC.

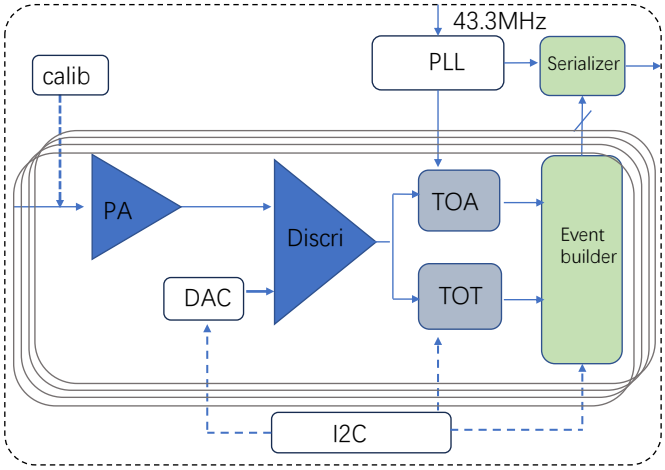


Figure 5.38: Global architecture of the LATRIC ASIC. The signal from the sensor is first amplified by the preamplifier (PA), and then discriminated through the discriminator (Discri) using a threshold provided by a Digital-to-Analog Converter (DAC). The Time-To-Digital Converter (TDC) measures both the Time-of-arrival (TOA) and the Time-over-threshold (TOT). A Phase-Locked Loop (PLL) supplies the reference clock, and the data are transmitted via a serializer. An Inter-Integrated Circuit (I2C) interface is implemented to configure key parameters of the DAC, TDC, and the event builder.

Table 5.12: Configuration for the LATRIC ASIC (assuming a detector capacitance C_d = 8 pF)

Parameter	Value
Chip size	1.2 cm × 0.5 cm
Voltage	1.2 V
Number of channels	128
Channel pitch	< 100 μm
Single channel noise (ENC)	0.8 fC
Cross-talk	< 10%
Maximum jitter	30 ps at 16 fC
Minimum threshold	4 fC
Dynamic range	8 fC–50 fC
TDC conversion time	< 23 ns
Power dissipation per ASIC	1.5 W (for occupancy < 1%)
Data size per fired channel	48 bits
e-link driver bandwidth	43.33 Mbps or 86.67 Mbps
Technology node	55 nm

5.3.5.2 Single-channel readout electronics

This section presents key considerations in the designs of single-channel electronics — preamplifier, discriminator, and TDC — to achieve high performance in terms of compact area, low power consumption, and high precision.

Preamplifier and Discriminator As illustrated in Figure 5.39 (a), the preamplifier comprises two stages: a cascade amplifier (M1 and M2) as the first stage and a source follower (M3)

as the second stage. The gain and bandwidth of the preamplifier depend on the transconductance (*Gm*) of transistor M1 and *Rf*.

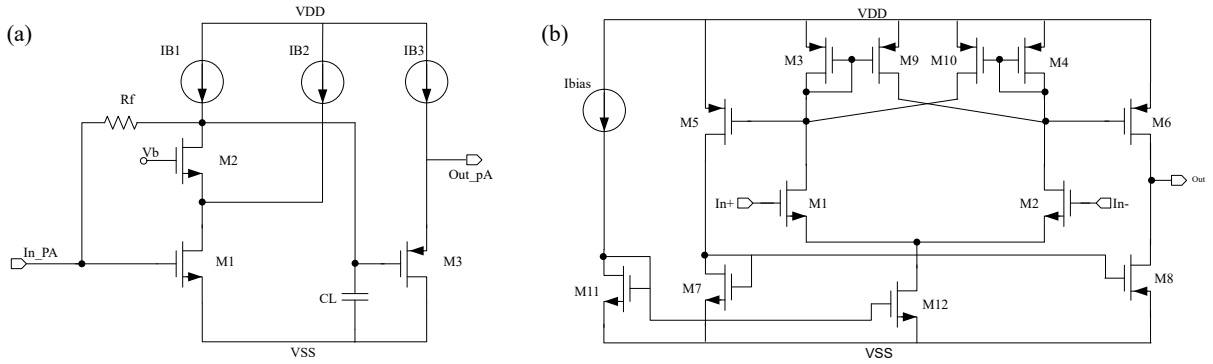


Figure 5.39: Schematic of the (a) preamplifier and (b) discriminator in LATRIC. The preamplifier is a transimpedance amplifier, where the feedback resistor *Rf* converts the input current to a voltage, followed by a buffer stage. The discriminator consists of two stages, with transistors M9 and M10 used for hysteresis regulation.

The discriminator comprises three stages of fully differential amplifiers, a comparator, and an internal buffer. The three amplifier stages receive small input pulses and amplify them to generate larger pulses suitable for the comparator. As illustrated in Figure 5.39 (b), the comparator consists of two stages. The first stage is a high-gain common-source differential amplifier using transistors M1 and M2. The second stage converts the differential output of the first stage into a single-ended signal. The discriminator threshold is connected to the inverting input and is set by an internal 10-bit DAC.

TDC The schematic of the TDC core [24] is illustrated in Figure 5.40. The LATRIC design faces two primary challenges: the limited area per channel and the need to achieve both time and charge measurements while maintaining low power consumption. Additionally, the pitch of the LGAD strips is only 100 µm, which necessitates that the height of the single-channel circuitry must also be less than 100 µm.

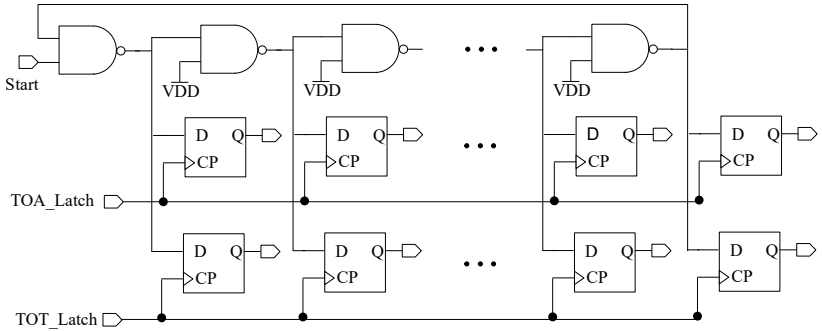


Figure 5.40: Basic structure of the TDC design based on a single multi-tapped delay line. The delay line consists of several NAND gates. The Time of Arrival (TOA) and Time Over Threshold (TOT) are measured independently. The states are latched upon the arrival of a rising or falling edge.

To address these constraints within a smaller area, a single delay line is employed to simultaneously measure the time of TOA and TOT, with each delay cell providing a delay of 30 ps. Flip-flops record the times of the signal's rising edge, falling edge, and the reference clock's rising edge, storing these values sequentially in registers. The chip employs a single delay line without a Delay-Locked Loop (DLL), using a cyclic structure to minimize the number of delay cells.

The delay of the delay line is affected by process variations, power supply voltage, and temperature. Therefore, a pulse self-calibration scheme is essential to compensate for these variations. This calibration is performed periodically using the system clock to measure and adjust the delay chain. The TDC output data width comprises 8 bits for TOT, 9 bits for TOA, 1 bit for hit flag, 8 bits for calibration, 7 bits for channel identification (128 channels), 8 bits for bunch ID, and 7 bits for chip ID, resulting in a total of up to 48 bits.

5.3.5.3 Digital blocks and data handling

The digital blocks complement the analog front-end circuitry and operate at the full chip level to perform precise clock distribution, robust configuration, and ensure efficient data readout across all channels.

Clock generation unit The clock generator unit supplies clock signals to all functional blocks within the LATRIC chip. The oscillator in the PLL operates at 1.39 GHz, the highest frequency, and receives a 43.33 MHz clock as input. Effective clock distribution, particularly minimizing skew and jitter, is a critical design challenge. A binary tree, the most common and conservative clock distribution scheme, is planned for implementation. In this scheme, the clock signal branches from a central point to all destination nodes. The 7-stage tree structure ensures a balanced clock distribution network, with equal path lengths from the clock source to each channel. Buffers are added along the transmission path to maintain the quality of the clock signal.

Data readout process The TDC data from each channel is stored in a circular buffer. A scrambler is employed, and a Pseudo-Random Binary Sequence (PRBS) block is incorporated for testing purposes. The LATRIC chip supports three serial output data rates, depending on the anticipated occupancy of the chip.

The serial output data rate is configurable at either 43.33 Mbps or 86.67 Mbps for each LATRIC chip. Forward error correction schemes, such as 8b/10b or 64b/66b encoding, are applied to the serial output.

Slow control Slow control mechanisms are implemented to configure the registers within the chip. The chip includes various registers that manage different functions and operating modes, such as amplifier gain settings, test modes, data acquisition modes, and calibration controls. An I2C link is integrated into the ASIC and is configured through the I2C master in the FEDI chip.

Monitoring The ASIC monitoring primarily focuses on operational temperature, supply voltage, and the leakage current of the sensors. Although the ASIC itself is not highly sensitive to temperature, the performance of the LGAD sensors is temperature-dependent. Temperature monitoring via the ASIC channels also enables the detection of cooling failures. Voltage monitoring within the chip is used to assess functionality and can trigger the shutdown of malfunctioning modules when necessary.

5.3.5.4 Prototype

A prototype chip, Fast Photomultiplier Readout Chip (FPMROC), has been designed, incorporating eight complete readout channels. Each channel consists of a low-noise preamplifier, a discriminator, and a TDC for measuring both the TOA and TOT [24]. An integrated data event builder manages the data flow, while fast data serialization and a data driver handle the output. Peripheral circuits include DACs for calibration and threshold adjustment, a PLL to generate high-quality clocks, and a Serial Peripheral Interface (SPI) module for slow control. Additionally, the prototype features a charge injection circuit for testing and calibration purposes.

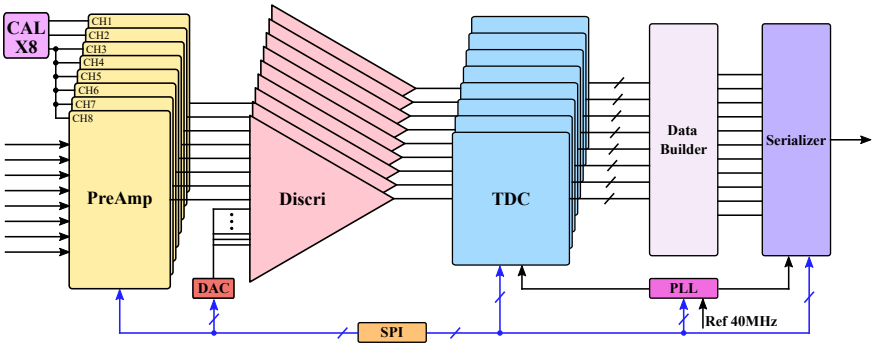


Figure 5.41: Block diagram of the FPMROC. It integrates eight channel circuits, including preamplifier, discriminator, TDC, event builder, and serializer. The TDC measures the Time of Arrival (TOA) and Time Over Threshold (TOT) of signals from the Microchannel Plate Photomultiplier Tube (MCP-PMT). Chip configuration is realized via Serial Peripheral Interface (SPI).

Figure 5.41 illustrates the block diagram of the FPMROC ASIC. Eight channels collectively employ a data event builder for buffering, framing, scrambling, and encoding parallel data from multiple channels. The ASIC incorporates a serializer for off-chip data transmission at a rate of 10.24 Gbps, as well as a low-jitter LC-based PLL to generate 5.12 GHz and 40 MHz clocks for the serializer and TDCs, respectively. Additionally, an SPI interface is integrated to provide configurations of up to 200 bits.

Testing of this chip was successfully completed at the end of 2024. Further details on the design and performance of FPMROC can be found in Ref. [25]. In the second half of 2024, a new readout ASIC scheme was designed and submitted for wafer production in April 2025, along with the design of the new ASIC test system. This ASIC is intended to validate the performance

of its key components — including the preamplifier, discriminator, and TDC modules — as well as to finalize the design of the ASIC test system. Performance testing, including radiation hardness testing for each component, is expected to be completed by the end of 2025. Further R&D plan are covered in Section 5.3.6.

5.3.6 Future plan

Significant R&D efforts are required to meet the design requirements of the OTK detector. These include major advancements in AC-LGAD sensor area scaling, substantial progress in ASIC development, and system-level prototyping of mechanical structures and cooling systems.

5.3.6.1 Development of AC-LGAD strip sensor

The development of high-performance long strip sensors is still challenging as the impact of strip length on both timing and spatial resolution is not fully understood. It is one of the main focus of future R&D. Figure 5.43 shows a detailed tape-out plan for the LGAD strip sensors and their testing schedule, with key elements summarized below.

Sensor Development and Testing Using TCAD tools, models of AC-LGAD with various strip lengths and process parameters will be developed to study the impact of strip length on signal quality and to optimize spatial and timing performance of strip AC-LGAD. Prototypes with strip lengths of 1 cm, 2 cm, and 4 cm will be fabricated and tested. Meanwhile, sensors with one strip length will also have prototypes with different n+ dose and coupled capacitance. Testing will cover current-voltage, capacitance-voltage, spatial resolution, and timing performance, with subsequent radiation and beam tests.

Design Adjustments Based on test results, the strip length and pitch size may be modified to balance performance, yield, and readout requirements. One of our backup plans includes reducing the strip length from 4 cm to 2 cm and increasing the pitch size from 100 μm to 200 μm to maintain similar readout channels and power consumption. The final decision will be made based on the performance and yield.

5.3.6.2 Development of LGAD readout ASIC

The development timeline of the LGAD readout ASIC (LATRIC) is closely aligned with that of the LGAD sensor, with the main focus on the design of a multi-channel ASIC, as shown in Figure 5.43.

Following the successful development and testing of the single-channel LATRIC V0, an 8-channel ASIC (LATRIC V1) will be developed in Q4 2025, incorporating a digital logic control section. This integrated ASIC design will then be submitted for wafer fabrication. By the first half of 2026, the test system design for this ASIC will be finalized. In mid-2026, the

performance of the 8-channel ASIC will be evaluated, including crosstalk studies, followed by connection, debugging, and radiation-hardness testing in conjunction with the LGAD sensor.

By the end of 2026, the ASIC design will be refined, and the 64-channel ASIC (LATRIC V2) will be submitted for wafer fabrication. Simultaneously, a prototype of the LGAD readout frontend electronic system will be developed. In the mid-2027, performance tests of the 64-channel ASIC will be conducted, along with evaluations of the frontend prototype, ensuring seamless integration with the LGAD sensor.

By the end of 2027, the 128-channel LATRIC will be designed, integrated, and finalized for submission, paving the way for mass production.

Throughout the development process, the performance of the sensor-ASIC module will be thoroughly evaluated. A key focus will be on verifying whether the TOA and TOT metrics provide sufficient information to achieve the required timing and spatial resolutions. Additional efforts will aim to identify improvements in both the ASIC and the sensor to enhance the overall performance of the OTK detector.

Currently, wire bonding is the commonly used technique for connecting sensors and ASICs. This mature and reliable technology has been extensively applied in numerous experiments. However, alternative packaging and interconnection methods, such as solder-ball connections to the sensor or via an interposer board, will also be explored to further optimize the detector design and functionality.

In addition, to construct an OTK detector prototype, auxiliary chips — including the prototypes of data-link chip series (FEDI, FEDA, and OAT) and the power management DC-DC converters (PAL) — are scheduled for demonstration before 2027, while their final versions will be completed in the subsequent years.

5.3.6.3 Development of mechanical and cooling system

Besides, the assembly methodologies and mechanics of the supporting units will be investigated. This includes studying the support structure and materials, establishing the manufacturing procedures, and designing an efficient cooling system.

For the cooling system, trials will be conducted using various coolants, alongside the development of prototypes for the future cooling system. In addition to the water cooling, two-phase CO_2 flow cooling is also being explored as an alternative solution. In this approach, CO_2 undergoes a phase change from liquid to gas, allowing more heat to be removed and improving temperature uniformity. Although water cooling has been selected as the baseline for the current design due to its overall system simplicity, ongoing R&D efforts are progressing in parallel for both cooling approaches.

For example, Figure 5.42 shows the simulation result for OTK stave two-phase CO_2 cooling, with a pipe inner diameter of 5 mm (the same as for water cooling in Figure 5.29), an inlet temperature of -20 °C, a gauge pressure of 2 MPa, and a flow velocity of 0.53 m/s. The resulting

Figure 5.42: Simulation result of two-phase CO_2 cooling for the OTK stave, with an inlet temperature of -20 °C, a gauge pressure of 2 MPa, and a flow velocity of 0.53 m/s. The resulting outlet vapor quality is 0.3. The color-coded temperature scale is comparable to that of water cooling in Figure 5.29. Compared with water cooling, the two-phase CO_2 cooling achieves a reduced inlet coolant flow rate, lower temperature, and improved temperature uniformity.

outlet vapor quality is 0.3 (30% gaseous CO_2). With this CO_2 cooling configuration, the lowest sensor temperature is -16.9 °C and the highest is -13.8 °C, resulting in a temperature gradient along the full stave length of 3.1 °C, which is much smaller than the 8.6 °C observed with water cooling (Figure 5.29).

In addition to reduced inlet coolant flow rate and better temperature uniformity, CO_2 cooling can also maintain lower temperature compared with water cooling. This is expected to reduce leakage current and electronic noise, thereby improving signal-to-noise ratio and enhancing both timing and spatial resolution. More detailed studies will be carried out in future work. These advantage also apply to the ITK cooling.

5.3.6.4 Summary

All the R&D mentioned above is part of a 3-year plan, as detailed in Figure 5.43. Considering the project timeline of more than 5 years from construction, the CEPC project is flexible enough to adjust its technical approach and has sufficient backup plans for the engineering phase.

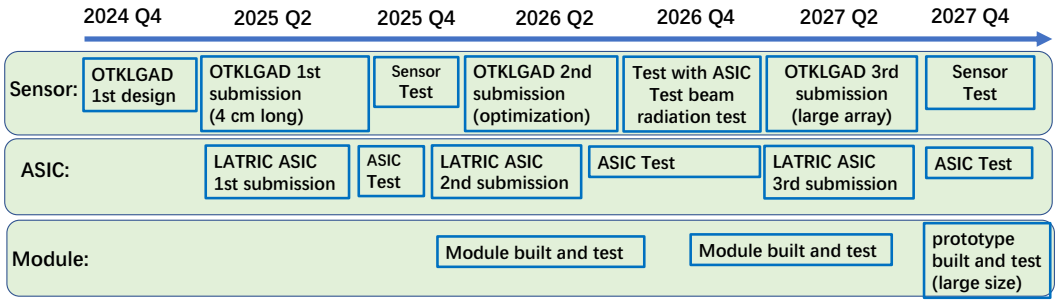


Figure 5.43: R&D timeline for the OTK, including sensor, ASIC, module, and mechanical and cooling components

For instance, if the performance of the AC-LGAD strip sensor degrades significantly for large-dimension strip sensor, we may consider using a smaller sensor, or a conventional large-dimension sensor with or without an external ToF detector. Additionally, if monolithic AC-

LGAD technology reaches maturity by the engineering phase, the AC-LGAD sensor could be applied not only to the OTK layer but also to the outermost ITK layer. In addition to precise spatial measurement, this would enable accurate timing measurement, enhancing Particle Identification (PID) for very low-momentum particles that cannot penetrate the TPC, thereby extending PID coverage from > 0.7 GeV/c down to > 0.3 GeV/c.

5.4 Survey and alignment

Precise knowledge of the silicon sensor positions is critical for achieving micron-level track position resolution for the Silicon Tracker. The tracker alignment process consists of two key steps: optical survey (mechanical assembly precision) and track-based alignment.

5.4.1 Mechanical assembly and optical survey

The assembly of both the ITK and OTK follows a hierarchical structure, starting from small modules and progressively building up to larger components. Sensors are first integrated into modules, which are then mounted onto ladders, staves, or endcap plates. These mechanical units are subsequently installed onto their respective docking structures, forming the barrels and endcaps of the Silicon Tracker.

The electrical and mechanical sensor modules will be assembled using manual alignment jigs or pick-and-place machines. Each sensor in a module has fiducial reference marks precisely engraved and aligned with the pixel or strip array. A three-dimensional Coordinate Measuring Machine (CMM), equipped with an optical probe, will measure the relative positions of the sensors within a module and verify their alignment with the next supporting structure, such as a ladder, stave, or endcap plate serving as the module's local support. These measurements will be compared against external reference markers on the FPC or module local support as part of an optical survey.

5.4.1.1 ITK installation and survey

For the ITK, the next step involves the precise mounting and measurement of the relative positions of staves and endcaps on their common docking structure (end-wheels). The positions of staves and endcaps will be measured and referenced against designated reference points on the end-wheels, using reference markers on the staves or endcap plates, including FPCs and sensor markers.

After each ITK layer is installed, a comprehensive survey of all targets on the end-wheels, staves, and endcaps within that layer will be conducted using a tracking system.

Once the ITK construction is complete, the entire detector will be inserted into the TPC inner barrel (see Figure 5.1). Due to the limited viewing angles for accessing the ITK through the TPC inner barrel holes, a laser tracking system will be used to reach the reference markers

on the outermost ITK endcaps. This system will establish the reference between the ITK local coordinate system and the global coordinate system.

5.4.1.2 OTK installation and survey

For the OTK barrel, the relative positions of the ladders will be measured against the stepped ramp rings on the TPC outer barrel (see Figure 5.28). Reference markers on the ladders will be compared against targets on the stepped ramp rings. Once the entire OTK barrel is assembled, a complete optical survey of all ladders will be performed relative to the reference points on the TPC end-wheels.

For the OTK endcap, the assembly involves joining 16 sectors, which are then mounted onto the common endcap support frame shared with the OTK and the Electromagnetic Calorimeter (ECAL). The docking points among sectors, sector connection rods, inner ring, and outer ring will be carefully monitored to ensure precise mounting. During installation, the OTK endcap will be referenced against the OTK&ECAL common endcap support frame.

By using reference targets on the TPC end-wheels and the OTK&ECAL common endcap support frame, the local coordinates of both the OTK barrel and endcap will be referenced to the global coordinate system.

5.4.1.3 Target optical survey precision

Table 5.13 summarizes the targeted optical survey precision for the Silicon Tracker. These metrology and survey data serve as starting points for the final track-based alignment.

Table 5.13: Target optical survey precision for ITK and OTK

Component	Sensor in module	Module on plate	Plate to end-wheel	End-wheel to global
ITK Barrel	~ 5 μm	~ 10 μm	~ 100 μm	~ 100 μm
ITK Endcap	~ 5 μm	~ 10 μm	~ 100 μm	~ 100 μm
OTK Barrel	~ 5 μm	~ 10 μm	~ 100 μm	~ 100 μm
OTK Endcap	~ 5 μm	~ 10 μm	~ 100 μm	~ 100 μm

5.4.2 Track-based alignment

Track-based alignment is a method for achieving high-precision detector positioning, based on reconstructed particle tracks. The global composite alignment approach [26] will be applied to the track-based alignment.

5.4.2.1 Global composite alignment

The tracker components are assembled in a hierarchical mechanical support structure. For example, in the ITK barrel, sensors are first assembled into modules, modules are then glued

onto staves, and staves are mounted onto the tracker end-wheels. Each component is positioned relative to its immediate support structure with six degrees of freedom: three translations and three rotations.

Since all subcomponents within the same supporting structure are subject to common shifts and highly correlated displacements, applying alignment directly at the sensor level would neglect these correlations and could distort the detector geometry.

The global composite alignment approach addresses this by defining alignment parameters at each hierarchical level relative to its immediate supporting structure. A global alignment procedure is then applied to simultaneously determine the displacement parameters of all detector components across different mechanical hierarchical levels, ensuring all correlations are properly accounted for. In this approach, both the global detector alignment parameters and the local track parameters are determined simultaneously through a vast χ^2 minimization.

5.4.2.2 Alignment plan and datasets

The planned track-based alignment consists of two stages: (a) alignment using cosmic muons without a magnetic field, and (b) alignment during $e^+ e^-$ collisions.

Cosmic muon data is crucial for the alignment process. Unlike beam-induced tracks, cosmic muons traverse the detector along various paths, making them valuable for constraining and correcting detector deformations. This helps resolve the so-called χ^2 invariance issue in beam-induced track alignment for $e^+ e^-$ collisions.

A dedicated data collection phase using straight muon tracks (with the magnetic field off) is planned after the completion of ITK and OTK detector construction. The detector will be installed $\sim$ 100 m underground. Due to significant energy loss in the ground materials such as rock and reinforced concrete, only a small fraction of high-energy muons (with $E > 100$ GeV) can penetrate and reach the detector. Therefore, a cosmic muon data-taking period of several months is planned to achieve sufficient statistics for precise alignment.

In addition to cosmic muon data, potential deformations of the tracking detectors after the magnetic field is turned on must be considered. During beam operation, the process $e^+e^- \rightarrow \mu^+\mu^-$ is a "golden channel" for the track alignment. Continuous data acquisition allows for real-time alignment of the tracker system, correcting potential displacements or deformations caused by external factors such as mechanical vibrations, thermoelastic movement, and differential settling of detector components. This alignment process must be periodically repeated to maintain optimal tracking performance.

5.5 Performance

This section highlights key tracking performance of the tracking system, focusing on the tracking momentum resolution and PID capabilities.

The total momentum resolution of a tracking system is mainly determined by two main factors: (a) the intrinsic spatial resolution of the position measurements and (b) the effects of multiple scattering from particle interactions with detector materials, which cause track deflections. For low-momenta tracks, the impact of multiple scattering dominates due to its inverse dependence on momentum, whereas for high-momenta tracks, the intrinsic spatial resolution of the tracker becomes the dominant factor. The CEPC tracking system benefits significantly from the integration of a gaseous detector TPC with a very low material budget and silicon detectors (VTX and STK) with high intrinsic spatial precision.

The tracking system also provides good PID performance, particularly in K/π/p separation, which is critical for CEPC flavor physics, searches for long-lived particles, and studies of jet substructure composition. This is primarily achieved by combining precise time measurement from the OTK as the ToF and the $\mathrm{d}n/\mathrm{d}x$ measurement (primary cluster counting) from the gaseous detector TPC.

5.5.1 Momentum resolution of the barrel region

Figure 5.44 shows the transverse momentum resolution ($\sigma_{p_\mathrm{T}}/p_\mathrm{T}$) as a function of transverse momentum at a polar angle of 85°, for three configurations: the silicon tracker including the VTX (in blue), the TPC alone (in red), and the full tracking system (in black). As expected, in the low momentum (< 10 GeV/c) region, the TPC provides better resolution. At high momenta, the silicon tracker significantly outperforms the TPC. The combination of both detectors provides the best performance across the entire momentum range.

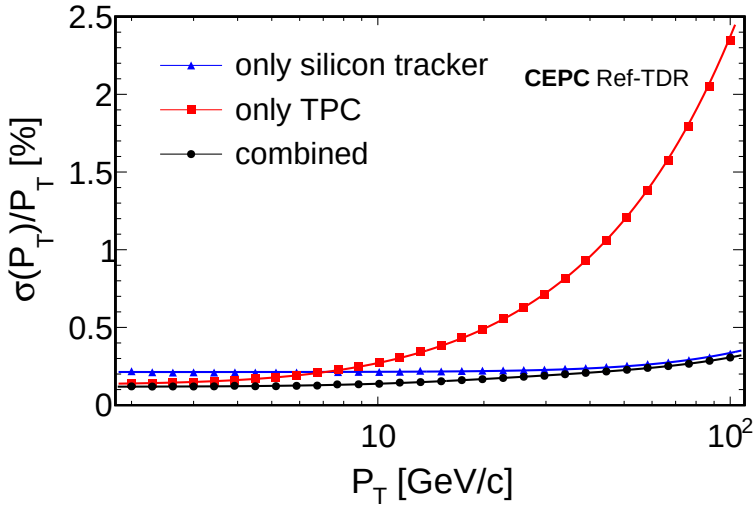


Figure 5.44: Transverse momentum resolution as a function of transverse momentum for the silicon tracker only (including the VTX, blue dots), TPC only (red dots), and the complete tracking system (black dots) at a polar angle of 85°. The TPC performance includes the effects of space-point distortions in Higgs mode.

Figure 5.45 presents the overall momentum resolution of the combined tracking system in

the barrel region for three representative polar angles, satisfying the CEPC tracking requirement. As shown in Figure 5.45, the momentum resolution of the combined tracking system at a given polar angle θ in the barrel can be parameterized as:

$$\begin{aligned}\left(\frac{\sigma_{p_\mathrm{T}}}{p_\mathrm{T}}\right)_\mathrm{Si} &= a p_\mathrm{T} \oplus \frac{b}{\beta\sqrt{\sin\theta}} \\ \left(\frac{\sigma_{p_\mathrm{T}}}{p_\mathrm{T}}\right)_\mathrm{TPC} &= a s_1 p_\mathrm{T} \oplus \frac{b s_2}{\beta\sqrt{\sin\theta}} \\ \left(\frac{\sigma_{p_\mathrm{T}}}{p_\mathrm{T}}\right)_\mathrm{Combined} &= \frac{1}{\sqrt{\left(\frac{\sigma_{p_\mathrm{T}}}{p_\mathrm{T}}\right)_\mathrm{Si}^{-2} + \left(\frac{\sigma_{p_\mathrm{T}}}{p_\mathrm{T}}\right)_\mathrm{TPC}^{-2}}}\end{aligned} \tag{5.3}$$

where $a \approx 2.3 \times 10^{-5}$, $b \approx 2.2 \times 10^{-3}$, $s_1 \approx 4.1$, and $s_2 \approx 0.64$. In this parameterization, contributions from both the silicon tracker and the TPC are taken into account.

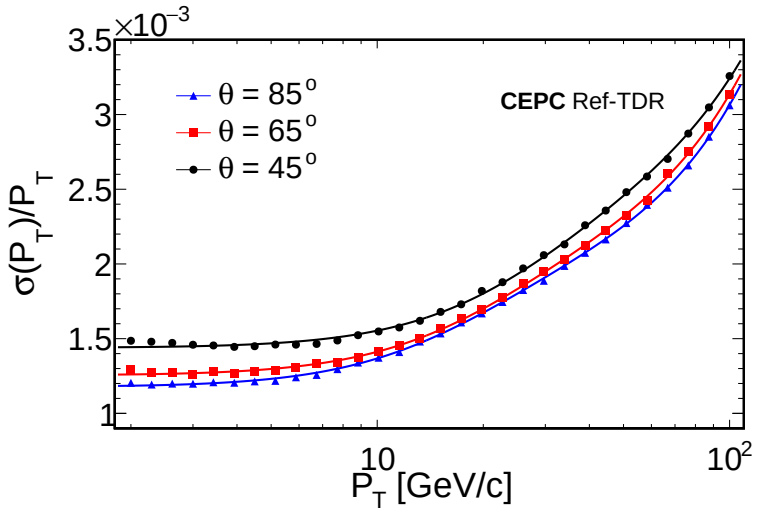


Figure 5.45: Transverse momentum resolution as a function of transverse momentum for the complete tracking system at polar angles of 85° (blue dots), 65° (red dots), and 45° (blue dots), where the curves are the fitting results with Equation 5.3.

5.5.2 Momentum resolution of the forward region (endcap)

The endcap region of the tracking system covers polar angle $8° < \theta < 30°$, including the silicon tracker and TPC overlap region ($11.5° < \theta < 30°$) and the very forward region ($8° < \theta < 11.5°$), which is exclusively covered by the silicon tracker. In this region, the tracking performance is primarily limited by the relatively short bending lever arm. This effect is partially mitigated by the extended barrel design of the CEPC tracking system.

Figure 5.46 illustrates the transverse momentum resolution as a function of transverse momentum for the endcap region, using the silicon tracker alone. The momentum resolution of the silicon tracker in the endcap region can be parameterized as:

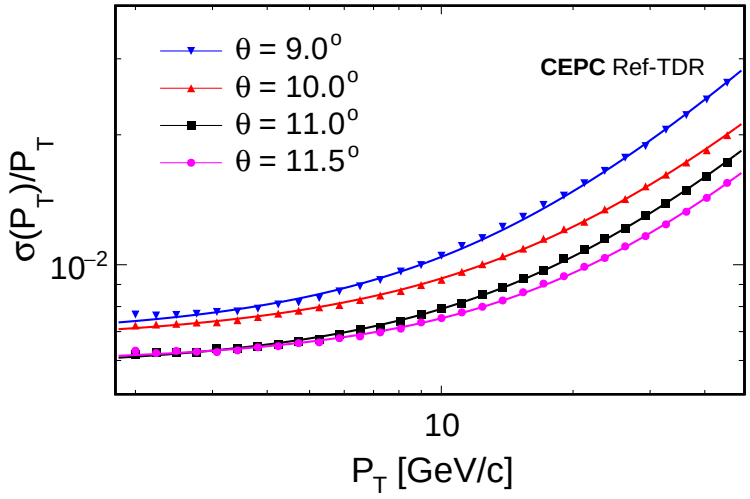


Figure 5.46: Transverse momentum resolution as a function of the transverse momentum for different polar angles at endcap region. The curves are fitting results with Equation (5.4).

$$\frac{\sigma_{p_{\mathrm{T}}}}{p_{\mathrm{T}}} = \frac{a' p_{\mathrm{T}}}{(\tan\theta)^2} \oplus \frac{b'}{\beta \tan\theta \sqrt{\cos\theta}} \oplus \frac{c'\sqrt{p_{\mathrm{T}}}}{\sqrt{\beta}(\tan\theta)^{\frac{3}{2}}(\cos\theta)^{\frac{1}{4}}} \tag{5.4}$$

where $a' \approx 1.1 \times 10^{-5}$, $b' \approx 1.1 \times 10^{-3}$, and $c' \approx 1.2 \times 10^{-4}$.

5.5.3 Particle identification performance

The separation power, η_{AB}, for distinguishing two particle types, A and B, can be defined as:

$$\eta_{AB} = \frac{|\mu_A - \mu_B|}{\sqrt{(\sigma_A^2 + \sigma_B^2)/2}} \tag{5.5}$$

where μ_A and μ_B are the mean values of the PID estimator for particles A and B, and σ_A and σ_B are the standard deviations of the PID estimator.

Figure 5.47 shows the separation power between K and π as a function of momentum, using the ToF (OTK) with a 50 ps timing resolution. The blue curve corresponds to the barrel region at a polar angle of $\theta = 85°$, while the red curve corresponds to the endcap region at $\theta = 25°$. As seen, compared with the the barrel region, the ToF in the endcap region exhibits better PID performance due to the longer flight path to the OTK endcaps. Overall, the ToF provides good PID performance below 2–3 GeV/c.

The momentum cutoff of the ToF below $\sim$ 0.9 GeV/c is caused by the particle's inability to penetrate the OTK detector, which results from the curvature bending in the magnetic field.

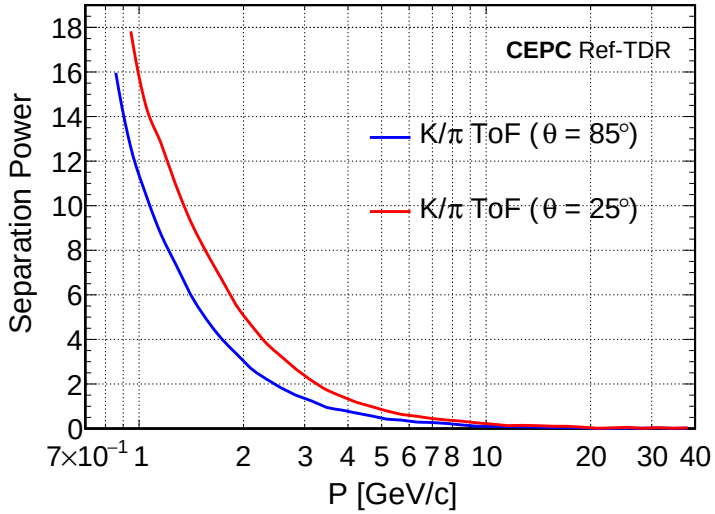


Figure 5.47: Separation power between K and π as a function of momentum at the polar angles $\theta = 85°$ (blue curve) in the barrel region and $\theta = 25°$ (red curve) in the endcap region, using the ToF (OTK) with a 50 ps timing resolution. As shown, the ToF provides good K/π separation below 2–3 GeV/c.

5.6 Summary

The Silicon Tracker is a vital detector system for the CEPC, essential for precise particle trajectory determination and particle identification. As the system evolves through continuous technological improvements and optimizations, it will be steadily transitioning into the engineering phase in the next few years. Continuous innovations in sensor technology, readout electronics, mechanical design, and the development of the cooling system will ensure that the Silicon Tracker meets the high demanding requirements of CEPC physics.

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Part II

Other CEPC Detector Concepts

Glossary

AC Alternating Current 23, 24, 35, 36, 44–46

AC-LGAD AC-coupled Low Gain Avalanche Detector 3, 5, 27, 28, 44–50, 55, 57, 58

ASIC Application Specific Integrated Circuit 5, 12, 25, 27–31, 33–38, 41, 50, 51, 53–57

BEE Back-End Electronics 8, 11–13, 35

BNL Brookhaven National Laboratory 44

CC Concentrator Card 37

CEPC Circular Electron Positron Collider 3, 4, 21–23, 50, 57, 61, 62, 64

CIS CMOS Image Sensor 4, 21

CMM Coordinate Measuring Machine 58

CMOS Complementary Metal Oxide Semiconductor 4, 6, 21, 22, 24, 26, 27

CSA Charge-Sensitive Preamplifier 24

DAC Digital-to-Analog Converter 51, 52, 54

DC Direct Current 48

DC-DC Direct Current-Direct Current 6–8, 11–14, 28–30, 33–38, 41, 56

DLL Delay-Locked Loop 53

DUT Device Under Test 47

ECAL Electromagnetic Calorimeter 59

FBK Fondazione Bruno Kessler 44

FE Front-End 35–37

FEDA Front-End Data Aggregator 12, 13, 35–37, 56

FEDI Front-End Data Interface 12, 13, 35–38, 53, 56

FPC Flexible Printed Circuit 6–8, 11–16, 19, 29, 30, 33, 34, 37, 38, 58

FPGA Field-Programmable Gate Array 25

FPMROC Fast Photomultiplier Readout Chip 54

HGTD High Granularity Timing Detector 44

HPK Hamamatsu 44

HV High Voltage 8, 11, 29, 33, 36, 37

HV-CMOS High Voltage Complementary Metal-Oxide-Semiconductor 3, 4, 6, 7, 9, 11, 21, 22, 26, 27

HVMUX High-Voltage Multiplexer 8, 36

I/O Input/Output 13, 37

I2C Inter-Integrated Circuit 13, 36, 37, 51, 53

ID Identification 36, 53
IHEP Institute of High Energy Physics 44, 45, 48
INFN National Institute for Nuclear Physics 44
ITK Inner Silicon Tracker 3–21, 27, 38, 40, 43, 57–60

JTAG Joint Test Action Group 37
JTE Junction Termination Extension 44, 45

LATRIC LGAD Timing and Readout Integrated Chip 35, 36, 50–53, 55, 56
LGAD Low Gain Avalanche Detector 35, 36, 44, 45, 47–50, 52, 54–56
LV Low Voltage 8, 11, 13, 29, 33, 36, 37

MAPS Monolithic Active Pixel Sensor 21
MCP-PMT Microchannel Plate Photomultiplier Tube 54
MIP Minimum Ionizing Particle 47, 50
MPV Most Probable Value 50
MPW Multi-Project Wafer 21, 22, 26, 27

NMOS Negative channel Metal-Oxide-Semiconductor 24, 26, 27

OAT Optical Array Tranceiver 12–14, 35, 37, 38, 56
OTK Outer Silicon Tracker 3–5, 27–45, 49, 50, 55–61, 63, 64

PAL Power-at-Load 12–14, 35–37, 56
PCB Printed Circuit Board 10, 28–30, 33, 34, 38, 40, 41, 43
PEEK Polyether Ether Ketone 18, 42
PID Particle Identification 58, 60, 61, 63
PLL Phase-Locked Loop 37, 51, 53, 54
PMOS Positive channel Metal-Oxide-Semiconductor 24, 26
PRBS Pseudo-Random Binary Sequence 53

R&D Research and Development 21, 26, 27, 45, 46, 55–57

SPI Serial Peripheral Interface 54
STK Silicon Tracker 3, 5, 61

TCAD Technology Computer Aided Design 24, 45, 55
TCT Transient Current Technique 46, 47, 49
TDAQ Trigger and Data Acquisition 12
TDC Time-To-Digital Converter 26, 50–55
TOA Time-of-arrival 50–54, 56
ToF Time-of-Flight 3, 27, 44, 57, 61, 63, 64
TOT Time-over-threshold 50–54, 56

TPC Time Projection Chamber 3–5, 14, 29, 30, 38, 39, 58, 59, 61, 62

VCSEL Vertical-Cavity Surface-Emitting Laser 14

VTX Vertex Detector 3, 5, 21, 61