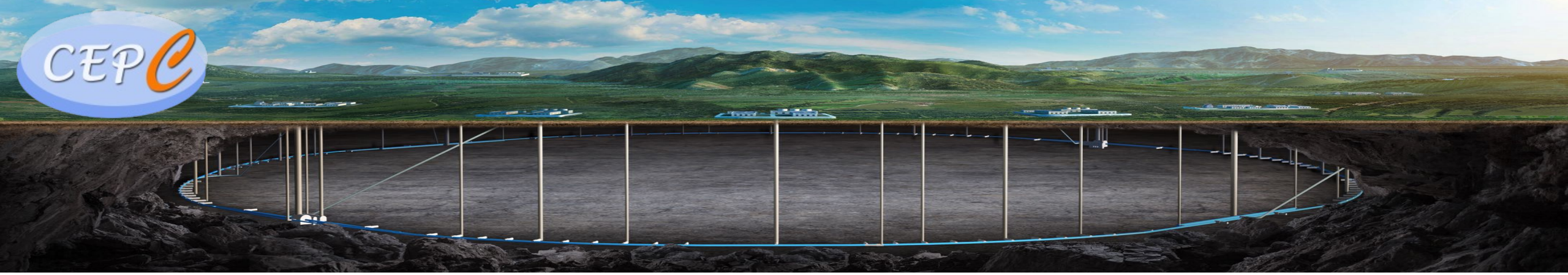

In Response to the Latest IDRC Feedback: Silicon Tracker

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Summary of Responses to Latest IDRC Feedback

[Added]

1. Include a detailed description for pursuing CO_2 cooling in Section 5.3.6.
2. Please note that revisions to include more details on "Future Plans" for the HVCMOS sensor (Section 5.2.5) and the LATRIC ASIC (Section 5.3.6), in line with the IDRC's recommendations, were already incorporated in the previous arXiv version.

[Changed]

1. Summary of textual revisions following IDRC suggestions (Note: Most revisions were already implemented in the previous arXiv version):
   (a) L3151 - conventional partly depleted CMOS are probably meant as MAPS without external HV bias, which more accurately describes these devices. Amended: "conventional CMOS sensors with shallow depletion, as in typical CMOS Image Sensor (CIS) processes."
   (b) A sentence on proposed HV distribution/granularity plan and associated services would be welcome. Added: "To allow isolation of individual malfunctioning sensors, High-Voltage Multiplexers (HVMUXs) are planned for possible integration into each module FPC."
   (c) L4172 - for mip particle. Added: "The Most Probable Value (MPV) of the charge collected from the LGAD sensor for a MIP is approximately 16 fC."
   (d) Similarly to ITK a sentence on proposed HV distribution/granularity plan and associated services would be welcome. Added: "200 V HV is used for sensor biasing, with HVMUXs considered for integration on the FE board to allow isolation of individual malfunctioning sensors."
   (e) The heat dissipation is very inhomogeneously distributed (dominated at the place of the LATRIC). It is not clear to us if it was taken into account with all the implications to the mechanics/services. Amended: "The detector dissipates heat at a flux of 300 mW/cm^2, simply assumed to be uniformly distributed across the sensors."
   (f) L3781 - please mention the process in which ATRIC is made. "55 nm" included in Table 5.12.
   (g) Fig. 34 - units of charge are not correct. Corrected.
   (h) please put also the size of the LATRIC (dimensions). Chip size of "1.2 cm×0.5 cm" included in Table 5.12.

Inner Tracker (ITK)

Recommendations

- The TDR should include a more detailed description of the thermal studies, clearly identifying the assumptions underlying the sensor thermal requirements and quantifying the expected benefits of CO_2 cooling. Given that the current baseline water-cooling system appears sufficient, a quantitative comparison of both approaches would clarify whether parallel R&D is warranted.

5.3.6 Future plan

Besides, the assembly methodologies and mechanics of the supporting units will be investigated. This includes studying the support structure and materials, establishing the manufacturing procedures, and designing an efficient cooling system.

For the cooling system, trials will be conducted using various coolants, alongside the development of prototypes for the future cooling system. In addition to the water cooling, two-phase CO_2 flow cooling is also being explored as an alternative solution. In this approach, CO_2 undergoes a phase change from liquid to gas, allowing more heat to be removed and improving temperature uniformity. Although water cooling has been selected as the baseline for the current design due to its overall system simplicity, ongoing R&D efforts are progressing in parallel for both cooling approaches.

For example, Figure 5.42 shows the simulation result for OTK stave two-phase CO_2 cooling, with a pipe inner diameter of 5 mm (the same as for water cooling in Figure 5.29), an inlet temperature of -20 °C, a gauge pressure of 2 MPa, and a flow velocity of 0.53 m/s. The resulting outlet vapor quality is 0.3 (30% gaseous CO_2). With this CO_2 cooling configuration, the lowest sensor temperature is -16.9 °C and the highest is -13.8 °C, resulting in a temperature gradient along the full stave length of 3.1 °C, which is much smaller than the 8.6 °C observed with water cooling (Figure 5.29).

In addition to reduced inlet coolant flow rate and better temperature uniformity, CO_2 cooling can also maintain lower temperature compared with water cooling. This is expected to reduce leakage current and electronic noise, thereby improving signal-to-noise ratio and enhancing both timing and spatial resolution. More detailed studies will be carried out in future work. These advantage also apply to the ITK cooling.

New simulation result with CO_2 cooling added

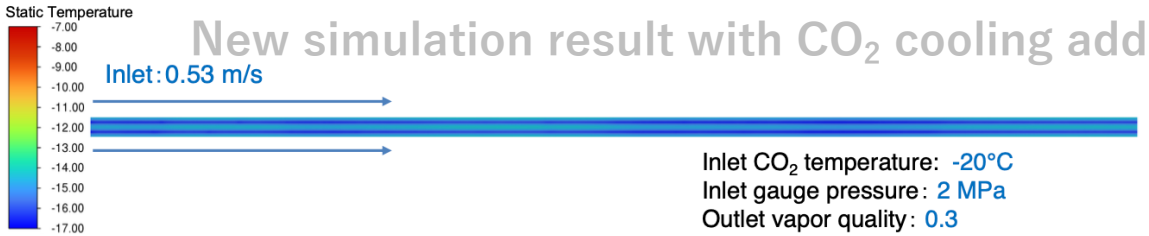
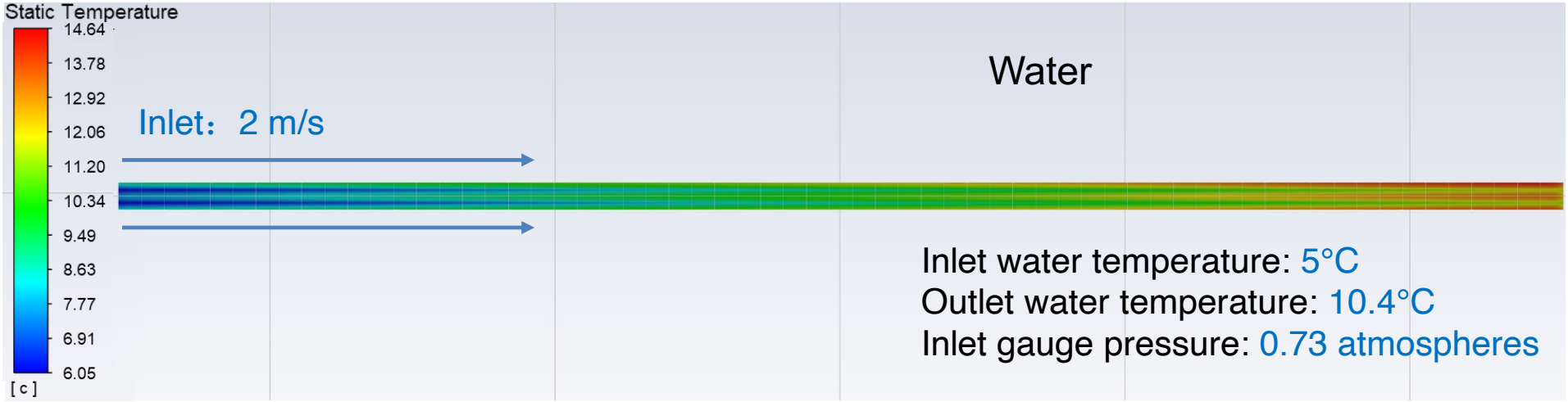
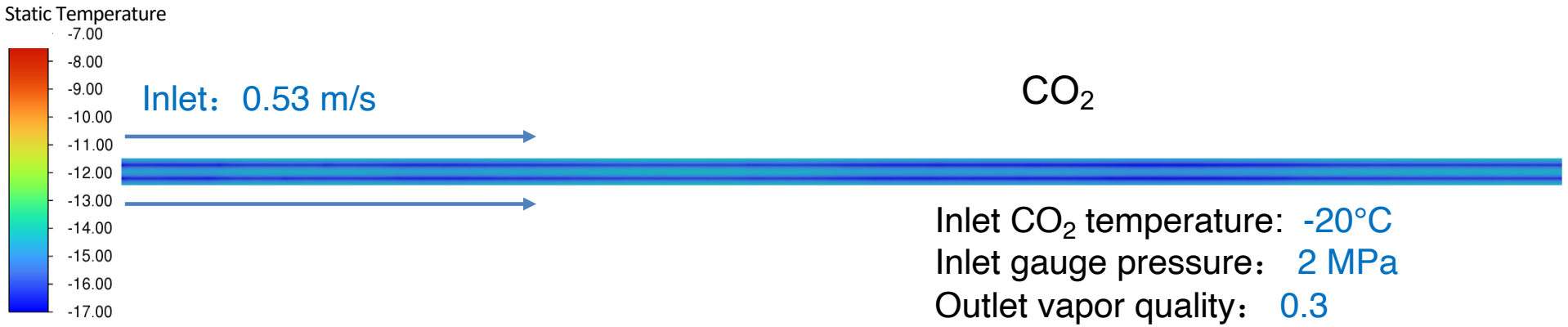


Figure 5.42: Simulation result of two-phase CO_2 cooling for the OTK stave, with an inlet temperature of -20 °C, a gauge pressure of 2 MPa, and a flow velocity of 0.53 m/s. The resulting outlet vapor quality is 0.3. The color-coded temperature scale is comparable to that of water cooling in Figure 5.29. Compared with water cooling, the two-phase CO_2 cooling achieves a reduced inlet coolant flow rate, lower temperature, and improved temperature uniformity.

ITK & OTK addressed together

Comparison of water cooling and two-phase CO_2 cooling for OTK (5,680 mm) stave using 5 mm pipe diameters





Recommendations

- The “Future Plans” section should provide a detailed schedule for the testing, redesign, and manufacturing of the COFFEE ASIC family. This would allow progress tracking and ensure timely achievement of critical milestones.

5.2.5 Future plan

In the coming years, substantial efforts will be dedicated to developing the full-size HV-CMOS sensor, evolving from small MPW productions to full reticle size. In parallel, module level and system level integration, including R&D on supporting electronics, mechanical structures, cooling systems, and detailed integration methodologies, will also be carried out.

Among the target sensor design specifications listed in Table 5.3, achieving a timing resolution of a few nanoseconds to tag the 23 ns bunch crossings is particularly challenging, especially when combined with the requirement for moderate power consumption and high hit density tolerance. To address this, a novel data-driven readout architecture featuring in-pixel Coarse-Fine Time-To-Digital Converters (TDCs) has been implemented in the latest sensor prototype, COFFEE3 (see Figure 5.21). This design fully exploits the 55 nm process’s small feature size, enabling more functionality within the limited pixel area. The chip has been recently submitted and is currently undergoing comprehensive characterization.

Continuous efforts are also focus on improving the sensor design and fabrication processes. In the current HV-CMOS process used for the COFFEE series, the n-well of the PMOS transistor is directly in contact with the charge-collecting deep n-well (Figure 5.15). This configuration can induce voltage variations in the deep n-well due to PMOS transistor flipping, which are further amplified by the front-end electronics. To mitigate this cross-talk effect, a deep p-type layer has been proposed to separate the n-well from the charge collection electrode. Efforts are ongoing to enable such separation through a “quadruple-well process”. As an alternative to process modification, cross-talk can also be avoided by designing the pixel circuitry using only NMOS transistors. Both a CMOS-based array and an NMOS-only pixel array have been designed in COFFEE3, as shown in Figure 5.21. However, process modification remains the preferred solution, as it provides greater flexibility and enhanced pixel circuitry functionality.

Following COFFEE3 verification in late 2025, the focus will shift to process modification. In collaboration with the foundry, a new MPW submission using the “quadruple-well process” is planned for early 2026, followed by testing around mid-2026 to evaluate the modified process. In parallel, a quarter-size chip will be designed and submitted for tape-out after process verification. Testing of this chip, from late 2026 to mid-2027, will serve as an intermediate validation step before full-scale development.

From late 2026 through 2027, the project will advance to the full-size chip design, integrating all validated circuit and process improvements. The designed chip is scheduled for submission by the end of 2027. Final full-size chip testing is planned for 2028 to confirm complete functionality, performance, and production readiness. By the end of 2028, a fully validated, high-performance, and scalable HV-CMOS sensor is expected to be delivered for mass production.

Prototyping of ITK detector modules, along with their mechanical and cooling support structures for integration, will proceed in parallel with the development of the sensor chips. This includes the development of electronic components, methodologies, and tools for detector module assembly, studying support structures to optimize manufacturing procedures, and designing an efficient cooling system.

As the full-sized sensor prototype will only become available after several submissions, small-scale sensor chips together with the evolving off-chip electronic components, will serve as key intermediate steps for the system level R&D for both electrical and mechanical functionalities. Extensive prototyping studies — particularly on the mechanics, assembly and tooling — can be conducted using dummy silicon sensors. Specific traces can be added to these dummy sensors to define assembly procedures, especially when using an automatic gantry system. Dummy sensor modules, and other mechanical and cooling mockups, incorporating additional components that dissipate heat or generate external stress loads, will be useful for thermal and mechanical studies. Prototyping of the cooling system is currently underway.

More detailed plans added

Outer Tracker (OTK)

Recommendations

OTK

- The TDR should include more detailed information about the thermal simulations, clearly stating the assumptions underlying the sensor thermal requirements. This would strengthen the justification for pursuing CO_2 cooling as an alternative to the water-based system.

5.3.6 Future plan

Besides, the assembly methodologies and mechanics of the supporting units will be investigated. This includes studying the support structure and materials, establishing the manufacturing procedures, and designing an efficient cooling system.

For the cooling system, trials will be conducted using various coolants, alongside the development of prototypes for the future cooling system. In addition to the water cooling, two-phase CO_2 flow cooling is also being explored as an alternative solution. In this approach, CO_2 undergoes a phase change from liquid to gas, allowing more heat to be removed and improving temperature uniformity. Although water cooling has been selected as the baseline for the current design due to its overall system simplicity, ongoing R&D efforts are progressing in parallel for both cooling approaches.

For example, Figure 5.42 shows the simulation result for OTK stave two-phase CO_2 cooling, with a pipe inner diameter of 5 mm (the same as for water cooling in Figure 5.29), an inlet temperature of -20 °C, a gauge pressure of 2 MPa, and a flow velocity of 0.53 m/s. The resulting outlet vapor quality is 0.3 (30% gaseous CO_2). With this CO_2 cooling configuration, the lowest sensor temperature is -16.9 °C and the highest is -13.8 °C, resulting in a temperature gradient along the full stave length of 3.1 °C, which is much smaller than the 8.6 °C observed with water cooling (Figure 5.29).

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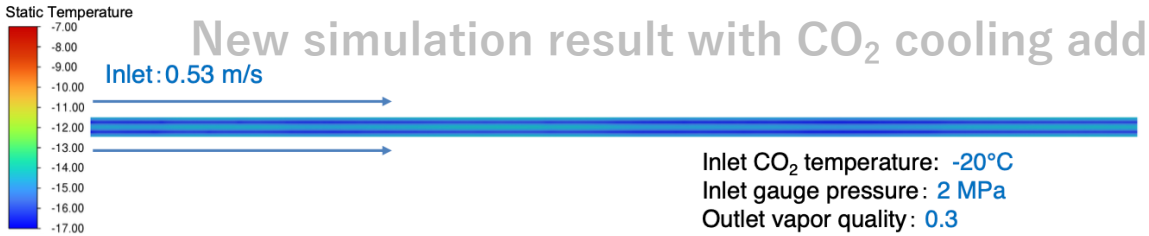
New simulation result with CO_2 cooling added



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ITK & OTK addressed together

Recommendations

OTK

- The “Future Plans” section should include a detailed schedule for the iterative development, testing, and validation of the LATRIC ASIC family, leading to the final multi-channel version. This should also cover auxiliary front-end and back-end electronics.

5.3.6 Future plan

The development timeline of the LGAD readout ASIC (LATRIC) is closely aligned with that of the LGAD sensor, with the main focus on the design of a multi-channel ASIC, as shown in Figure 5.42.

Following the successful development and testing of the single-channel LATRIC V0, an 8-channel ASIC (LATRIC V1) will be developed in Q4 2025, incorporating a digital logic control section. This integrated ASIC design will then be submitted for wafer fabrication. By the first half of 2026, the test system design for this ASIC will be finalized. In mid-2026, the performance of the 8-channel ASIC will be evaluated, including crosstalk studies, followed by connection, debugging, and radiation-hardness testing in conjunction with the LGAD sensor.

By the end of 2026, the ASIC design will be refined, and the 64-channel ASIC (LATRIC V2) will be submitted for wafer fabrication. Simultaneously, a prototype of the LGAD readout frontend electronic system will be developed. In the mid-2027, performance tests of the 64-channel ASIC will be conducted, along with evaluations of the frontend prototype, ensuring seamless integration with the LGAD sensor.

By the end of 2027, the 128-channel LATRIC will be designed, integrated, and finalized for submission, paving the way for mass production.

Throughout the development process, the performance of the sensor–ASIC module will be thoroughly evaluated. A key focus will be on verifying whether the TOA and TOT metrics provide sufficient information to achieve the required timing and spatial resolutions. Additional efforts will aim to identify improvements in both the ASIC and the sensor to enhance the overall performance of the OTK detector.

Currently, wire bonding is the commonly used technique for connecting sensors and ASICs. This mature and reliable technology has been extensively applied in numerous experiments. However, alternative packaging and interconnection methods, such as solder-ball connections to the sensor or via an interposer board, will also be explored to further optimize the detector design and functionality.

In addition, to construct an OTK detector prototype, auxiliary chips — including the prototypes of data-link chip series (FEDI, FEDA, and OAT) and the power management DC-DC converters (PAL) — are scheduled for demonstration before 2027, while their final versions will be completed in the subsequent years.

More detailed plans added

Other Minor Textual Revisions Implemented

- The heat dissipation is very inhomogeneously distributed (dominated at the place of the LATRIC). It is not clear to us if it was taken into account with all the implications to the mechanics/services.

Clarified in the paper: The detector dissipates heat at a flux of 300 mW/cm^2, simply assumed to be uniformly distributed across the sensors.

(We are unable to perform such a detailed simulation down to the ASIC level within such a short timeframe.)

- L3151 - conventional partly depleted CMOS are probably meant as MAPS without external HV bias, which more accurately describes these devices.

Clarified in the paper: “This performance, achieved with moderate power consumption, significantly outperforms conventional CMOS sensors with shallow depletion, as in typical CMOS Image Sensor (CIS) processes.”

- A sentence on proposed HV distribution/granularity plan and associated services would be welcome.

Added in the paper: To allow isolation of individual malfunctioning sensors, High-Voltage Multiplexers (HVMUXs) are planned for possible integration into each module FPC.

- L4172 - for mip particle

Added in the paper: The Most Probable Value (MPV) of the charge collected from the LGAD sensor for a MIP is approximately 16 fC.

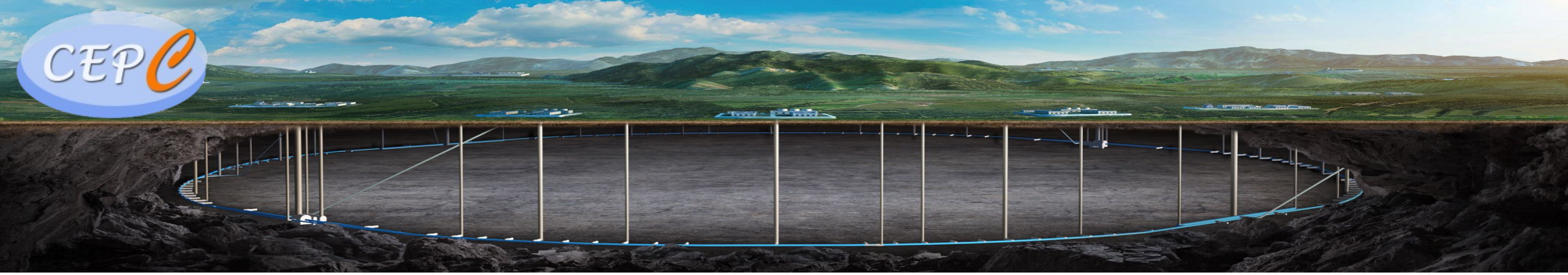
- Similarly to ITK a sentence on proposed HV distribution/granularity plan and associated services would be welcome.

Added in the paper: 200 V HV is used for sensor biasing, with HVMUXs considered for integration on the FE board to allow isolation of individual malfunctioning sensors.

- L3781 - please mention the process in which ATRIC is made. (Added)
- Fig. 34 - units of charge are not correct (Corrected)
- Table 5.12 - please put also the size of the LATRIC (dimensions) (Added)

Table 5.12: Configuration for the LATRIC ASIC (assuming a detector capacitance C_d = 8 pF)

Parameter	Value
Chip size	1.2 cm × 0.5 cm
Voltage	1.2 V
Number of channels	128
Channel pitch	< 100 µm
Single channel noise (ENC)	0.8 fC
Cross-talk	< 10%
Maximum jitter	30 ps at 16 fC
Minimum threshold	4 fC
Dynamic range	8 fC–50 fC
TDC conversion time	< 23 ns
Power dissipation per ASIC	1.5 W (for occupancy < 1%)
Data size per fired channel	48 bits
e-link driver bandwidth	43.33 Mbps or 86.67 Mbps
Technology node	55 nm



Backup

- Fig. 5.19 and L 3559-3571: It would be highly welcome to estimate the depletion depth from the capacitance measurement. This is essential to understand the minimum ionizing particle signal one can expect with this process using standard wafers.

The COFFEE2 chip was fabricated on a standard resistivity wafer (~10 Ω·cm). Capacitance measurements show an estimated depletion depth of ~10 μm, corresponding to a charge yield of ~1120 e^- for a minimum ionizing particle (MIP). COFFEE2/3 is intended primarily for sensor design validation. To increase the depletion depth and the resulting charge yield (or S/N ratio), high-resistivity wafers will be employed in future fabrication.

- 200V may not be enough to achieve optimum time resolution given the close to room temperature operation and the fact that you are not going to optimize the performance for radiation hardness as for HL-LHC.

The bias voltage of 200 V is not a fixed limit and can be increased if necessary. The optimal operating voltage will be determined through future performance evaluations, taking into account the detector characteristics and operating conditions.