Sensor Development for LHCb Upstream Pixel Tracker

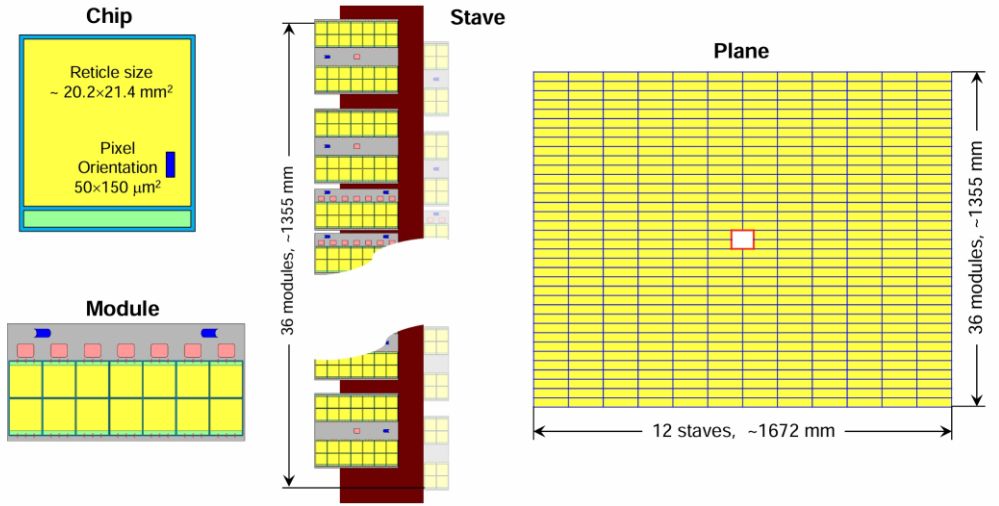
Cheng Zeng 曾程　(Institute of High Energy Physics, CAS)

On behalf of COFFEE team

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

HVCMOS for LHCb UP Tracker

- LHCb Upgrade II requires tracker with better radiation hardness and spatial resolution.



Upstream Pixel Tracker for LHCb Upgrade II

Area： $\sim 8\ \mathrm{m}^2$

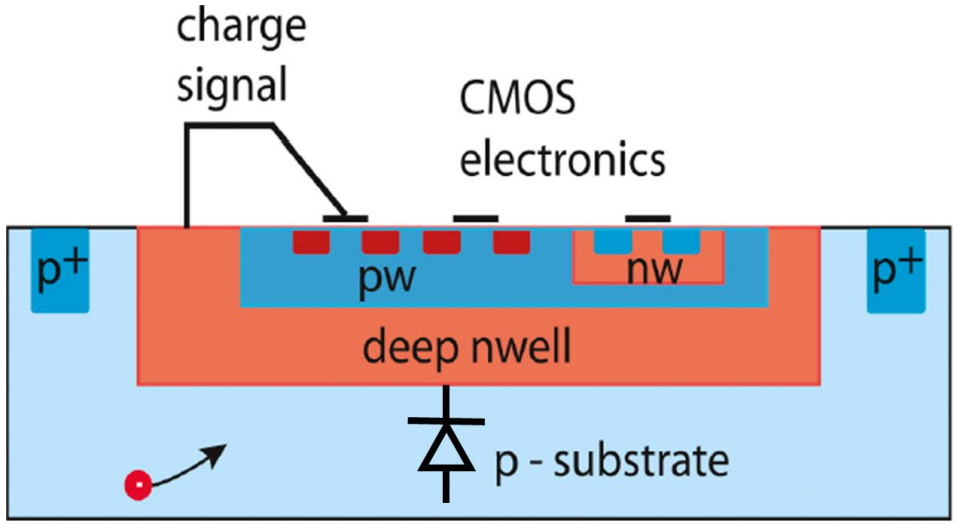
Radiation hardness： $\sim 3 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$

Bunch timing： $25\ \mathrm{ns}$

Time resolution： $3 - 5\ \mathrm{ns}$

Power consumption： $\sim 200\ \mathrm{mW/cm^2}$

- HVCMOS advantages:
  - Monolithic Active Pixel Sensor (MAPS), Excellent spatial resolution.
  - Large deep n-well as charge collection node. Fast charge collection.
  - Enclose readout circuit inside deep n-well. Great radiation tolerant.



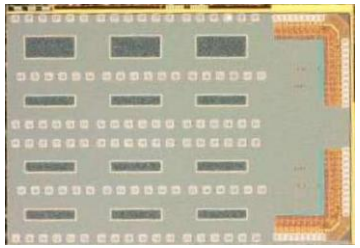
Sensor cross section

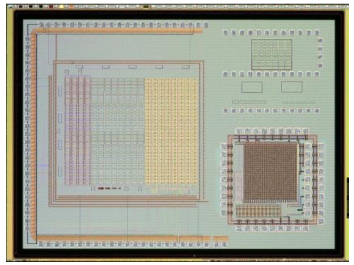
COFFEE Chips

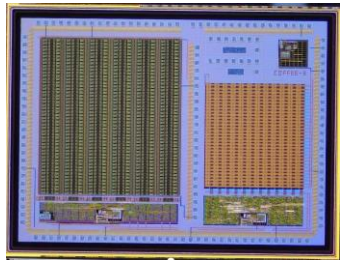
CMOS sensOr in Fifty-FivE nanometer procEss chips

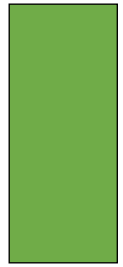
- Targeting to achieve full-size, full function chips meeting the LHCb UP Tracker requirements in few years.
  - COFFEE1: Validate the 55 nm low leakage process
  - COFFEE2: Explore and validate the 55 nm HV-CMOS process
  - COFFEE3: Validate the readout circuit structures and core performances

COFFEE1 2023.4 → COFFEE2 2024.1 → COFFEE3 2025.6 → COFFEE4 2026 → COFFEE5 2027

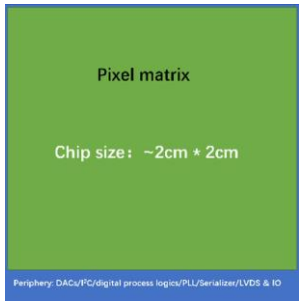








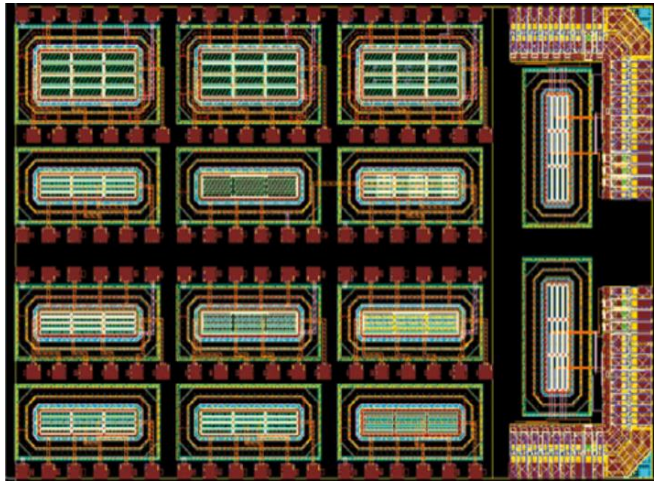
Quarter chip

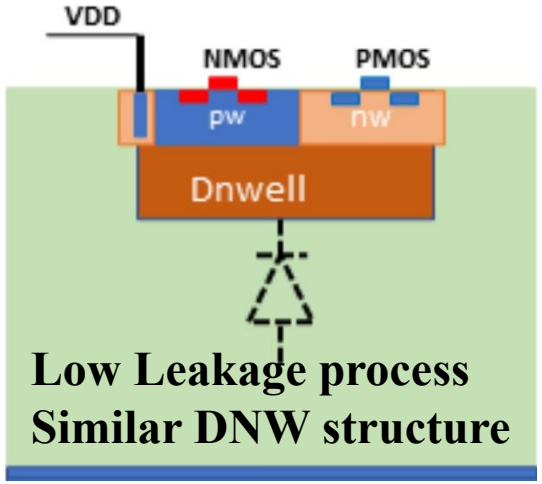


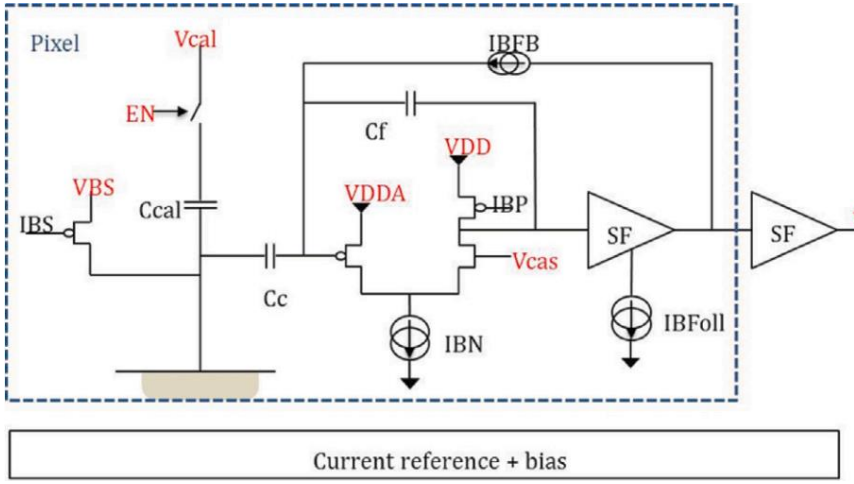
COFFEE1 Brief Result

COFFEE1 chip, 3×2 mm^2, verify the feasibility of 55 nm process. NIMA 1069 (2024) 169905

Pixel area
P-stop
DNW gap

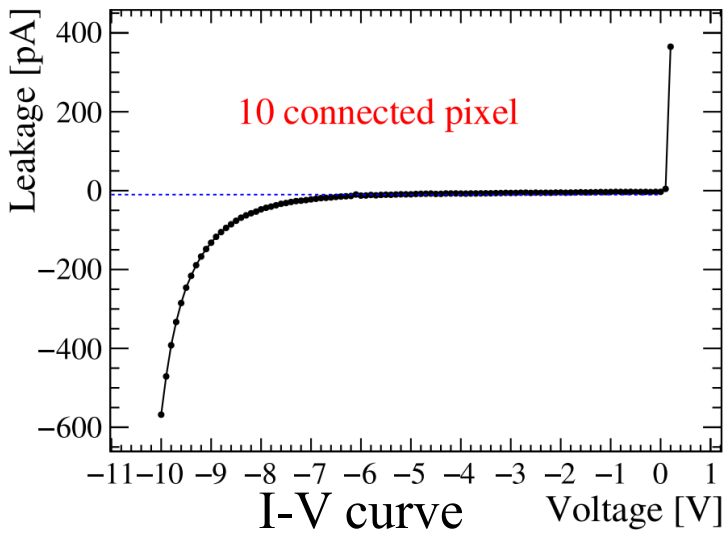


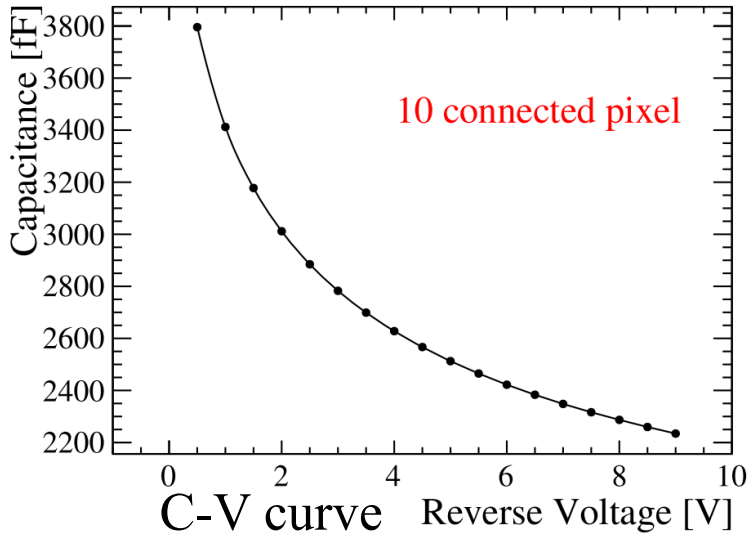


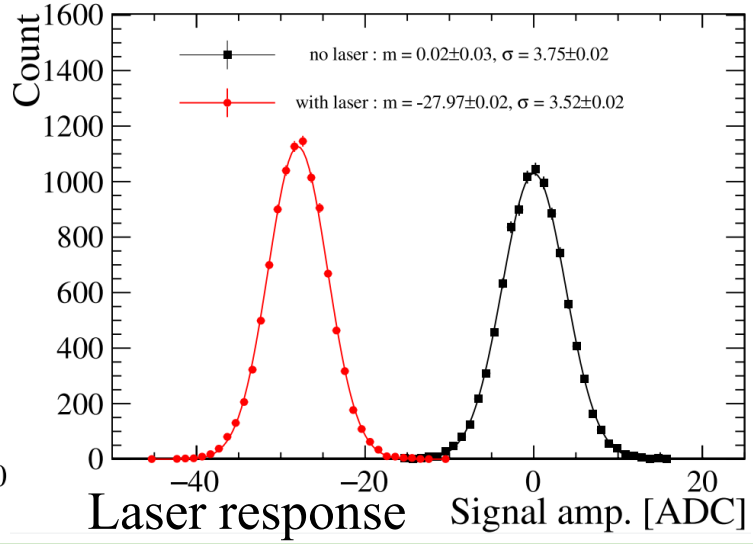


COFFEE1 chip floorplan Sensor cross section Schematic design of COFFEE1 in-pixel circuit

Breakdown Voltage: ~ − 9V, Leakage: ~pA, Capacitance: 150~200 fF, Laser response

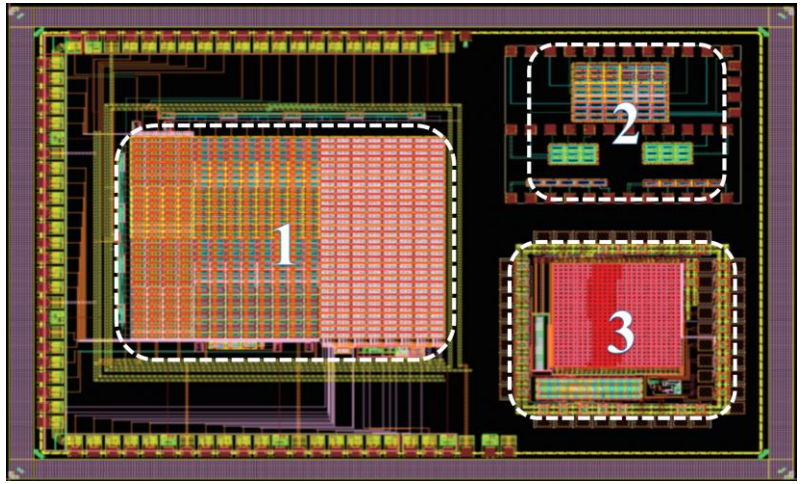




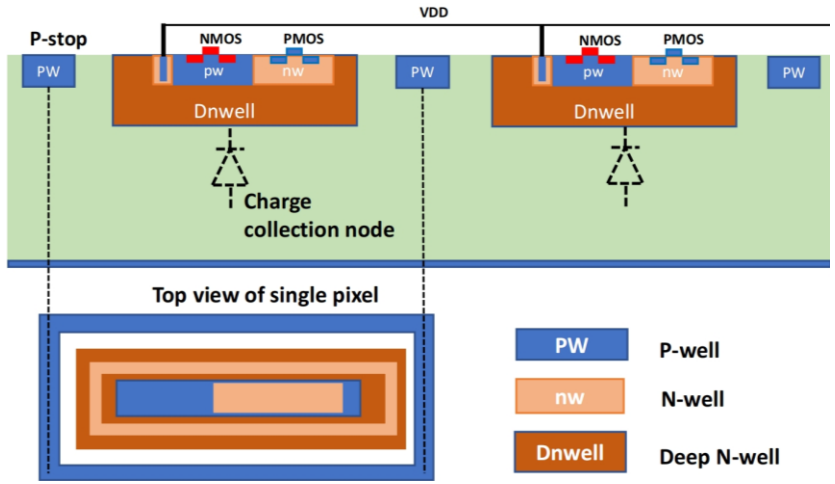


COFFEE2 Introduction

COFFE2 chip, 3×4 mm^2, the first HVCMOS chip in 55 nm process, triple-well structure



COFFEE2 chip floorplan



Sensor cross section

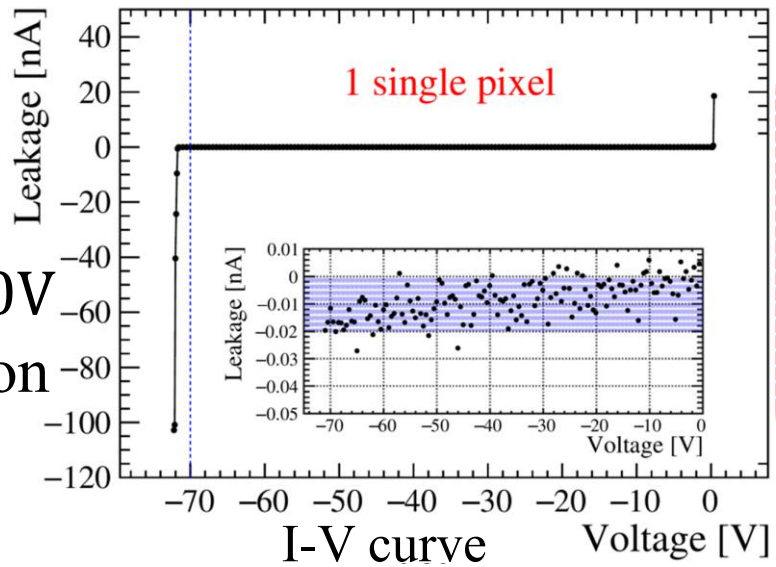
- Section 1: 32 rows × 20 columns pixels matrix, with sensor and in-pixel circuit. Studying for in-pixel charge sensitive amplifier (CSA), CMOS and NMOS comparator design for process validation. JINST 20 (2025) C10011
- Section 2: Passive diode, real validation of sensor.
- Section 3: 26 rows × 26 columns pixels matrix, with digital readout periphery for novel electronics structure study. JINST 20 (2025) C03023

COFFEE2 Test

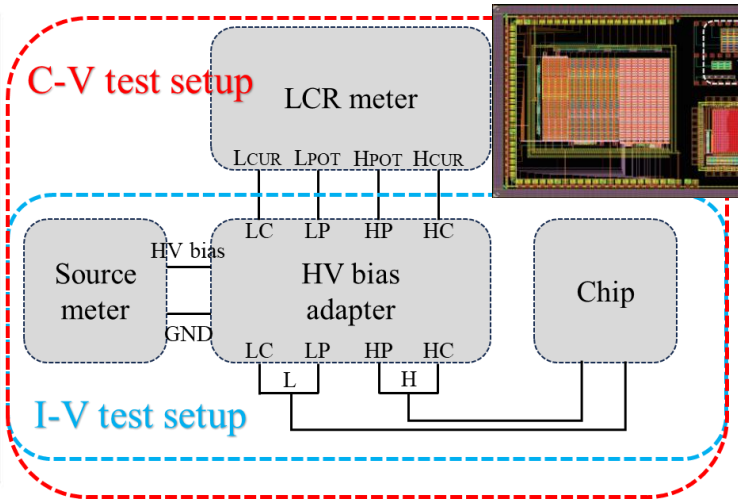
Section 2, Passive diode

- Breakdown Voltage: ~ -70V
- Leakage: ~10 pA
- Capacitance: 30~40 fF at -70V
- After ~ 10^{14} n_{eq}/cm^2 radiation
  - Leakage raise to ~1 nA

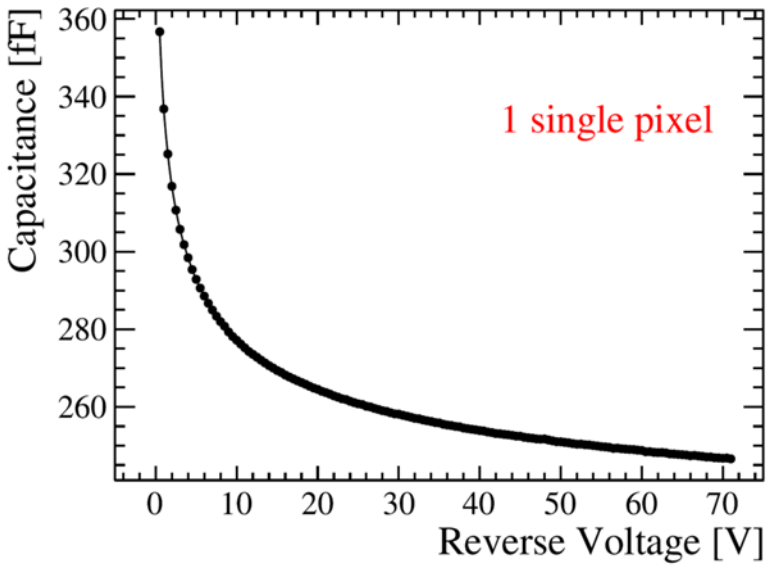
JINST 20 (2025) C10011

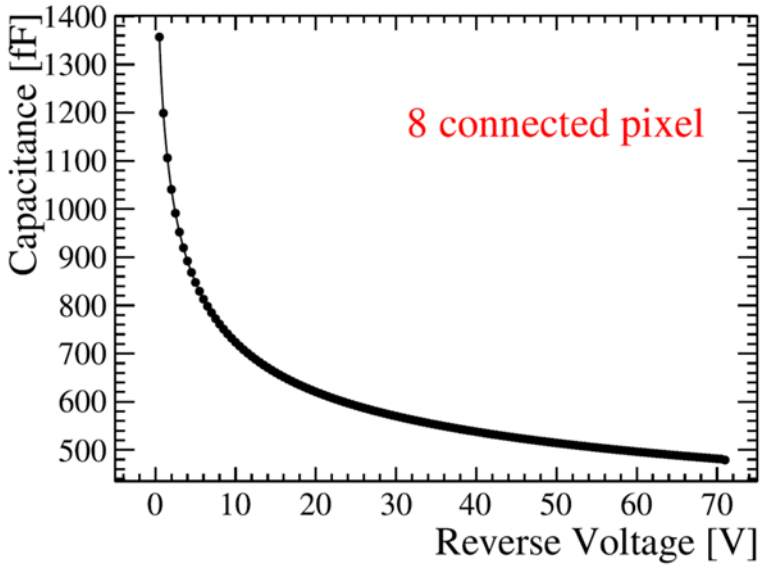


I-V curve

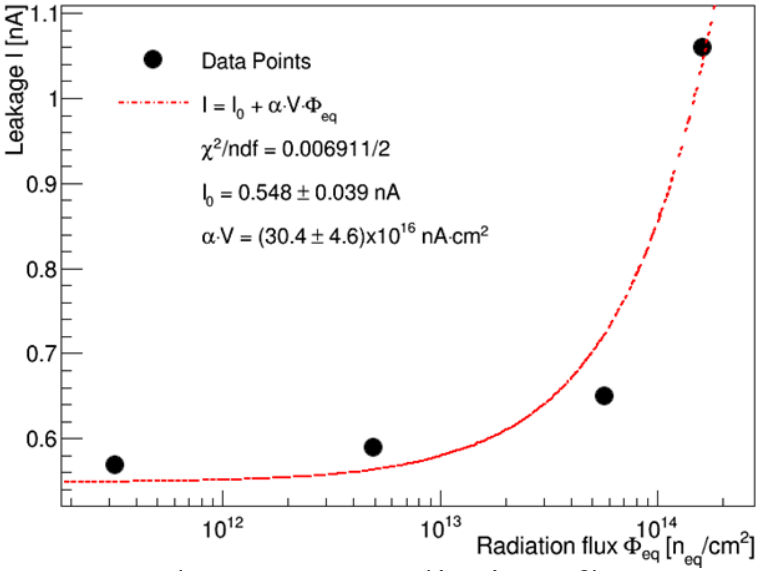


Bench setup





C-V curve for 1 and 8 pixels, not fully depletion when breakdown



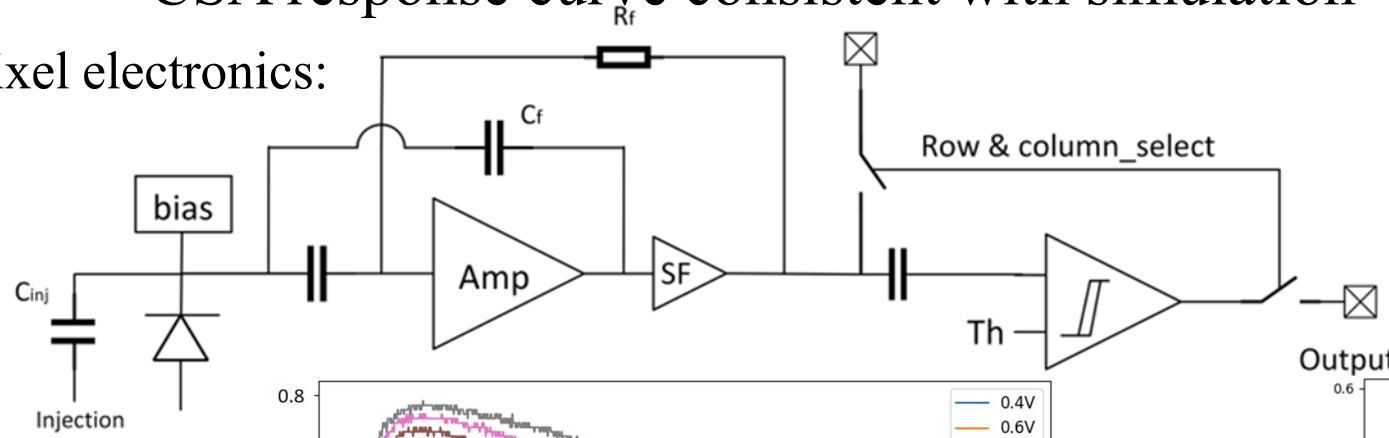
Leakage vs Radiation flux

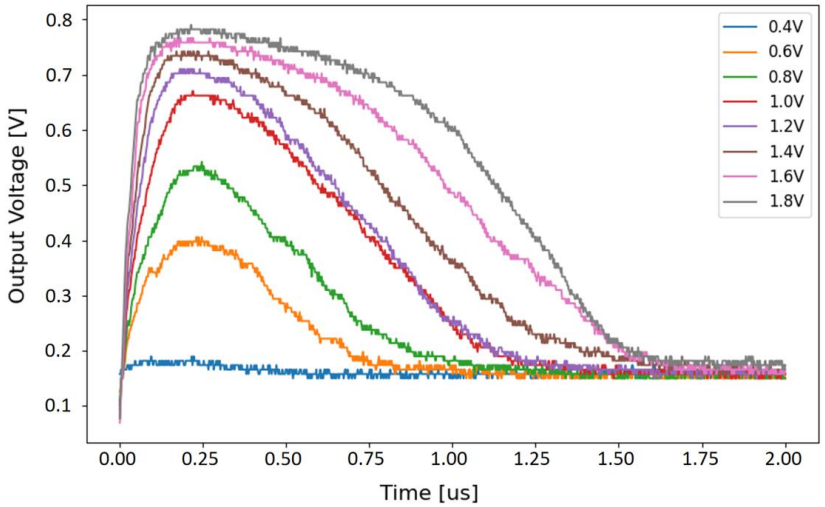
COFFEE2 Test

Section 1

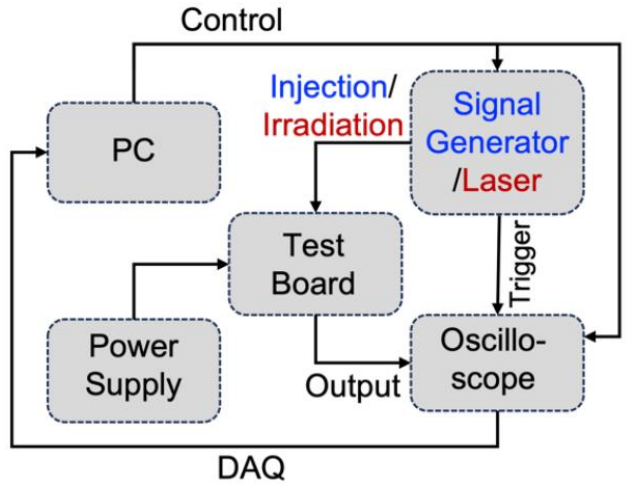
- Charge injection test: JINST 20 (2025) C10011
  - CSA work well
  - CSA response curve consistent with simulation

In-pixel electronics:

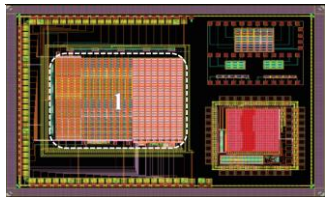


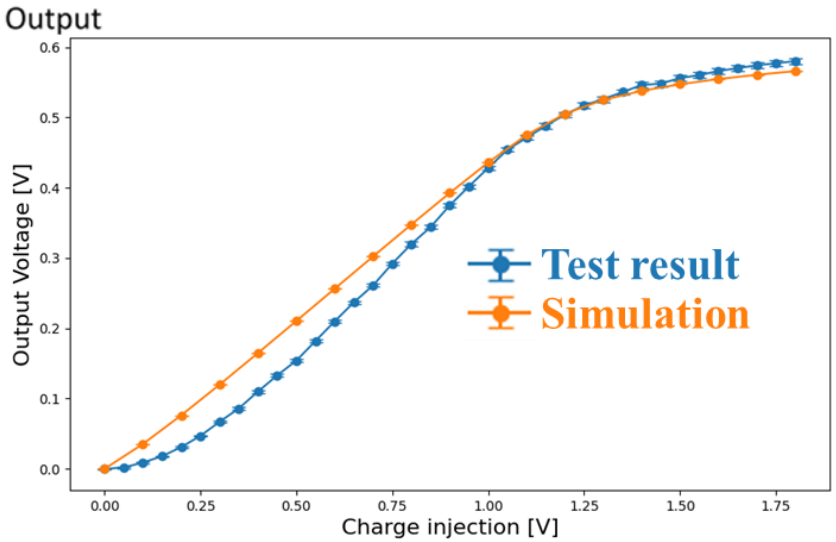


CSA output vs Vinj



Bench setup



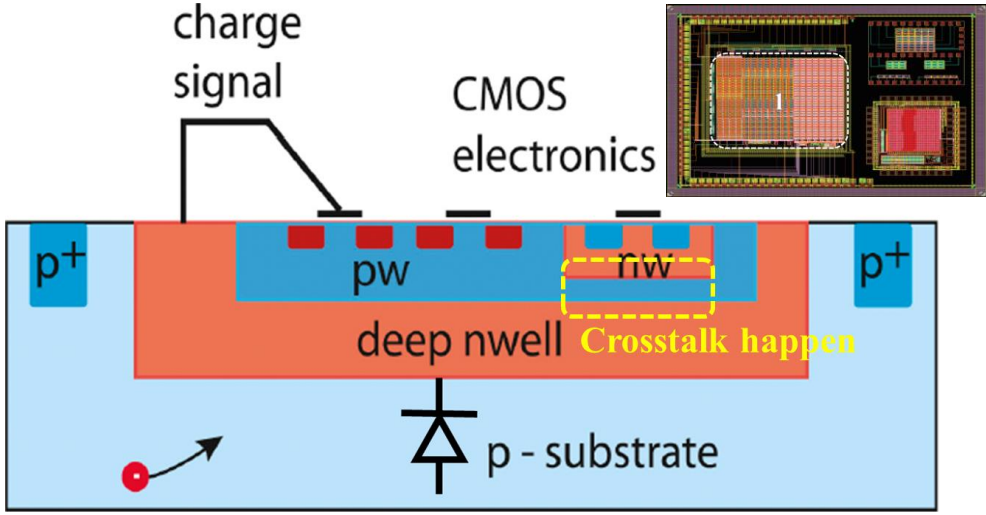


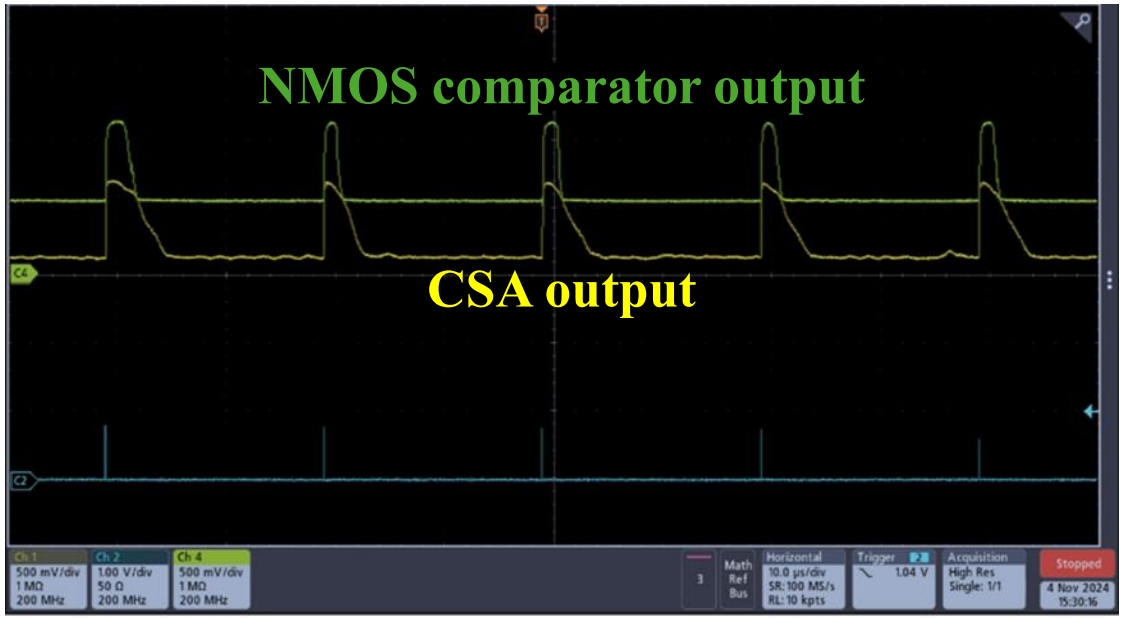
CSA response curve

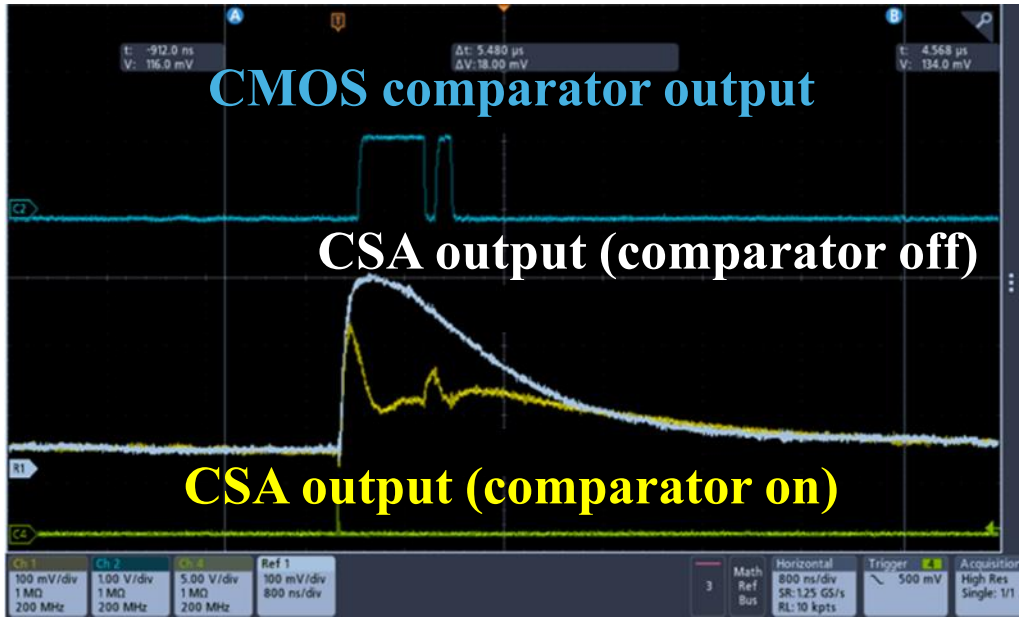
COFFEE2 Test

Section 1

- Laser test : JINST 20 (2025) C10011
  - NMOS comparator work well
  - Crosstalk happen when CMOS comparator on
  - Power supply noise from the digital circuitry couples through the N-well of the PMOS bulk terminal to the signal collection electrode (DNW).



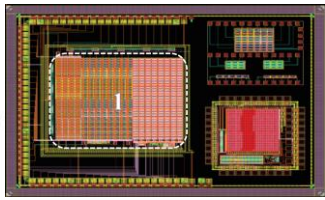




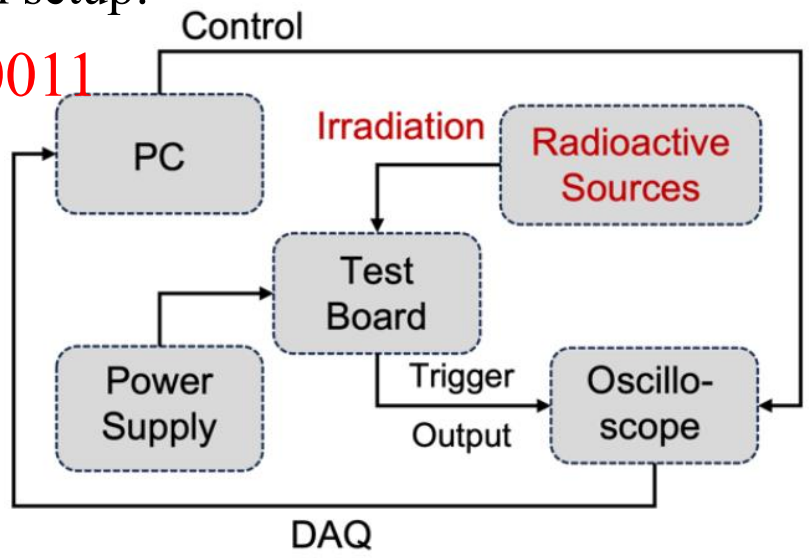
COFFEE2 Test

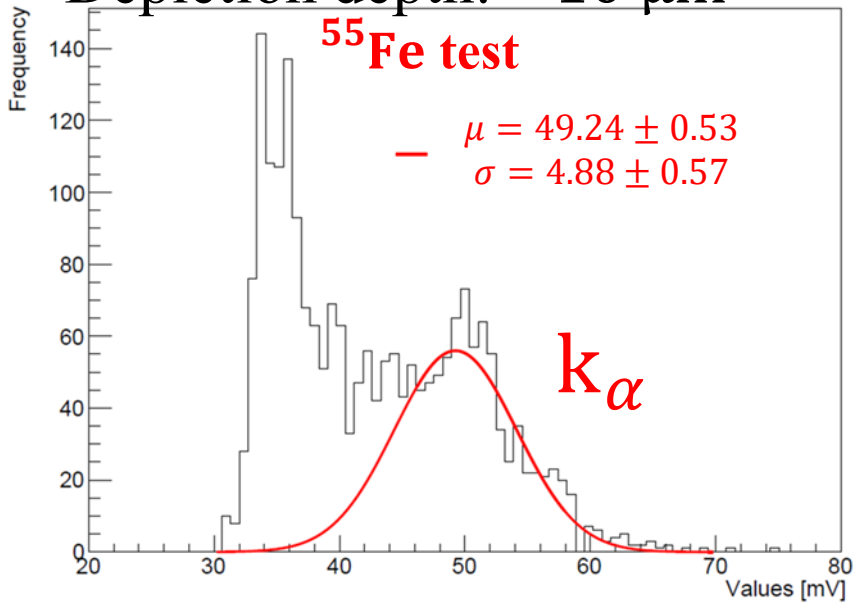
Section 1

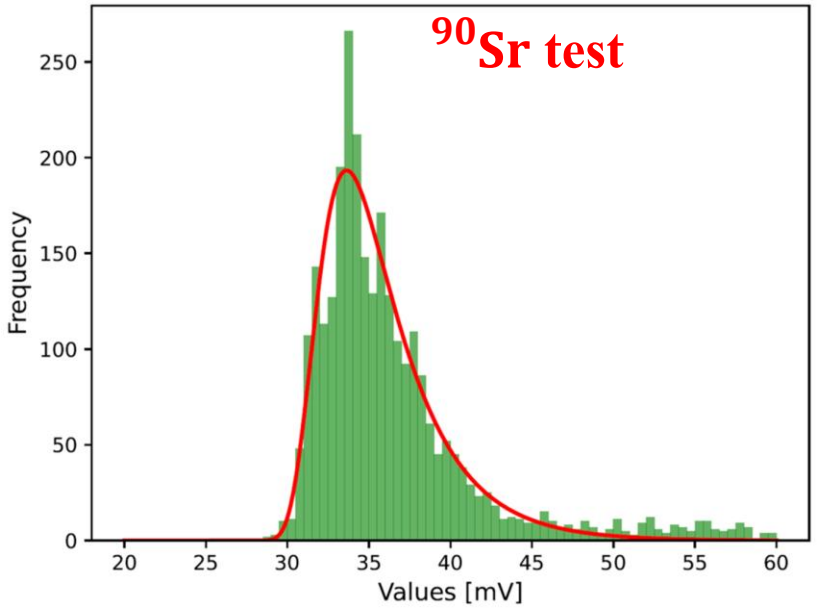
- Radioactive sources test: JINST 20 (2025) C10011
  - ^{55}Fe (5.9 keV X-ray), Gaussian fit
    - μ~49 mV~1640 e$^-$
    - σ~4.9 mV~160 e$^-$
  - ^{90}Sr (β-source), Landau fit
    - MPV: ~34 mV~1120 e$^-$
    - Depletion depth: ~10 μm



Bench setup:



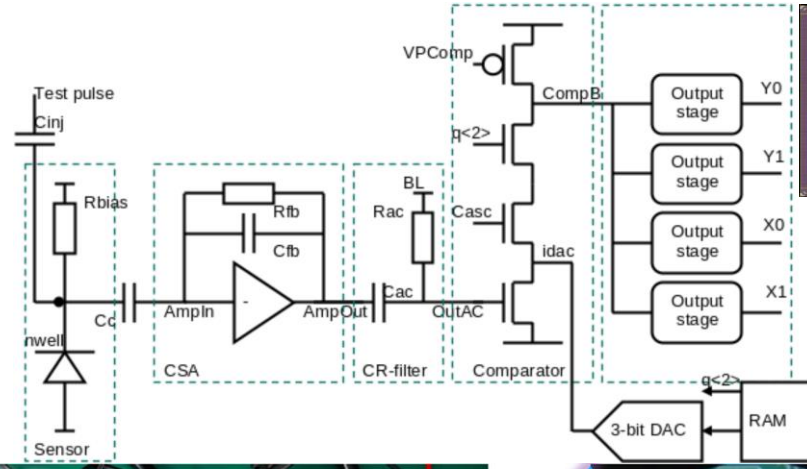


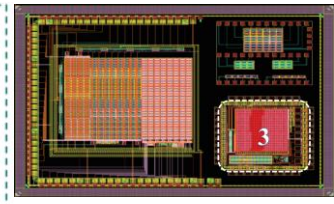


COFFEE2 Test

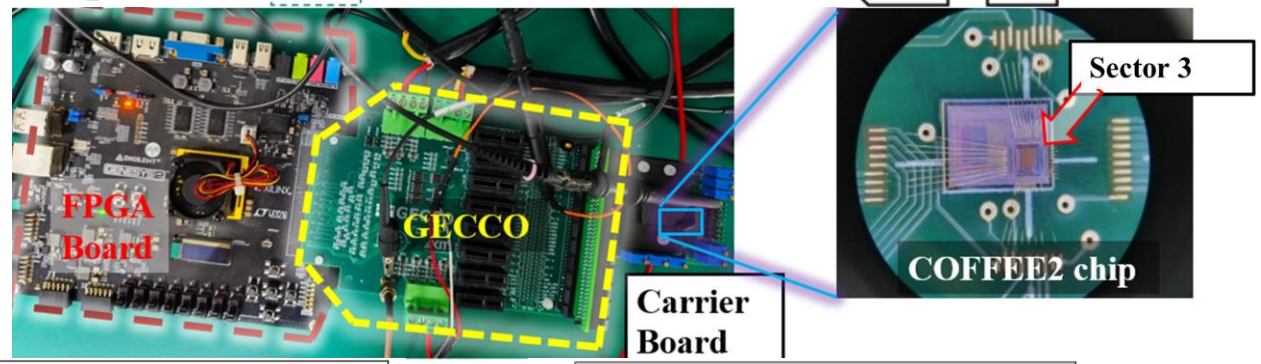
Section 3

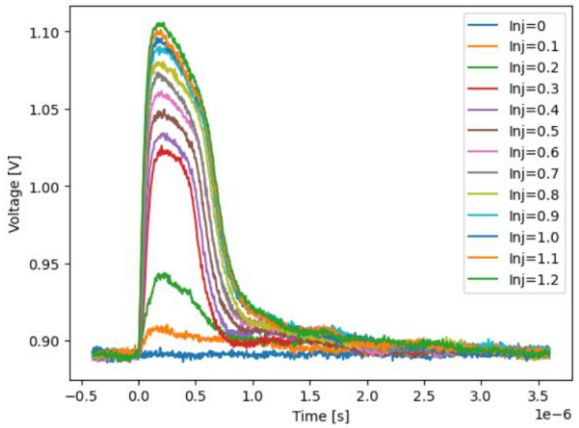
- Charge injection test: JINST 20 (2025) C03023
  - CSA work well
- Radioactive sources test:
  - ^{55}Fe (5.9 keV X-ray), Gaussian fit
    - μ~73 mV~1640 e$^-$
    - σ~2.6 mV~58 e$^-$
  - ^{90}Sr (β-source), Landau fit
    - MPV: ~50 mV~1100 e$^-$
    - Depletion depth: ~10 μm

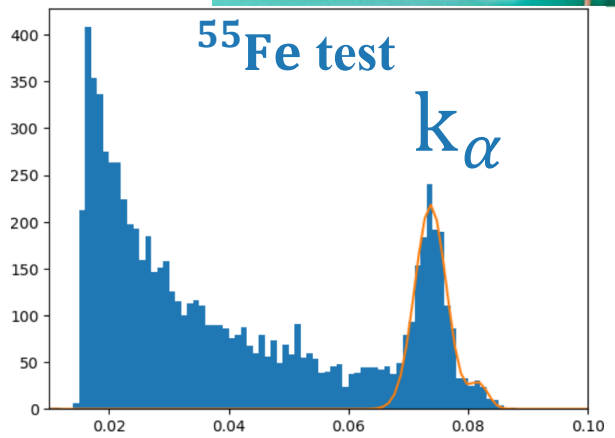


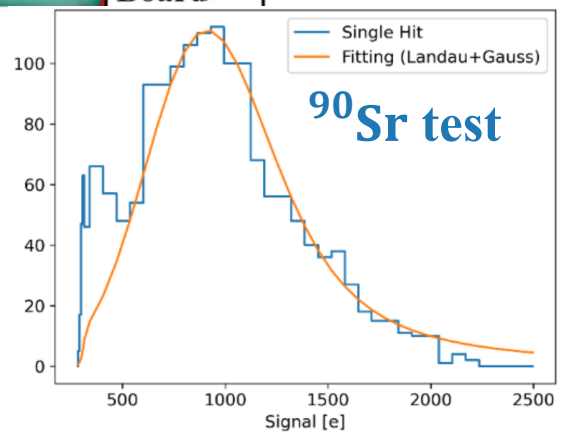


Test setup:



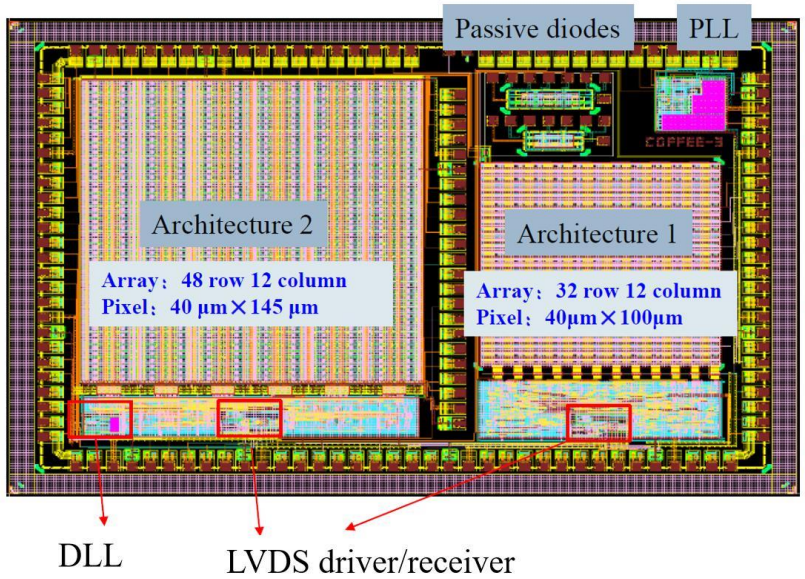


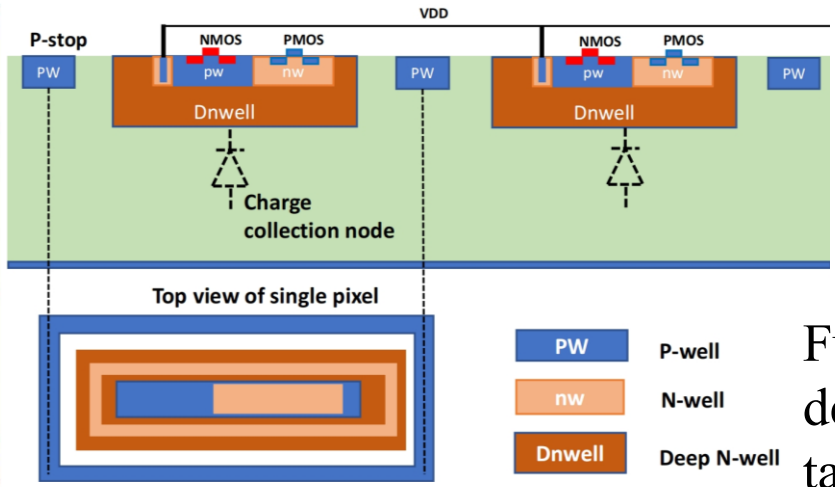




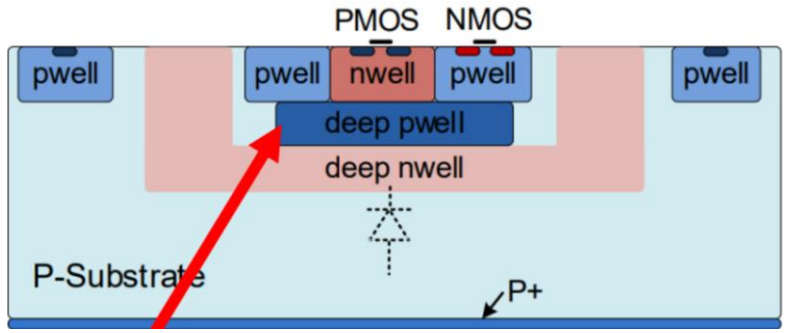
COFFEE3 Introduction

COFFEE3 chip, 3 × 4 mm², peripheral digital readout and function modules, design for future quadruple-well process





Sensor cross section



Future quadruple-well process, add a deep p-well under n-well, reduce cross-talk between n-well and deep n-well.

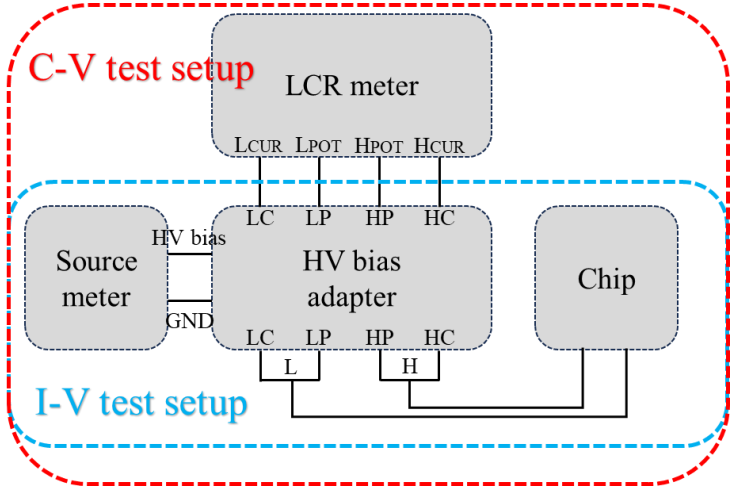
- Architecture 1: NMOS comparator and CSA, for current triple-well process
- Architecture 2: CMOS comparator and CSA, for future quadruple-well process
- Peripheral digital readout matched with the pixel array
- Peripheral function modules: DLL, LVDS, PLL
- Passive diodes: same design as COFFEE2 chip, pixel areas are the same as architecture 1 and 2, for further study of sensor and process.

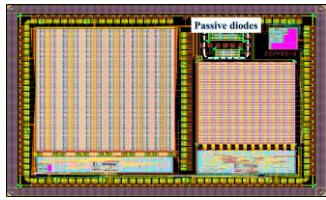
COFFEE3 Test

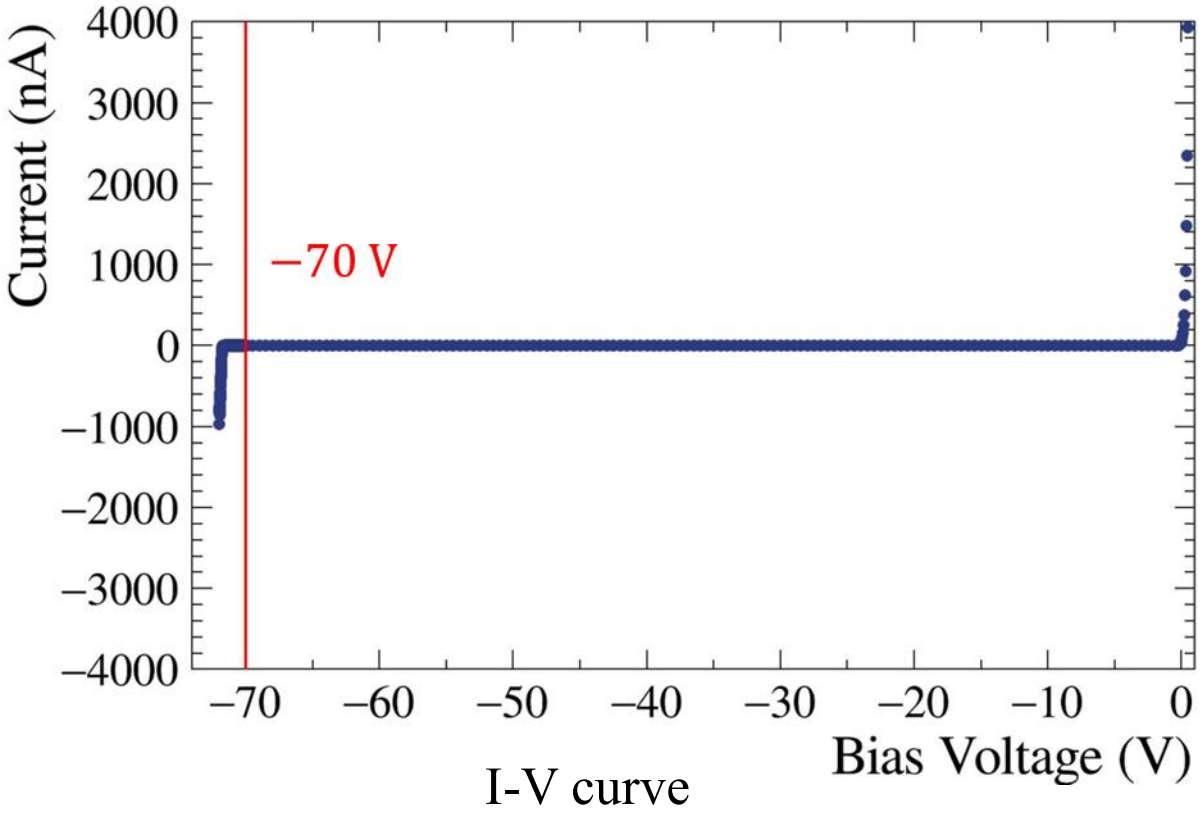
Passive diode

- Breakdown Voltage: ~ − 70V
- Leakage: ~10 pA
- Not fully depletion when breakdown
- Capacitance: ~100 fF at −70V

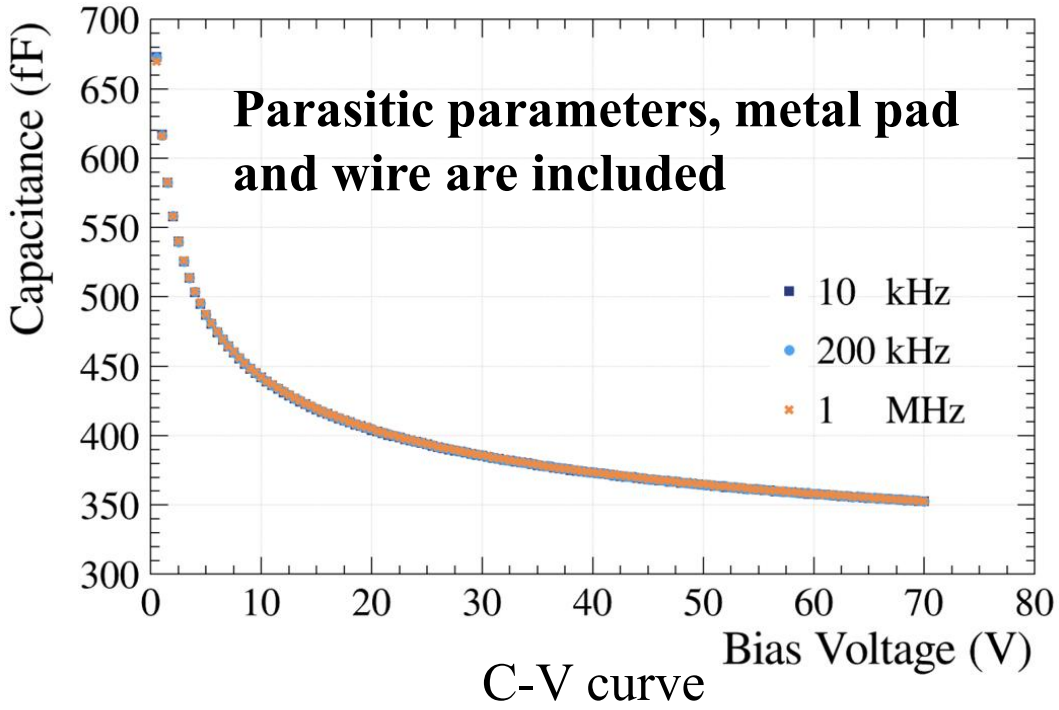
Bench setup:







I-V curve

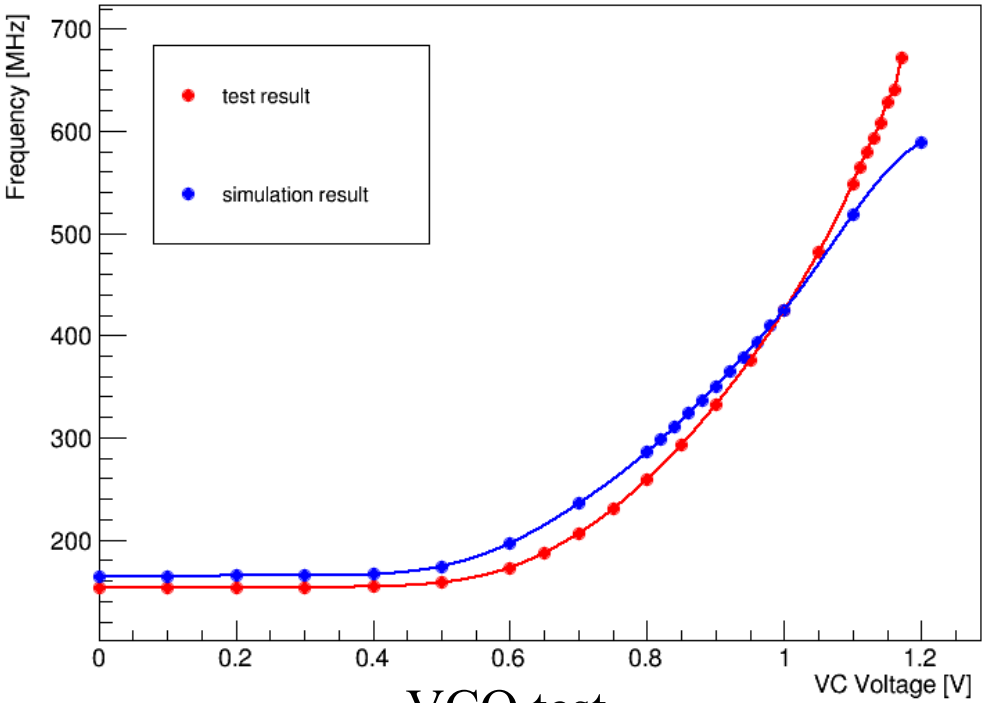


C-V curve

COFFEE3 Test

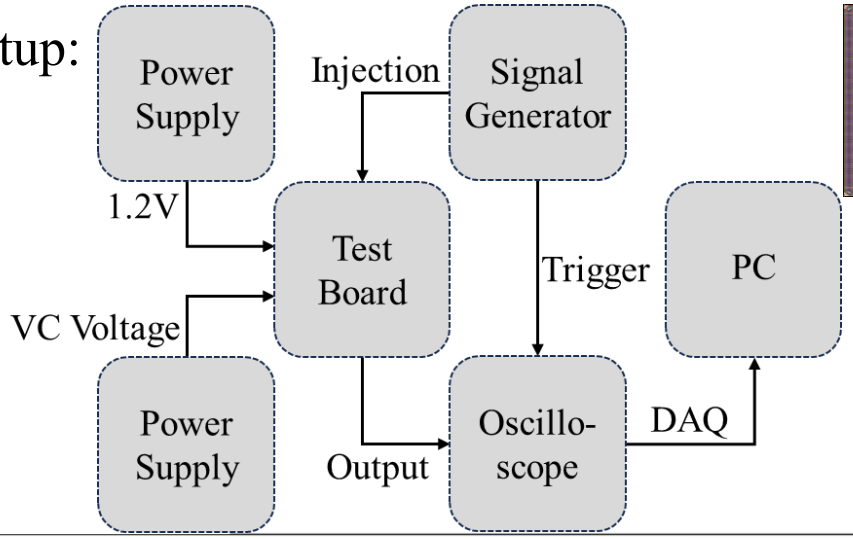
Phase locked loop (PLL) module

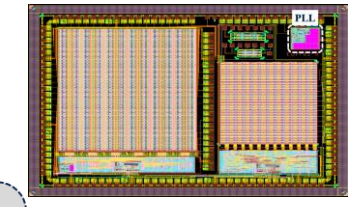
- Design for synchronizing the clock among chips and back-end electronics
- Voltage-Controlled Oscillator (VCO) and frequency multiply functions work well within the range up to 640 MHz

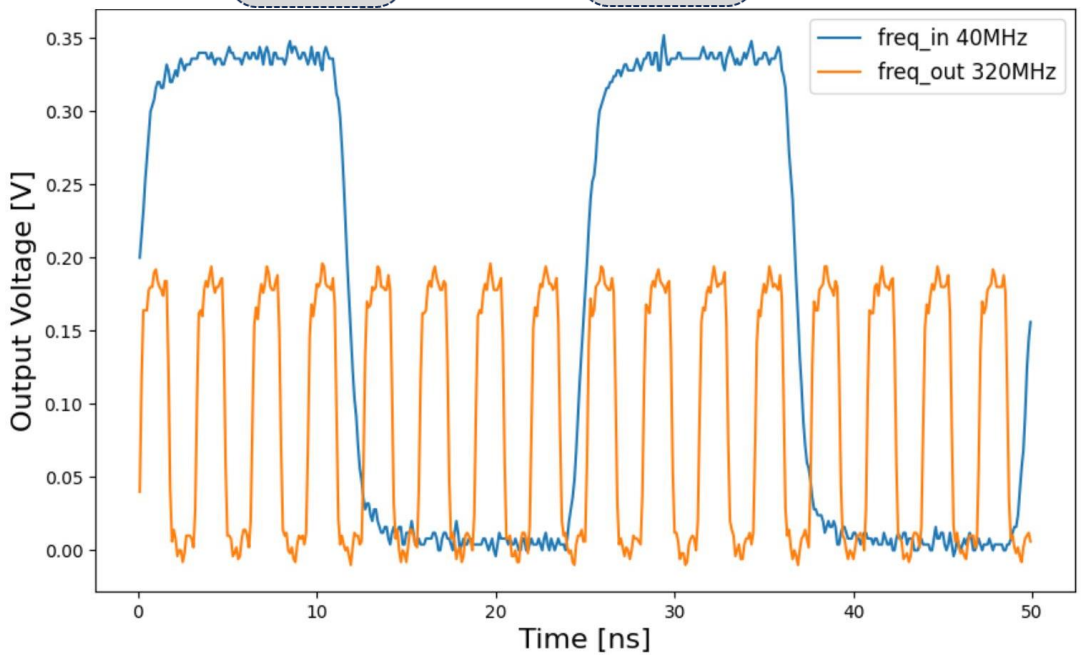


VCO test

Bench setup:







8x test, input 40 MHz, output 320 MHz

Pixels matrix array test system

Test platform based on Caribou system

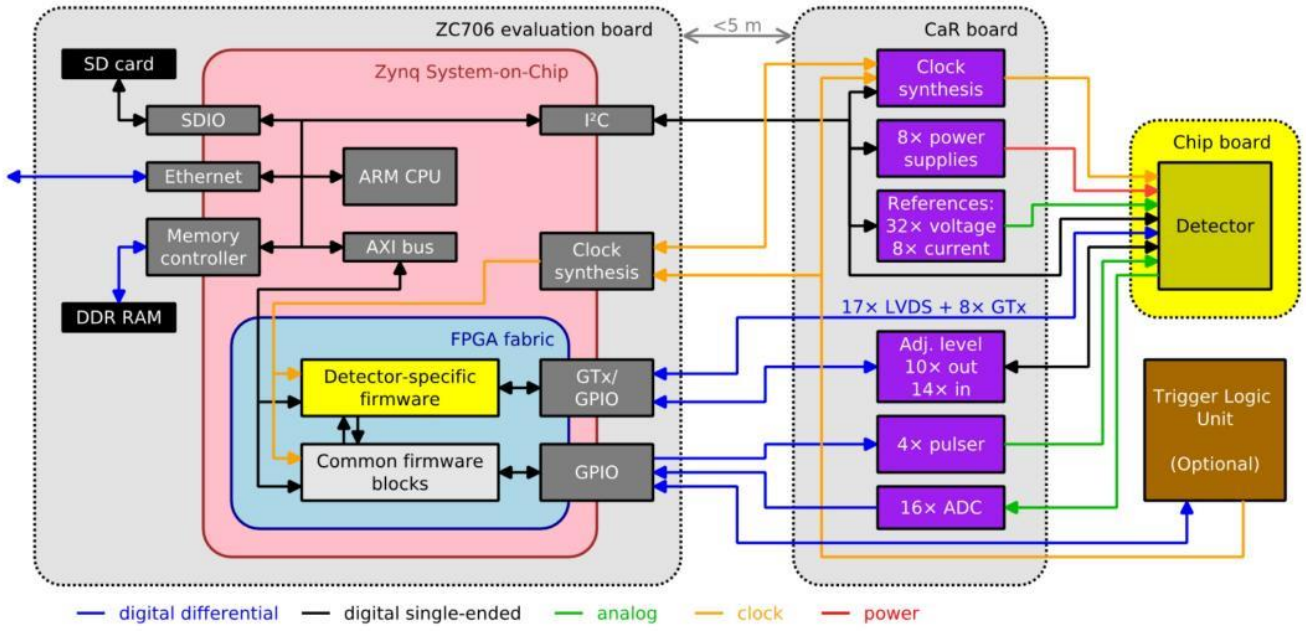
PC + ZC706/ZCU102 + Caribou board + chip carrier board

Control and Readout (CaR) board

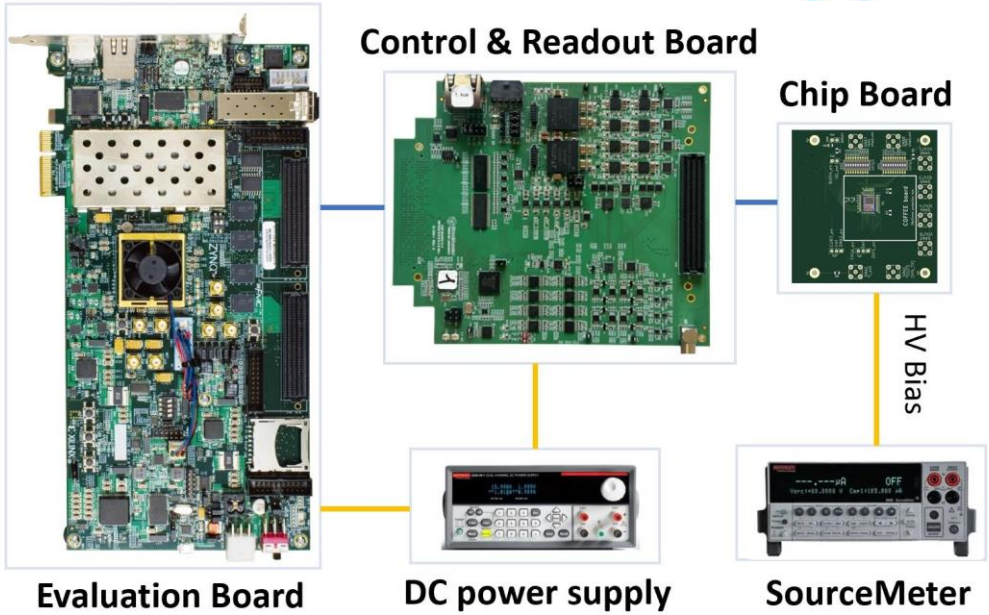
DRD3

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

Caribou system architecture



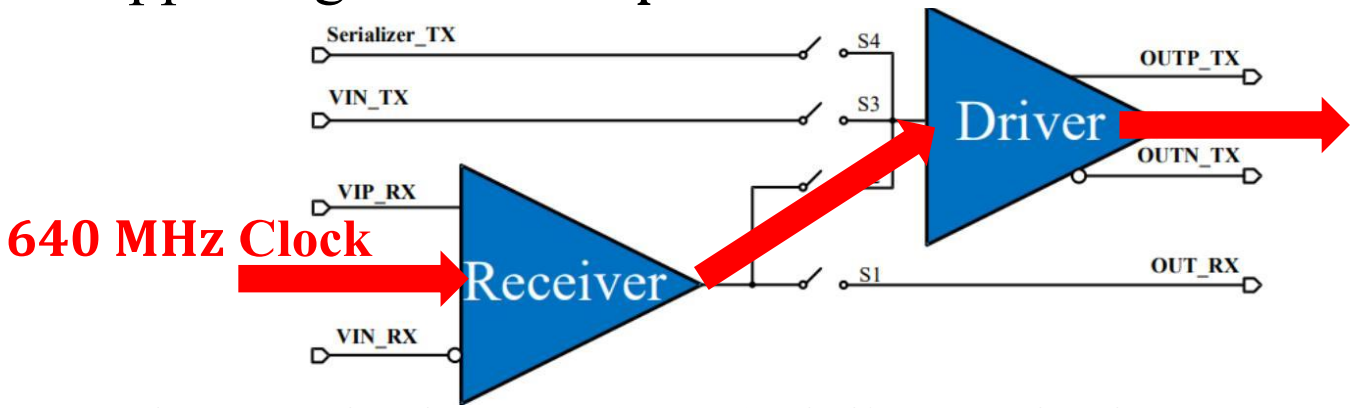
Resources for various target applications

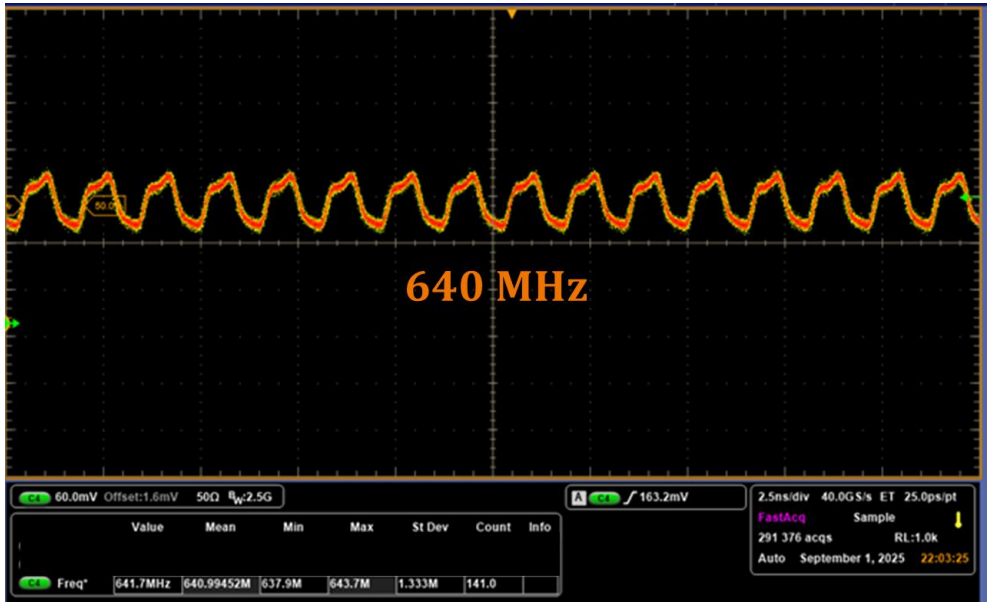


中国科学院高能物理研究所
Institute of High Energy Physics, CAS

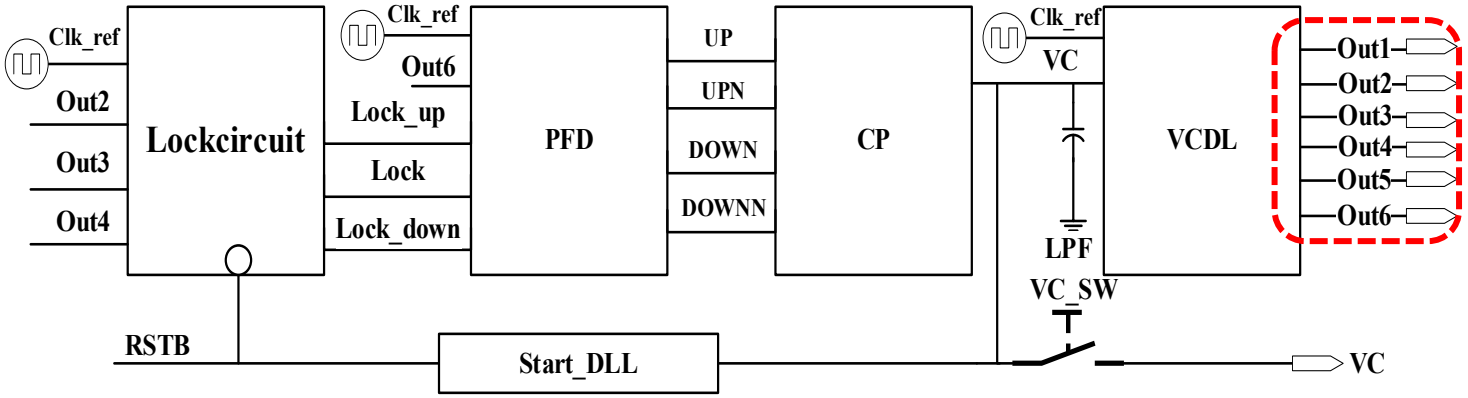
Peripheral circuit

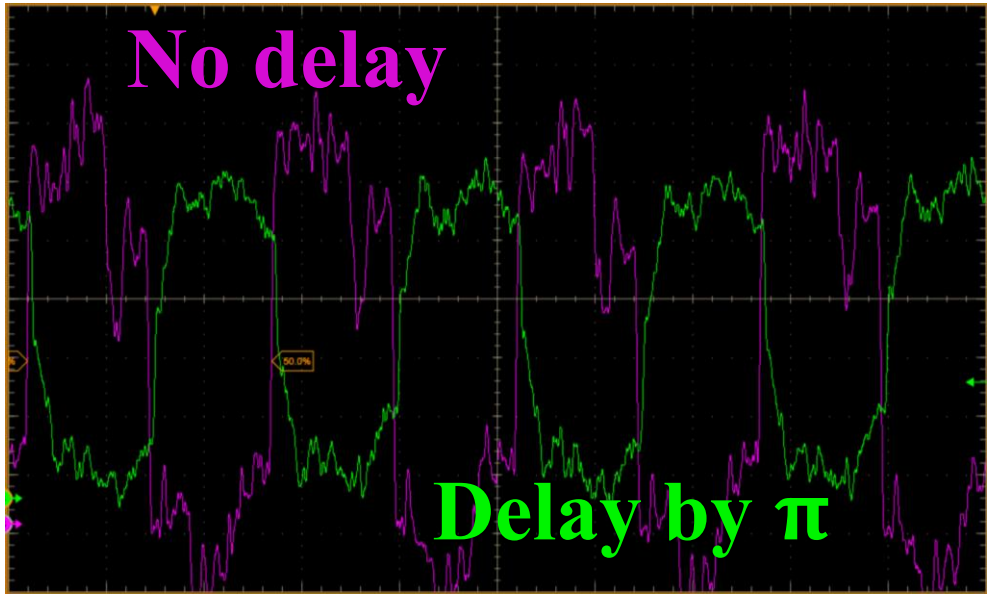
- Data LVDS transceiver works up to 640 MHz supporting to 1.28 Gbps data transmission





- Delay Locked Loop (DLL) delivers clock phase delay as expected

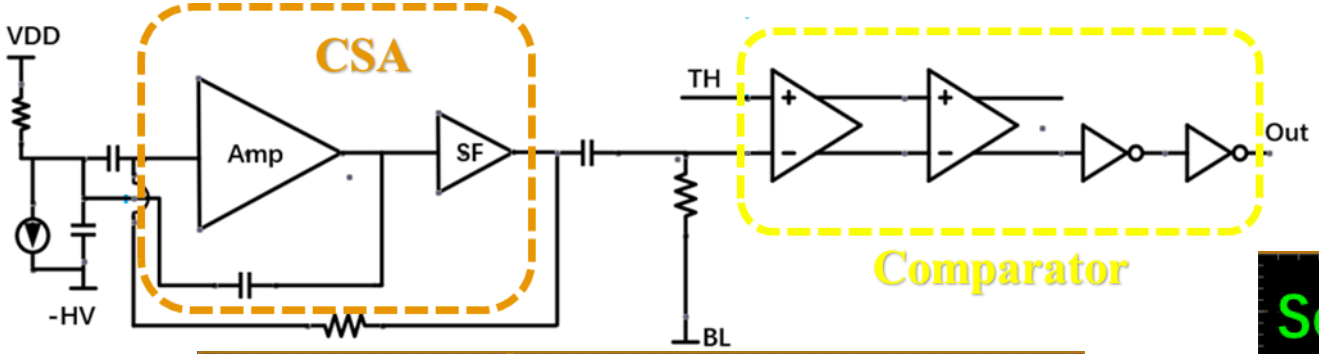


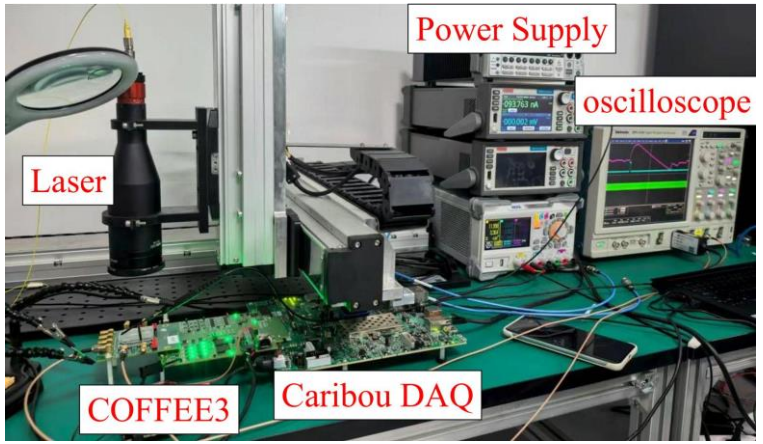


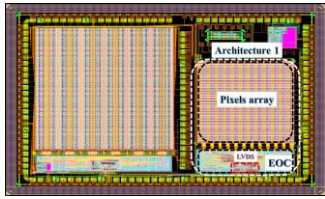
COFFEE3 Test

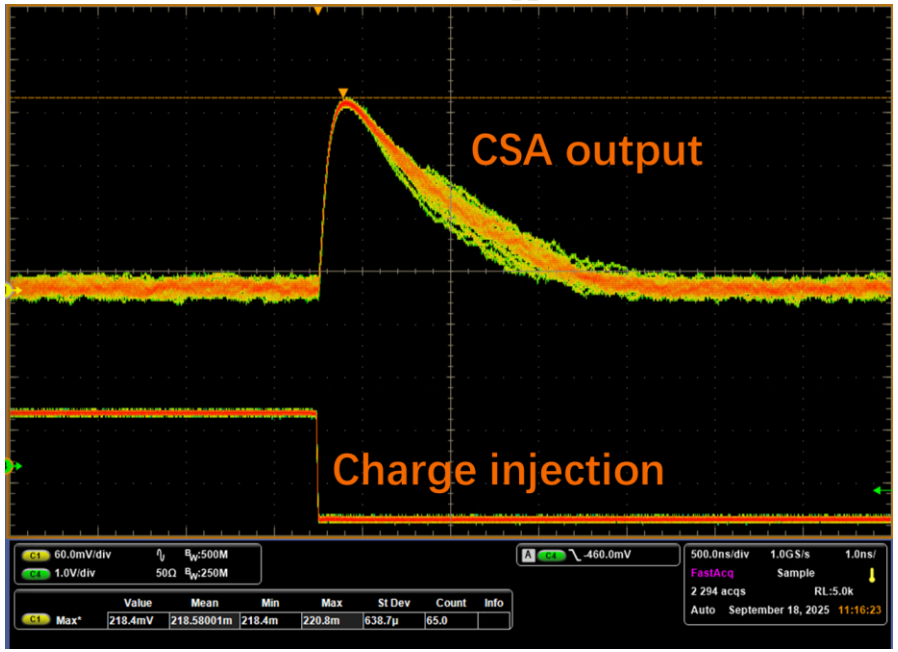
Architecture 1 test

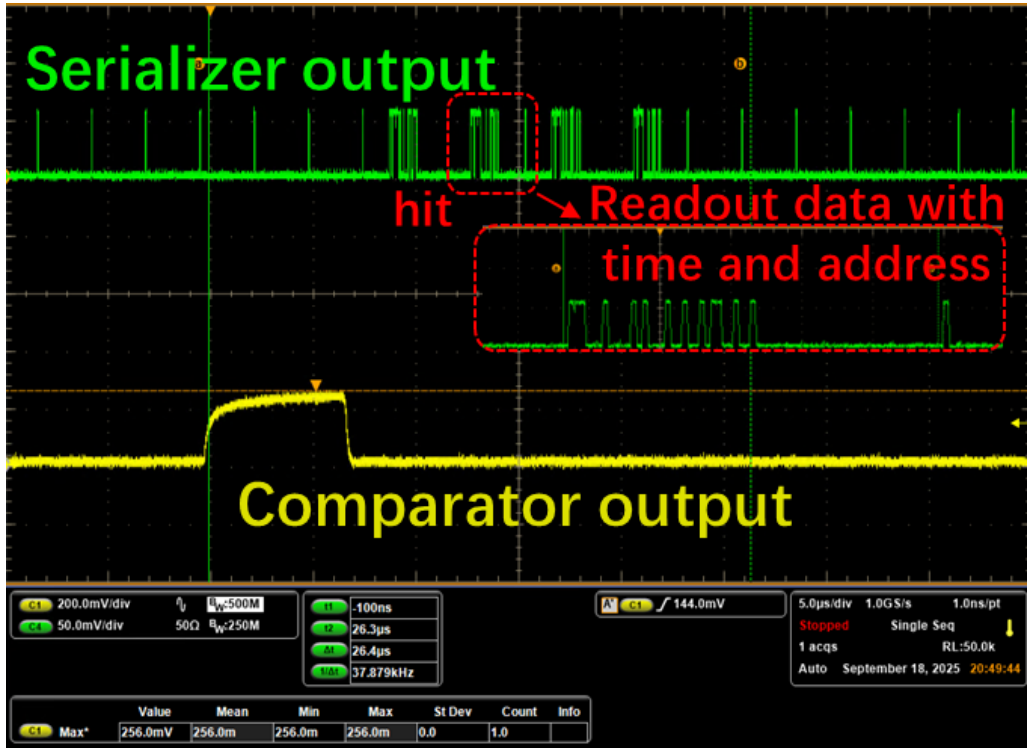
- CSA working as expected with charge injection
- End of column readout function validated







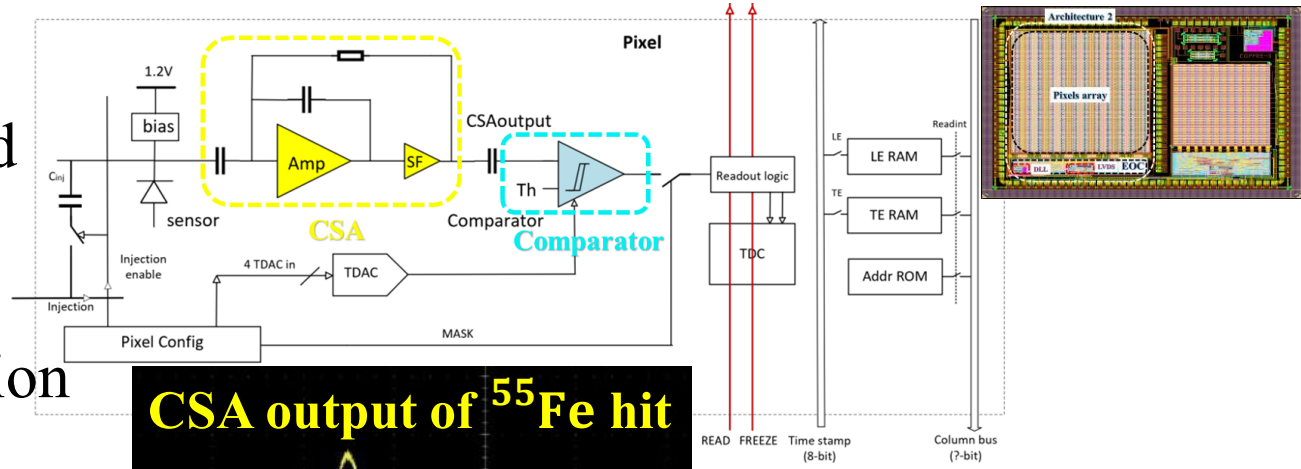


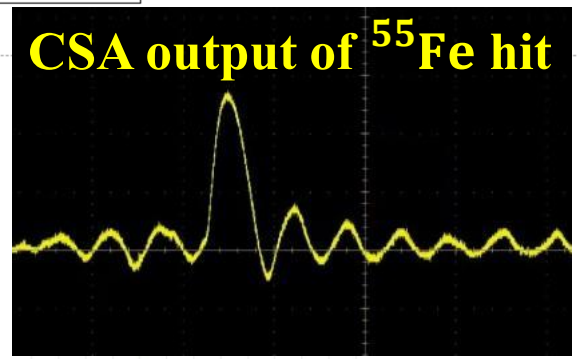


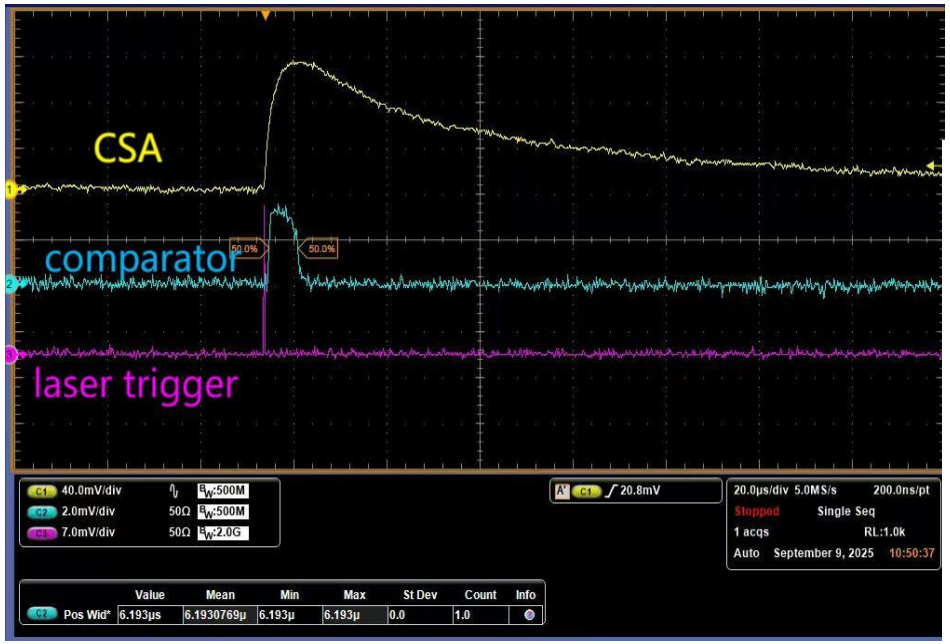
COFFEE3 Test

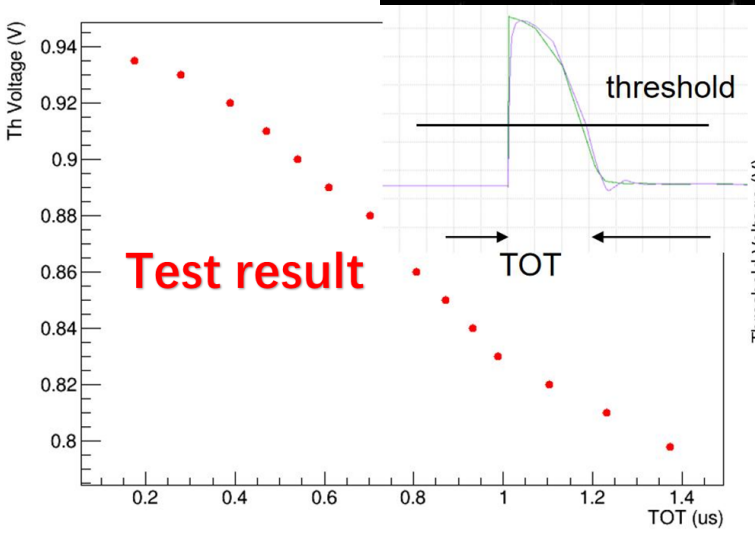
Architecture 2 test

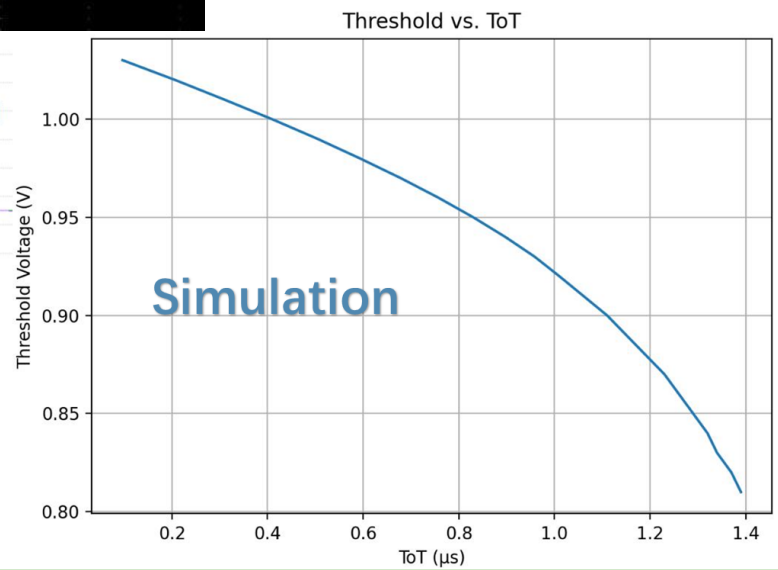
- CSA and comparator working as expected
  - CSA and comparator output is clear
  - Typical time over threshold (TOT) of laser signal is consistent with simulation
- ^{55}Fe signal can be seen

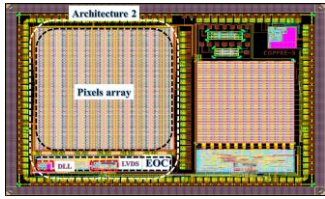








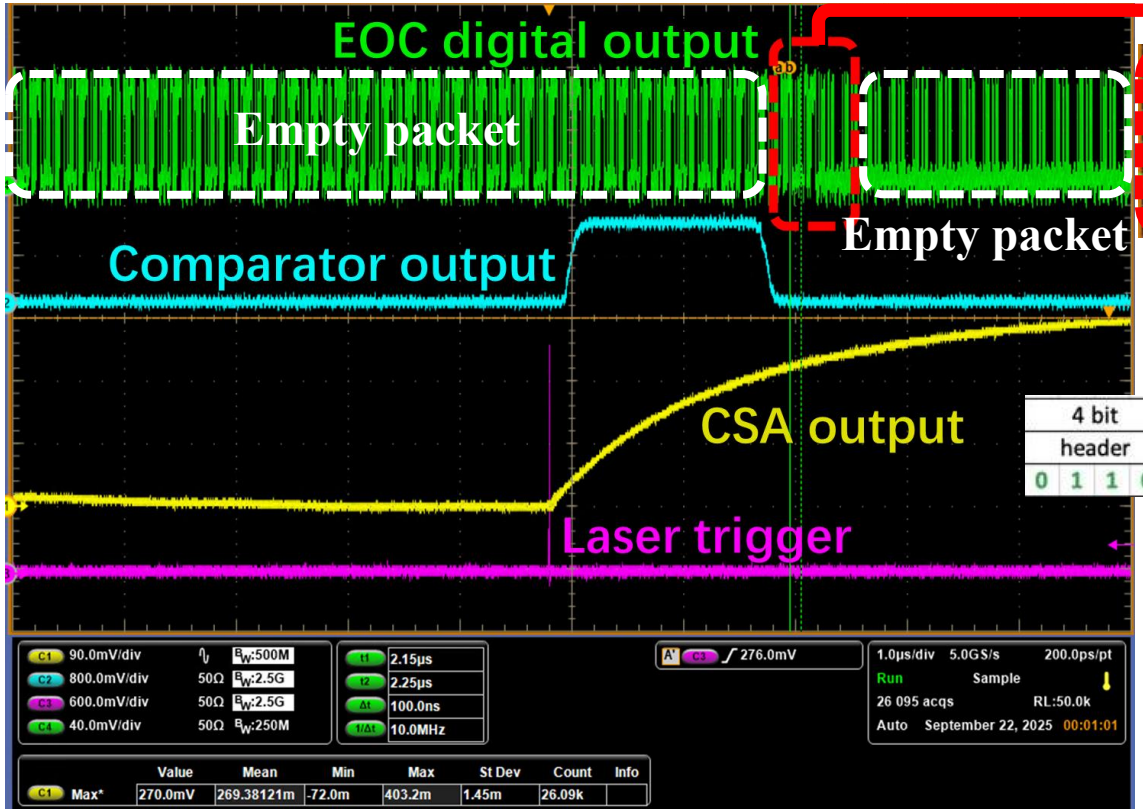


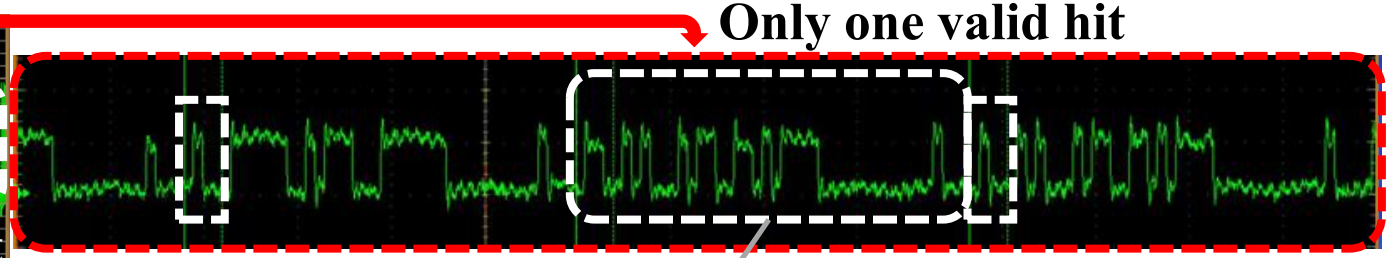


Architecture 2 test

- Full readout chain works well with laser test
  - Only unmask pixel column 0, row 1

Sensor → in-pixel CSA and comparator → End of column readout circuit





4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

Valid hit
header: 0110

Row and column
address are correct

Summary

- HVCMOS prototyping chip in 55 nm process for UP

- Many encouraging results from COFFEE chip:
  - Breakdown Voltage > -70 V, leakage ~ 10 pA
  - Sensor, in-pixel CSA and comparator, digital circuit work well

- Future plan:
  - Using high resistance wafer
  - Quadruple-well process